3.3 V Dual-Loop 50 Mbps to 3.3 Gbps Laser Diode Driver

Data Sheet

ADN2847

FEATURES

50 Mbps to 3.3 Gbps operation
Single 3.3 V operation
Typical rise/fall time: 80 ps
Bias current range: 2 mA to 100 mA
Modulation current range: 5 mA to 80 mA
Monitor photodiode current: 50 µA to 1200 µA
Dual MPD functionality for DWDM
50 mA supply current at 3.3 V
Closed-loop control of power and extinction ratio
Full current parameter monitoring
Laser fail and laser degrade alarms
Automatic laser shutdown (ALS)
Optional clocked data
Supports FEC rates
48-lead (7 mm × 7 mm) LFCSP package
32-lead (5 mm × 5 mm) LFCSP package

APPLICATIONS

SONET OC-1/3/12/48
SDH STM-0/1/4/16
Fibre Channel
Gigabit Ethernet
DWDM dual MPD wavelength control

GENERAL DESCRIPTION

The ADN2847 uses a unique control algorithm to control both average power and extinction ratio of the laser diode (LD) after initial factory setup. External component count and PCB area are low, as both power and extinction ratio control are fully integrated. Programmable alarms are provided for laser fail (end of life) and laser degrade (impending fail).

Optional dual MPD current monitoring is designed into the ADN2847 specifically for DWDM wavelength control.

The ADN2847 is specified for the −40°C to +85°C temperature range and is available in a 48-lead LFCSP package and a 32-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

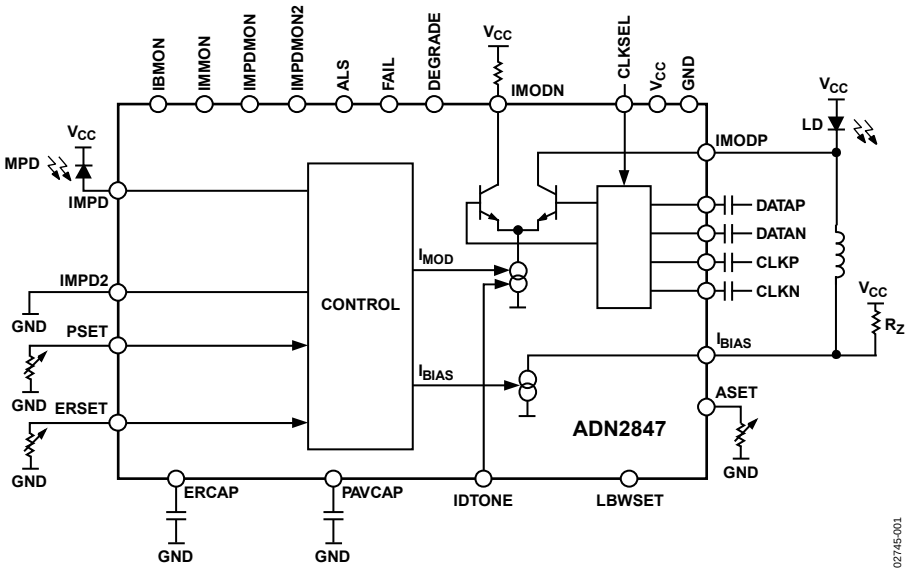


Figure 1.

Rev. B
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REVISION HISTORY

3/12—Rev. A to Rev. B

Added EPAD Notation ... 7
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

10/06—Rev. 0 to Rev. A

Updated Format ... Universal
Change to Data Sheet Title ... 1
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Added I_{BIAS} Section ... 10
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1/03—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V. Temperature range: −40°C to +85°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values specified at T_A = 25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
LASER BIAS CURRENT (I_{BIAS}, ALS)					
Output Current I_{BIAS}	2		100	mA	
I_{BIAS} when ALS is asserted			0.1	mA	
ALS Assertion Time			5	µs	I_{BIAS} < 10% of nominal
I_{BIAS} Compliance Voltage	1.2		V_{CC}	V	
CCBIAS Compliance Voltage	1.2		V_{CC}	V	
MODULATION CURRENT (IMODP, IMODN)[1]					
Output Current I_{MOD}	5		80	mA	
Compliance Voltage	1.5		V_{CC}	V	
I_{MOD} when ALS is Asserted			0.1	mA	
Rise Time[2]		80	120	ps	See Figure 3 for device rise time histogram
Fall Time[2]		80	120	ps	See Figure 4 for device fall time histogram
Random Jitter[2]		1	1.5	ps	RMS
Pulse Width Distortion[2]		15		ps	I_{MOD} = 40 mA
MONITOR PD (MPD, MPD2)					
Current	50		1200	µA	Average current
Compliance Voltage			1.65	V	
POWER SET INPUT (PSET)					
Capacitance			80	pF	
Monitor Photodiode Current into RPSET Resistor	50		1200	µA	Average current
Voltage	1.1	1.2	1.3	V	
EXTINCTION RATIO SET INPUT (ERSET)					
Allowable Resistance Range	1.2		25	kΩ	
Voltage	1.1	1.2	1.3	V	
ALARM SET (ASET)					
Allowable Resistance Range	1.2		25	kΩ	
Voltage	1.1	1.2	1.3	V	
Hysteresis		5		%	
CONTROL LOOP					Low Loop Bandwidth selection
Time Constant		0.22		sec	LBWSET = GND
		2.25		sec	LBWSET = V_{CC}
DATA INPUTS (DATAP, DATAN, CLKP, CLKN)[3]					
V p-p (Single-Ended, Peak-to-Peak)	100		500	mV	Data and clock inputs are ac-coupled
Input Impedance (Single-Ended)		50		Ω	
t_{SETUP}[4]	50			ps	See Figure 2
t_{HOLD}[4]	100			ps	See Figure 2
LOGIC INPUTS (ALS, LBWSET, CLKSEL)					
V_{IH}	2.4			V	
V_{IL}			0.8	V	
ALARM OUTPUTS (FAIL, DEGRADE)					Internal 30 kΩ Pull-Up
V_{OH}	2.4			V	
V_{OL}			0.8	V	
IDTONE					User to supply current sink in the range of 50 µA to 4 mA
Compliance Voltage		V_{CC} – 1.5		V	
I_{OUT}/I_{IN} Ratio		2			
f_{IN}[5]	0.01		1	MHz	

Parameter	Min	Typ	Max	Unit	Conditions/Comments
IBMON, IMMON, IMPDMON, IMPDMON2					
IBMON, IMMON Division Ratio		100		A/A	
IMPDMON, IMPDMON2		1		A/A	
IMPDMON to IMPDMON2 Matching			2	%	I_{MPD} = 1200 µA
Compliance Voltage	0		V_{CC} −1.2	V	
SUPPLY					
I_{CC}[6]		50		mA	$I_{BIAS} = I_{MOD} = 0$
V_{CC}[7]	3.0	3.3	3.6	V	

[1] The high speed performance for the die version of ADN2847 can be achieved when using the bonding diagram shown in Figure 6.
[2] Measured into a 25 Ω load using a 11110000 pattern at 2.5 Gbps.
[3] When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows in the IMODP pin.
[4] Guaranteed by design and characterization. Not production tested.
[5] IDTONE can cause eye distortion.
[6] I_{CCMIN} for power calculation in the Power Consumption section is the typical I_{CC} given.
[7] All V_{CC} pins should be shorted together.

TIMING DIAGRAMS

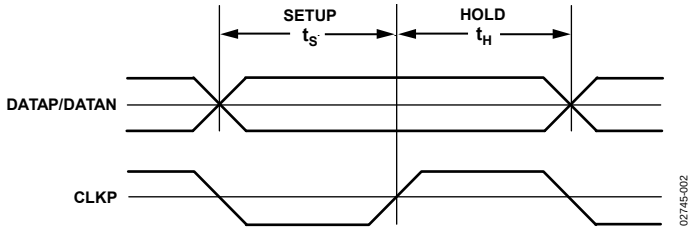


Figure 2. Setup and Hold Time

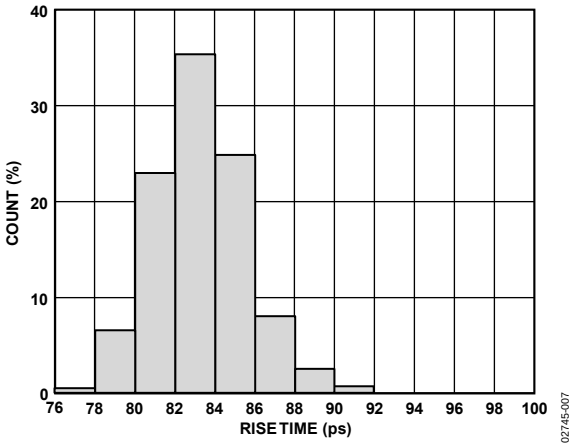


Figure 3. Rise Time Distribution Under Worst-Case Operating Conditions

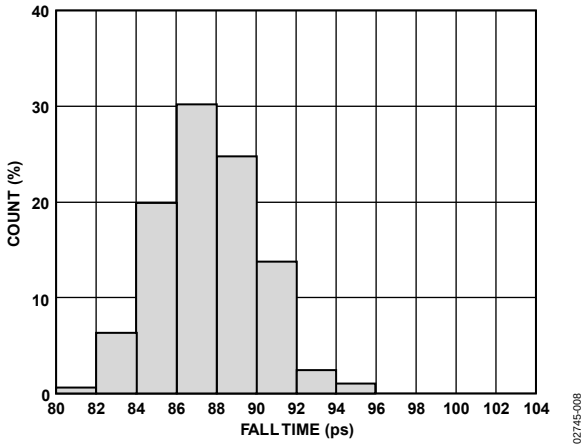


Figure 4. Fall Time Distribution Under Worst-Case Operating Conditions

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC} to GND	4.2 V
Digital Inputs (ALS, LBWSET, CLKSEL)	−0.3 V to V_{CC} + 0.3 V
IMODN, IMODP	V_{CC} + 1.2 V
Operating Temperature Range Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation[1] (W)	(T_J max − T_A)/ θ_{JA}
Lead Temperature (Soldering 10 sec)	300°C

[1] Power consumption formulae are provided in the Power Consumption section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
48-lead LFCSP	25	°C/W
32-lead LFCSP	32	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

DIE PAD COORDINATES

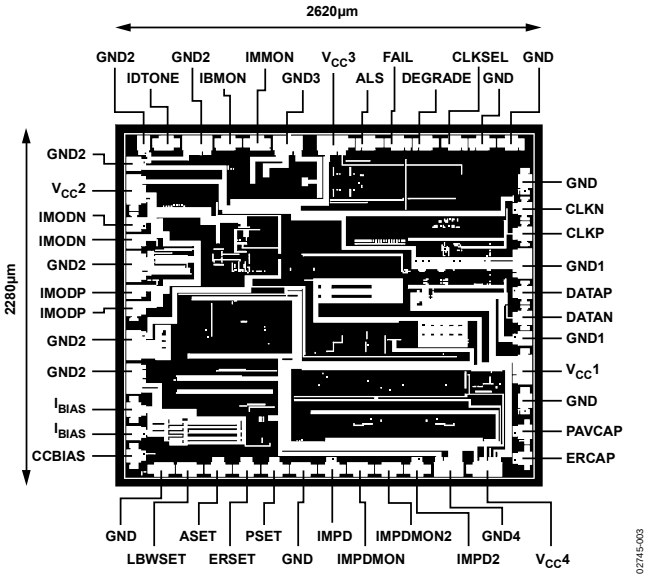


Figure 5. Metallization Photograph

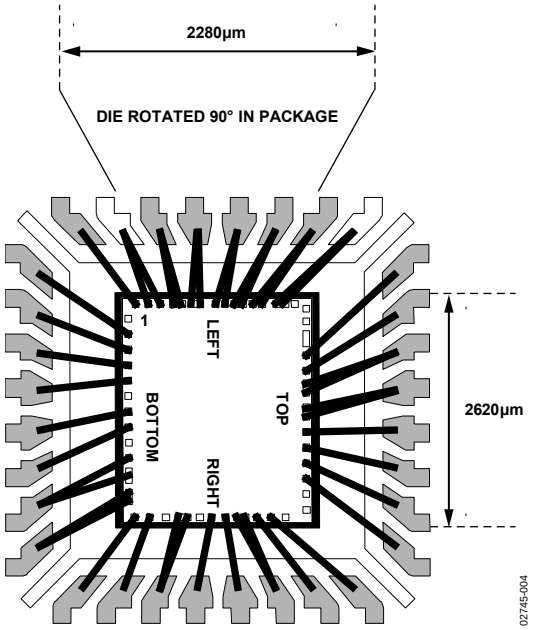


Figure 6. Bonding Diagram

Table 4. Die Pad Coordinates[1]

Pad Number	Pad Name	x[µm]	y[µm]
1	TP1 (GND)	−996	1026
2	LBWSET	−996	853
3	ASET	−996	679
4	ERSET	−996	506
5	PSET	−996	332
6	TP2 (GND)	−996	159
7	IMPD	−996	−15
8	IMPDMON	−996	506
9	IMPDMON2	−996	−361
10	IMPD2	−996	−534
11	GND4	−996	−724
12	$V_{CC}4$	−995	−964
13	ERCAP	−925	−1191
14	PAVCAP	−777	−1191
15	TP3 (GND)	−606	−1191
16	$V_{CC}1$	−389	−1191
17	GND1	−200	−1191
18	DATAN	−70	−1191
19	DATAP	83	−1191
20	GND1	263	−1191
21	CLKP	442	−1191
22	CLKN	596	−1191
23	TP4 (GND)	762	−1191
24	TP5 (GND)	996	−1109
25	TP6 (GND)	996	−935
26	CLKSEL	996	−762
27	DEGRADE	996	−589
28	FAIL	996	−415
29	ALS	996	−242
30	$V_{CC}3$	996	−19
31	GND3	996	251
32	IMMON	996	441
33	IBMON	996	614
34	GND2	996	804
35	IDTONE	995	993
36	GND2	995	1133
37	GND2	867	1191
38	$V_{CC}2$	713	1191
39	IMODN	500	1191
40	IMODN	396	1191
41	GND2	242	1191
42	IMODP	88	1191
43	IMODP	−16	1191
44	GND2	−239	1191
45	GND2	−443	1191
46	I_{BIAS}	−633	1191
47	I_{BIAS}	−772	1191
48	CCBIAS	−912	1191

[1] With the origin in the center of the die (see Figure 5).

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

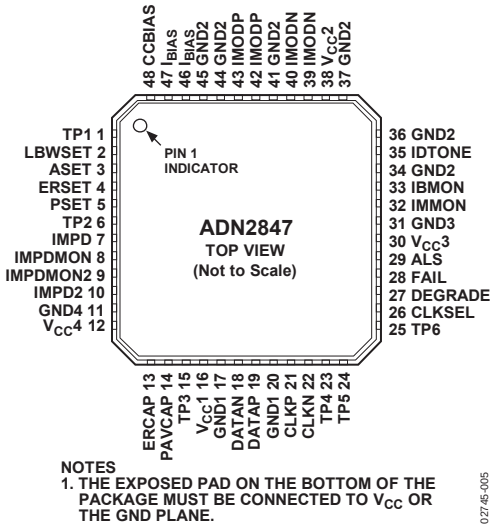


Figure 7. 48-Lead LFCSP

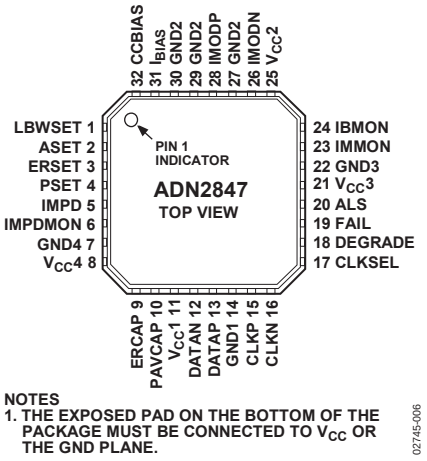


Figure 8. 32-Lead LFCSP

Table 5. Pin Function Descriptions

Pin Number			
48-Lead	**32-Lead**	**Mnemonic**	**Description**
1	N/A	TP1	Test Pin. In normal operation, TP1 = GND.
2	1	LBWSET	Select Low Loop Bandwidth.
3	2	ASET	Alarm Current Threshold Setting Pin.
4	3	ERSET	Extinction Ratio Set Pin.
5	4	PSET	Average Optical Power Set Pin.
6	N/A	TP2	Test Pin. In normal operation, TP2 = GND.
7	5	IMPD	Monitor Photodiode Input.
8	6	IMPDMON	Mirrored Current from Monitor Photodiode.
9	N/A	IMPDMON2	Mirrored Current from Monitor Photodiode 2. (For use with two MPDs).
10	N/A	IMPD2	Monitor Photodiode Input 2. (For use with two MPDs).
11	7	GND4	Supply Ground.
12	8	$V_{CC}4$	Supply Voltage.
13	9	ERCAP	Extinction Ratio Loop Capacitor.
14	10	PAVCAP	Average Power Loop Capacitor.
15	N/A	TP3	Test Pin. In normal operation, TP3 = GND.
16	11	$V_{CC}1$	Supply Voltage.
17	N/A	GND1	Supply Ground.
18	12	DATAN	Data, Negative Differential Terminal.
19	13	DATAP	Data, Positive Differential Terminal.
20	14	GND1	Supply Ground.
21	15	CLKP	Data Clock Positive Differential Terminal. Used if CLKSEL = V_{CC}.
22	16	CLKN	Data Clock Negative Differential Terminal. Used if CLKSEL = V_{CC}.
23	N/A	TP4	Test Pin. In normal operation, TP4 = GND.
24	N/A	TP5	Test Pin. In normal operation, TP5 = GND.
25	N/A	TP6	Test Pin. In normal operation, TP6 = GND.
26	17	CLKSEL	Clock Select. Active = V_{CC}. Used if data is clocked into chip.
27	18	DEGRADE	Degrade Alarm Output.
28	19	FAIL	Fail Alarm Output.
29	20	ALS	Automatic Laser Shutdown.

Pin Number			
48-Lead	**32-Lead**	**Mnemonic**	**Description**
30	21	$V_{CC}3$	Supply Voltage.
31	22	GND3	Supply Ground.
32	23	IMMON	Modulation Current Mirror Output.
33	24	IBMON	Bias Current Mirror Output.
34	N/A	GND2	Supply Ground.
35	N/A	IDTONE	IDTONE. Requires external current sink to ground.
36	N/A	GND2	Supply Ground.
37	N/A	GND2	Supply Ground.
38	25	$V_{CC}2$	Supply Voltage.
39	26	IMODN	Modulation Current Negative Output. Connect via a matching resistor to V_{CC}.
40	N/A	IMODN	Modulation Current Negative Output. Connect via a matching resistor to V_{CC}.
41	27	GND2	Supply Ground.
42	28	IMODP	Modulation Current Positive Output. Connect to laser diode.
43	N/A	IMODP	Modulation Current Positive Output. Connect to laser diode.
44	29	GND2	Supply Ground.
45	30	GND2	Supply Ground.
46	31	I_{BIAS}	Laser Diode Bias Current.
47	N/A	I_{BIAS}	Laser Diode Bias Current.
48	32	CCBIAS	Extra Laser Diode Bias. (Connected to Vcc when dc-coupled to laser diode. Connected to I_{BIAS} when ac-coupled to laser diode).
EP	EP	EPAD	Exposed Pad. The exposed pad on the bottom of the package must be connected to V_{CC} or the GND plane.

THEORY OF OPERATION

Laser diodes have current-in to light-out transfer functions, as shown in Figure 9. Two key characteristics of this transfer function are the threshold current, I_{TH}, and the slope in the linear region beyond the threshold current, referred to as slope efficiency (LI).

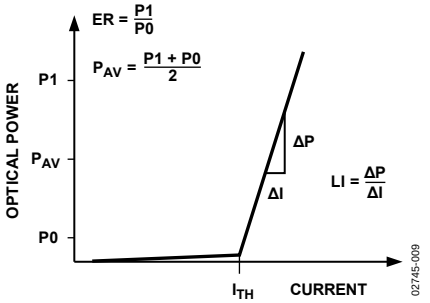


Figure 9. Laser Transfer Function

CONTROL

A monitor photodiode (MPD) is required to control the LD. The MPD current is fed into the ADN2847 to control the power and extinction ratio, continuously adjusting the bias current and modulation current in response to the changing threshold current and light-to-current slope efficiency of the laser.

The ADN2847 uses automatic power control (APC) to maintain a constant average power over time and temperature.

The ADN2847 uses closed-loop extinction ratio control to allow optimum setting of the extinction ratio for every device. Thus, SONET/SDH interface standards can be met over device variation, temperature, and laser aging. Closed-loop modulation control eliminates the need to either overmodulate the LD or include external components for temperature compensation. This reduces research and development time and second sourcing issues caused by characterizing LDs.

Average power and extinction ratio are set using the PSET pin and the ERSET pin, respectively. Potentiometers are connected between these pins and ground. The potentiometer R_{PSET} is used to change the average power. The potentiometer R_{ERSET} is used to adjust the extinction ratio. Both PSET and ERSET are kept 1.2 V above GND.

The R_{PSET} and R_{ERSET} potentiometers can be calculated using the following formulas:

$$R_{PSET} = \frac{1.2\ \text{V}}{I_{AV}}\ (\Omega)$$

$$R_{ERSET} = \frac{1.2\ \text{V}}{\frac{I_{MPD_CW}}{P_{CW}} \times \frac{ER - 1}{ER + 1} \times P_{AV}}\ (\Omega)$$

where:

I_{AV} is the average MPD current.
P_{CW} is the dc optical power specified on the laser data sheet.
I_{MPD_CW} is the MPD current at that specified P_{CW}.
P_{AV} is the average power required.
ER is the desired extinction ratio (ER = P1/P0).

Note that I_{ERSET} and I_{PSET} changes from device to device; however, the control loops determines actual values. It is not required to know exact values for LI or MPD optical coupling.

LOOP BANDWIDTH SELECTION

For continuous operation, the user should hardwire the LBWSET pin high and use 1 µF capacitors to set the actual loop bandwidth. These capacitors are placed between the PAVCAP pin and the ERCAP pin and ground. It is important that these capacitors are low leakage multilayer ceramics with an insulation resistance greater than 100 GΩ or a time constant of 1000 seconds, whichever is less.

Table 6.

Operation Mode	LBWSET	Recommended PAVCAP	Recommended ERCAP
Continuous 50 Mbps to 3.3 Gbps	High	1 µF	1 µF
Optimized for 2.5 Gbps to 3.3 Gbps	Low	22 nF	22 nF

Setting LBSET low and using 22 nF capacitors results in a shorter loop time constant (a 10× reduction over using 1 µF capacitors and keeping LBWSET high.)

ALARMS

The ADN2847 is designed to allow interface compliance to ITUT-G958 (11/94) section 10.3.1.1.2 (transmitter fail) and section 10.3.1.1.3 (transmitter degrade). The ADN2847 has two active high alarms, DEGRADE and FAIL. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 100:1 to the FAIL alarm threshold. The DEGRADE alarm is raised at 90% of this level.

Example:

$$I_{FAIL} = 50\ \text{mA so } I_{DEGRADE} = 45\ \text{mA}$$

$$I_{ASET} = \frac{I_{FAIL}}{100} = \frac{50\ \text{mA}}{100} = 500\ \mu\text{A}$$

$$R_{ASET} = \frac{1.2\ \text{V}}{I_{ASET}} = \frac{1.2}{500\ \mu\text{A}} = 2.4\ \text{k}\Omega$$

where the smallest valid value for R_{ASET} is 1.2 kΩ, because this corresponds to the I_{BIAS} maximum of 100 mA.

The laser degrade alarm, DEGRADE, is provided to give a warning of imminent laser failure if the laser diode degrades further or environmental conditions continue to stress the LD, such as increasing temperature.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH compliant. This occurs when one of the following conditions arises:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resulting in the MPD current dropping to zero. This gives closed-loop feedback to the system that ALS has been enabled.

DEGRADE is raised only when the bias current exceeds 90% of ASET current.

MONITOR CURRENTS

IBMON, IMMON, IMPDMON, and IMPDMON2 are current controlled current sources from V_{CC}. They mirror the bias, modulation, and MPD current for increased monitoring functionality. An external resistor to GND gives a voltage proportional to the current monitored.

If the monitoring functions IMPDMON and IMPDMON2 are not required, the IMPD pin and the IMPD2 pin must be grounded and the monitor photodiode output must be connected directly to the PSET pin.

DUAL MPD DWDM FUNCTION (48-LEAD LFCSP ONLY)

The ADN2847 has circuitry for a second monitor photodiode, MPD2. The second photodiode current is mirrored to IMPDMON2 for wavelength control purposes and is summed internally with the first monitor photodiode current for the power control loop. For single MPD circuits, the MPD2 pin is tied to GND.

This enables the system designer to use the two currents to control the wavelength of the laser diode using various optical filtering techniques inside the laser module.

If the monitor current functions IMPDMON and IMPDMON2 are not required, then the IMPD pin and IMPD2 pin can be grounded and the monitor photodiode output can be connected directly to PSET.

IDTONE (48-LEAD LFCSP ONLY)

The IDTONE pin is supplied for fiber identification/supervisory channels or control purposes in WDM. This pin modulates the optical one level over a possible range of 2% of minimum I_{MOD} to 10% of maximum I_{MOD}. The level of modulation is set by connecting an external current sink between the IDTONE pin and ground. There is a gain of two from this pin to the I_{MOD} current. Figure 12 shows how the AD9850/AD9851 or the AD9834 can be used with the ADN2847 to allow fiber identification.

If the ID_TONE function is not used, the IDTONE pin should be tied to V_{CC}. Note that using IDTONE during transmission can cause optical eye degradation.

DATA AND CLOCK INPUTS

Data and clock inputs are ac-coupled (10 nF capacitors are recommended) and terminated via a 100 Ω internal resistor between DATAP and DATAN, and also between the CLKP pin and the CLKN pin. There is a high impedance circuit to set the common-mode voltage that is designed to allow for maximum input voltage headroom over temperature. It is necessary that ac coupling is used to eliminate the need for matching between common-mode voltages.

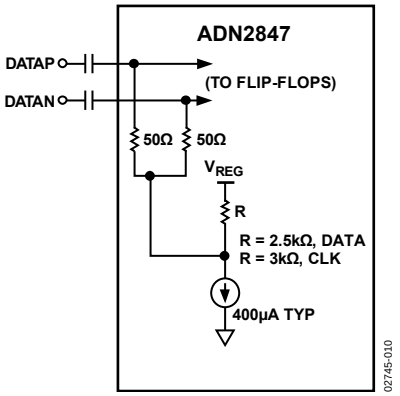


Figure 10. AC Coupling of Data Inputs

For input signals that exceed 500 mV p-p single-ended, it is necessary to insert an attenuation circuit as shown in Figure 11.

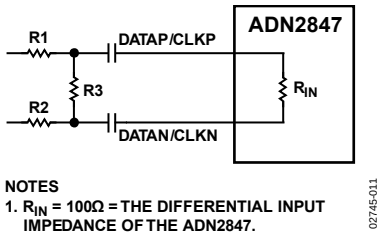


Figure 11. Attenuation Circuit

CCBIAS

When the laser is used in ac-coupled mode, the CCBIAS pin and the I_{BIAS} pin should be tied together (Figure 15). In dc-coupled mode, CCBIAS should be tied to V_{CC}.

I_{BIAS}

To achieve optimum eye quality, one pull-up resistor (R_Z) is necessary, as shown in both circuits in Figure 14 and Figure 15. The recommended resistor R_Z value is approximately 200 Ω ~ 500 Ω.

AUTOMATIC LASER SHUTDOWN

The ADN2847 ALS allows compliance to ITU-T-G958 (11/94), section 9.7. When ALS is logic high, both bias and modulation currents are turned off. Correct operation of ALS can be confirmed if the FAIL alarm is raised when ALS is asserted. Note that this is the only time DEGRADE is low while FAIL is high.

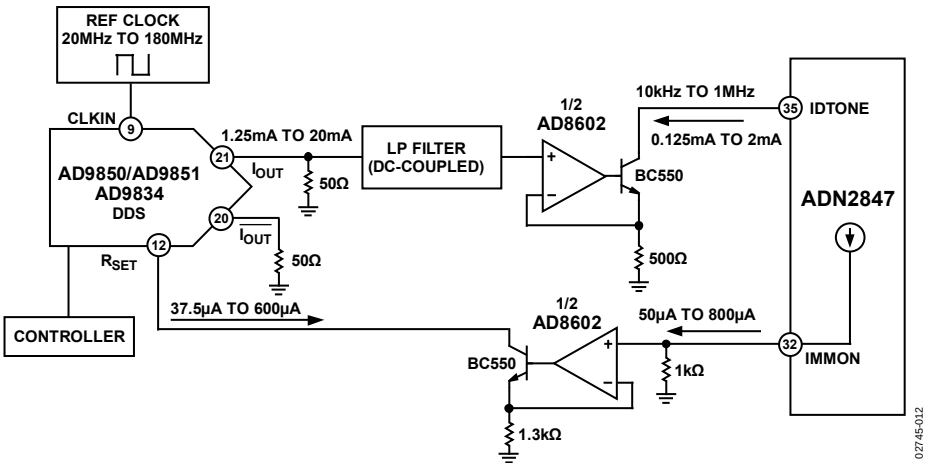


Figure 12. Application Circuit to Allow Fiber Identification Using the AD9850/AD9851

ALARM INTERFACES

The FAIL and DEGRADE outputs have an internal pull-up resistor of 30 kΩ, used to pull the digital high value to V_{CC}. However, the alarm can be overdriven with an external resistor allowing alarm interfacing to non-V_{CC} levels. Non-V_{CC} alarm output levels must be below the V_{CC} used for the ADN2847.

POWER CONSUMPTION

The ADN2847 die temperature must be kept below 125°C. Both LFCSP packages have an exposed paddle that should be connected in such a manner that is at the same potential as the ADN2847 ground pins. The θ_{JA} for both packages is specified in the Absolute Maximum Ratings section. Power consumption can be calculated using

$$I_{CC} = I_{CCMIN} + 0.3\ I_{MOD}$$

$$P = V_{CC} \times I_{CC} + (I_{BIAS} \times V_{BIAS_PIN}) + I_{MOD}\ (V_{MODP_PIN} + V_{MODN_PIN})/2$$

$$T_{DIE} = T_{AMBIENT} + \theta_{JA} \times P$$

Thus, the maximum combination of $I_{BIAS} + I_{MOD}$ must be calculated, where:

I_{CCMIN} = 50 mA (typical value of I_{CC} provided in the Specifications section)
$I_{BIAS} = I_{MOD} = 0$
T_{DIE} = die temperature
$T_{AMBIENT}$ = ambient temperature
V_{BIAS_PIN} = voltage at I_{BIAS} pin
V_{MODP_PIN} = average voltage at IMODP pin
V_{MODN_PIN} = average voltage at IMODN pin

LASER DIODE INTERFACING

Many laser diodes designed for 2.5 Gbps operation are packaged with an internal resistor to bring the effective impedance up to 25 Ω to minimize transmission line effects. In high current applications, the voltage drop across this resistor combined with the laser diode forward voltage makes direct connection between the laser and the driver impractical in a 3 V system. AC coupling the driver to the laser diode removes this headroom constraint.

Caution must be taken when choosing component values for ac coupling (see Figure 15) to ensure that the time constants (L/R and RC) are sufficiently long for the data rate and expected number of consecutive identical digits (CIDs). Failure to do this can lead to pattern dependent jitter and vertical eye closure.

For designs with low series resistance, or where external components become impractical, the ADN2847 supports direct connection to the laser diode (see Figure 14). In this case, care must be taken to ensure that the voltage drop across the laser diode does not violate the minimum compliance voltage on the IMODP pin.

OPTICAL SUPERVISOR

The PSET and ERSET potentiometers can be replaced with a dual-digital potentiometer, the ADN2850 (see Figure 13). The ADN2850 provides an accurate digital control for the average optical power and extinction ratio and ensures excellent stability over temperature.

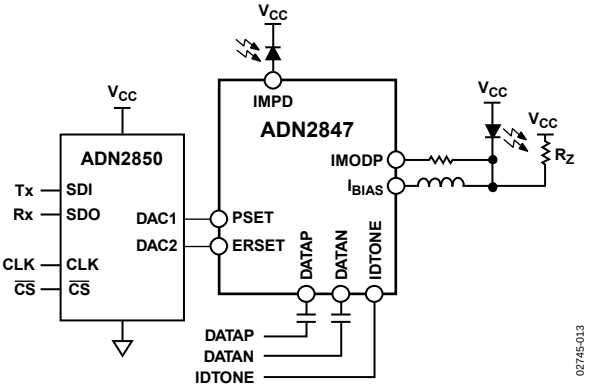


Figure 13. Application Using the ADN2850 a Dual 10-Bit Digital Potentiometer with an Extremely Low Temperature Coefficient as an Optical Supervisor

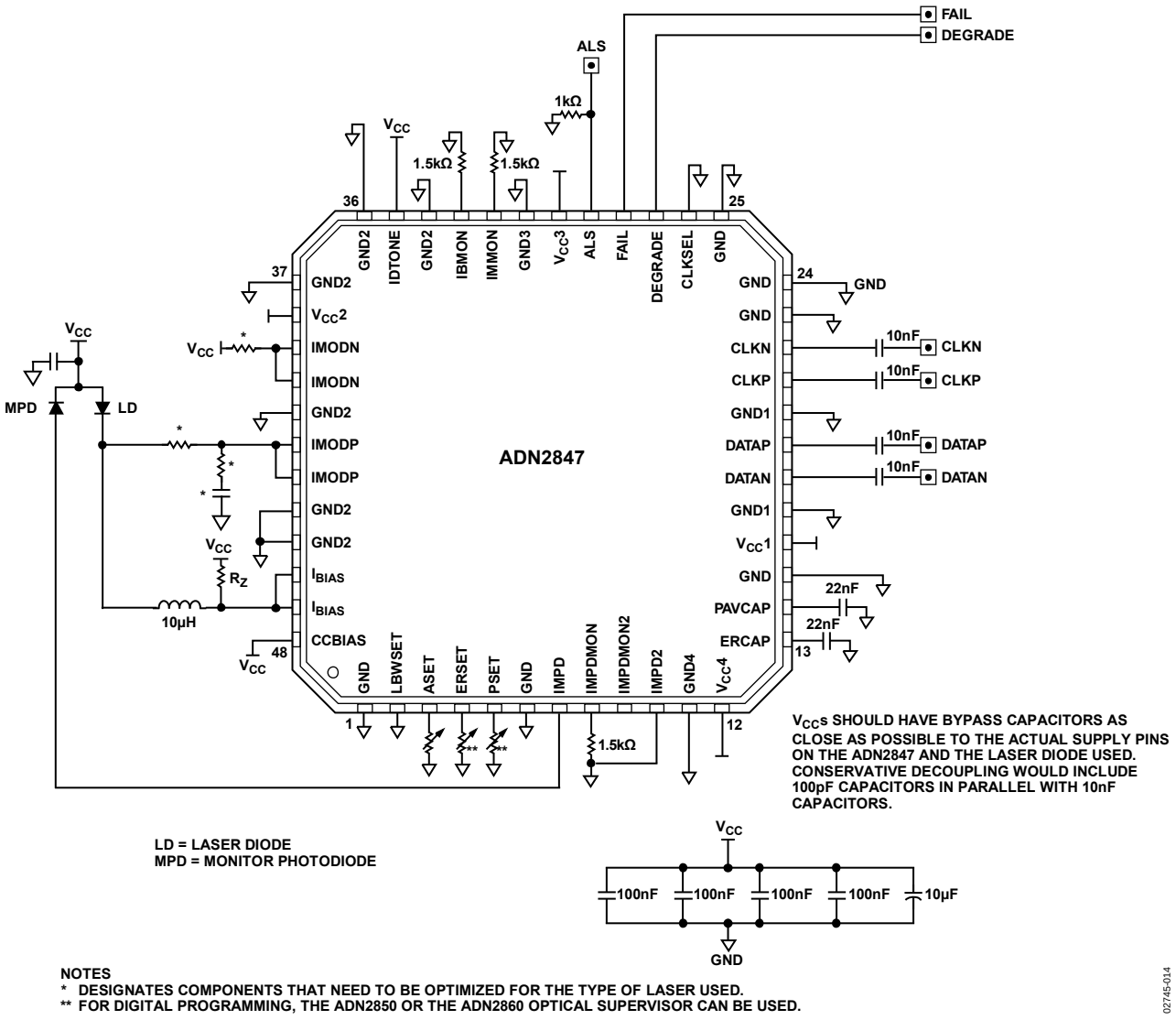


Figure 14. DC-Coupled 3.3 Gbps Test Circuit, Data Not Clocked

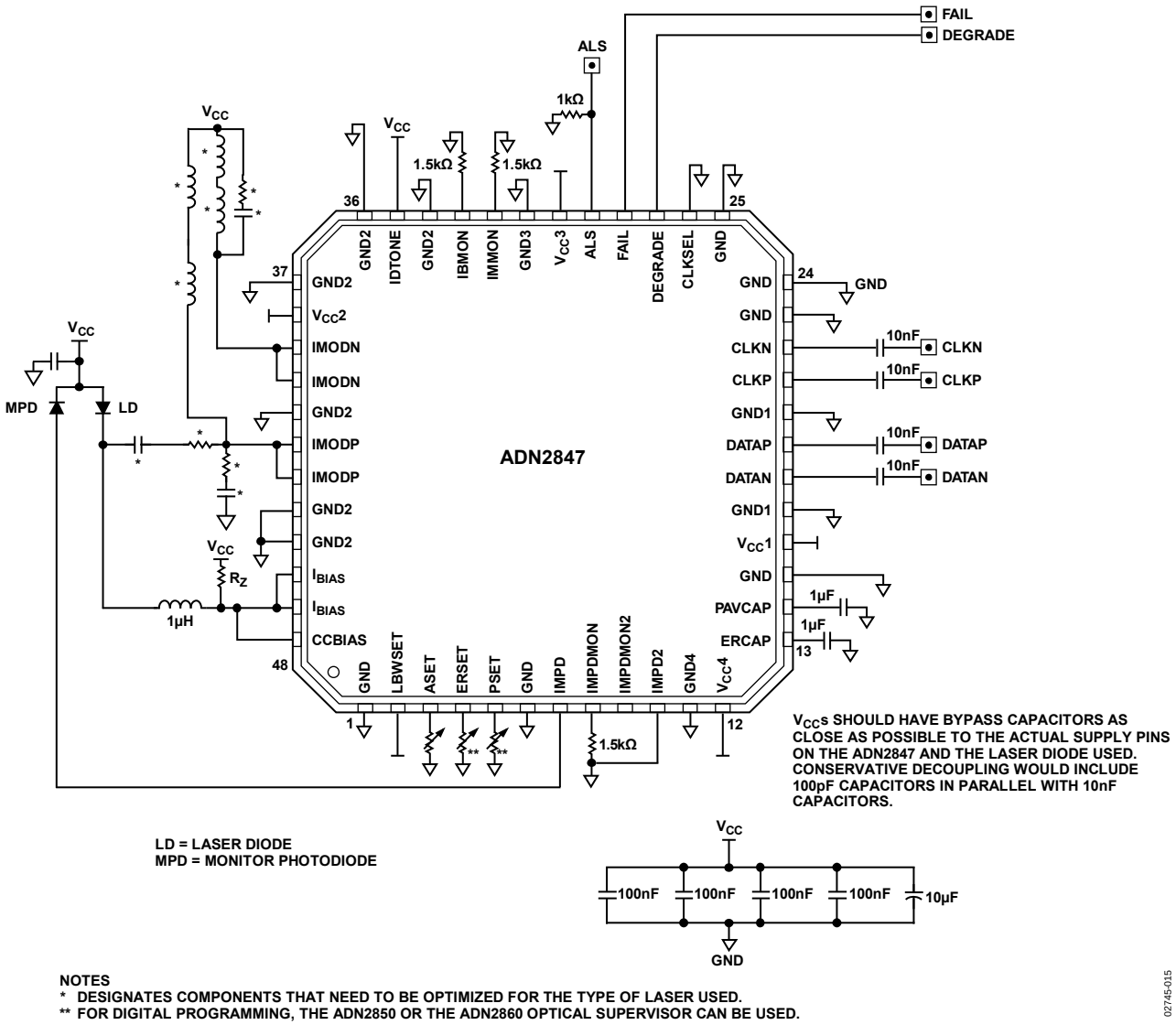


Figure 15. AC-Coupled 50 Mbps to 3.3 Gbps Test Circuit, Data Not Clocked

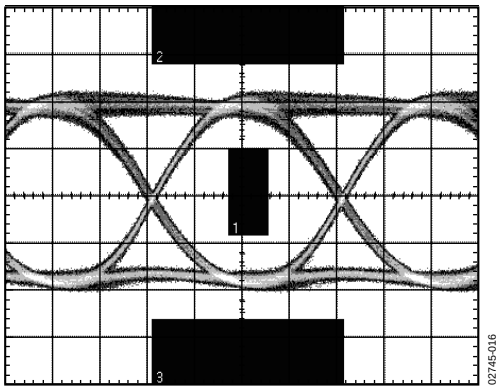


Figure 16. 2.5 Gbps Optical Eye at 25°C. Average Power = 0 dBm, Extinction Ratio = 10 dB, PRBS 31 Pattern. Eye Obtained Using a DFB Laser.

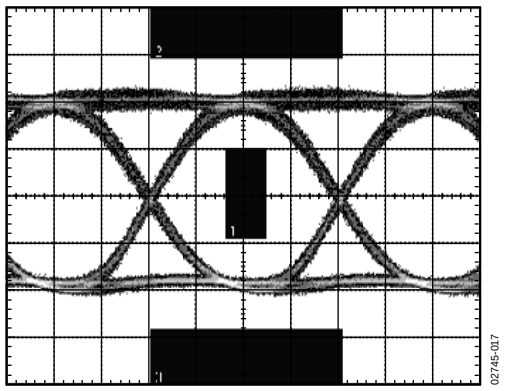
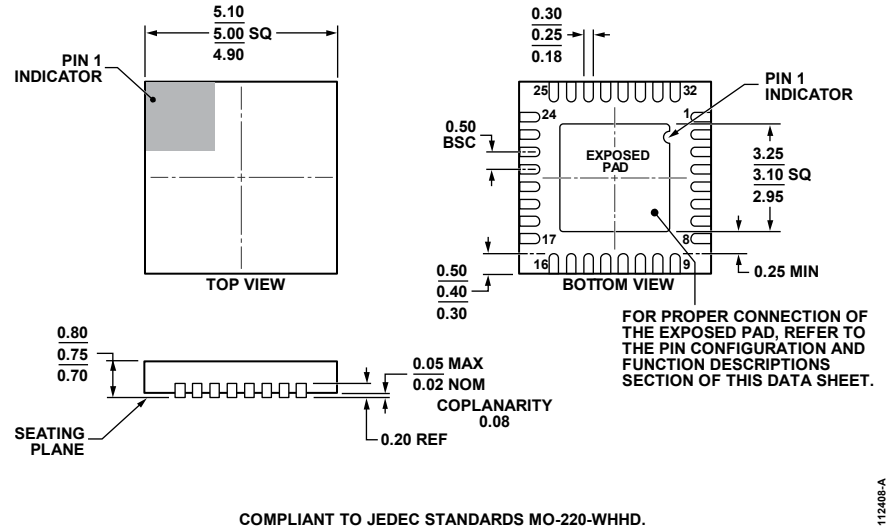


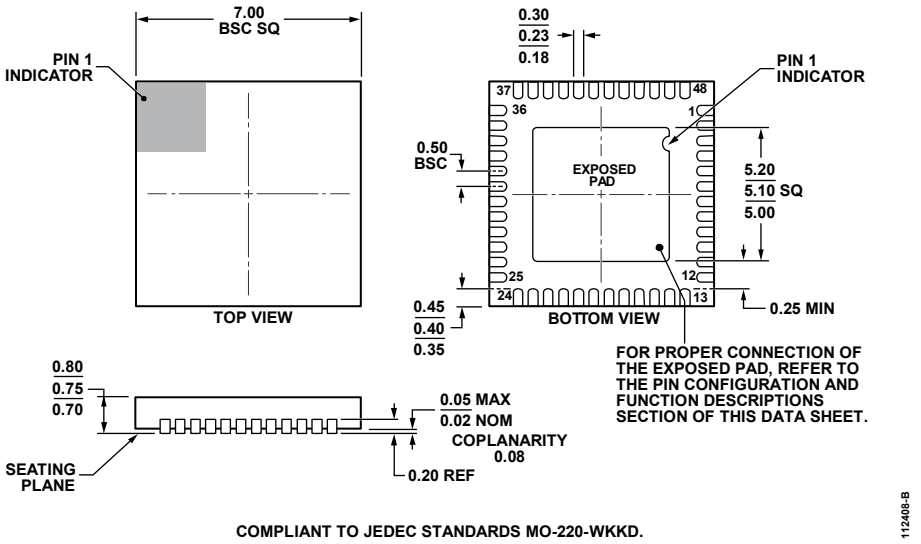
Figure 17. 2.5 Gbps Optical Eye at 85°C. Average Power = 0 dBm, Extinction Ratio = 10 dB, PRBS 31 Pattern. Eye Obtained Using a DFB Laser.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 18. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD.

Figure 19. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN2847ACPZ-32	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
ADN2847ACPZ-32-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
ADN2847ACPZ-32-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
ADN2847ACPZ-48	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-4

[1] Z = RoHS Compliant Part.

NOTES

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