OC-48/OC-48 FEC Clock and Data Recovery

Data Sheet **ADN2811**

FEATURES

- Meets SONET requirements for jitter transfer/generation/tolerance
- Quantizer sensitivity: 4 mV typical
- Adjustable slice level: ±100 mV
- 1.9 GHz minimum bandwidth
- Patented clock recovery architecture
- Loss of signal detect range: 3 mV to 15 mV
- Single reference clock frequency for both native SONET and 15/14 (7%) wrapper rate
- Choice of 19.44 MHz, 38.88 MHz, 77.76 MHz, or 155.52 MHz REFCLK
- LVPECL/LVDS/LVCMOS/LVTTL compatible inputs (LVPECL/LVDS only at 155.52 MHz)
- 19.44 MHz on-chip oscillator to be used with external crystal
- Loss of lock indicator
- Loopback mode for high speed test data
- Output squelch and bypass features
- Single-supply operation: 3.3 V
- Low power: 540 mW typical
- 7 mm × 7 mm, 48-lead LFCSP

APPLICATIONS

- SONET OC-48, SDH STM-16, and 15/14 FEC
- WDM transponders
- Regenerators/repeaters
- Test equipment
- Backplane applications

PRODUCT DESCRIPTION

The ADN2811 provides the receiver functions of quantization, signal level detect, and clock and data recovery at OC-48 and OC-48 FEC rates. All SONET jitter requirements are met, including jitter transfer, jitter generation, and jitter tolerance. All specifications are quoted for −40°C to +85°C ambient temperature, unless otherwise noted.

The device is intended for WDM system applications and can be used with either an external reference clock or an on-chip oscillator with external crystal. Both the 2.48 Gbps and 2.66 Gbps digital wrapper rates are supported by the ADN2811, without any change of reference clock.

This device, together with a PIN diode and a TIA preamplifier, can implement a highly integrated, low cost, low power, fiber optic receiver.

The receiver front end signal detect circuit indicates when the input signal level has fallen below a user-adjustable threshold. The signal detect circuit has hysteresis to prevent chatter at the output.

The ADN2811 is available in a compact, 7 mm × 7 mm, 48-lead chip scale package.

FUNCTIONAL BLOCK DIAGRAM

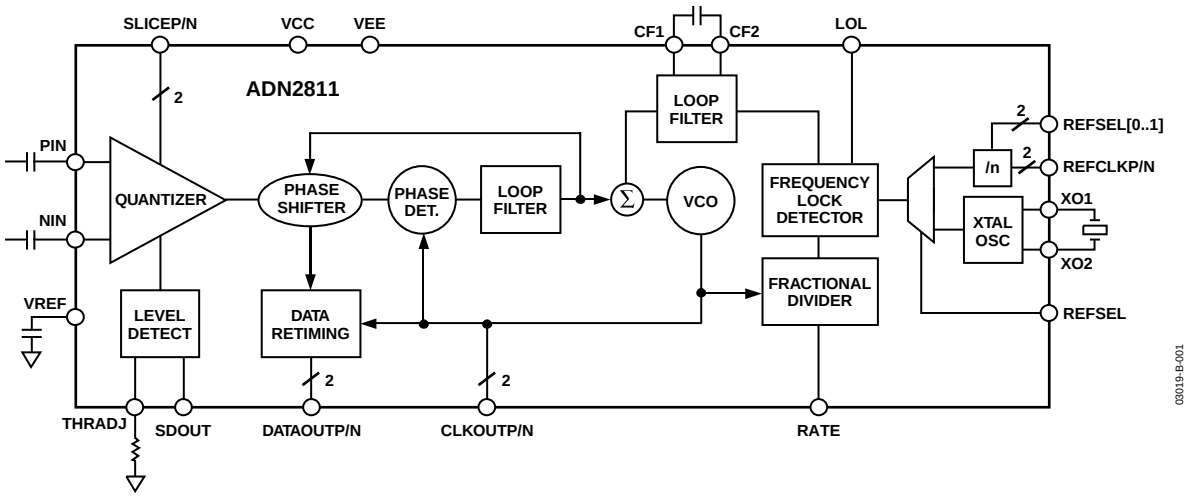

Figure 1.

Rev. C

Document Feedback

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SPECIFICATIONS

Table 1. $T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, V_{EE} = 0 V, C_F = 4.7 µF, SLICEP = SLICEN = VCC, unless otherwise noted

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
QUANTIZER—DC CHARACTERISTICS					
Input Voltage Range	At PIN or NIN, dc-coupled	0		1.2	V
Peak-to-Peak Differential Input				2.4	V
Input Common-Mode Level	DC-coupled. (See Figure 24)	0.4			V
Differential Input Sensitivity	PIN–NIN, ac-coupled[1], BER = 1×10^{-10}		4	10	mV p-p
Input Overdrive	Figure 6		2	5	mV p-p
Input Offset			500		µV
Input rms Noise	BER = 1×10^{-10}		244		µV rms
QUANTIZER—AC CHARACTERISTICS					
Upper –3 dB Bandwidth			1.9		GHz
Small Signal Gain	Differential		54		dB
S11	At 2.5 GHz		−15		dB
Input Resistance	Differential		100		Ω
Input Capacitance			0.65		pF
Pulse Width Distortion[2]			10		ps
QUANTIZER SLICE ADJUSTMENT					
Gain	SliceP – SliceN = ±0.5 V	0.115	0.200	0.300	V/V
Control Voltage Range	SliceP – SliceN	−0.8		+0.8	V
	At SliceP or SliceN	1.3		VCC	V
Slice Threshold Offset			±1.0		mV
LEVEL SIGNAL DETECT (SDOUT)					
Level Detect Range (See Figure 4)	R_{THRESH} = 2 kΩ	9.4	13.3	18.0	mV
	R_{THRESH} = 20 kΩ	2.5	5.3	7.6	mV
	R_{THRESH} = 90 kΩ	0.7	3.0	5.2	mV
Response Time, DC-Coupled		0.1	0.3	5	µs
Hysteresis (Electrical), PRBS 2^{23}	R_{THRESH} = 2 kΩ	5.6	6.6	7.8	dB
	R_{THRESH} = 20 kΩ	3.9	6.1	8.5	dB
	R_{THRESH} = 90 kΩ	3.2	6.7	9.9	dB
LOSS OF LOCK DETECT (LOL)					
LOL Response Time	From f_{VCO} error > 1000 ppm		60		µs
POWER SUPPLY VOLTAGE		3.0	3.3	3.6	V
POWER SUPPLY CURRENT		150	164	215	mA
PHASE-LOCKED LOOP CHARACTERISTICS	PIN – NIN = 10 mV p-p				
Jitter Transfer Bandwidth	OC-48		590	880	kHz
Jitter Peaking	OC-48		0.025		dB
Jitter Generation	OC-48, 12 kHz – 20 MHz			0.003[3]	UI rms
			0.05	0.09	UI p-p
Jitter Tolerance	OC-48 (See Figure 11)				
	600 Hz	92[3]			UI p-p
	6 kHz	20[3]			UI p-p
	100 kHz	5.5			UI p-p
	1 MHz	1.0[3]			UI p-p
CML OUTPUTS (CLKOUTP/N, DATAOUTP/N)					
Single-Ended Output Swing	V_{SE} (See Figure 5)	300	455	600	mV
Differential Output Swing	V_{DIFF} (See Figure 5)	600	910	1200	mV
Output High Voltage	V_{OH}		VCC		V
Output Low Voltage	V_{OL}	VCC – 0.6		VCC – 0.3	V
Rise Time	20% to 80%		84	150	ps
Fall time	80% to 20%		84	150	ps

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Setup Time	T_S (See Figure 3) OC-48	140			ps
Hold Time	T_H (See Figure 3) OC-48	150			ps
REFCLK DC INPUT CHARACTERISTICS					
Input Voltage Range	At REFCLKP or REFCLKN	0		VCC	V
Peak-to-Peak Differential Input		100			mV
Common-Mode Level	DC-Coupled, Single-Ended		VCC/2		V
TEST DATA DC INPUT CHARACTERISTICS[4] (TDINP/N)	CML Inputs				
Peak-to-Peak Differential Input Voltage			0.8		V
LVTTL DC INPUT CHARACTERISTICS					
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
Input Current	V_{IN} = 0.4 V or V_{IN} = 2.4 V	−5		+5	µA
LVTTL DC OUTPUT CHARACTERISTICS					
Output High Voltage	V_{OH}, I_{OH} = −2.0 mA	2.4			V
Output Low Voltage	V_{OL}, I_{OL} = +2.0 mA			0.4	V

[1] PIN and NIN must be differentially driven, ac-coupled for optimum sensitivity.
[2] PWD measurement made on quantizer outputs in Bypass mode.
[3] Measurement is equipment limited.
[4] TDINP/N are CML inputs. If the drivers to the TDINP/N inputs are anything other than CML, they must be ac-coupled.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
Supply Voltage (VCC)	5.5 V
Minimum Input Voltage (All Inputs)	VEE – 0.4 V
Maximum Input Voltage (All Inputs)	VCC + 0.4 V
Maximum Junction Temperature	165°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 Sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

48-lead LFCSP, 4-layer board with exposed paddle soldered to VCC. θ_{JA} = 25°C/W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

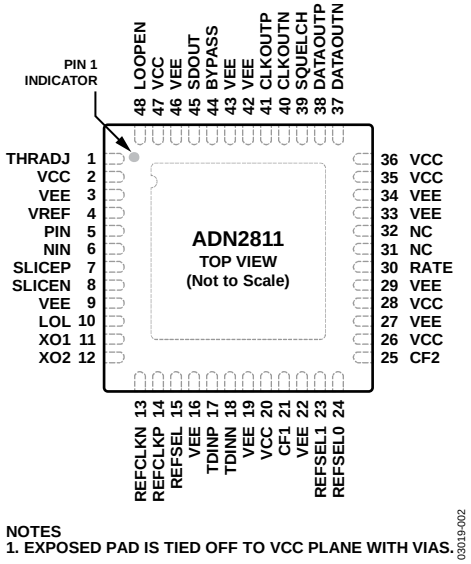


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	THRADJ	AI	LOS Threshold Setting Resistor.
2, 26, 28	VCC	P	Analog Supply.
3, 9, 16, 19, 22, 27, 29, 33, 34, 42, 43, 46	VEE	P	Ground.
4	VREF	AO	Internal VREF Voltage. Decouple to GND with a 0.1 µF capacitor.
5	PIN	AI	Differential Data Input. CML.
6	NIN	AI	Differential Data Input. CML.
7	SLICEP	AI	Differential Slice Level Adjust Input.
8	SLICEN	AI	Differential Slice Level Adjust Input.
10	LOL	DO	Loss of Lock Indicator. LVTTL active high.
11	XO1	AO	Crystal Oscillator.
12	XO2	AO	Crystal Oscillator.
13	REFCLKN	DI	Differential REFCLK Input. LVTTL, LVCMOS, LVPECL, LVDS (LVPECL, LVDS only at 155.52 MHz).
14	REFCLKP	DI	Differential REFCLK Input. LVTTL, LVCMOS, LVPECL, LVDS (LVPECL, LVDS only at 155.52 MHz).
15	REFSEL	DI	Reference Source Select. 0 = on-chip oscillator with external crystal; 1 = external clock source, LVTTL.
17	TDINP	AI	Differential Test Data Input.
18	TDINN	AI	Differential Test Data Input.
20, 47	VCC	P	Digital Supply.
21	CF1	AO	Frequency Loop Capacitor.
23	REFSEL1	DI	Reference Frequency Select (See Table 5) LVTTL.
24	REFSEL0	DI	Reference Frequency Select (See Table 5) LVTTL.
25	CF2	AO	Frequency Loop Capacitor.
30	RATE	DI	Data Rate Select (See Table 4) LVTTL.
31, 32	NC	DI	No Connect.
35, 36	VCC	P	Output Driver Supply.
37	DATAOUTN	DO	Differential Retimed Data Output. CML.
38	DATAOUTP	DO	Differential Retimed Data Output. CML.
39	SQUELCH	DI	Disable Clock and Data Outputs. Active high. LVTTL.
40	CLKOUTN	DO	Differential Recovered Clock Output. CML.
41	CLKOUTP	DO	Differential Recovered Clock Output. CML.
44	BYPASS	DI	Bypass CDR Mode. Active high. LVTTL.
45	SDOUT	DO	Loss of Signal Detect Output. Active high. LVTTL.
48	LOOPEN	DI	Enable Test Data Inputs. Active high. LVTTL.
Not applicable	EPAD	FP	Exposed Pad. Exposed pad is tied off to VCC plane with vias.

[1] Type: P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output, FP = floating pad.

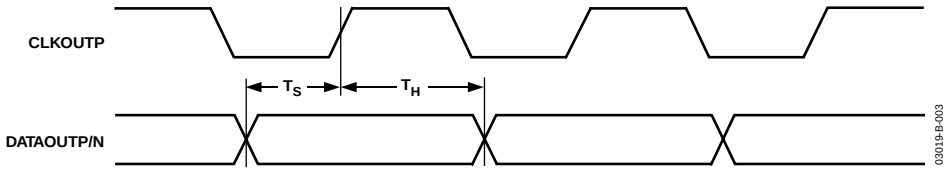


Figure 3. Output Timing

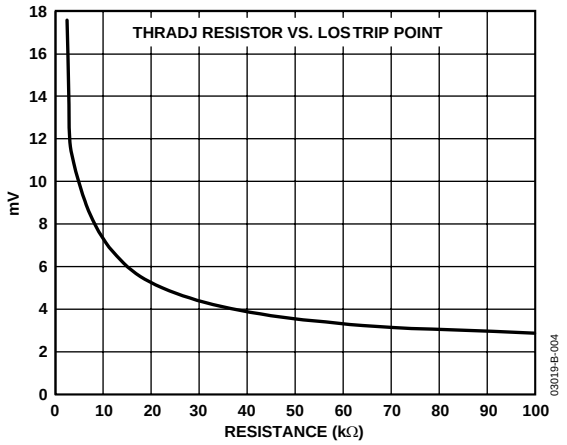


Figure 4. LOS Comparator Trip Point Programming

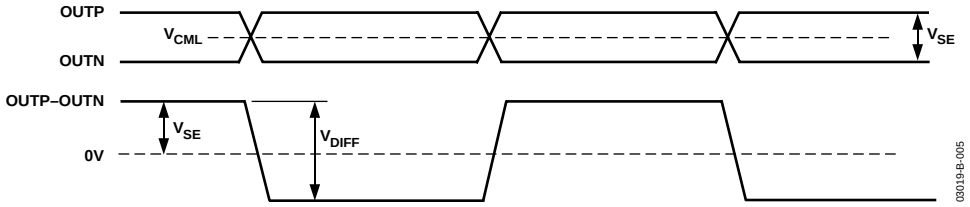


Figure 5. Single-Ended vs. Differential Output Specs

DEFINITION OF TERMS

MAXIMUM, MINIMUM, AND TYPICAL SPECIFICATIONS

Specifications for every parameter are derived from statistical analyses of data taken on multiple devices from multiple wafer lots. Typical specifications are the mean of the distribution of the data for that parameter. If a parameter has a maximum (or a minimum), that value is calculated by adding to (or subtracting from) the mean six times the standard deviation of the distribution. This procedure is intended to tolerate production variations. If the mean shifts by 1.5 standard deviations, the remaining 4.5 standard deviations still provide a failure rate of only 3.4 parts per million. For all tested parameters, the test limits are guardbanded to account for tester variation and therefore guarantee that no device is shipped outside of data sheet specifications.

INPUT SENSITIVITY AND INPUT OVERDRIVE

Sensitivity and overdrive specifications for the quantizer involve offset voltage, gain, and noise. The relationship between the logic output of the quantizer and the analog voltage input is shown in Figure 6. For a sufficiently large positive input voltage, the output is always Logic 1; similarly for negative inputs, the output is always Logic 0. However, the transitions between output Logic Levels 1 and 0 are not at precisely defined input voltage levels but occur over a range of input voltages. Within this zone of confusion, the output may be either 1 or 0, or it may even fail to attain a valid logic state. The width of this zone is determined by the input voltage noise of the quantizer. The center of the zone of confusion is the quantizer input offset voltage. Input overdrive is the magnitude of signal required to guarantee the correct logic level with 1×10^{-10} confidence level.

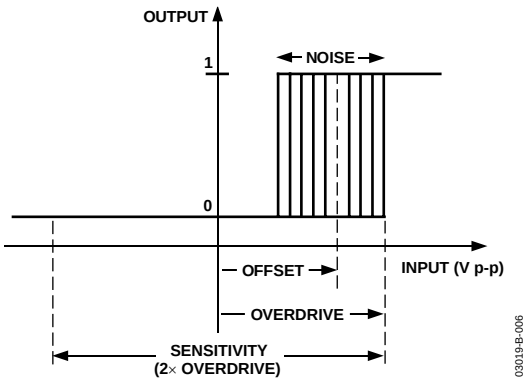


Figure 6. Input Sensitivity and Input Overdrive

SINGLE-ENDED VS. DIFFERENTIAL

AC-coupling typically drives the inputs to the quantizer. The inputs are internally dc biased to a common-mode potential of ~0.6 V. Driving the ADN2811 single-ended and observing the quantizer input with an oscilloscope probe at the point indicated in Figure 7 shows a binary signal with an average value equal to the common-mode potential and instantaneous values both above and below the average value. It is convenient to measure the peak-to-peak amplitude of this signal and call the minimum required value the quantizer sensitivity. Referring to Figure 6, since both positive and negative offsets need to be accommodated, the sensitivity is twice the overdrive.

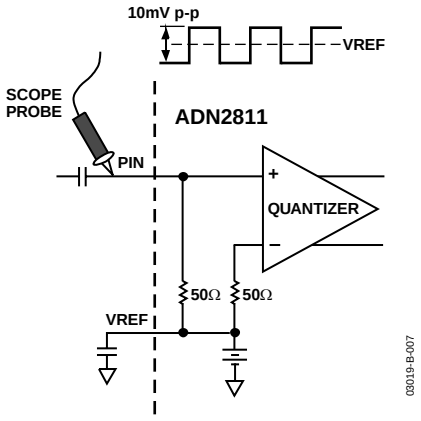


Figure 7. Single-Ended Sensitivity Measurement

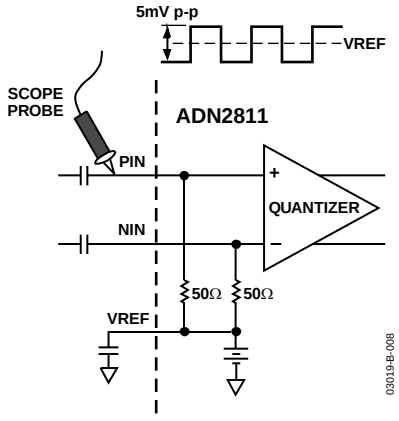


Figure 8. Differential Sensitivity Measurement

Driving the ADN2811 differentially (see Figure 8), sensitivity seems to improve by observing the quantizer input with an oscilloscope probe. This is an illusion caused by the use of a single-ended probe. A 5 mV p-p signal appears to drive the ADN2811 quantizer. However, the single-ended probe measures only half the signal. The true quantizer input signal is twice this value since the other quantizer input is complementary to the signal being observed.

LOS RESPONSE TIME

The LOS response time is the delay between the removal of the input signal and the indication of loss of signal (LOS) at SDOUT. The LOS response time of the ADN2811 is 300 ns typ when the inputs are dc-coupled. In practice, the time constant of the ac-coupling at the quantizer input determines the LOS response time.

JITTER SPECIFICATIONS

The ADN2811 CDR is designed to achieve the best bit-error-rate (BER) performance, and has exceeded the jitter generation, transfer, and tolerance specifications proposed for SONET/SDH equipment defined in the Telcordia Technologies specification.

Jitter is the dynamic displacement of digital signal edges from their long-term average positions measured in UI (unit intervals), where 1 UI = 1 bit period. Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

The following sections briefly summarize the specifications of jitter generation, transfer, and tolerance in accordance with the Telcordia document (GR-253-CORE, Issue 3, September 2000) for the optical interface at the equipment level and the ADN2811 performance with respect to those specifications.

Jitter Generation

Jitter generation specification limits the amount of jitter that can be generated by the device with no jitter and wander applied at the input. For OC-48 devices, the band-pass filter has a 12 kHz high-pass cutoff frequency with a roll-off of 20 dB/decade and a low-pass cutoff frequency of at least 20 MHz. The jitter generated must be less than 0.01 UI rms and 0.1 UI p-p.

Jitter Transfer

Jitter transfer function is the ratio of the jitter on the output signal to the jitter applied on the input signal versus the frequency. This parameter measures the limited amount of jitter on an input signal that can be transferred to the output signal (see Figure 9).

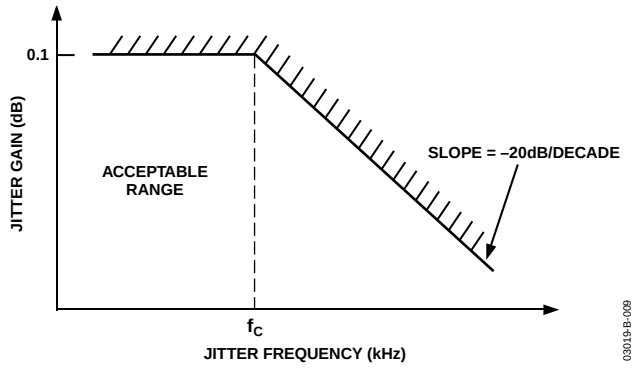


Figure 9. Jitter Transfer Curve

Jitter Tolerance

Jitter tolerance is defined as the peak-to-peak amplitude of the sinusoidal jitter applied on the input signal that causes a 1 dB power penalty. This is a stress test that is intended to ensure no additional penalty is incurred under the operating conditions (see Figure 10). Figure 11 shows the typical OC-48 jitter tolerance performance of the ADN2811.

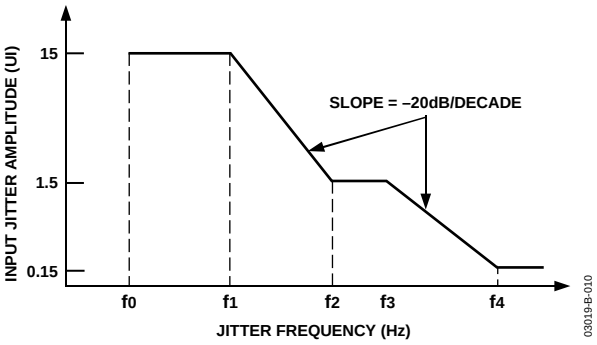


Figure 10. SONET Jitter Tolerance Mask

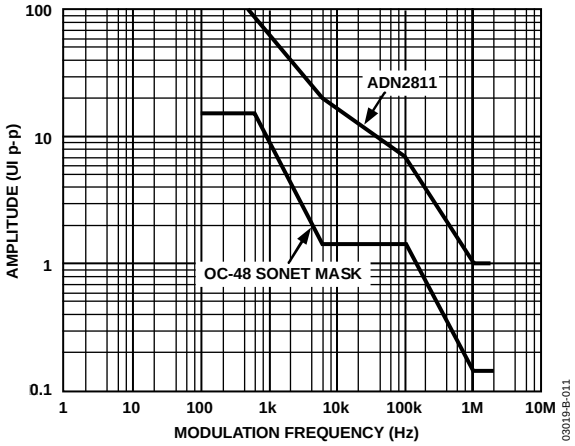


Figure 11. OC-48 Jitter Tolerance Curve

THEORY OF OPERATION

The ADN2811 is a delay-locked and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops that share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of the input jitter. A separate phase control loop, comprised of the VCO, tracks the low frequency components of the input jitter. The initial frequency of the VCO is set by yet a third loop, which compares the VCO frequency with the reference frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the VCO by the fine tuning control.

The delay-locked and phase-locked loops together track the phase of the input data signal. For example, when the clock lags input data, the phase detector drives the VCO to a higher frequency and also increases the delay through the phase shifter. Both of these actions serve to reduce the phase error between the clock and data. The faster clock picks up phase while the delayed data loses phase. Since the loop filter is an integrator, the static phase error is driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for the frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path and therefore does not appear in the closed-loop transfer function. Jitter peaking in a conventional second-order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Since this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay- and phase-locked loops together simultaneously provide wideband jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 12 shows that the jitter transfer function, Z(s)/X(s), is a second-order low-pass providing excellent filtering. Note that the jitter transfer has no zero, unlike an ordinary second-order phase-locked loop. This means the main phase-locked loop has low jitter peaking (see Figure 13), which makes this circuit ideal for signal regenerator applications where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

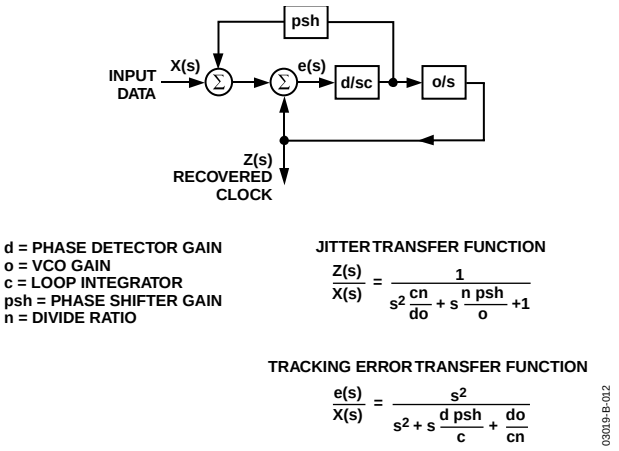


Figure 12. Phase-Locked Loop/Delay-Locked Loop Architecture

The error transfer, e(s)/X(s), has the same high-pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wideband jitter accommodation since the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering.

The delay- and phase-locked loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case, the VCO is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the VCO tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of the range, and therefore contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the VCO are not large enough to track the input jitter. In this case, the VCO control voltage becomes large and saturates, and the VCO frequency dwells at one or the other extreme of the tuning range. The size of the VCO tuning range therefore has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger; thus the phase shifter takes on the burden of tracking input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of 2 UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region, the gain of the integrator determines the jitter accommodation. Since the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. Jitter accommodation is roughly 0.5 UI in this region. The corner frequency between the declining slope and the flat region is the closed-loop bandwidth of the delay-locked loop, which is roughly 5 MHz.

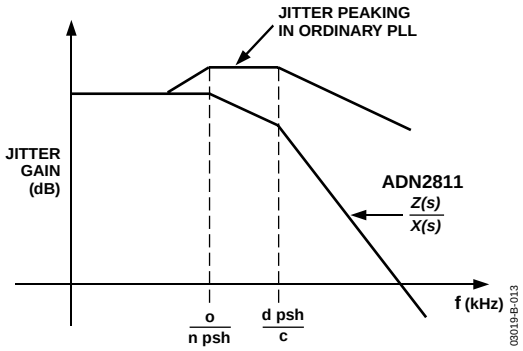


Figure 13. Jitter Response vs. Conventional PLL

FUNCTIONAL DESCRIPTION

CLOCK AND DATA RECOVERY

The ADN2811 recovers clock and data from serial bit streams at OC-48 as well as the 15/14 FEC rates. The data rate is selected by the RATE input (see Table 4).

Table 4. Data Rate Selection

RATE	Data Rate	Frequency (MHz)
0	OC-48	2488.32
1	OC-48 FEC	2666.06

LIMITING AMPLIFIER

The limiting amplifier has differential inputs (PIN/NIN) that are internally terminated with 50 Ω to an on-chip voltage reference (VREF = 0.6 V typically). These inputs are normally ac-coupled, although dc coupling is possible as long as the input common-mode voltage remains above 0.4 V (see Figure 22, Figure 23, and Figure 24). Input offset is factory trimmed to achieve better than 4 mV typical sensitivity with minimal drift. The limiting amplifier can be driven differentially or single-ended.

SLICE ADJUST

The quantizer slicing level can be offset by ±100 mV to mitigate the effect of amplified spontaneous emission (ASE) noise by applying a differential voltage input of ±0.8 V to SLICEP/N inputs. If no adjustment of the slice level is needed, SLICEP/N must be tied to VCC.

LOSS OF SIGNAL (LOS) DETECTOR

The receiver front end level signal detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The threshold is set with a single external resistor from Pin 1, THRADJ, to GND. The LOS comparator trip point versus the resistor value is illustrated in Figure 4 (this is only valid for SLICEP = SLICEN = VCC). If the input level to the ADN2811 drops below the programmed LOS threshold, SDOUT (Pin 45) indicates the loss of signal condition with a Logic 1. The LOS response time is ~300 ns by design, but is dominated by the RC time constant in ac-coupled applications.

If using the LOS detector, the quantizer slice adjust pins must both be tied to VCC. This is to avoid interaction with the LOS threshold level.

Note that it is not expected to use both LOS and slice adjust at the same time; systems with optical amplifiers need the slice adjust to evade ASE. However, a loss of signal in an optical link that uses optical amplifiers causes the optical amplifier output to be full-scale noise. Under this condition, the LOS does not detect the failure. In this case, the loss of lock signal indicates the failure because the CDR circuitry is unable to lock onto a signal that is full-scale noise.

REFERENCE CLOCK

There are three options for providing the reference frequency to the ADN2811: differential clock, single-ended clock, or crystal oscillator. See Figure 14, Figure 15, and Figure 16 for example configurations.

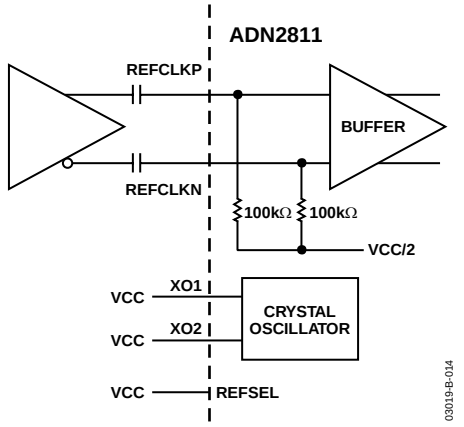


Figure 14. Differential REFCLK Configuration

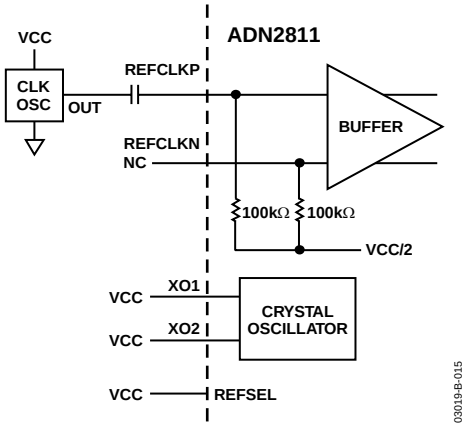


Figure 15. Single-Ended REFCLK Configuration

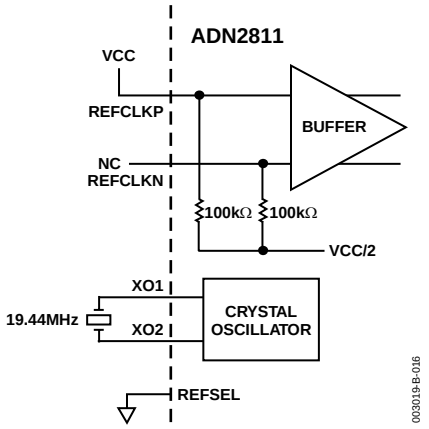


Figure 16. Crystal Oscillator Configuration

The ADN2811 can accept any of the following reference clock frequencies: 19.44 MHz, 38.88 MHz, 77.76 MHz at LVTTL/LVCMOS/LVPECL/LVDS levels, or 155.52 MHz at LVPECL/LVDS levels via the REFCLKN/P inputs, independent of data rate. The input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (for example, LVPECL or LVDS) or a standard single-ended low voltage TTL input, providing maximum system flexibility. The appropriate division ratio can be selected using the REFSEL0/1 pins, according to Table 5. Phase noise and duty cycle of the reference clock are not critical, and 100 ppm accuracy is sufficient.

Table 5. Reference Frequency Selection

REFSEL	REFSEL[1..0]	Applied Reference Frequency (MHz)
1	00	19.44
1	01	38.88
1	10	77.76
1	11	155.52
0	XX	REFCLKP/N Inactive. Use 19.44 MHz XTAL oscillator on Pins XO1, XO2 (Pull REFCLKP to VCC).

An on-chip oscillator to be used with an external crystal is also provided as an alternative to using the REFCLKN/P inputs. Details of the recommended crystal are given in Table 6.

Table 6. Required Crystal Specifications

Parameter	Value
Mode	Series Resonant
Frequency/Overall Stability	19.44 MHz ±100 ppm
Frequency Accuracy	±100 ppm
Temperature Stability	±100 ppm
Aging	±100 ppm
ESR	50 Ω max

REFSEL must be tied to VCC when the REFCLKN/P inputs are active, or tied to VEE when the oscillator is used. No connection between the XO pin and REFCLK input is necessary (see Figure 14, Figure 15, and Figure 16). Note that the crystal must operate in series resonant mode, which renders it insensitive to external parasitics. No trimming capacitors are required.

LOCK DETECTOR OPERATION

The lock detector monitors the frequency difference between the VCO and the reference clock and deasserts the loss of lock signal when the VCO is within 500 ppm of center frequency (see Figure 17). This enables the phase loop, which pulls the VCO frequency in the remaining amount and also acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is reasserted and control returns to the frequency loop, which reacquires and maintains a stable clock signal at the output.

The frequency loop requires a single external capacitor between CF1 and CF2. The capacitor specification is given in Table 7.

Table 7. Recommended C_F Capacitor Specification

Parameter	Value
Temperature Range	−40°C to +85°C
Capacitance	>3.0 µF
Leakage	<80 nA
Rating	>6.3 V

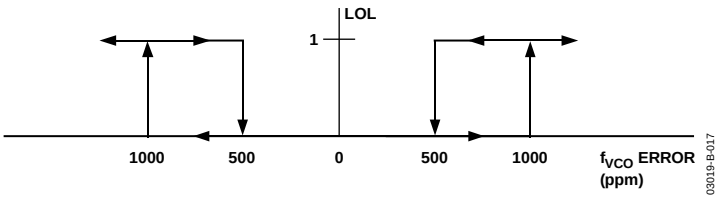


Figure 17. Transfer Function of LOL

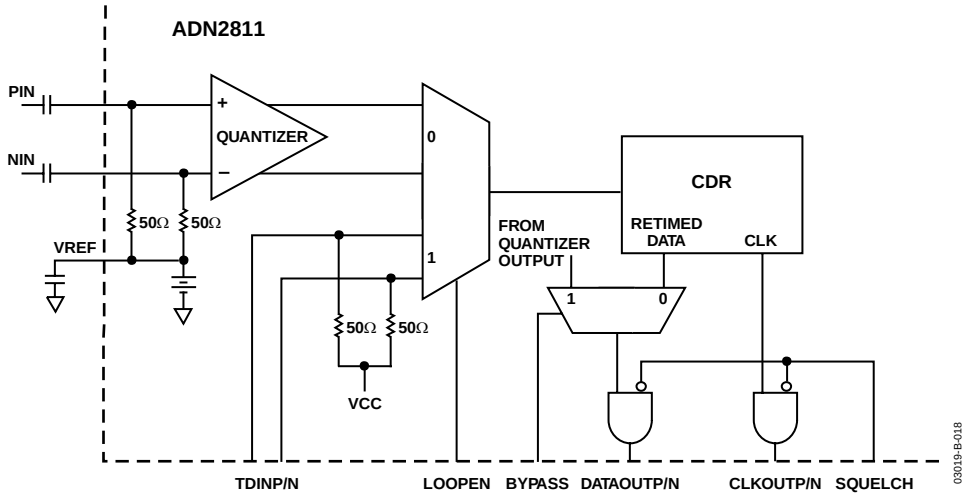


Figure 18. Test Modes

SQUELCH MODE

When the squelch input is driven to a TTL high state, both the clock and data outputs are set to the zero state to suppress downstream processing. If desired, this pin can be directly driven by the LOS detector output, SDOUT. If the squelch function is not required, the pin must be tied to VEE.

TEST MODES: BYPASS AND LOOPBACK

When the bypass input is driven to a TTL high state, the quantizer output is connected directly to the buffers driving the data out pins, thus bypassing the clock recovery circuit (see Figure 18). This feature can help the system deal with nonstandard bit rates.

The loopback mode can be invoked by driving the LOOPEN pin to a TTL high state, which facilitates system diagnostic testing. This connects the test inputs (TDINP/N) to the clock and data recovery circuit (per Figure 18). The test inputs have internal 50 Ω terminations and can be left floating when not in use. TDINP/N are CML inputs and can only be dc-coupled when being driven by CML outputs. The TDINP/N inputs must be ac-coupled if being driven by anything other than CML outputs. Bypass and loopback modes are mutually exclusive. Only one of these modes can be used at any given time. The ADN2811 is put into an indeterminate state if the BYPASS and LOOPEN pins are set to Logic 1 at the same time.

APPLICATIONS INFORMATION

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

Use of one low impedance ground plane to both analog and digital grounds is recommended. The VEE pins must be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias may be used in parallel to reduce the series inductance, especially on Pins 33 and 34, which are the ground returns for the output buffers.

Use of a 10 µF electrolytic capacitor between VCC and GND is recommended at the location where the 3.3 V supply enters the PCB. 0.1 µF and 1 nF ceramic chip capacitors must be placed between IC power supply VCC and GND as close as possible to the ADN2811 VCC pins. Again, if connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance, especially on Pins 35 and 36, which supply power to the high speed CLKOUTP/N and DATAOUTP/N output buffers. Refer to the schematic in Figure 19 for recommended connections.

Transmission Lines

Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections, including PIN, NIN, CLKOUTP, CLKOUTN, DATAOUTP, and DATAOUTN (also REFCLKP, REFCLKN for a 155.2 MHz REFCLK). It is also recommended that the PIN/NIN input traces are matched in length and that the CLKOUTP/N and DATAOUTP/N output traces are matched in length. All high speed CML outputs, CLKOUTP/N and DATAOUTP/N, also require 100 Ω back termination chip resistors connected between the output pin and VCC. These resistors must be placed as close as possible to the output pins. These 100 Ω resistors are in parallel with on-chip 100 Ω termination resistors to create a 50 Ω back termination (see Figure 20).

The high speed inputs, PIN and NIN, are internally terminated with 50 Ω to an internal reference voltage (see Figure 21). A 0.1 µF capacitor is recommended between VREF, Pin 4, and GND to provide an ac ground for the inputs.

As with any high speed mixed-signal design, care must be taken to keep all high speed digital traces away from sensitive analog nodes.

Soldering Guidelines for Chip-Scale Package

The lands on the 48-lead LFCSP are rectangular. The printed circuit board pad for these must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land must be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the printed circuit board must be at least as large as this exposed pad. The user must connect the exposed pad to analog VCC.

If vias are used, they must be incorporated into the pad at 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz. copper to plug the via.

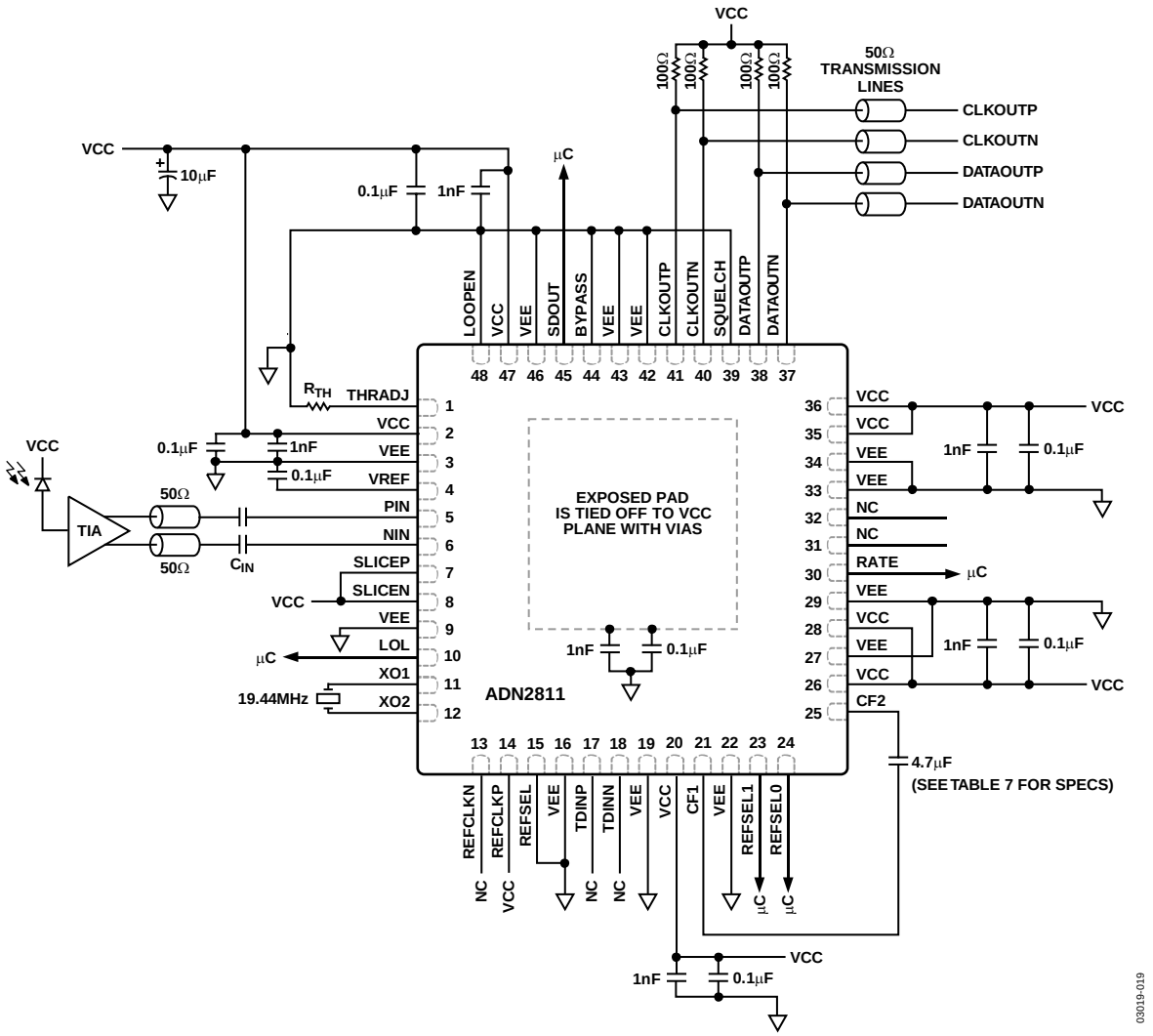


Figure 19. Typical Application Circuit

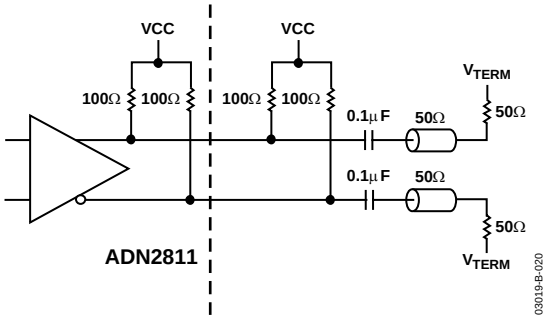


Figure 20. AC-Coupled Output Configuration

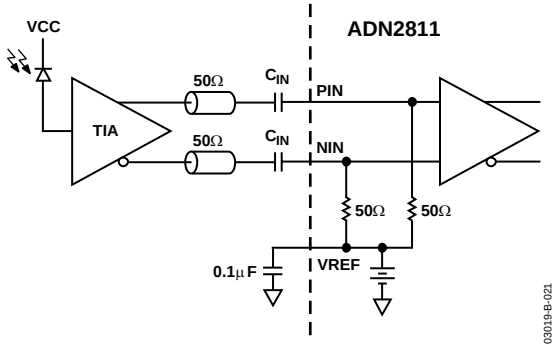
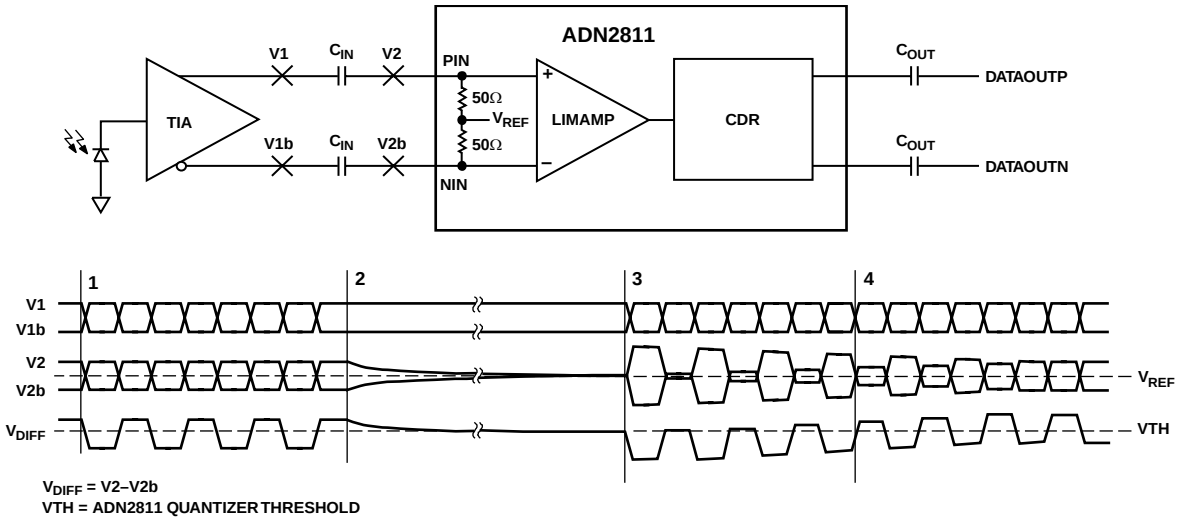


Figure 21. AC-Coupled Input Configuration

CHOOSING AC-COUPLING CAPACITORS

The choice of ac-coupling capacitors at the input (PIN, NIN) and output (DATAOUTP, DATAOUTN) of the ADN2811 must be chosen carefully. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can drop due to baseline wander (see Figure 22), causing pattern dependent jitter (PDJ).

For the ADN2811 to work robustly at OC-48, a minimum capacitor of 0.1 µF to PIN/NIN and 0.1 µF on DATAOUTP/DATAOUTN must be used. This is based on the assumption that 1000 CIDs must be tolerated and that the PDJ must be limited to 0.01 UI p-p.



NOTES
1. DURING DATA PATTERNS WITH HIGH TRANSITION DENSITY, DIFFERENTIAL DC VOLTAGE AT V1 AND V2 IS 0.
2. WHEN THE OUTPUT OF THE TIA GOES TO CID, V1 AND V1b ARE DRIVEN TO DIFFERENT DC LEVELS. V2 AND V2b DISCHARGE TO THE V_{REF} LEVEL, WHICH EFFECTIVELY INTRODUCES A DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS.
3. WHEN THE BURST OF DATA STARTS AGAIN, THE DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS IS APPLIED TO THE INPUT LEVELS, CAUSING A DC SHIFT IN THE DIFFERENTIAL INPUT. THIS SHIFT IS LARGE ENOUGH SUCH THAT ONE OF THE STATES, EITHER HIGH OR LOW DEPENDING ON THE LEVELS OF V1 AND V1b WHEN THE TIA WENT TO CID, IS CANCELLED OUT. THE QUANTIZER WILL NOT RECOGNIZE THIS AS A VALID STATE.
4. THE DC OFFSET SLOWLY DISCHARGES UNTIL THE DIFFERENTIAL INPUT VOLTAGE EXCEEDS THE SENSITIVITY OF THE ADN2811. THE QUANTIZER WILL BE ABLE TO RECOGNIZE BOTH HIGH AND LOW STATES AT THIS POINT.

03019-B-022

Figure 22. Example of Baseline Wander

DC-COUPLED APPLICATION

The inputs to the ADN2811 can also be dc-coupled. This may be necessary in burst mode applications where there are long periods of CIDs and baseline wander cannot be tolerated. If the inputs to the ADN2811 are dc-coupled, care must be taken not to violate the input range and common-mode level requirements of the ADN2811 (see Figure 23, Figure 24, and Figure 25). If dc-coupling is required and the output levels of the TIA do not adhere to the levels shown in Figure 24 and Figure 25, there needs to be level shifting and/or an attenuator between the TIA outputs and the ADN2811 inputs.

LOL TOGGLING DURING LOSS OF INPUT DATA

If the input data stream is lost due to a break in the optical link (or for any reason), the clock output from the ADN2811 stays within 1000 ppm of the VCO center frequency as long as there is a valid reference clock. The LOL pin toggles at a rate of several kHz because the LOL pin toggles between a Logic 1 and a Logic 0 while the frequency loop and phase loop swap control of the VCO. The chain of events is as follows:

- The ADN2811 is locked to the input data stream; LOL = 0.
- The input data stream is lost due to a break in the link. The VCO frequency drifts until the frequency error is greater than 1000 ppm. LOL is asserted to a Logic 1 as control of the VCO is passed back to the frequency loop.
- The frequency loop pulls the VCO to within 500 ppm of the center frequency. Control of the VCO is passed back to the phase loop and LOL is deasserted to a Logic 0.
- The phase loop tries to acquire, but there is no input data present so the VCO frequency drifts.
- The VCO frequency drifts until the frequency error is greater than 1000 ppm. LOL is asserted to a Logic 1 as control of the VCO is passed back to the frequency loop. This process is repeated until a valid input data stream is re-established.

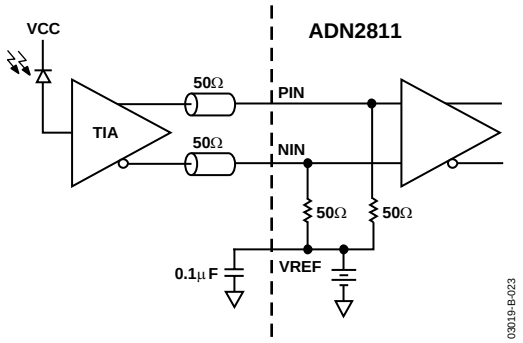


Figure 23. ADN2811 with DC-Coupled Inputs

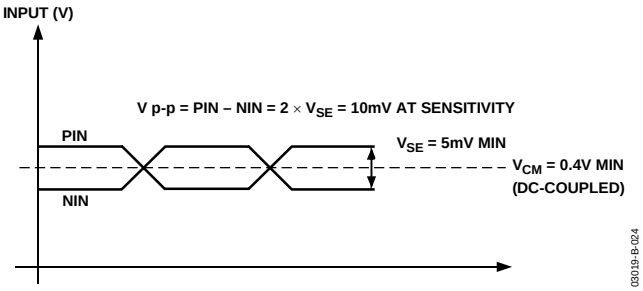


Figure 24. Minimum Allowed DC-Coupled Input Levels

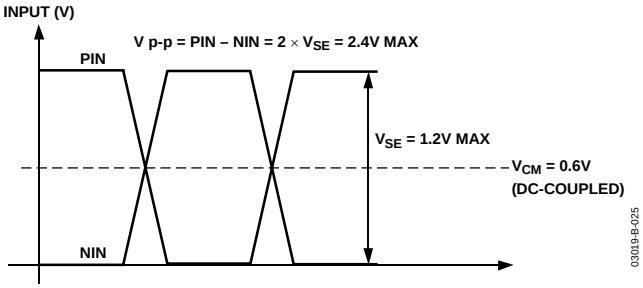
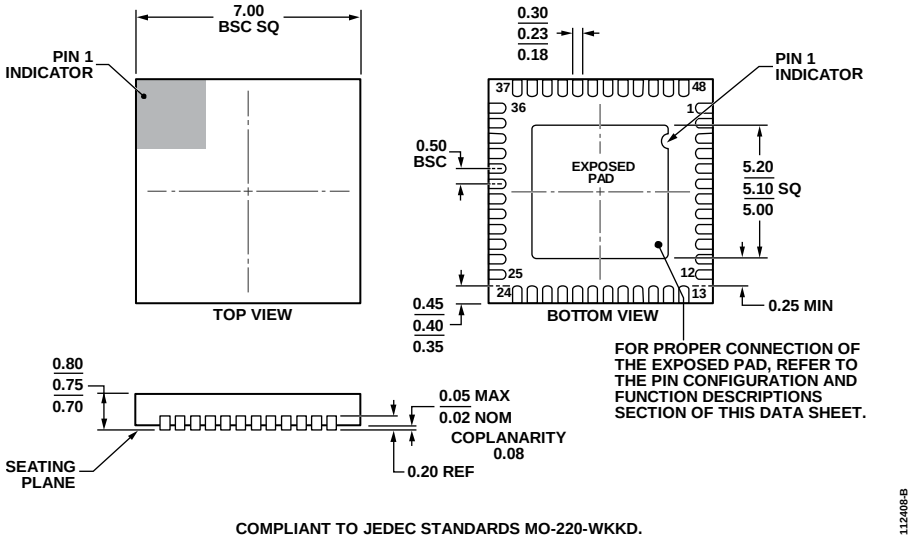


Figure 25. Maximum Allowed DC-Coupled Input Levels

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD.

Figure 26. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN2811ACPZ-CML	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-4
ADN2811ACPZ-CML-RL	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package, Tape-Reel, 2500 pcs [LFCSP]	CP-48-4
EVAL-ADN2811-CML		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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