800 mA Ultralow Noise, High PSRR, RF Linear Regulator

Data Sheet

ADM7151

FEATURES

- Input voltage range: 4.5 V to 16 V
- Maximum output current: 800 mA
- Adjustable output from 1.5 V to 5.1 V
- Low noise
  - 1.0 µV rms total integrated noise from 100 Hz to 100 kHz
  - 1.6 µV rms total integrated noise from 10 Hz to 100 kHz
- Noise spectral density: 1.7 nV√Hz from 10 kHz to 1 MHz
- Power supply rejection ratio (PSRR) at 400 mA load
  - >90 dB from 1 kHz to 100 kHz, V_{OUT} = 5 V
  - >60 dB at 1 MHz, V_{OUT} = 5 V
- Dropout voltage: 0.6 V at V_{OUT} = 5 V, 800 mA load
- Initial voltage accuracy: ±1%
- Voltage accuracy over line, load and temperature: ±2%
- Quiescent current (I_{GND}): 4.3 mA at no load
- Low shutdown current: 0.1 µA
- Stable with a 10 µF ceramic output capacitor
- 8-lead LFCSP package and 8-lead SOIC package

APPLICATIONS

- Regulated power noise sensitive applications
  - RF mixers, phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), and PLLs with integrated VCOs
- Clock distribution circuits
- Ultrasound and other imaging applications
- High speed RF transceivers
- High speed, 16-bit or greater ADCs
- Communications and infrastructure
- Cable digital-to-analog converter (DAC) drivers

TYPICAL APPLICATION CIRCUIT

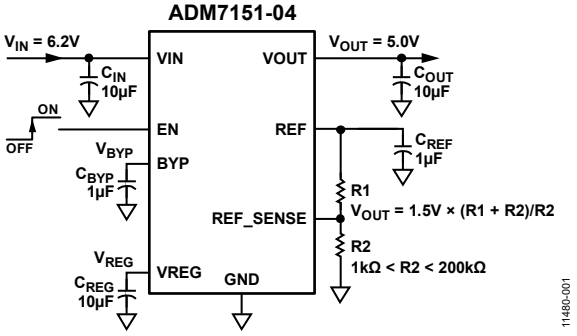


Figure 1. ADM7151-04 with V_{OUT} = 5 V

GENERAL DESCRIPTION

The ADM7151 is a low dropout (LDO) linear regulator that operates from 4.5 V to 16 V and provides up to 800 mA of output current. Using an advanced proprietary architecture, it provides high power supply rejection (>90 dB from 1 kHz to 1 MHz), ultralow noise (1.7 nV√Hz from 10 kHz to 1 MHz), and excellent line and load transient response with a 10 µF ceramic output capacitor. The output voltage can be set to any voltage between 1.5 V and 5.1 V with two resistors.

The ADM7151 is available in two models that optimize power dissipation and PSRR performance as a function of input and output voltage. See Table 6 and Table 7 for selection guides.

The ADM7151 regulator output noise is 1.0 µV rms from 100 Hz to 100 kHz, and the noise spectral density is 1.7 nV/√Hz from 10 kHz to 1 MHz.

The ADM7151 is available in 8-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages, making it not only a very compact solution, but also providing excellent thermal performance for applications requiring up to 800 mA of output current in a small, low profile footprint.

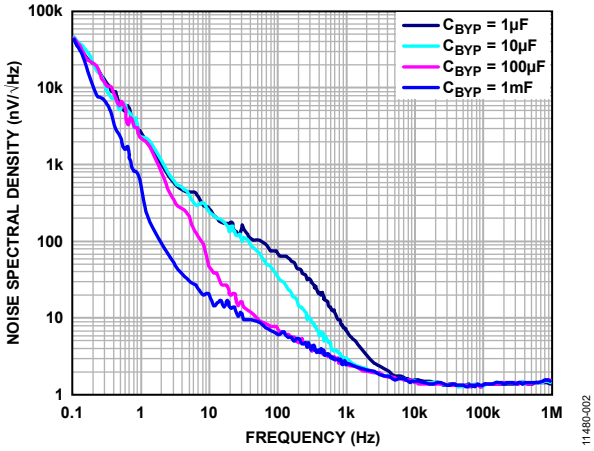


Figure 2. Noise Spectral Density (NSD) vs. Frequency for Various C_{BYP}

Rev. B Document Feedback

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REVISION HISTORY

8/2019—Rev. A to Rev. B

Changes to Figure 18 ... 9
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 24

4/2015—Rev. 0 to Rev. A

Change to Figure 4 ... 6
Change to Figure 39 ... 12

9/2013—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 4.5 V, V_{OUT} = 1.5 V, V_{REF} = V_{REF_SENSE} (unity gain), V_{EN} = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = C_{REG} = 10 µF, C_{REF} = C_{BYP} = 1 µF. T_A = 25°C for typical specifications. T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		4.5		16	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		4.3	7.0	mA
		I_{OUT} = 800 mA		8.6	12	mA
SHUTDOWN CURRENT	I_{IN-SD}	V_{EN} = GND		0.1	3	µA
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, independent of output voltage		1.6		µV rms
		100 Hz to 100 kHz, independent of output voltage		1.0		µV rms
NOISE SPECTRAL DENSITY	NSD	10 kHz to 1 MHz, independent of output voltage		1.7		nV/√Hz
POWER SUPPLY REJECTION RATIO	PSRR					
ADM7151-04		1 kHz to 100 kHz, V_{IN} = 6.2 V, V_{OUT} = 5 V at 800 mA		84		dB
		1 MHz, V_{IN} = 6.2 V, V_{OUT} = 5 V at 800 mA		53		dB
		1 kHz to 100 kHz, V_{IN} = 6.2 V, V_{OUT} = 5 V at 400 mA		94		dB
		1 MHz, V_{IN} = 6.2 V, V_{OUT} = 5 V at 400 mA		67		dB
ADM7151-02		1 kHz to 100 kHz, V_{IN} = 5.2 V, V_{OUT} = 4 V at 800 mA		91		dB
		1 MHz, V_{IN} = 5.2 V, V_{OUT} = 4 V at 800 mA		50		dB
		1 kHz to 100 kHz, V_{IN} = 5.2 V, V_{OUT} = 4 V at 400 mA		94		dB
		1 MHz, V_{IN} = 5.2 V, V_{OUT} = 4 V at 400 mA		58		dB
V_{OUT} VOLTAGE ACCURACY		V_{OUT} = V_{REF}				
Voltage Accuracy	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		1 mA < I_{OUT} < 800 mA, over line, load and temperature	−2		+2	%
V_{OUT} REGULATION						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.5 V to 16 V	−0.01		+0.01	%/V
Load Regulation[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 800 mA		0.5	1.0	%/A
CURRENT-LIMIT THRESHOLD	I_{LIMIT}					
V_{REF} Current Limit Threshold				20		mA
V_{OUT} Current Limit Threshold[2]			1.0	1.3	1.6	A
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 400 mA, V_{OUT} = 5 V		0.30	0.60	V
		I_{OUT} = 800 mA, V_{OUT} = 5 V		0.60	1.20	V
PULL-DOWN RESISTANCE						
V_{OUT} Pull-Down Resistance	$V_{OUT-PULL}$	V_{EN} = 0 V, V_{OUT} = 1 V		600		Ω
V_{REG} Pull-Down Resistance	$V_{REG-PULL}$	V_{EN} = 0 V, V_{REG} = 1 V		34		kΩ
V_{REF} Pull-Down Resistance	$V_{REF-PULL}$	V_{EN} = 0 V, V_{REF} = 1 V		800		Ω
V_{BYP} Pull-Down Resistance	$V_{BYP-PULL}$	V_{EN} = 0 V, V_{BYP} = 1 V		500		Ω
START-UP TIME[4]		V_{OUT} = 5 V				
V_{OUT} Start-Up Time	$t_{START-UP}$			2.8		ms
V_{REG} Start-Up Time	$t_{REG-START-UP}$			1.0		ms
V_{REF} Start-Up Time	$t_{REF-START-UP}$			1.8		ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		155		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
UNDERVOLTAGE THRESHOLDS						
Input Voltage Rising	$UVLO_{RISE}$	T_J = −40°C to +125°C			4.49	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = −40°C to +125°C	3.85			V
Hysteresis	$UVLO_{HYS}$			240		mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
V_{REG}[5] UNDERVOLTAGE THRESHOLDS						
V_{REG} Rise	$VREGUVLO_{RISE}$	T_J = −40°C to +125°C			3.1	V
V_{REG} Fall	$VREGUVLO_{FALL}$	T_J = −40°C to +125°C	2.55			V
Hysteresis	$VREGUVLO_{HYS}$			210		mV
EN INPUT		4.5 V ≤ V_{IN} ≤ 16 V				
EN Input Logic High	EN_{HIGH}		3.2			V
EN Input Logic Low	EN_{LOW}				0.8	V
EN Input Logic Hysteresis	EN_{HYS}	V_{IN} = 5 V		225		mV
EN Input Leakage Current	I_{EN-LKG}	V_{EN} = V_{IN} or GND		0.1	1.0	µA

[1] Based on an end-point calculation using 1 mA and 800 mA loads. See Figure 6 and Figure 13 for typical load regulation performance for loads less than 1 mA.
[2] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 5.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0 V, or 4.5 V.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to achieve the nominal output voltage. Dropout applies only for output voltages above 4.5 V.
[4] Start-up time is defined as the time between the rising edge of V_{EN} to V_{OUT}, V_{REG}, or V_{REF} being at 90% of its nominal value.
[5] The output voltage is turned off until the V_{REG} UVLO rise threshold is crossed. The V_{REG} output is turned off until the input voltage UVLO rising threshold is crossed.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CAPACITANCE		T_A = −40°C to +125°C				
Minimum Input[1]	C_{IN}		7.0			µF
Minimum Regulator[1]	C_{REG}		7.0			µF
Minimum Output[1]	C_{OUT}		7.0			µF
Minimum Bypass	C_{BYP}		0.1			µF
Minimum Reference	C_{REF}		0.7			µF
CAPACITOR EQUIVALENT SERIES RESISTANCE (ESR)	R_{ESR}	T_A = −40°C to +125°C				
C_{REG}, C_{OUT}, C_{IN}, C_{REF}			0.001		0.2	Ω
C_{BYP}			0.001		2.0	Ω

[1] The minimum input, regulator, and output capacitance must be greater than 7.0 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; however, Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +18 V
VREG to GND	−0.3 V to VIN, or +6 V (whichever is less)
VOUT to GND	−0.3 V to VREG, or +6 V (whichever is less)
VOUT to BYP	±0.3 V
EN to GND	−0.3 V to18 V
BYP to GND	−0.3 V to VREG, or +6 V (whichever is less)
REF to GND	−0.3 V to VREG, or +6 V (whichever is less)
REF_SENSE to GND	−0.3 V to +6 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Operating Ambient Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADM7151 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction to ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction to ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction.

Ψ_{JB} is the junction to board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and the calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA}, θ_{JC}, and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead LFCSP	36.7	23.5	13.3	°C/W
8-Lead SOIC	36.9	27.1	18.6	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

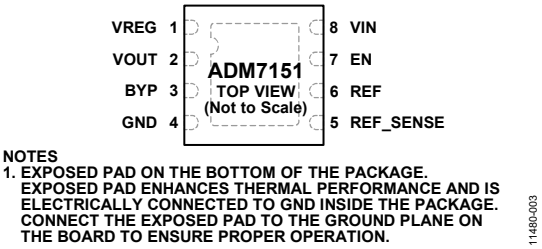


Figure 3. 8-Lead LFCSP Pin Configuration

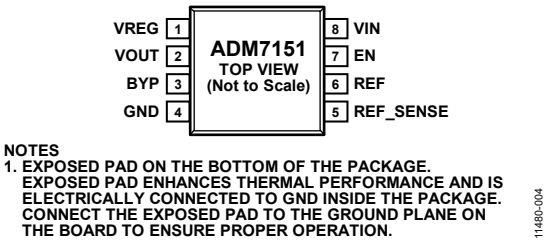


Figure 4. 8-Lead SOIC Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VREG	Regulated Input Supply to LDO Amplifier. Bypass VREG to GND with a 10 µF or greater capacitor. Do not connect a load to ground.
2	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 10 µF or greater capacitor.
3	BYP	Low Noise Bypass Capacitor. Connect a 1 µF capacitor to GND to reduce noise. Do not connect a load to ground.
4	GND	Ground Connection.
5	REF_SENSE	External Resistor Divider Used to Set the Output Voltage. $V_{OUT} = V_{REF} \times (R1 + R2)/R2$, where $V_{REF} = 1.5$ V.
6	REF	Low Noise Reference Voltage Output. Bypass REF to GND with a 1 µF capacitor. Short REF_SENSE to REF for fixed output voltages. Do not connect a load to ground.
7	EN	Enable. Drive EN high to turn on the regulator and drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
8	VIN	Regulator Input Supply. Bypass VIN to GND with a 10 µF or greater capacitor.
EP	EP	Exposed Pad on the Bottom of the Package. Exposed pad enhances thermal performance and is electrically connected to GND inside the package. Connect the exposed pad to the ground plane on the board to ensure proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{OUT} + 1.2 V or V_{IN} = 4.5 V, whichever is greater, EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = C_{REG} = 10 µF, C_{REF} = C_{BYP} = 1 µF, T_A = 25°C, unless otherwise noted.

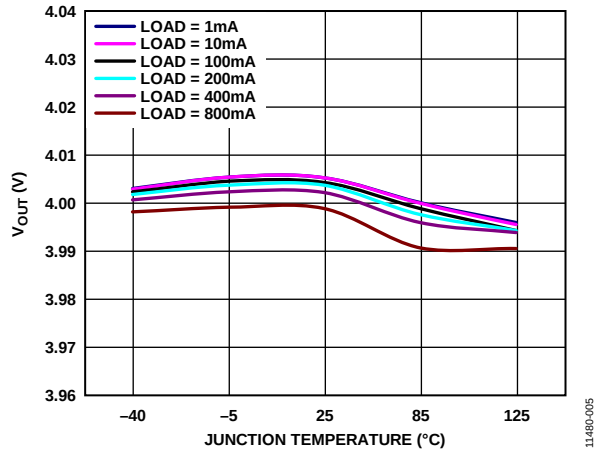


Figure 5. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), ADM7151-02, V_{OUT} = 4 V

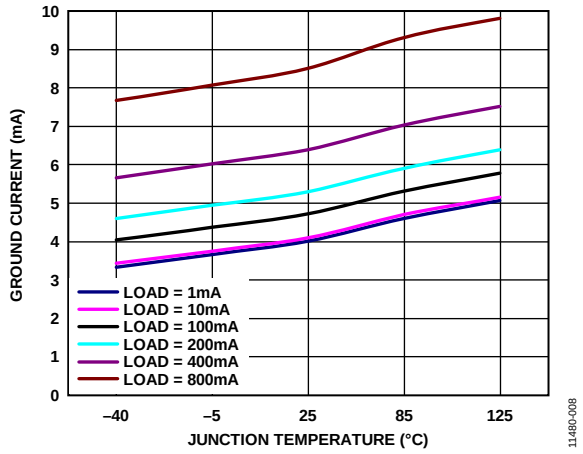


Figure 8. Ground Current vs. Junction Temperature (T_J), ADM7151-02, V_{OUT} = 4 V

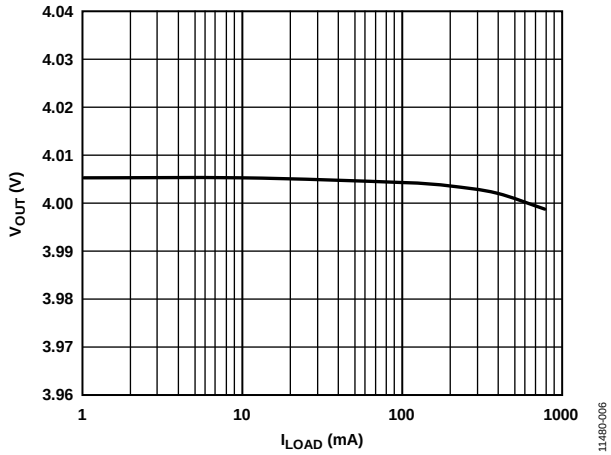


Figure 6. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), ADM7151-02, V_{OUT} = 4 V

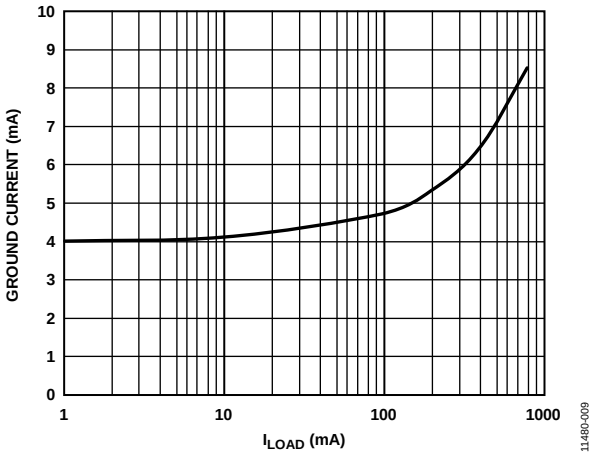


Figure 9. Ground Current vs. Load Current (I_{LOAD}), ADM7151-02, V_{OUT} = 4 V

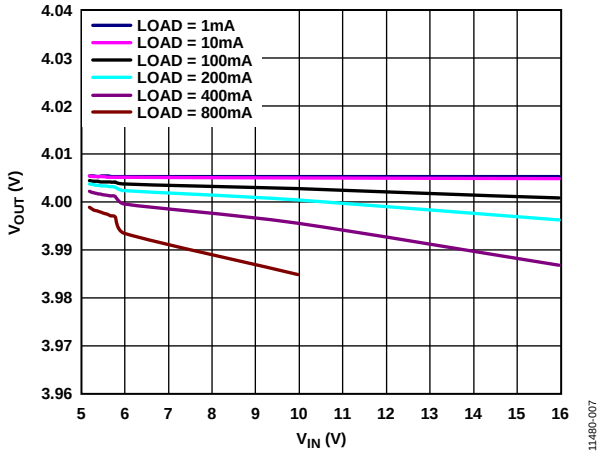


Figure 7. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), ADM7151-02, V_{OUT} = 4 V

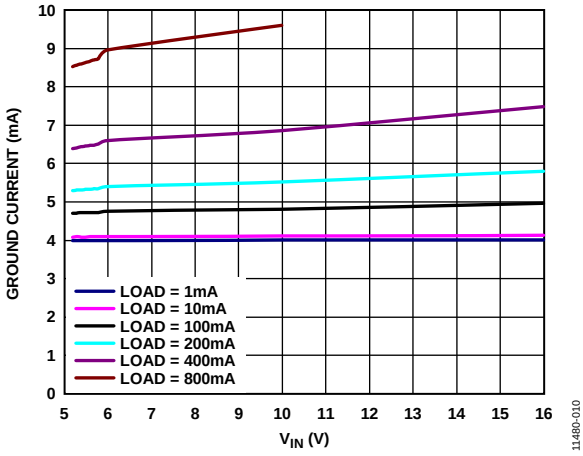


Figure 10. Ground Current vs. Input Voltage (V_{IN}), ADM7151-02, V_{OUT} = 4 V

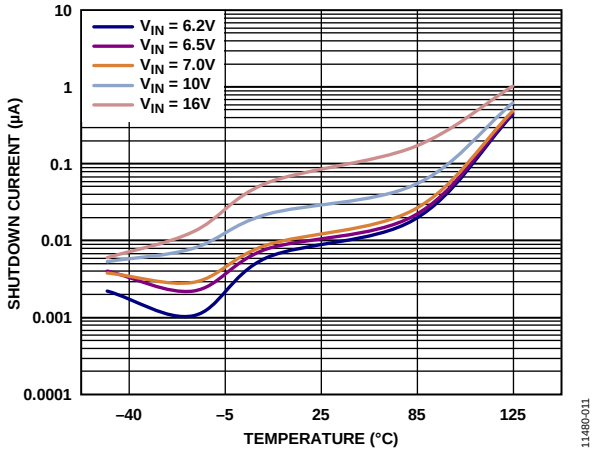


Figure 11. Shutdown Current vs. Temperature at Various Input Voltages

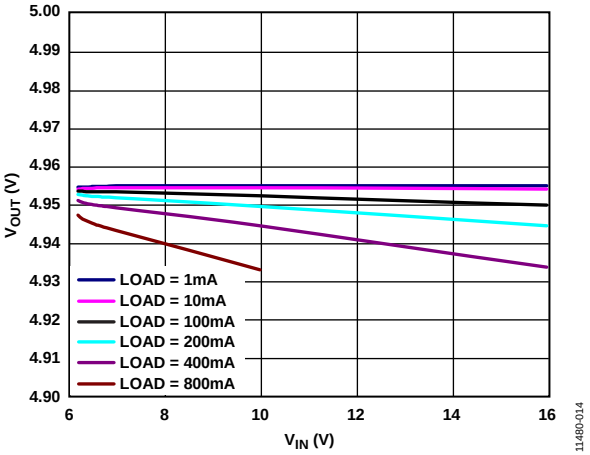


Figure 14. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), ADM7151-04, V_{OUT} = 5 V

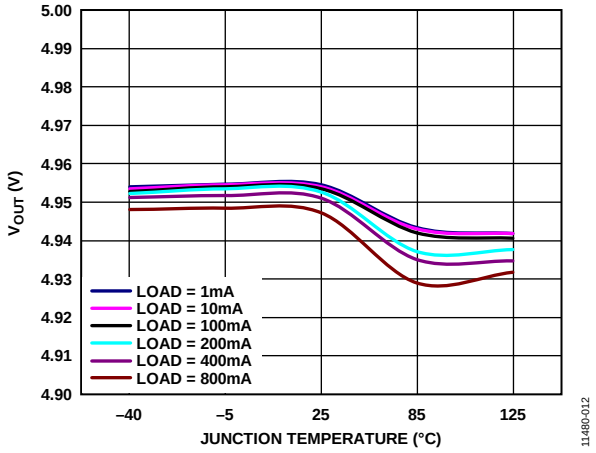


Figure 12. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), ADM7151-04, V_{OUT} = 5 V

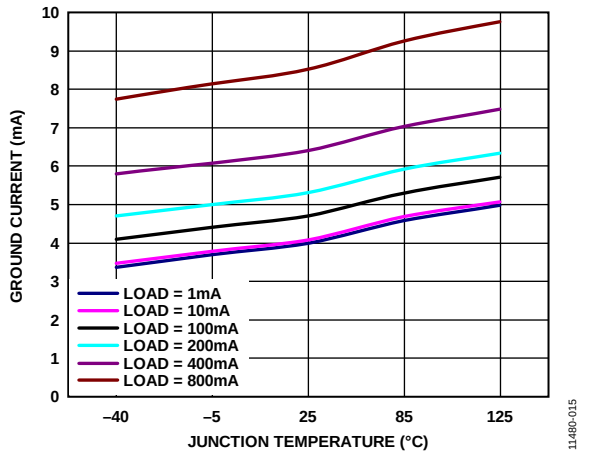


Figure 15. Ground Current vs. Junction Temperature (T_J), ADM7151-04, V_{OUT} = 5 V

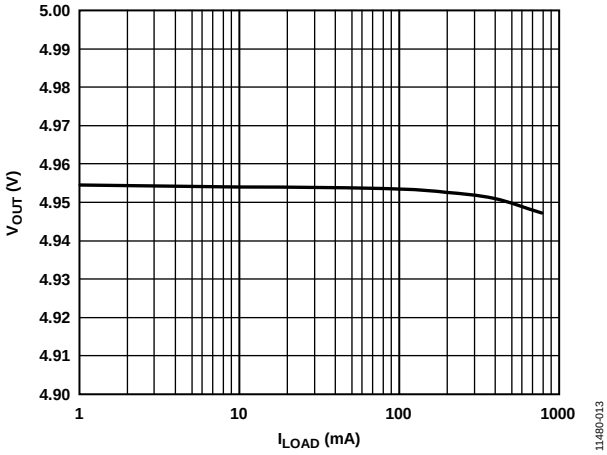


Figure 13. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), ADM7151-04, V_{OUT} = 5 V

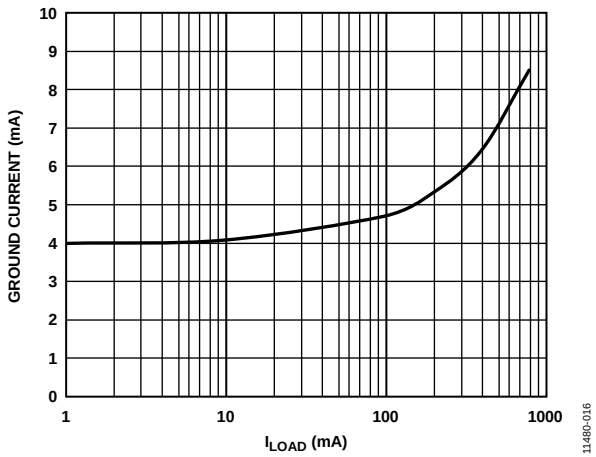


Figure 16. Ground Current vs. Load Current (I_{LOAD}), ADM7151-04, V_{OUT} = 5 V

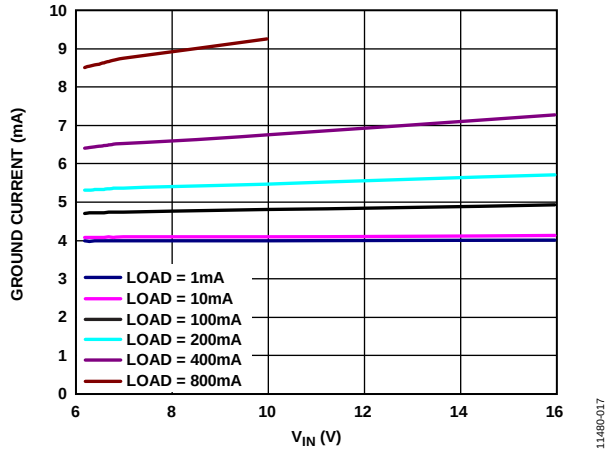


Figure 17. Ground Current vs. Input Voltage (V_{IN}), ADM7151-04, V_{OUT} = 5 V

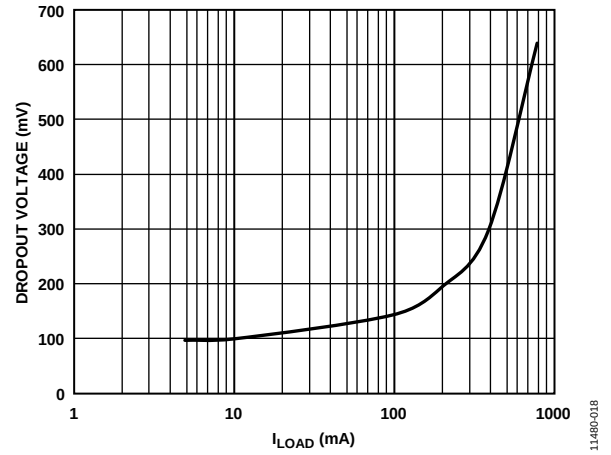


Figure 18. Dropout Voltage vs. Load Current (I_{LOAD}), ADM7151-04, V_{OUT} = 5 V

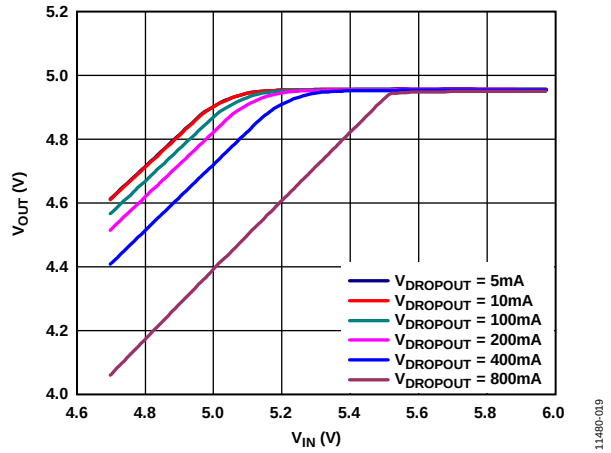


Figure 19. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, ADM7151-04, V_{OUT} = 5 V

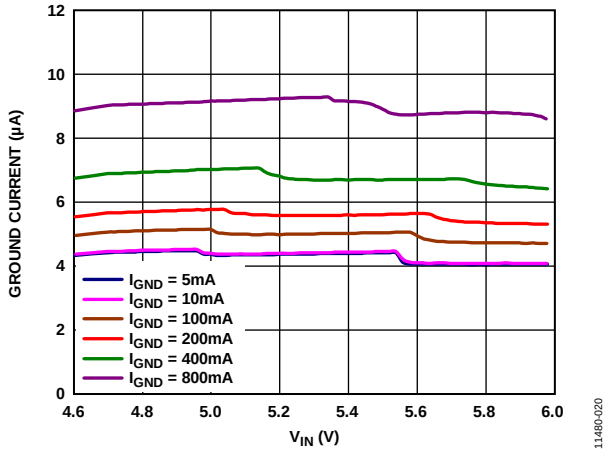


Figure 20. Ground Current vs. Input Voltage (V_{IN}) in Dropout, ADM7151-04, V_{OUT} = 5 V

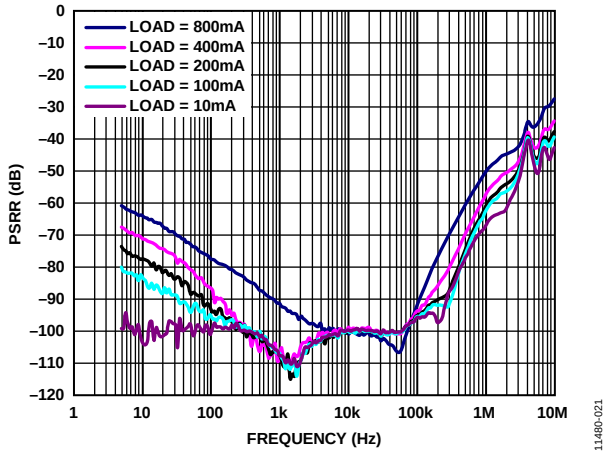


Figure 21. Power Supply Rejection Ratio (PSRR) vs. Frequency, ADM7151-02, V_{OUT} = 4 V

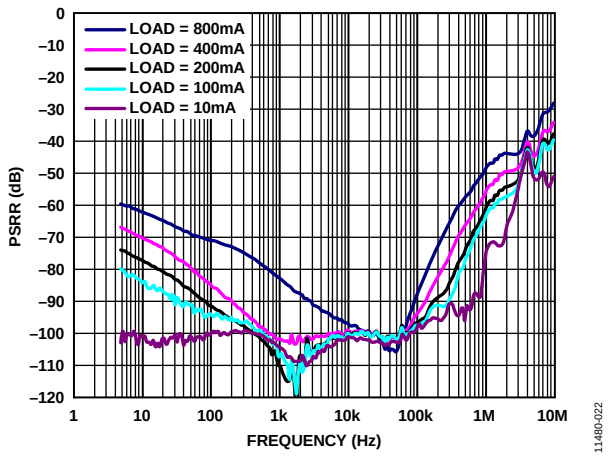


Figure 22. Power Supply Rejection Ratio (PSRR) vs. Frequency, ADM7151-04, V_{OUT} = 5 V

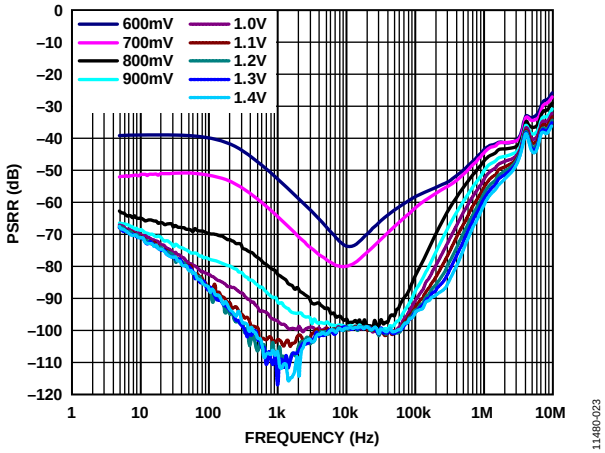


Figure 23. Power Supply Rejection Ratio (PSRR) vs. Frequency for Various Headroom Voltages, ADM7151-02, V_{OUT} = 4 V, 400 mA Load

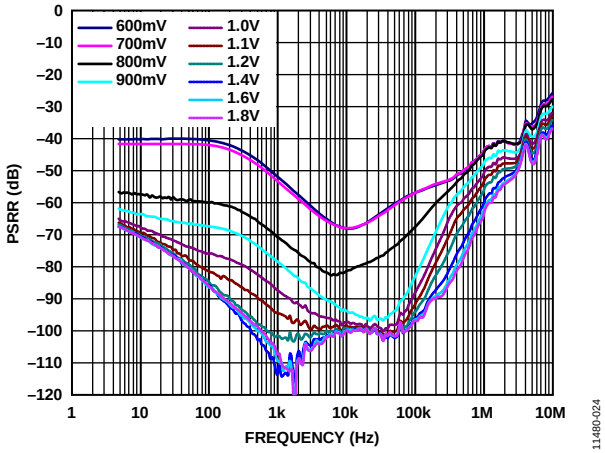


Figure 24. Power Supply Rejection Ratio (PSRR) vs. Frequency for Various Headroom Voltages, ADM7151-04, V_{OUT} = 5 V, 400 mA Load

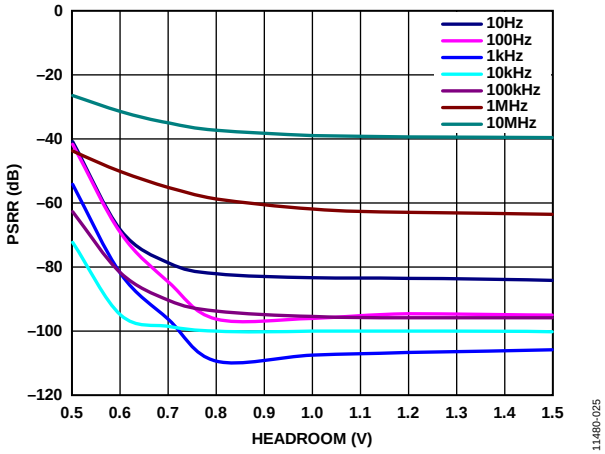


Figure 25. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, ADM7151-02, V_{OUT} = 4 V, 100 mA Load

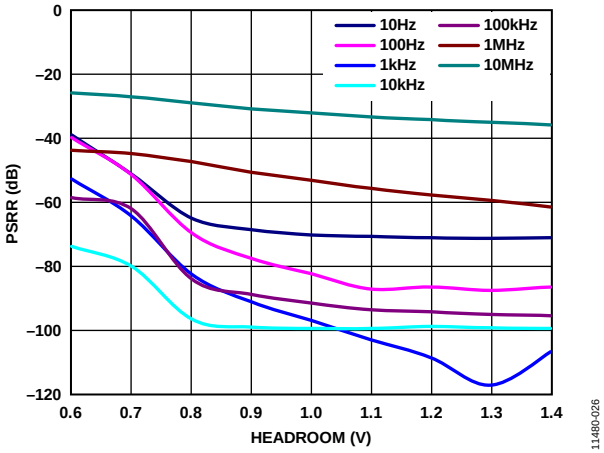


Figure 26. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, ADM7151-02, V_{OUT} = 4 V, 400 mA Load

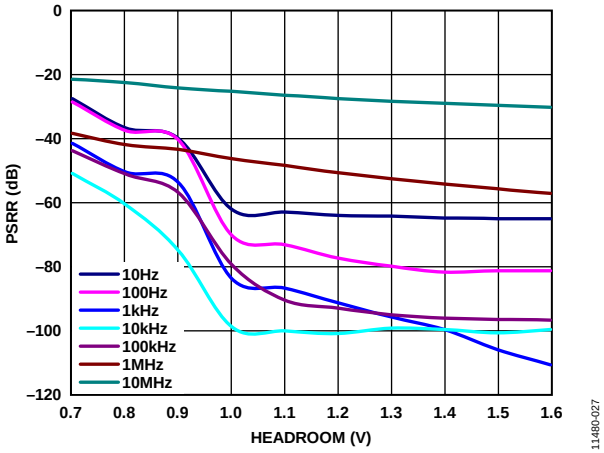


Figure 27. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, ADM7151-02, V_{OUT} = 4 V, 800 mA Load

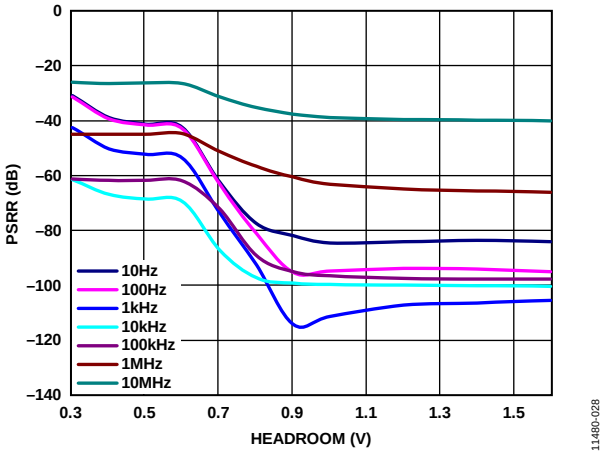


Figure 28. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, ADM7151-04, V_{OUT} = 5 V, 100 mA Load

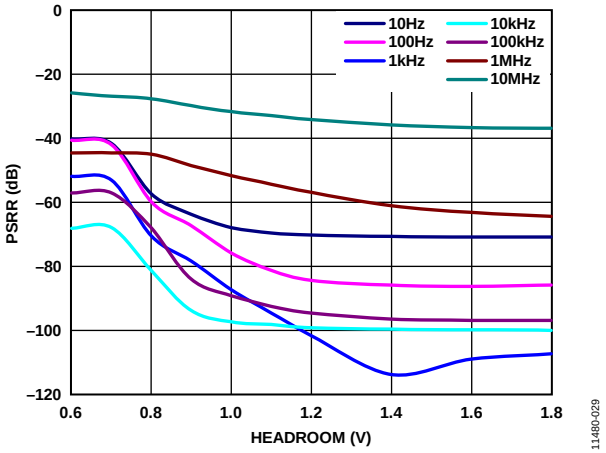


Figure 29. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, ADM7151-04, V_{OUT} = 5 V, 400 mA Load

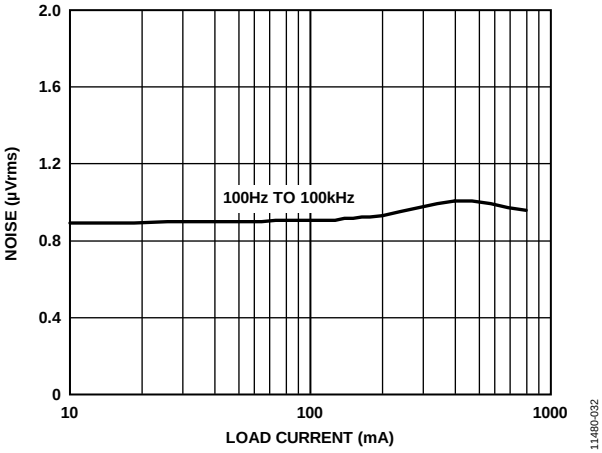


Figure 32. RMS Output Noise vs. Load Current (I_{LOAD}), 100 Hz to 100 kHz, ADM7151-04, V_{OUT} = 5 V

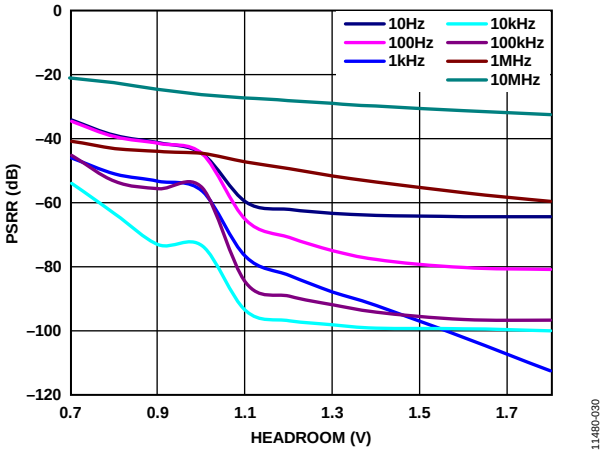


Figure 30. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, ADM7151-04, V_{OUT} = 5 V, 800 mA Load

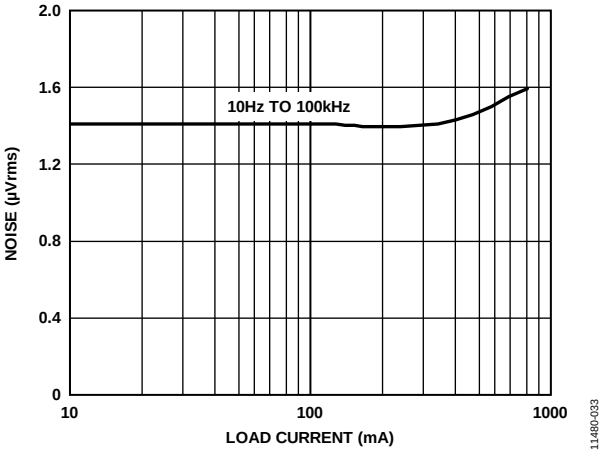


Figure 33. RMS Output Noise vs. Load Current (I_{LOAD}), 10 Hz to 100 kHz, ADM7151-02, V_{OUT} = 4 V

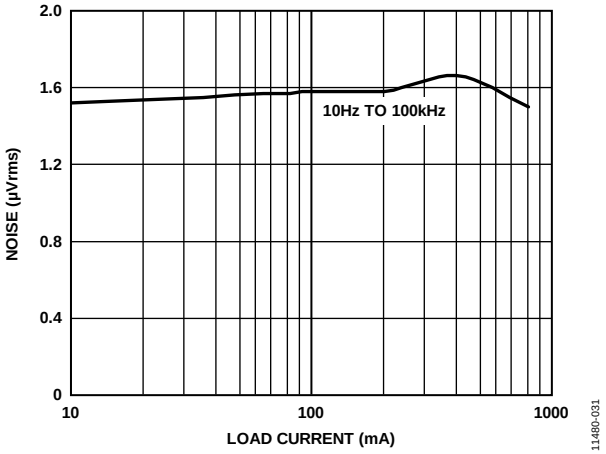


Figure 31. RMS Output Noise vs. Load Current (I_{LOAD}), 10 Hz to 100 kHz, ADM7151-04, V_{OUT} = 5 V

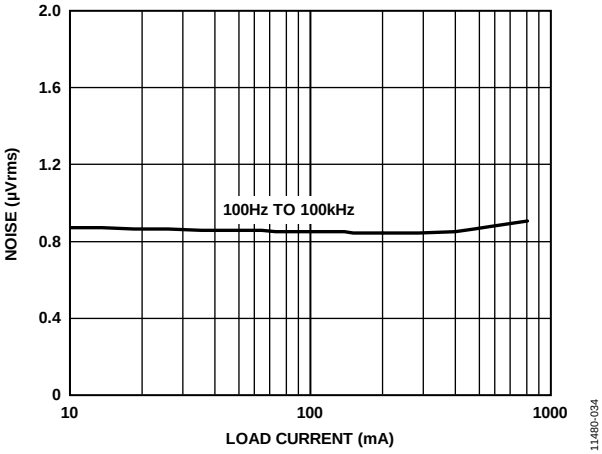


Figure 34. RMS Output Noise vs. Load Current (I_{LOAD}), 100 Hz to 100 kHz, ADM7151-02, V_{OUT} = 4 V

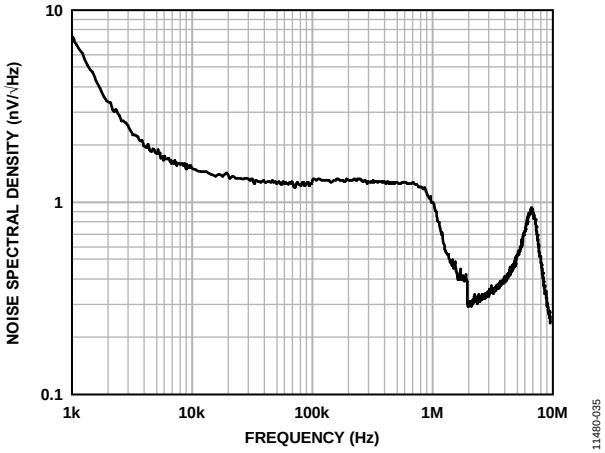


Figure 35. Output Noise Spectral Density, 1 kHz to 10 MHz, I_{LOAD} = 10 mA

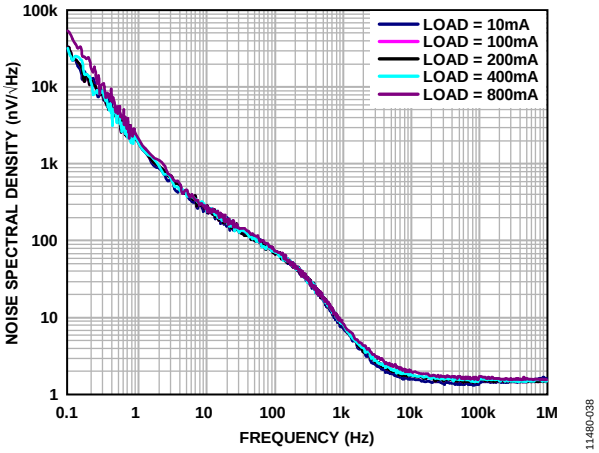


Figure 38. Output Noise Spectral Density at Different Load Currents, 0.1 Hz to 1 MHz

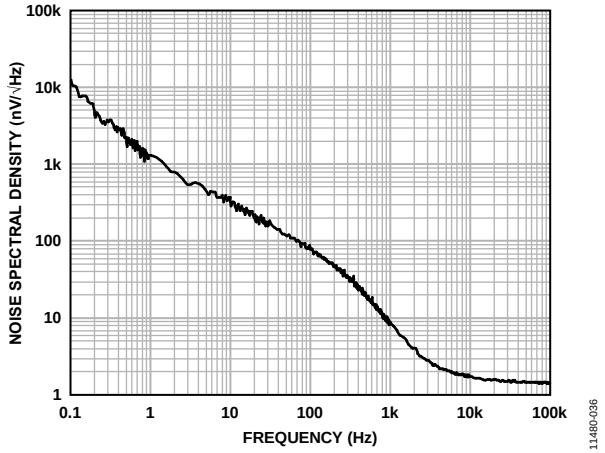


Figure 36. Output Noise Spectral Density, 0.1 Hz to 10 kHz, I_{LOAD} = 10 mA

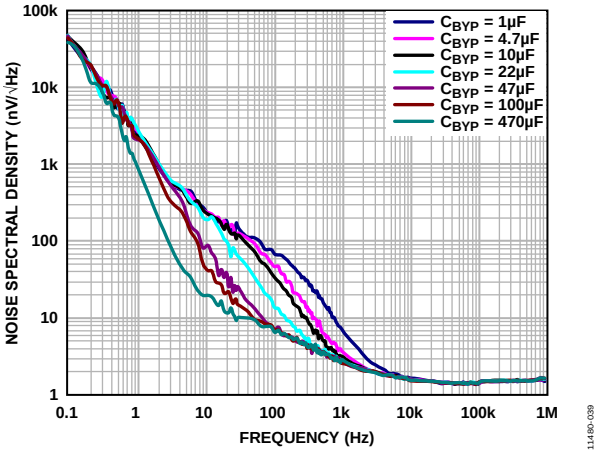


Figure 39. Output Noise Spectral Density vs. at Different C_{BYP}, Load Current = 10 mA

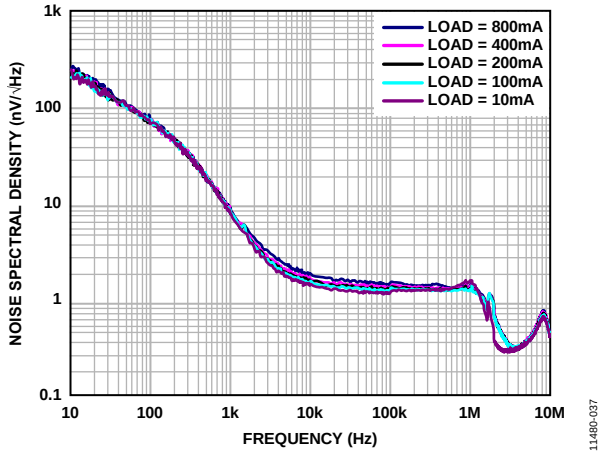


Figure 37. Output Noise Spectral Density at Different Load Currents, 10 Hz to 10 MHz

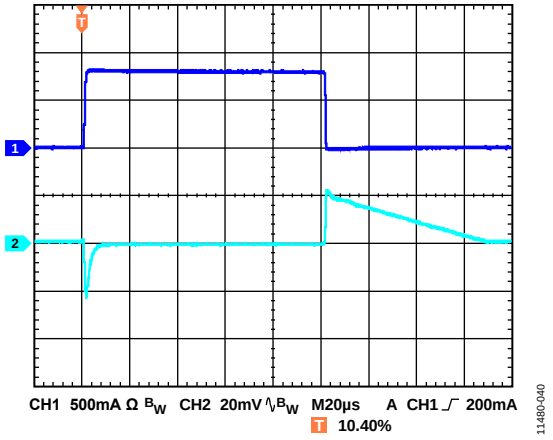


Figure 40. Load Transient Response, I_{LOAD} = 1 mA to 800 mA, V_{OUT} = 5 V, V_{IN} = 6.2 V, CH1 = I_{OUT}, CH2 = V_{OUT}

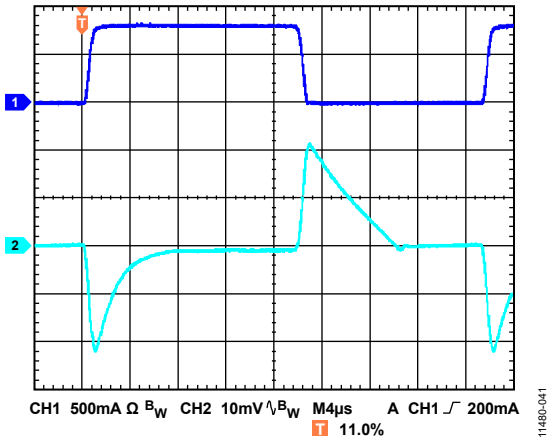


Figure 41. Load Transient Response, I_{LOAD} = 10 mA to 800 mA, V_{OUT} = 5 V, V_{IN} = 6.2 V, CH1 = I_{OUT}, CH2 = V_{OUT}

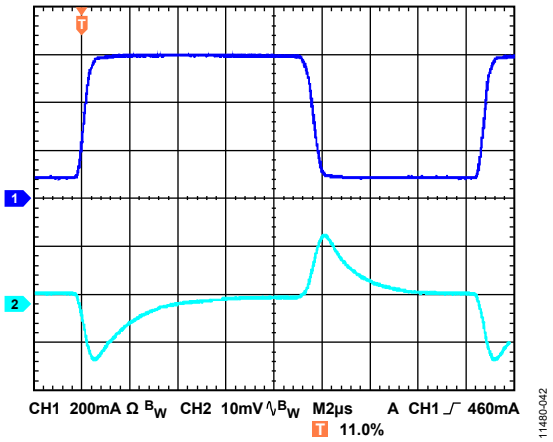


Figure 42. Load Transient Response, I_{LOAD} = 100 mA to 600 mA, V_{OUT} = 5 V, V_{IN} = 6.2 V, CH1 = I_{OUT}, CH2 = V_{OUT}

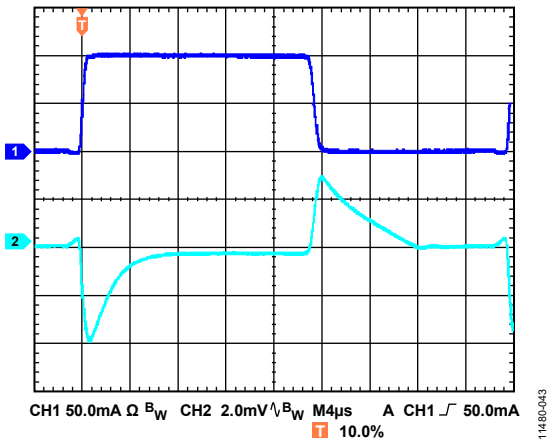


Figure 43. Load Transient Response, I_{LOAD} = 1 mA to 100 mA, V_{OUT} = 5 V, V_{IN} = 6.2 V, CH1 = I_{OUT}, CH2 = V_{OUT}

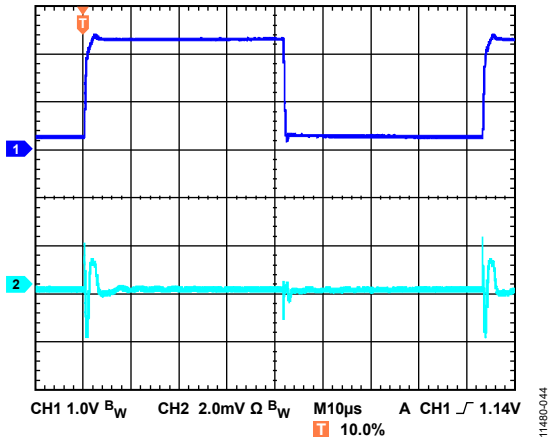


Figure 44. Line Transient Response, 2 V Input Step, I_{LOAD} = 800 mA, V_{OUT} = 1.8 V, V_{IN} = 4.5 V, CH1 = V_{IN}, CH2 = V_{OUT}

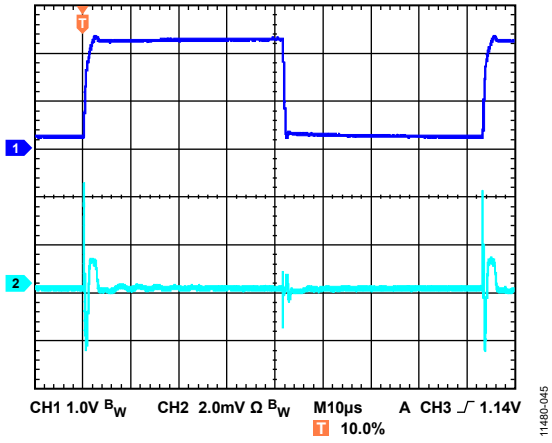


Figure 45. Line Transient Response, 2 V Input Step, I_{LOAD} = 800 mA, V_{OUT} = 3.3 V, V_{IN} = 4.5 V, CH1 = V_{IN}, CH2 = V_{OUT}

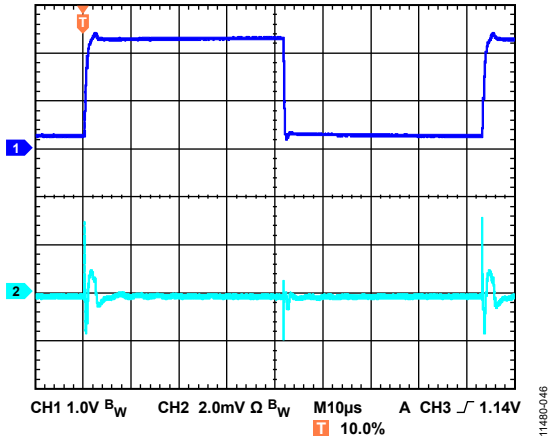


Figure 46. Line Transient Response, 2 V Input Step, I_{LOAD} = 800 mA, V_{OUT} = 5 V, V_{IN} = 6.2 V, CH1 = V_{IN}, CH2 = V_{OUT}

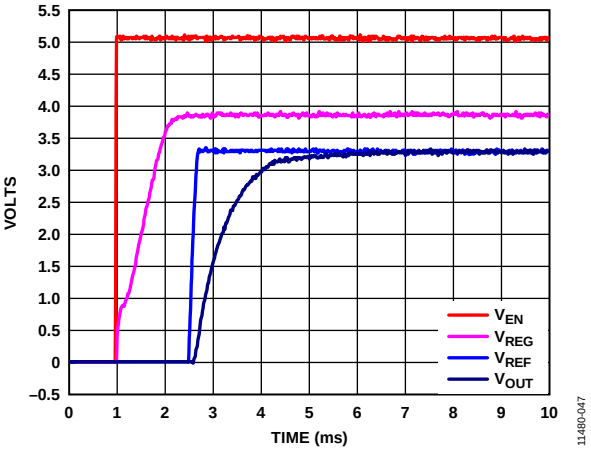


Figure 47. V_{OUT}, V_{REF}, V_{REG} Start-Up Times After V_{EN} Rising, V_{OUT} = 3.3 V, V_{IN} = 5 V

THEORY OF OPERATION

The ADM7151 is an adjustable, ultralow noise, high power supply rejection ratio (PSRR) linear regulator targeting radio frequency (RF) applications. The input voltage range is 4.5 V to 16 V, and it can deliver up to 800 mA of output current. Typical shutdown current consumption is 0.1 µA at room temperature.

Optimized for use with 10 µF ceramic capacitors, the ADM7151 provides excellent transient performance.

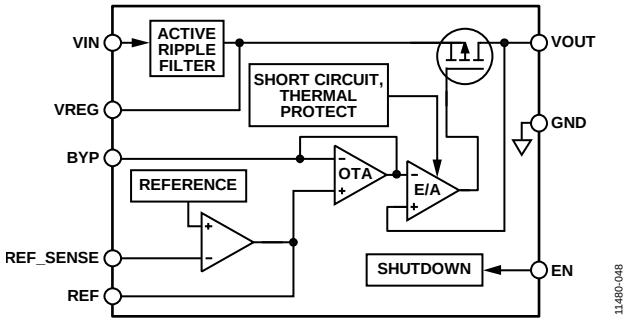


Figure 48. Adjustable Output Voltage Internal Block Diagram

Internally, the ADM7151 consists of a reference, an error amplifier, a feedback voltage divider, and a P-channel MOSFET pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

By heavily filtering the reference voltage, the ADM7151 is able to achieve 1.7 nV/√Hz output typical from 10 kHz to 1 MHz. Because the error amplifier is always in unity gain, the output noise is independent of the output voltage.

To maintain very high PSRR over a wide frequency range, the ADM7151 architecture uses an internal active ripple filter. This stage isolates the low output noise LDO from noise on VIN. The result is that the ADM7151 PSRR is significantly higher over a wider frequency range than any single stage LDO.

The ADM7151 output voltage can be adjusted between 1.5 V and 5.1 V and is available in two models that optimize the input voltage and output voltage ranges to keep power dissipation as low as possible without compromising PSRR performance. The output voltage is determined by an external voltage divider according to the following equation:

$$V_{OUT} = 1.5\ V \times (1 + R1/R2)$$

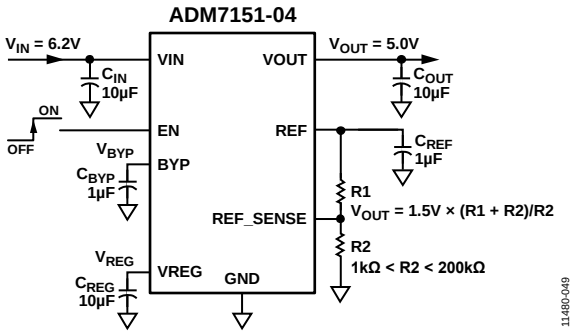


Figure 49. Typical Adjustable Output Voltage Application Schematic

The R2 value must be greater than 1 kΩ to prevent excessive loading of the reference voltage appearing on the REF pin. To minimize errors in the output voltage caused by the REF_SENSE pin input current, the R2 value must be less than 200 kΩ. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 3.0 V. The output voltage error introduced by the REF_SENSE pin input current is 10 mV or 0.33%, assuming a maximum REF_SENSE pin input current of 100 nA at 125°C.

The ADM7151 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on, and when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

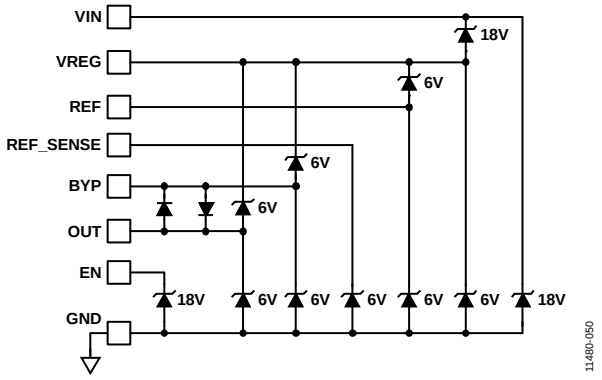


Figure 50. Simplified ESD Protection Block Diagram

The ESD protection devices are shown in the block diagram as Zener diodes (see Figure 50).

APPLICATIONS INFORMATION

MODEL SELECTION

The ADM7151 is available in two models to allow the user to select the best combination of power dissipation and PSRR performance for a given application.

CAPACITOR SELECTION

Output Capacitor

The ADM7151 is designed for operation with ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 10 µF capacitance with an ESR of 0.2 Ω or less is recommended to ensure the stability of the ADM7151. Output capacitance also affects transient response to changes in load current. Using a larger value of output capacitance improves the transient response of the ADM7151 to large changes in load current. Figure 51 shows the transient responses for an output capacitance value of 10 µF.

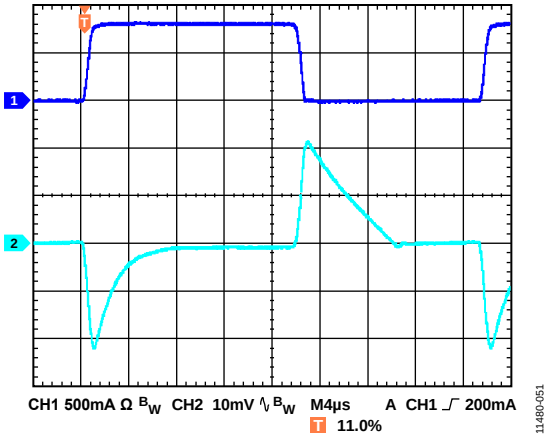


Figure 51. Output Transient Response, V_{OUT} = 5 V, C_{OUT} = 10 µF

Input and VREG Capacitor

Connecting a 10 µF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered.

To maintain the best possible stability and PSRR performance, connect a 10 µF capacitor from VREG to GND. When more than 10 µF of output capacitance is required, increase the input and VREG capacitors to match it.

REF Capacitor

The REF capacitor is necessary to stabilize the reference amplifier. Connect a capacitor of at least 1 µF between REF and GND.

Table 6. Model Selection Guide for PSRR

Model	V_{OUT} Range (V)	PSRR (dB) at 800 mA, 1.2 V Headroom			PSRR (dB) at 400 mA, 1 V Headroom		
		10 kHz	100 kHz	1 MHz	10 kHz	100 kHz	1 MHz
ADM7151-02	1.5 to 4.0	91	91	50	94	94	58
ADM7151-04	1.5 to 5.1	84	84	53	94	94	67

Table 7. Model Selection Guide for Input Voltage

Model	V_{OUT} Range (V)	Minimum V_{IN} at 800 mA Load				Minimum V_{IN} at 400 mA Load			
		V_{OUT} < 3.3 V	V_{OUT} < 5 V	V_{OUT} ≥ 3.3 V	V_{OUT} ≥ 5 V	V_{OUT} < 3.3 V	V_{OUT} < 5 V	V_{OUT} ≥ 3.3 V	V_{OUT} ≥ 5 V
ADM7151-02	1.5 to 4.0	4.5 V	N/A[1]	V_{OUT} + 1.2 V	N/A[1]	4.5 V	N/A[1]	V_{OUT} + 1.0 V	N/A[1]
ADM7151-04	1.5 to 5.1	N/A[1]	6.2 V	N/A[1]	V_{OUT} + 1.2 V	N/A[1]	6 V	N/A[1]	V_{OUT} + 1.0 V

[1] N/A = not applicable.

BYP Capacitor

The BYP capacitor is necessary to filter the reference buffer. A 1 µF capacitor is typically connected between BYP and GND. Capacitors as small as 0.1 µF can be used; however, the output noise voltage of the LDO increases as a result.

In addition, the BYP capacitor can be increased to reduce the noise below 1 kHz at the expense of increasing the start-up time of the LDO. Very large values of C_{BYP} significantly reduce the noise below 10 Hz. Tantalum capacitors are recommended for capacitors larger than about 33 µF. A 1 µF ceramic capacitor in parallel with the larger tantalum capacitor is required to retain good noise performance at higher frequencies.

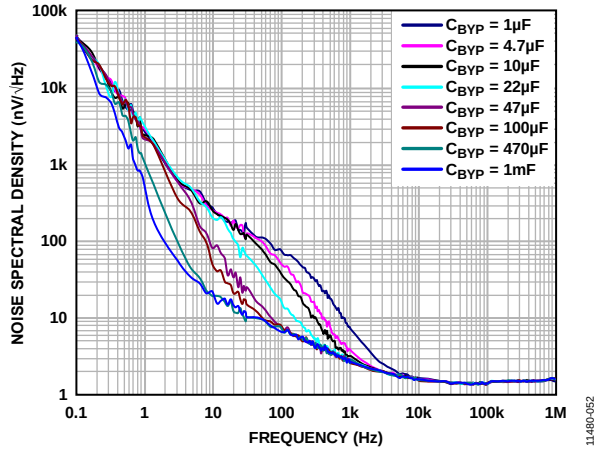


Figure 52. Noise Spectral Density vs. Frequency, C_{BYP} = 1 µF to 1 mF

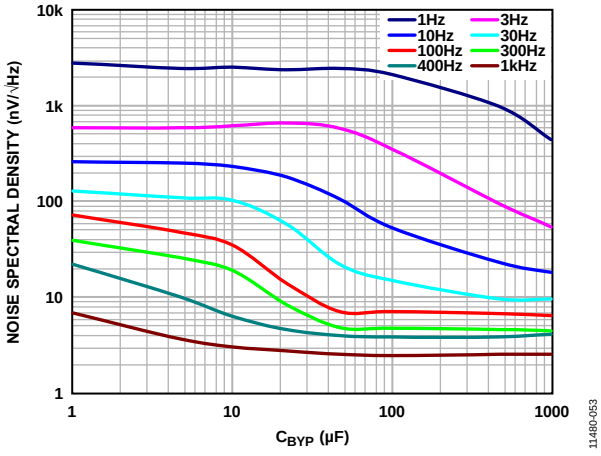


Figure 53. Noise Spectral Density vs. C_{BYP} for Different Frequencies

Capacitor Properties

Any good quality ceramic capacitors can be used with the ADM7151 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions.

X5R or X7R dielectrics with a voltage rating of 6.3 V to 50 V are recommended. However, Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics.

Figure 54 depicts the capacitance vs. dc bias voltage of a 1206, 10 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

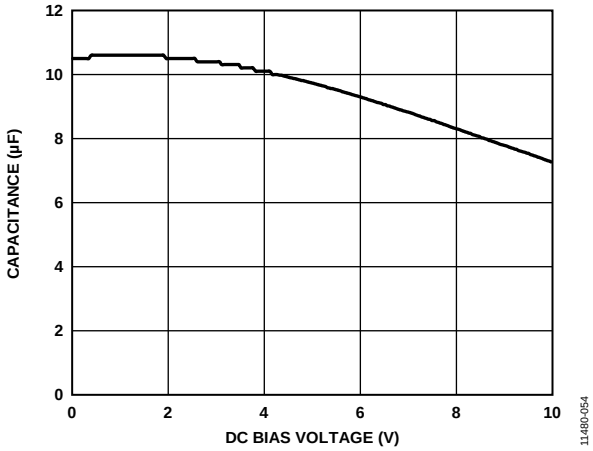


Figure 54. Capacitance vs. DC Bias Voltage

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 9.72 µF at 5 V, as shown in Figure 54.

Substituting these values in Equation 1 yields

$$C_{EFF} = 9.72\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.44\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADM7151, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

ENABLE (EN) AND UNDERVOLTAGE LOCKOUT (UVLO)

The ADM7151 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 55, when a rising voltage on EN crosses the upper threshold, VOUT turns on. When a falling voltage on EN crosses the lower threshold, VOUT turns off. The hysteresis varies as a function of the input voltage. For example, the EN hysteresis is approximately 200 mV with an input voltage of 4.5 V.

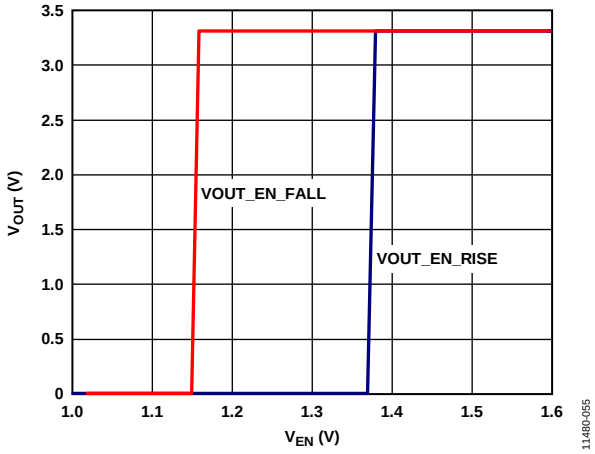


Figure 55. Typical V_{OUT} Response to EN Pin Operation, V_{OUT} = 3.3 V, V_{IN} = 5 V

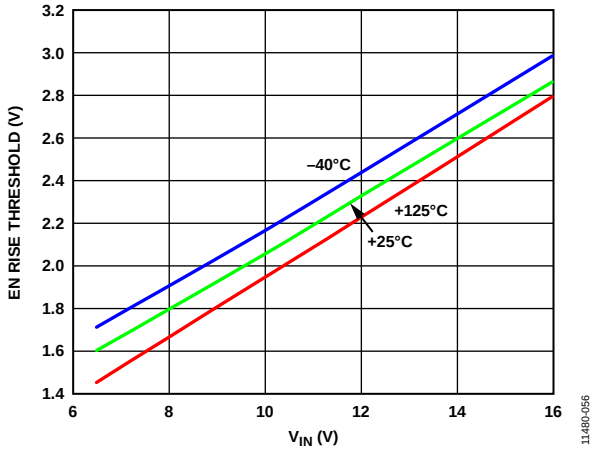


Figure 56. Typical EN Rise Threshold vs. Input Voltage (V_{IN}) for Various Temperatures

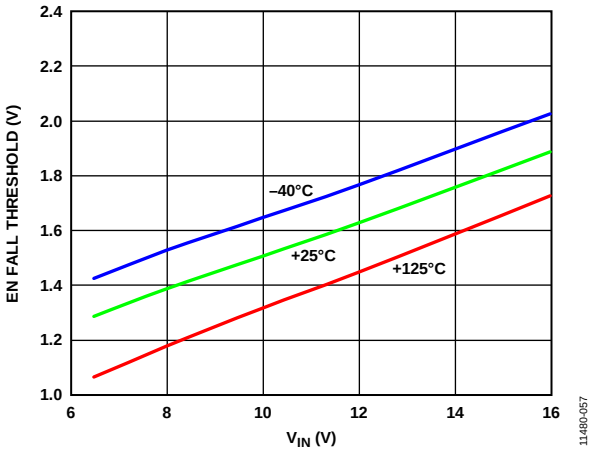


Figure 57. Typical EN Fall Threshold vs. Input Voltage (V_{IN}) for Various Temperatures

The ADM7151 also incorporates an internal undervoltage lockout circuit to disable the output voltage when the input voltage is less than the minimum input voltage rating of the regulator. The upper and lower thresholds are internally fixed with approximately 300 mV of hysteresis.

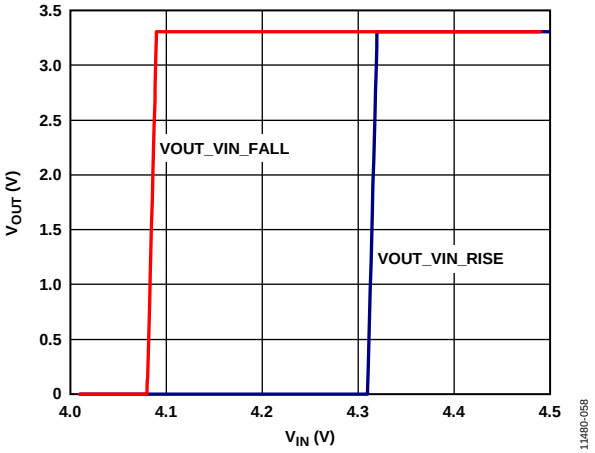


Figure 58. Typical UVLO Hysteresis, V_{OUT} = 3.3 V

Figure 58 shows the typical hysteresis of the UVLO function. This hysteresis prevents on/off oscillations that can occur due to noise on the input voltage as it passes through the threshold points.

START-UP TIME

The ADM7151 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for a 5 V output is approximately 3 ms from the time the EN active threshold is crossed to when the output reaches 90% of its final value.

The rise time of the output voltage (10% to 90%) is approximately

$$0.0012 \times C_{BYP} \text{ seconds}$$

where C_{BYP} is in microfarads.

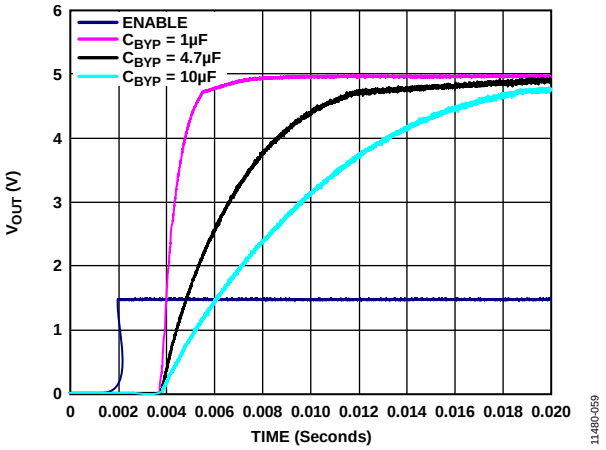


Figure 59. Typical Start-Up Behavior with C_{BYP} = 1 µF to 10 µF

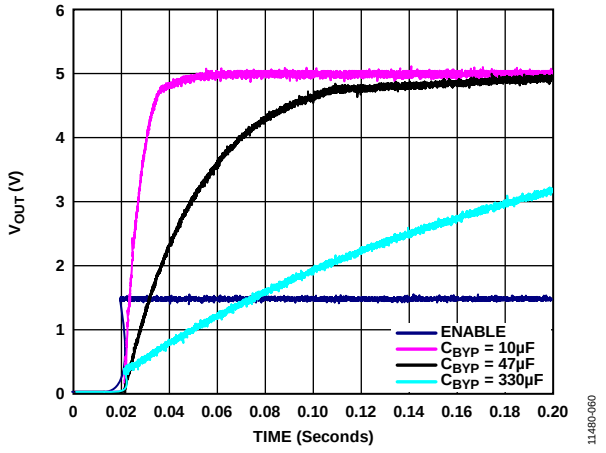


Figure 60. Typical Start-Up Behavior with C_{BYP} = 10 µF to 330 µF

REF, BYP, AND VREG PINS

REF, BYP, and VREG are internally generated voltages that require external bypass capacitors for proper operation. Do not, under any circumstances, connect any loads to these pins because doing so compromises the noise and PSRR performance of the ADM7151. Using larger values of C_{BYP}, C_{REF}, and C_{REG} is acceptable but can increase the start-up time, as described in the Start-Up Time section.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADM7151 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADM7151 is designed to current limit when the output load reaches 1.3 A (typical). When the output load exceeds 1.3 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 155°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 155°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 140°C, the output is turned on again, and output current is restored to its operating value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADM7151 current limits, so that only 1.3 A is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 155°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 140°C, the output turns on and conducts 1.3 A into the short, again causing the junction temperature to rise above 155°C. This thermal oscillation between 140°C and 155°C causes a current oscillation between 1.3 A and 0 mA that continues as long as the short remains at the output.

Current-limit and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperature does not exceed 150°C.

THERMAL CONSIDERATIONS

In applications with low input to output voltage differential, the ADM7151 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package can become large enough that it causes the junction temperature of the die to exceed the maximum junction temperature of 150°C.

When the junction temperature exceeds 155°C, the converter enters thermal shutdown. It recovers only after the junction temperature decreases below 140°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADM7151 must not exceed 150°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pin and exposed pad to the PCB.

Table 8 shows typical θ_{JA} values of the 8-lead SOIC and 8-lead LFCSP packages for various PCB copper sizes.

Table 9 shows the typical Ψ_{JB} values of the 8-lead SOIC and 8-lead LFCSP.

Table 8. Typical θ_{JA} Values

	θ_{JA} (°C/W)	
Copper Size (mm²)	**8-Lead LFCSP**	**8-Lead SOIC**
25[1]	165.1	165
100	125.8	126.4
500	68.1	69.8
1000	56.4	57.8
6400	42.1	43.6

[1] Device soldered to minimum size pin traces.

Table 9. Typical Ψ_{JB} Values

Package	Ψ_{JB} (°C/W)
8-Lead LFCSP	15.1
8-Lead SOIC	17.9

The junction temperature of the ADM7151 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
V_{IN} and V_{OUT} are thinput and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the groune d current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 150°C.

The heat dissipation from the package can be improved by increasing the amount of copper attached to the pins and exposed pad of the ADM7151. Adding thermal planes under the package also improves thermal performance. However, as listed in Table 8, a point of diminishing returns is eventually reached, beyond which an increase in the copper area does not yield significant reduction in the junction to ambient thermal resistance.

Figure 61 to Figure 66 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

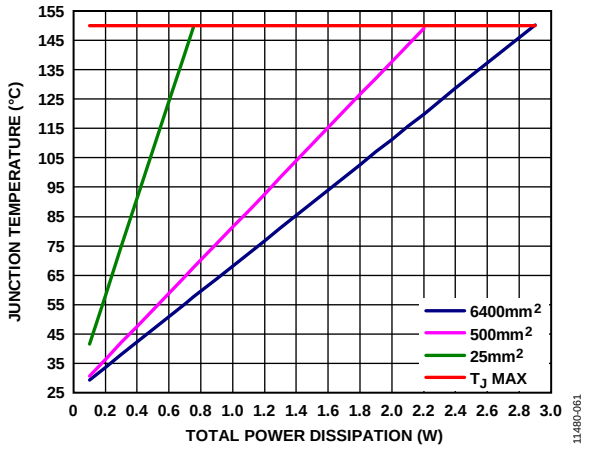


Figure 61. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 25°C

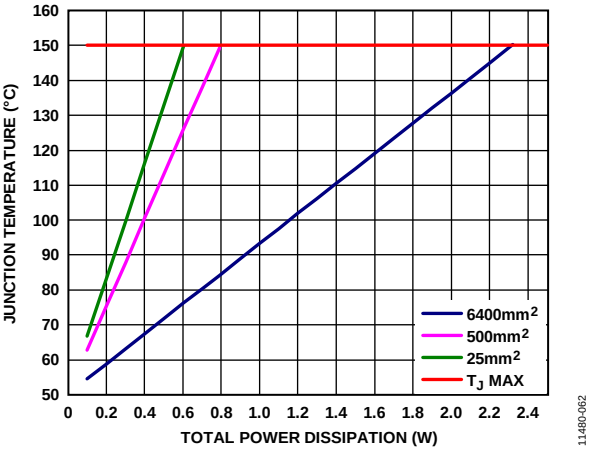


Figure 62. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 50°C

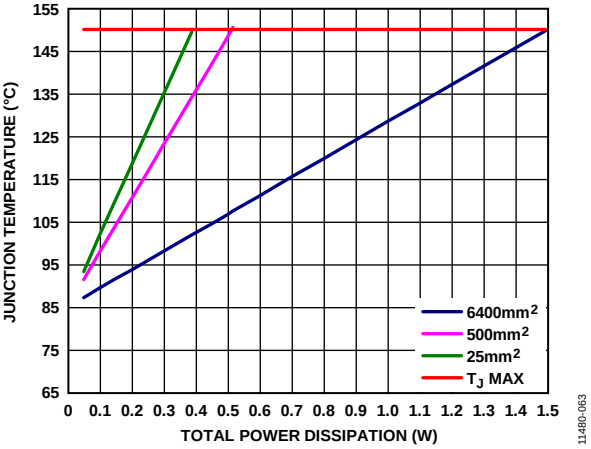


Figure 63. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 85°C

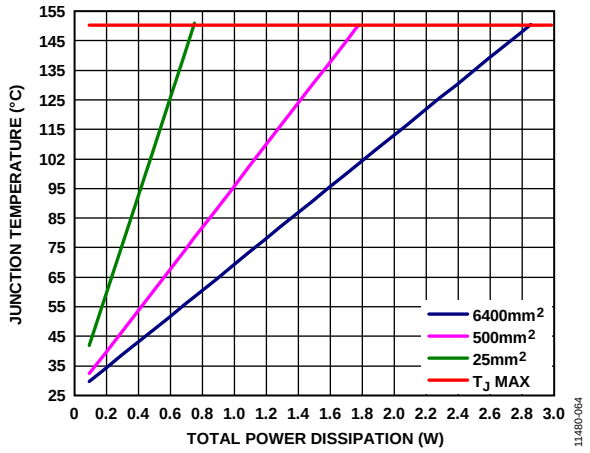


Figure 64. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 25°C

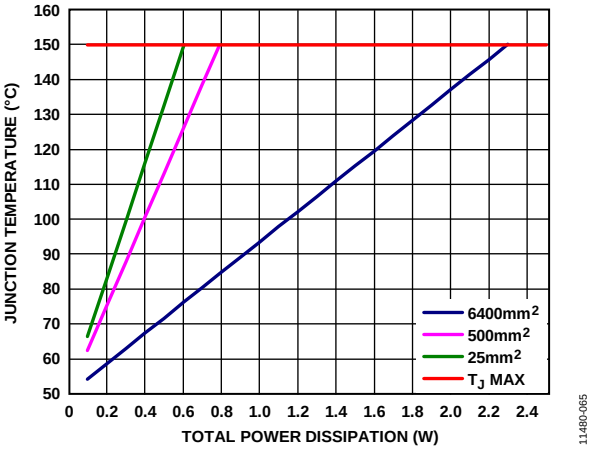


Figure 65. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 50°C

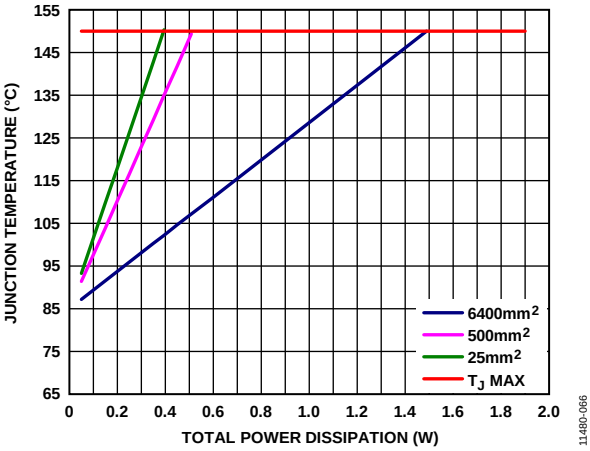


Figure 66. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 85°C

Thermal Characterization Parameter (Ψ_{JB})

When the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 67 and Figure 68). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 15.1°C/W for the 8-lead LFCSP package and 17.9°C/W for the 8-lead SOIC package.

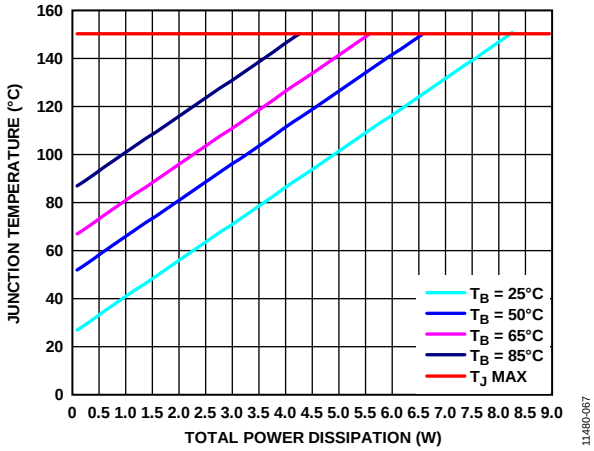


Figure 67. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP

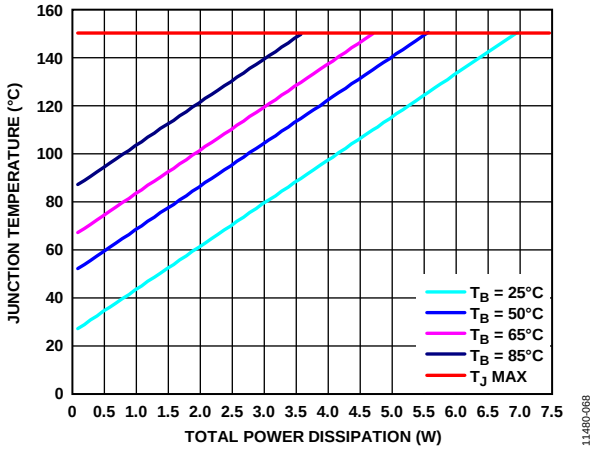


Figure 68. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Place the bypass capacitors for V_{REG}, V_{REF}, and V_{BYP} close to the respective pins and GND. Use of an 0805, 0603, or 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited.

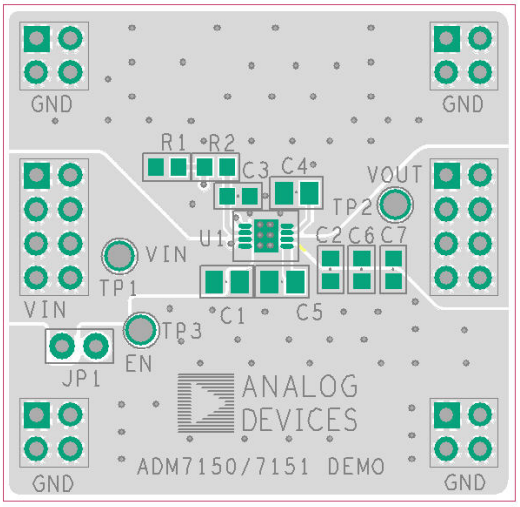


Figure 69. Example 8-Lead LFCSP PCB Layout

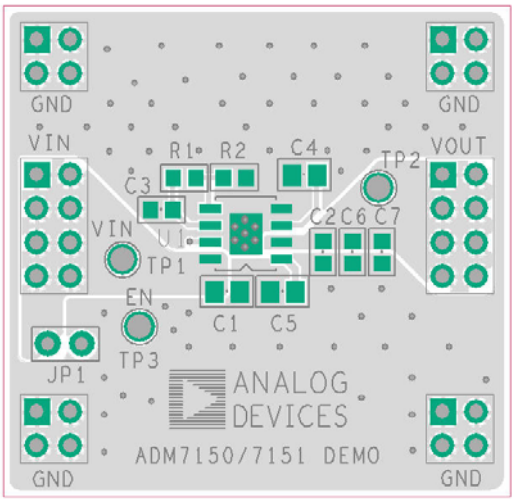
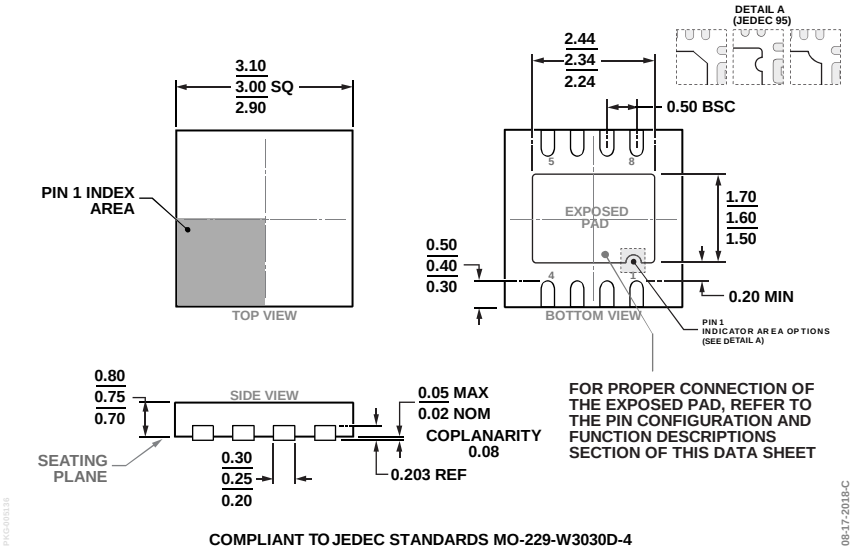


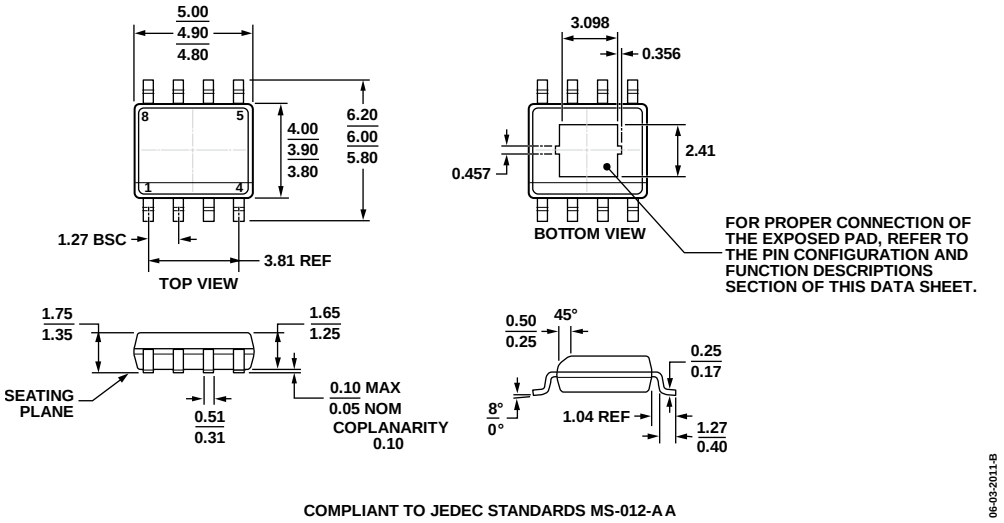
Figure 70. Example 8-Lead SOIC PCB Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229-W3030D-4

Figure 71. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-11)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

Figure 72. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage Range(V)	Package Description	Package Option	Marking Code
ADM7151ACPZ-02-R2	−40°C to +125°C	1.5 to 4.0	8-Lead LFCSP	CP-8-11	LNN
ADM7151ACPZ-02-R7	−40°C to +125°C	1.5 to 4.0	8-Lead LFCSP	CP-8-11	LNN
ADM7151ARDZ-02	−40°C to +125°C	1.5 to 4.0	8-Lead SOIC_N_EP	RD-8-2	
ADM7151ARDZ-02-R7	−40°C to +125°C	1.5 to 4.0	8-Lead SOIC_N_EP	RD-8-2	
ADM7151ACPZ-04-R2	−40°C to +125°C	1.5 to 5.1	8-Lead LFCSP	CP-8-11	LNP
ADM7151ACPZ-04-R7	−40°C to +125°C	1.5 to 5.1	8-Lead LFCSP	CP-8-11	LNP
ADM7151ARDZ-04	−40°C to +125°C	1.5 to 5.1	8-Lead SOIC_N_EP	RD-8-2	
ADM7151ARDZ-04-R7	−40°C to +125°C	1.5 to 5.1	8-Lead SOIC_N_EP	RD-8-2	
ADM7151CP-02-EVALZ		1.5 to 4.0	Evaluation Board		

[1] Z = RoHS Compliant Part.

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