5 kV rms/3 kV rms, Signal and Power Isolated, CAN Transceivers for CAN FD

Data Sheet

ADM3055E/ADM3057E

FEATURES

- 5 kV rms/3 kV rms signal and power isolated CAN transceivers
- *iso*Power integrated isolated dc-to-dc converter
- V_{IO} pin for 1.7 V to 5.5 V logic levels
- ISO 11898-2:2016 compliant (CAN FD)
- Data rates up to 12 Mbps for CAN FD
- Low maximum loop propagation delay: 150 ns
- Extended common-mode range: ±25 V
- Bus fault protection: ±40 V on CANH and CANL pins
- Low power standby support remote wake request
- Extra isolated signal for control (such as termination switches)
- Passes EN 55022 Class B by 6 dB
- Slope control for reduced EMI
- Safety and regulatory approvals (ADM3055E)
  - VDE certificate of conformity, VDE V 0884-10 (pending)
    - V_{IORM} = 849 V_{PEAK}
  - UL: 5000 V rms for 1 minute per UL 1577 (pending)
  - CSA Component Acceptance Notice 5A (pending)
    - IEC 60950-1, IEC 61010-1
- Creepage and clearance
  - ADM3055E: 8.3 mm minimum with 20-lead SOIC_IC
  - ADM3057E: 7.8 mm minimum with 20-lead SOIC_W
- High common-mode transient immunity: >75 kV/µs
- Industrial operating temperature range: −40°C to +105°C

APPLICATIONS

- CANOpen, DeviceNet, and other CAN bus implementations
- Industrial automation
- Process control and building control
- Transport and infrastructure

GENERAL DESCRIPTION

The ADM3055E/ADM3057E are 5 kV rms and 3 kV rms isolated controller area network (CAN) physical layer transceivers with integrated isolated dc-to-dc converters. The ADM3055E/ADM3057E meet flexible data rate (CAN FD) requirements for operation to 5 Mbps and higher and comply with the ISO 11898-2: 2016 standard. The ADM3055E/ADM3057E are capable of supporting data rates as high as 12 Mbps.

The devices employ Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a CAN transceiver, and an Analog Devices *iso*Power® dc-to-dc converter into a single, surface-mount, small outline integrated circuit (SOIC) package. The devices are powered by a single 5 V supply, realizing a fully isolated solution for CAN and CAN FD. Radiated emissions from the high frequency switching of the dc-to-dc convertors are kept below EN 55022 Class B limits by continuous adjustments to the switching frequency.

FUNCTIONAL BLOCK DIAGRAM

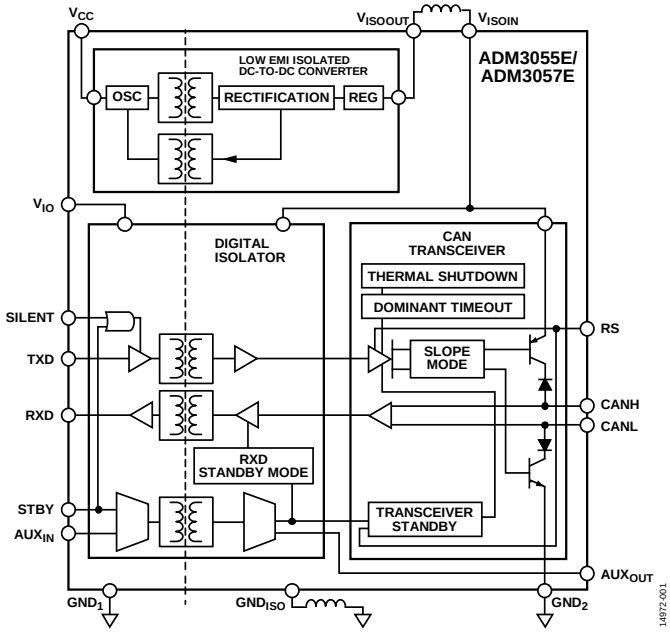

Figure 1.

The ADM3055E/ADM3057E provide complete isolation between the CAN controller and physical layer bus. Safety and regulatory approvals (pending) for 5 kV rms isolation voltage, 10 kV surge test, and 8.3 mm creepage and clearance ensure the ADM3055E meets application reinforced isolation requirements. The ADM3057E has an isolation voltage of 3 kV rms and 7.8 mm creepage in a 20-lead, wide body SOIC.

Low propagation delays through the isolation support longer bus cables. Slope control mode is available for standard CAN at low data rates. Standby mode minimizes power consumption when the bus is idle or if the node goes offline. Silent mode allows the TXD input to be ignored for listen only mode.

Dominant timeout functionality protects against bus lock up in a fault condition. The current limiting and thermal shutdown features protect against output short circuits. The devices are fully specified over an industrial temperature range of −40°C to +105°C.

Rev. B Document Feedback

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REVISION HISTORY

9/2019—Rev. A to Rev. B

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11/2018—Rev. 0 to Rev. A

Added ADM3057E and 20-Lead SOIC_W ... Universal
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8/2018—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground. 4.5 V ≤ V_{CC} ≤ 5.5 V, 1.7 V ≤ V_{IO} ≤ 5.5 V, T_{MIN} to T_{MAX}, and STBY low, unless otherwise noted. Typical specifications are at V_{CC} = V_{IO} = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Logic Side *iso*Power Current	I_{CC}					
Standby			13.5	30	mA	STBY high, AUX_{IN} low, load resistance (R_L) = 60 Ω
Recessive State (or Silent)			27	40	mA	TXD and/or SILENT high, R_L = 60 Ω
Dominant State			180	260	mA	Fault condition, see the Theory of Operation section, R_L = 60 Ω
70% Dominant/30% Recessive						Worst case, see the Theory of Operation section, R_L = 60 Ω
1 Mbps			138		mA	
5 Mbps			151	200	mA	
12 Mbps			177	220	mA	
Switching Frequency	f_{OSC}		180		MHz	Frequency hopping center
Logic Side *i*Coupler Current	I_{IO}					
Normal Mode			3.6	5	mA	TXD high, low or switching, AUX_{IN} low
Standby Mode			1.2	2	mA	STBY high
DRIVER						
Differential Outputs						See Figure 28
Recessive State, Normal Mode						TXD high, R_L and common-mode filter capacitor (C_F) open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	
Differential Output Voltage	V_{OD}	−500		+50	mV	
Dominant State, Normal Mode						TXD and SILENT low, C_F open
CANH Voltage	V_{CANH}	2.75		4.5	V	50 Ω ≤ R_L ≤ 65 Ω
CANL Voltage	V_{CANL}	0.5		2.0	V	50 Ω ≤ R_L ≤ 65 Ω
Differential Output Voltage	V_{OD}	1.5		3.0	V	50 Ω ≤ R_L ≤ 65 Ω
		1.4		3.3	V	45 Ω ≤ R_L ≤ 70 Ω
		1.5		5.0	V	R_L = 2240 Ω
Standby Mode						STBY high, R_L and C_F open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	−0.1		+0.1	V	
Differential Output Voltage	V_{OD}	−200		+200	mV	
Output Symmetry (V_{ISOIN} − V_{CANH} − V_{CANL})	V_{SYM}	−0.55		+0.55	V	R_L = 60 Ω, C_F = 4.7 nF, RS low
Short-Circuit Current	$\|I_{SC}\|$					R_L open
Absolute						
CANH				115	mA	V_{CANH} = −3 V
CANL				115	mA	V_{CANL} = 18 V
Steady State						
CANH				115	mA	V_{CANH} = −24 V
CANL				115	mA	V_{CANL} = 24 V
Logic Inputs (TXD, SILENT, STBY, AUX_{IN})						
Input Voltage						
High	V_{IH}	0.65 × V_{IO}			V	
Low	V_{IL}			0.35 × V_{IO}	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$\|I_{IH}\|$, $\|I_{IL}\|$			10	μA	Input high or low
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 29, C_{RXD} open, $-25\ V < V_{CANL}, V_{CANH} < +25\ V$
Recessive		−1.0		+0.5	V	
		−1.0		+0.4	V	STBY high
Dominant		0.9		5.0	V	
		1.15		5.0	V	STBY high
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$\|I_{IN\ (OFF)}\|$			10	μA	$V_{CANH}, V_{CANL} = 5\ V, V_{CC} = 0\ V$
Input Resistance						
CANH, CANL	R_{INH}, R_{INL}	6		25	kΩ	
Differential	R_{DIFF}	20		100	kΩ	
Matching	m_R	−0.03		+0.03	Ω/Ω	$m_R = 2 \times (R_{INH} - R_{INL})/(R_{INH} + R_{INL})$
Input Capacitance						
CANH, CANL	C_{INH}, C_{INL}		35		pF	
Differential	C_{DIFF}		12		pF	
Logic Outputs (RXD, AUX_{OUT})						
Output Voltage						
Low	V_{OL}		0.2	0.4	V	Output current (I_{OUT}) = 2 mA
High	V_{OH}					
RXD		$V_{IO} - 0.2$			V	$I_{OUT} = -2$ mA
AUX_{OUT}		+2.4			V	$I_{OUT} = -2$ mA
Short-Circuit Current	I_{OS}					
RXD		7		85	mA	Output voltage (V_{OUT}) = GND_1 or V_{IO}
COMMON-MODE TRANSIENT IMMUNITY[1]						Common-mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V
Input High, Recessive	$\|CM_H\|$	75	100		kV/μs	$V_{IN} = V_{IO}$ (AUX_{IN}, TXD) or CANH/CANL recessive
Input Low, Dominant	$\|CM_L\|$	75	100		kV/μs	$V_{IN} = 0\ V$ (AUX_{IN}, TXD) or CANH/CANL dominant
SLOPE CONTROL						
Input Voltage for Standby Mode	V_{STB}	4.0			V	
Current for Slope Control Mode	I_{SLOPE}			−240	μA	RS voltage (V_{RS}) = 0 V
Slope Control Mode Voltage	V_{SLOPE}	2.1			V	RS current (I_{RS}) = 10 μA
Input Voltage for High Speed Mode	V_{HS}			1	V	

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $AUX_{OUT} \geq 2.4\ V$, CANH/CANL recessive, or RXD ≥ $V_{IO} - 0.2\ V$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $AUX_{OUT} \leq 0.4\ V$, CANH/CANL dominant, or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All voltages are relative to their respective ground. 4.5 V ≤ V_{CC} ≤ 5.5 V, 1.7 V ≤ V_{IO} ≤ 5.5 V, T_{MIN} to T_{MAX}, and STBY low, unless otherwise noted. Typical specifications are at V_{CC} = V_{IO} = 5 V and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						SILENT low, bit time on the TXD pin as transmitted by the CAN controller (t_{BIT_TXD}) = 200 ns, see Figure 2 and Figure 30, slope resistance (R_{SLOPE}) = 0 Ω, R_L = 60 Ω, load capacitance (C_L) = 100 pF
Maximum Data Rate		12			Mbps	
Propagation Delay from TXD to Bus (Recessive to Dominant)	t_{TXD_DOM}		35	60	ns	
Propagation Delay from TXD to Bus (Dominant to Recessive)	t_{TXD_REC}		46	70	ns	
Transmit Dominant Timeout	t_{DT}	1175		4000	µs	TXD low, see Figure 5
RECEIVER						SILENT low, see Figure 2 and Figure 30, R_L = 60 Ω, C_L = 100 pF, RXD capacitance (C_{RXD}) = 15 pF
Falling Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_FALL}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Rising Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_RISE}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Loop Delay Symmetry (Minimum Recessive Bit Width)	t_{BIT_RXD}					
2 Mbps		450		550	ns	t_{BIT_TXD} = 500 ns
5 Mbps		160		220	ns	t_{BIT_TXD} = 200 ns
8 Mbps		85		140	ns	t_{BIT_TXD} = 125 ns
12 Mbps		50		91.6	ns	t_{BIT_TXD} = 83.3 ns
CANH, CANL SLEW RATE	|SR|		7		V/µs	SILENT low, see Figure 30, R_L = 60 Ω, C_L = 100 pF, R_{SLOPE} = 47 kΩ
STANDBY MODE						
Minimum Pulse Width Detected (Receiver Filter Time)	t_{FILTER}	1		5	µs	STBY high, see Figure 4
Wake-Up Pattern Detection Reset Time	t_{WUPR}	1175		4000	µs	STBY high, see Figure 4
Normal Mode to Standby Mode Time	t_{STBY_ON}			25	µs	
Standby Mode to Normal Mode Time	t_{STBY_OFF}			25	µs	Time until RXD valid
AUXILIARY SIGNAL						
Maximum Switching Rate	f_{AUX}	20			kHz	
AUX_{IN} to AUX_{OUT} Propagation Delay	t_{AUX}			25	µs	
SILENT MODE						
Normal Mode to Silent Mode Time	t_{SILENT_ON}		40	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3
Silent Mode to Normal Mode Time	t_{SILENT_OFF}		50	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3

Timing Diagrams

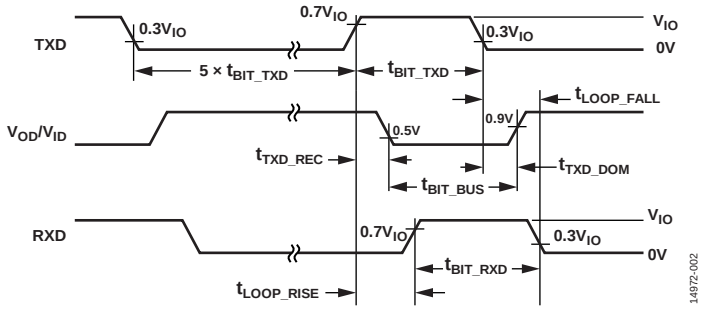


Figure 2. Transceiver Timing Diagram

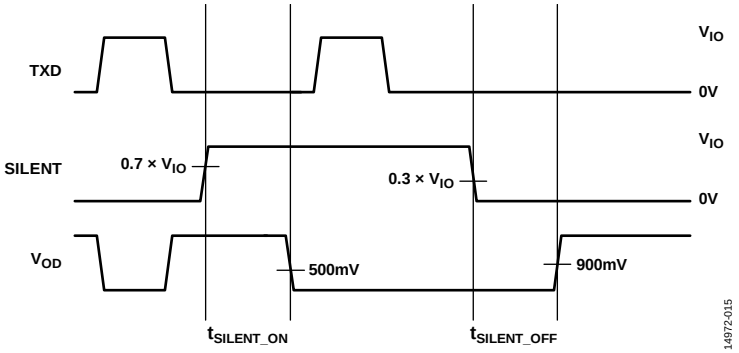


Figure 3. Silent Mode Timing Diagram

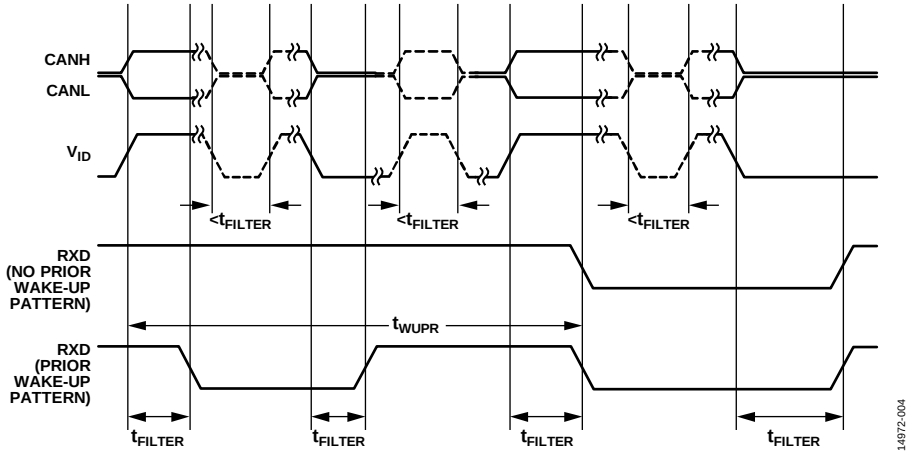


Figure 4. Wake-Up Pattern Detection and Filtered RXD in Standby Mode Timing Diagram

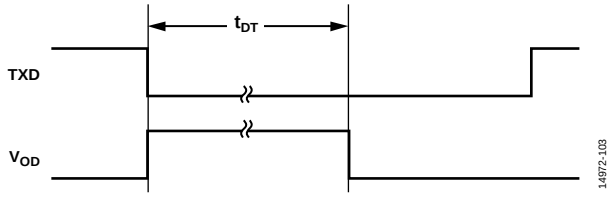


Figure 5. Dominant Timeout

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 3.

Parameter	Symbol	Value		Unit	Test Conditions/Comments
		ADM3055E	ADM3057E		
Rated Dielectric Insulation Voltage		5000	3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		21	21	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	V	IEC 60112
Material Group		I	I		Material Group (IEC 60664-1)

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		3.7		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	

[1] The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

ADM3055E

See Table 11 and the Insulation Lifetime section for details regarding maximum working voltages for specific cross isolation waveforms and insulation levels. The ADM3055E is approved or pending approval by the organizations listed in Table 5.

Table 5.

UL (Pending)[1]	CSA (Pending)	VDE (Pending)[2]	CQC (Pending)
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CQC11-471543-2012
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2 Basic insulation at 830 V rms (1174 V_{PEAK}) Reinforced insulation at 415 V rms (587 V_{PEAK}) IEC 60601-1 Edition 3.1: Basic insulation (1 MOPP), 519 V rms (734 V_{PEAK}) Reinforced insulation (2 MOPP), 261V rms (369 V_{PEAK}) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at 300 V rms mains, 830 V secondary (1174 V_{PEAK}) Reinforced insulation at 300 V rms mains, 415 V secondary (587 V_{PEAK})	Reinforced insulation 849 V_{PEAK}, surge isolation voltage (V_{IOTM}) = 8000 V_{PEAK}	GB4943.1-2011: basic insulation at 830 V rms (1174 V_{PEAK}) Reinforced insulation at 415 V rms (587 V_{PEAK})
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each ADM3055E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADM3055E is proof tested by applying an insulation test voltage ≥ 1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

ADM3057E

See Table 11 and the Insulation Lifetime section for details regarding maximum working voltages for specific cross isolation waveforms and insulation levels. The ADM3057E is approved or pending approval by the organizations listed in Table 6.

Table 6.

UL (Pending)[1]	CSA (Pending)	VDE (Pending)[2]	CQC (Pending)
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CQC11-471543-2012
Single Protection, 3000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2	Reinforced insulation 849 V_{PEAK}, surge isolation voltage (V_{IOTM}) = 6000 V_{PEAK}	GB4943.1-2011: basic insulation at 780 V rms (1103 V_{PEAK})
	Basic insulation at 780 V rms (1103 V_{PEAK})		Reinforced insulation at 390 V rms (552 V_{PEAK})
	Reinforced insulation at 390 V rms (552 V_{PEAK})		
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 MOPP), 490 V rms (693 V_{PEAK})		
	Reinforced insulation (2 MOPP), 250 V rms (353 V_{PEAK})		
	CSA 61010-1-12 and IEC 61010-1 third edition		
	Basic insulation at 300 V rms mains, 780 V secondary (1103 V_{PEAK})		
	Reinforced insulation at 300 V rms mains, 390 V secondary (552 V_{PEAK})		
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each ADM3057E is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADM3057E is proof tested by applying an insulation test voltage ≥ 1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. The protective circuits ensure the maintenance of the safety data. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 7. ADM3055E VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1273	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V_{PEAK}
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{IOTM}	8000	V_{PEAK}
Surge Isolation Voltage Reinforced	$V_{IOSM(TEST)}$ = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 6)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.55	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

Table 8. ADM3057E VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1273	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V_{PEAK}
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{IOTM}	6000	V_{PEAK}
Surge Isolation Voltage Reinforced	$V_{IOSM(TEST)}$ = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 7)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.35	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

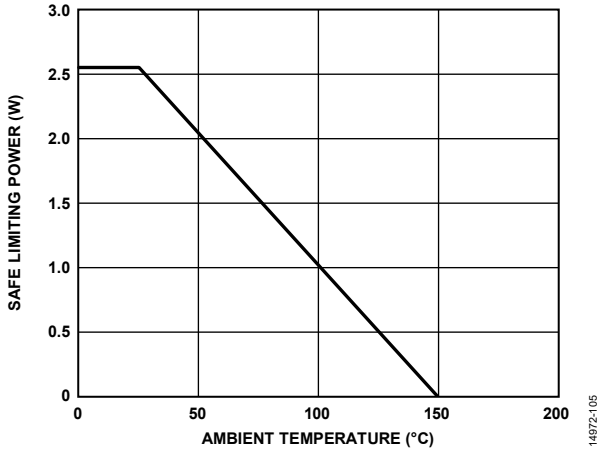


Figure 6. ADM3055E Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

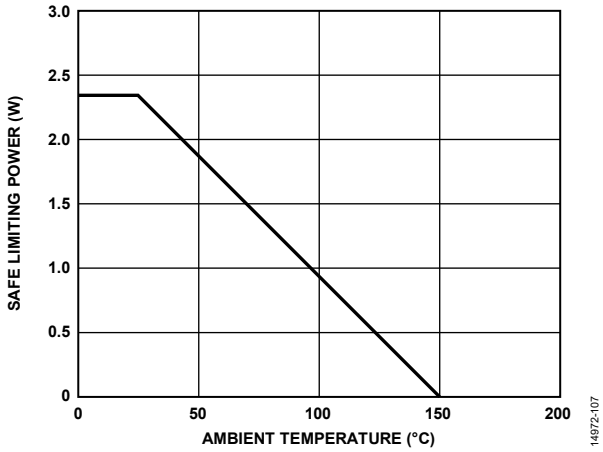


Figure 7. ADM3057E Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to GND_x are on the same side, unless otherwise noted.

Table 9.

Parameter	Rating
V_{CC}	−0.5 V to +6 V
V_{IO}	−0.5 V to +6 V
Logic Side Input/Output: TXD, RXD, AUX_{IN}, SILENT, STBY	−0.5 V to V_{IO} + 0.5 V
CANH, CANL	−40 V to +40 V
AUX_{OUT}, RS	−0.5 V to V_{ISOIN} + 0.5 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Electrostatic Discharge (ESD)	
IEC 61000-4-2, CANH/CANL	
Across Isolation Barrier to GND_1	±8 kV
Contact Discharge to GND_2	±8 kV
Air Discharge to GND_2	±15 kV
Human Body Model (HBM), All Pins, 1.5 kΩ, 100 pF	4 kV
Moisture Sensitivity Level (MSL)	3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 10. Thermal Resistance

Package Type[1]	θ_{JA}	Unit
RI-20-1	49	°C/W
RW-20	53	°C/W

[1] Thermocouple located at the center of the package underside, test conducted on a 4-layer board with thin traces. See the Thermal Analysis section for thermal model definitions.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 11. Maximum Continuous Working Voltage[1]

Parameter	Rating		Unit	Constraint
	ADM3055E	ADM3057E		
AC Voltage				
Bipolar Waveform				
Basic Insulation	566	566	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	467	467	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Unipolar Waveform				
Basic Insulation	1131	1131	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	933	933	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
DC Voltage				
Basic Insulation	1660	1560	V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
Reinforced Insulation	830	780	V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

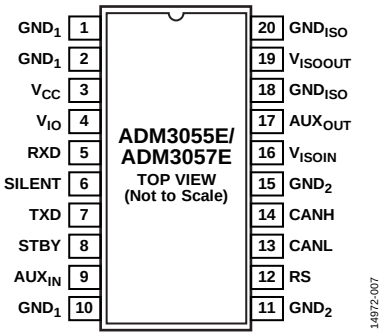


Figure 8. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 10	GND_1	Ground, Logic Side.
3	V_{CC}	*iso*Power Power Supply, 4.5 V to 5.5 V. This pin requires 0.1 µF and 10 µF decoupling capacitors.
4	V_{IO}	*i*Coupler Power Supply, 1.7 V to 5.5 V. This pin requires 0.01 µF and 0.1 µF decoupling capacitors.
5	RXD	Receiver Output Data.
6	SILENT	Silent Mode Select with Input High. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
7	TXD	Driver Input Data. This pin has a weak internal pull-up resistor to V_{IO}.
8	STBY	Standby Mode Select with Input High. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
9	AUX_{IN}	Auxiliary Channel Input. This pin sets the AUX_{OUT} output.
11, 15	GND_2	Ground, Bus Side.
12	RS	Slope Control Pin. Short this pin to ground for full speed operation or use a weak pull-down resistor (for example, 47 kΩ) for slope control mode. An input high signal places the CAN transceiver in standby mode.
13	CANL	CAN Low Input/Output.
14	CANH	CAN High Input/Output.
16	V_{ISOIN}	Isolated Power Supply Input for the CAN Transceiver Bus Side Digital Isolator. This pin requires 0.01 µF and 0.1 µF decoupling capacitors.
17	AUX_{OUT}	Isolated Auxiliary Channel Output. The state of AUX_{OUT} is latched when STBY is high. By default, AUX_{OUT} is low at startup or when V_{IO} is unpowered.
18, 20	GND_{ISO}	Ground for the Isolated DC-to-DC Converter. Connect these pins together through one ferrite bead to PCB ground (bus side).
19	V_{ISOOUT}	Isolated Power Supply Output. This pin requires 0.22 µF and 10 µF capacitors to GND_{ISO}. Connect this pin through a ferrite bead and short the PCB trace to V_{ISOIN} for operation.

OPERATIONAL TRUTH TABLE

Table 13. Truth Table

Power		Inputs[1, 2]						Outputs[2]		Input/Output
V_{CC}	V_{IO}	TXD	SILENT	STBY	AUX_{IN}	RS	Mode	RXD[3]	AUX_{OUT}	CANH/CANL
On	On	Low	Low	Low	Low	Low/ pull-down	Normal/ slope mode	Low	Low	Dominant[4]
On	On	Low	Low	Low	High	Low/ pull-down	Normal/ slope mode	Low	High	Dominant[4]
On	On	High	Low	Low	Low	Low/ pull-down	Normal/ slope mode	High/per bus	Low	Recessive/set by bus
On	On	High	Low	Low	High	Low/ pull-down	Normal/ slope mode	High/per bus	High	Recessive/set by bus
On	On	X	High	Low	Low	X	Listen only	High/per bus	Low	Recessive/set by bus
On	On	X	High	Low	High	X	Listen only	High/per bus	High	Recessive/set by bus
On	On	X	X	High	X	X	Standby	High/WUP/filtered	Last state	Bias to GND_2/set by bus
On	On	X	X	X	Low	Pull-up	Standby[5]	High/WUP/filtered	Low	Bias to GND_2/set by bus
On	On	X	X	X	High	Pull-up	Standby[5]	High/WUP/filtered	High	Bias to GND_2/set by bus
On	Off	Z	Z	Z	Z	Low/ pull-down	Normal/ slope mode	Z	Low	Recessive/set by bus
Off	On	X	X	X	X	X	Transceiver off	High	Z	High impedance/set by bus
Off	Off	Z	Z	Z	Z	Z	Transceiver off	Z	Z	High impedance/set by bus

[1] X means irrelevant.
[2] Z means high impedance within one diode drop of ground.
[3] WUP means remote wake-up pattern.
[4] Limited by t_{DT}.
[5] RS can only set the transceiver to standby mode. RS does not control the digital isolator.

TYPICAL PERFORMANCE CHARACTERISTICS

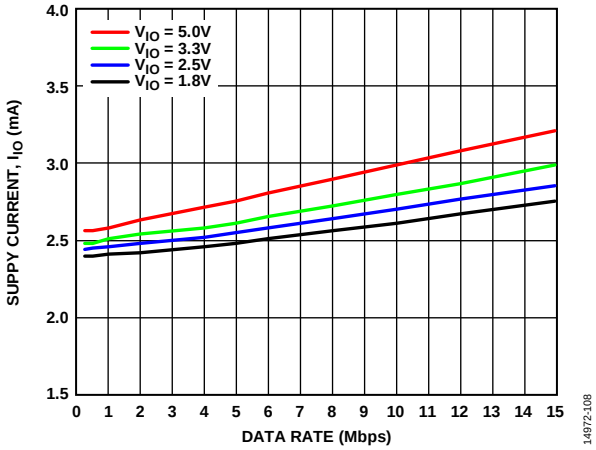


Figure 9. Supply Current, I_{IO} vs. Data Rate

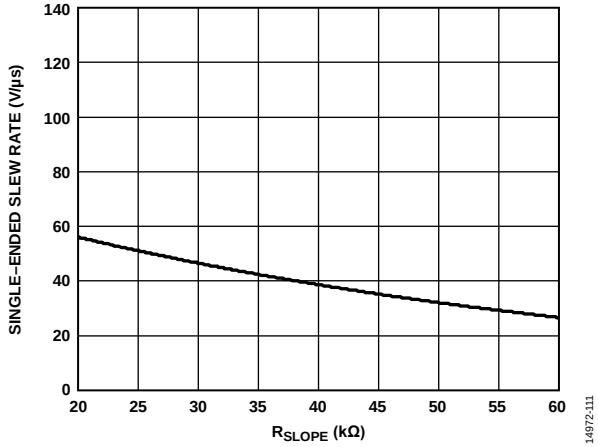


Figure 12. Single-Ended Slew Rate vs. R_{SLOPE}

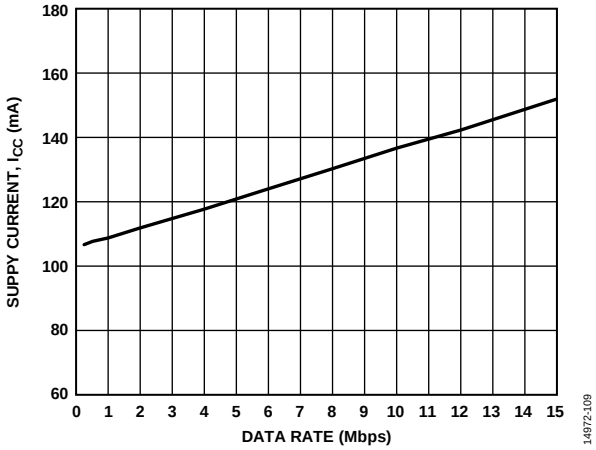


Figure 10. Supply Current, I_{CC} vs. Data Rate

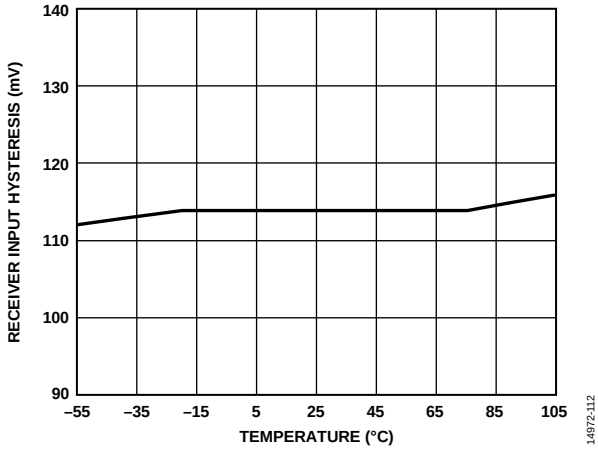


Figure 13. Receiver Input Hysteresis vs. Temperature

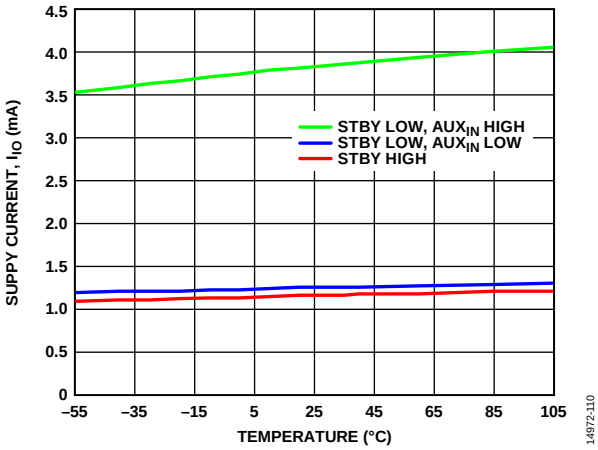


Figure 11. Supply Current, I_{IO} vs. Temperature (Inputs Idle)

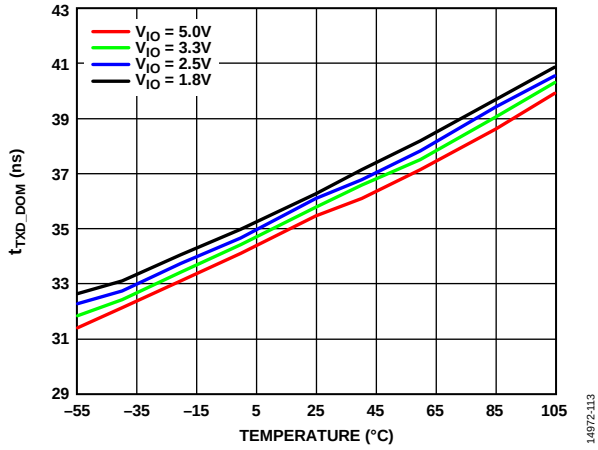


Figure 14. t_{TXD_DOM} vs. Temperature

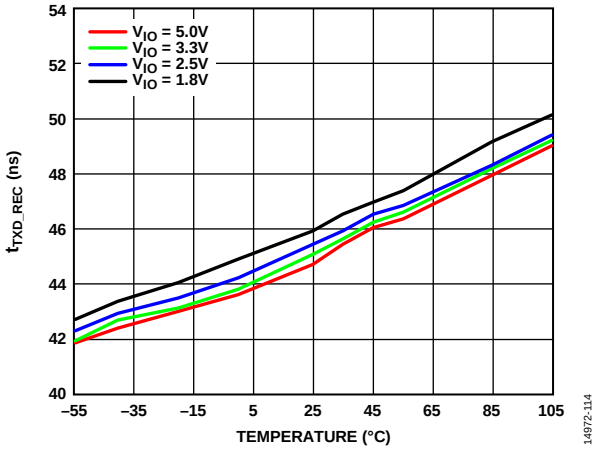


Figure 15. t_{TXD_REC} vs. Temperature

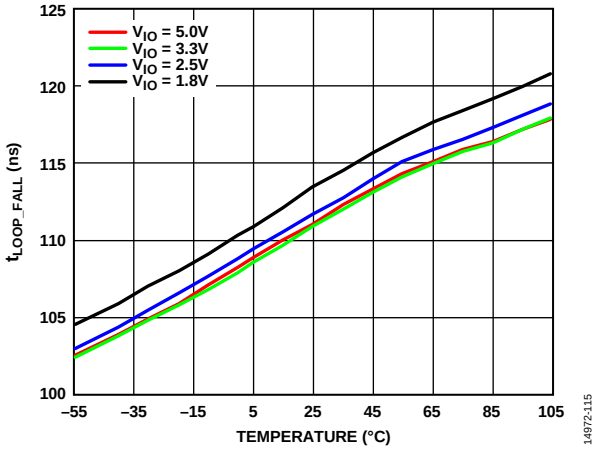


Figure 16. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 0 Ω)

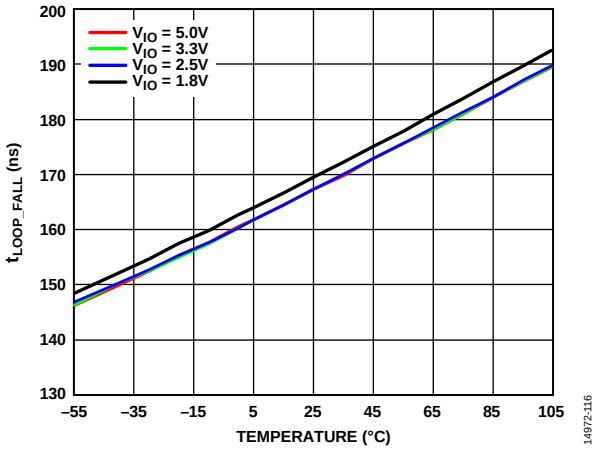


Figure 17. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 47 kΩ)

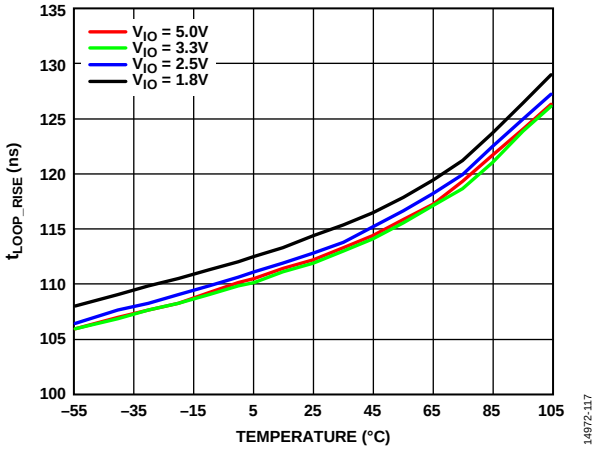


Figure 18. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 0 Ω)

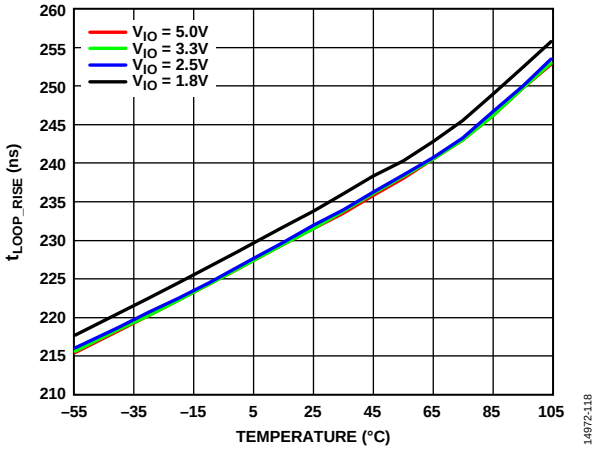


Figure 19. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 47 kΩ)

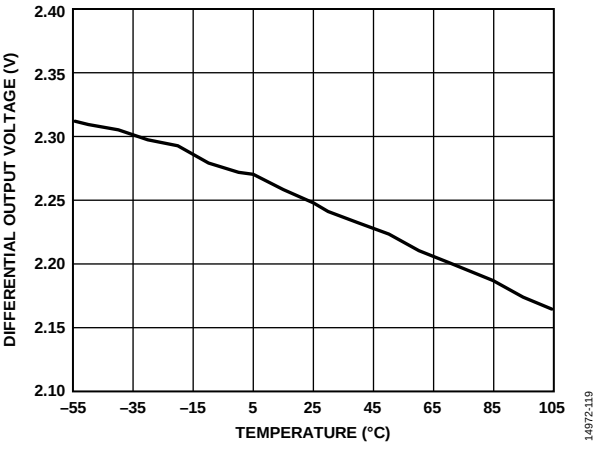


Figure 20. Differential Output Voltage (V_{OD}) vs. Temperature

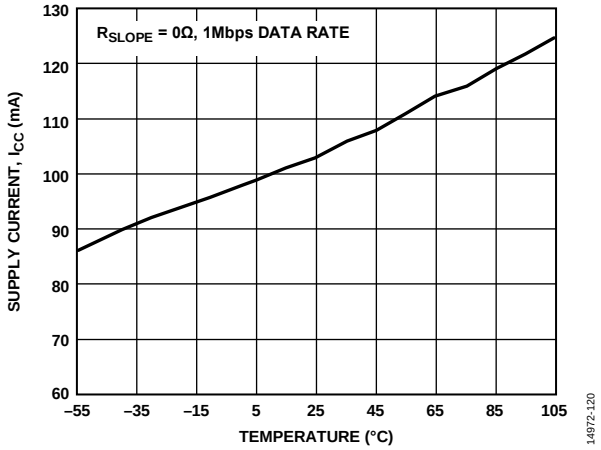


Figure 21. Supply Current, I_{CC} vs. Temperature

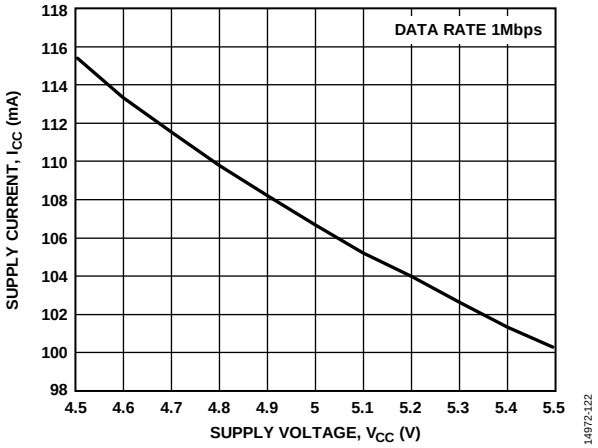


Figure 23. Supply Current, I_{CC} vs. Supply Voltage, V_{CC}, RS = 0 Ω, 1 Mbps

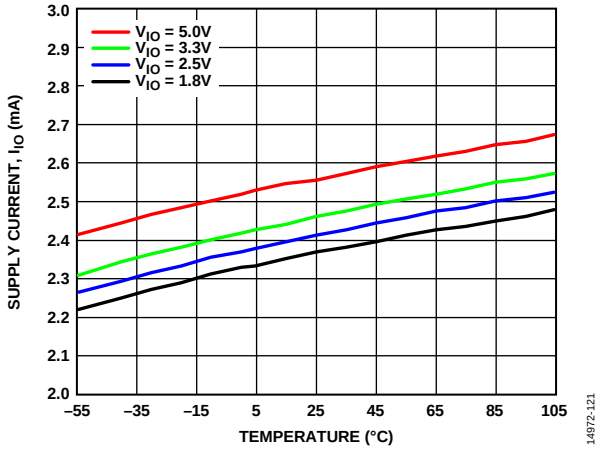


Figure 22. Supply Current, I_{IO} vs. Temperature, RS = 0 Ω, 1 Mbps

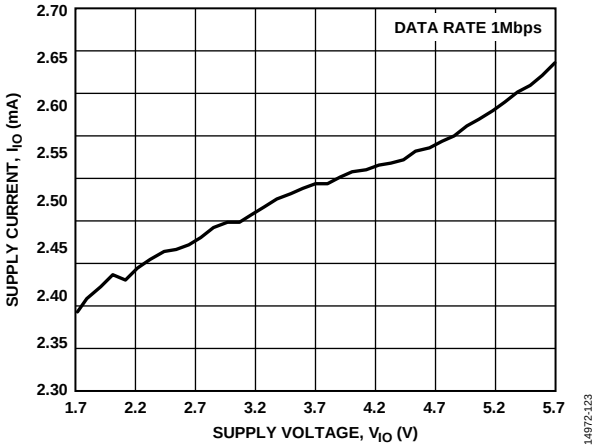


Figure 24. Supply Current, I_{IO} vs. Supply Voltage, V_{IO}, Data Rate = 1 Mbps

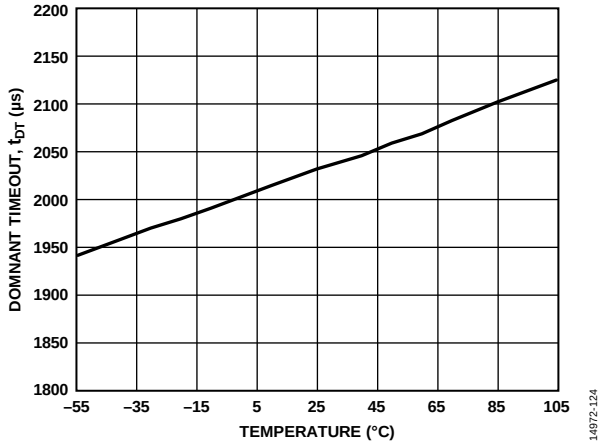


Figure 25. Dominant Timeout, t_{DT} vs. Temperature

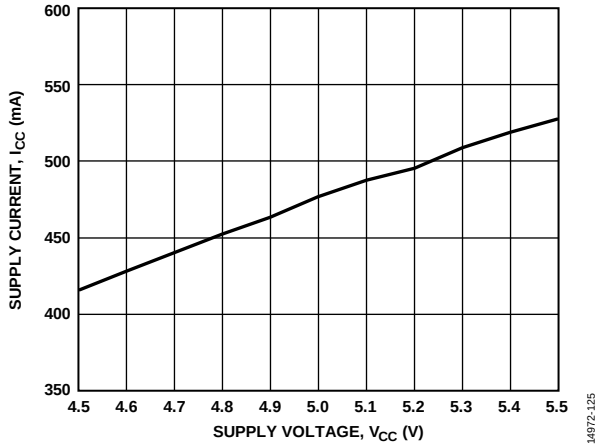


Figure 26. Supply Current, I_{CC} vs. Supply Voltage, V_{CC} (V_{ISOOUT} Shorted to GND_{ISO})

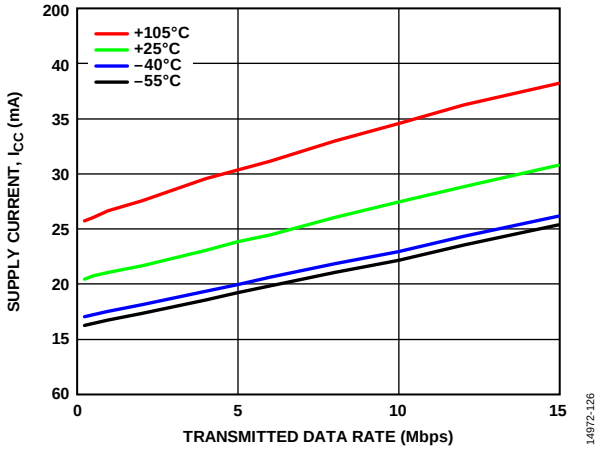


Figure 27. Supply Current, I_{CC} vs. Transmitted Data Rate

TEST CIRCUITS

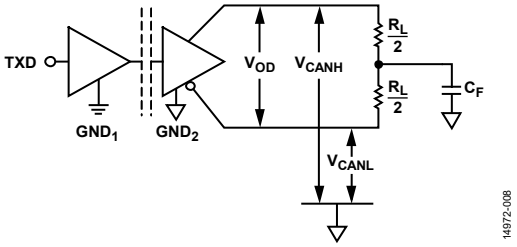


Figure 28. Driver Voltage Measurement

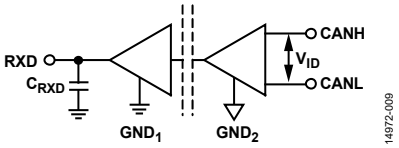


Figure 29. Receiver Voltage Measurement

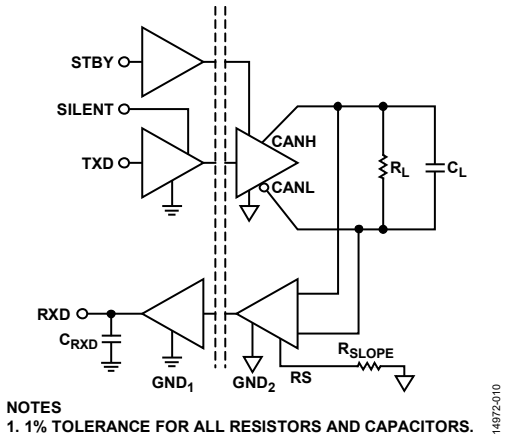


Figure 30. Switching Characteristics Measurements

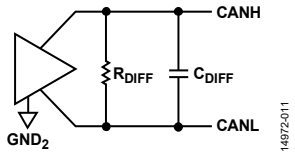


Figure 31. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

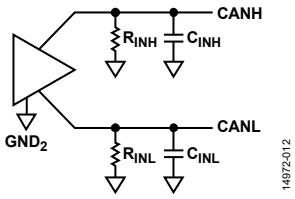


Figure 32. R_{IN} and C_{IN} Measured in Recessive State, Bus Disconnected

TERMINOLOGY

I_{CC}
I_{CC} is the current drawn by the V_{CC} pin. This pin powers the *iso*Power dc-to-dc converter.

I_{IO}
I_{IO} is the current drawn by the V_{IO} pin. This pin powers the *i*Coupler digital isolator.

I_{SC}
I_{SC} is the current drawn by the V_{ISOIN} pin under the specified fault condition.

V_{OD}
The V_{OD} is the difference of the CANH and CANL levels, which is V_{DIFF} in ISO 11898-2:2016.

f_{OSC}
f_{OSC} is the carrier frequency of the *iso*Power dc-to-dc converter that provides isolated power to the bus side.

t_{TXD_DOM}
t_{TXD_DOM} is the propagation delay from a low signal on TXD to transition the bus to a dominant state.

t_{TXD_REC}
t_{TXD_REC} is the propagation delay from a high signal on TXD to transition the bus to a recessive state.

t_{LOOP_FALL}
t_{LOOP_FALL} is the propagation delay of a low signal on the TXD pin to the bus dominant and transitions low on the RXD pin.

t_{LOOP_RISE}
t_{LOOP_RISE} is the propagation delay of a high signal on the TXD pin to the bus recessive and transitions high on the RXD pin.

t_{BIT_TXD}
t_{BIT_TXD} is the bit time on the TXD pin as transmitted by the CAN controller. See Figure 2 for level definitions.

t_{BIT_BUS}
t_{BIT_BUS} is the bit time transmitted by the transceiver to the bus. When compared with a given t_{BIT_TXD}, a measure of bit symmetry from the TXD digital isolation channel and CAN transceiver can be determined. See Figure 2 for level definitions.

t_{BIT_RXD}
t_{BIT_RXD} is the bit time on the RXD output pin that can be compared with t_{BIT_TXD} for a round trip measure of pulse width distortion through the TXD digital isolation channel, the CAN transceiver, and back through the RXD isolation channel.

Wake-Up Pattern (WUP)
WUP is a remote transmitted pattern required to trigger low speed data transmission by the CAN transceiver while in standby mode. The pattern does not force the transceiver out of standby mode.

THEORY OF OPERATION

CAN TRANSCEIVER OPERATION

The ADM3055E/ADM3057E facilitate communication between a CAN controller and the CAN bus. The CAN controller and the ADM3055E/ADM3057E communicate with standard 1.8 V, 2.5 V, 3.3 V, or 5.0 V CMOS levels. The internal transceiver translates the CMOS levels to and from the CAN bus.

The CAN bus has two states: dominant and recessive. The recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. In the recessive state, the CANH and CANL pins are set to high impedance and are loosely biased to a single-ended voltage of 2.5 V. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 1.5 V. The transceiver transmits a dominant state by driving the single-ended voltage of the CANH pin to 3.5 V and the CANL pin to 1.5 V. The recessive and dominant states correspond to CMOS high and CMOS low, respectively, on the RXD pin and TXD pin.

A dominant state from another node overwrites a recessive state on the bus. A CAN frame can be set for higher priority by using a longer string of dominant bits to gain control of the CAN bus during the arbitration phase. While transmitting, a CAN transceiver also reads back the state of the bus. When a CAN controller receives a dominant state while transmitting a recessive state during arbitration, the CAN controller surrenders the bus to the node still transmitting the dominant state. The node that gains control during the arbitration phase reads back only its own transmission. This interaction between recessive and dominant states allows competing nodes to negotiate for control of the bus while avoiding contention between nodes.

Industrial applications can have long cable runs. These long runs may have differences in local earth potential. Different sources may also power nodes. The ADM3055E transceiver has a ±25 V common-mode range (CMR) that exceeds the ISO 11898-2:2016 requirement and further increases the tolerance to ground variation.

See the AN-1123 Application Note for additional information on CAN.

SIGNAL AND POWER ISOLATION

The ADM3055E and the ADM3057E provide galvanic signal isolation implemented on the logic side of the interface. The RXD and TXD isolation channels transmit and receive with an on/off keying (OOK) architecture on the *i*Coupler digital isolation technology.

The ADM3055E and the ADM3057E feature independent power supply pins for isolated power (the V_{CC} pin) and isolated signal (the V_{IO} pin). The V_{CC} pin requires a nominal 5 V supply to produce the 5 V isolated power. The V_{IO} pin may be supplied with a nominal 1.8 V to a nominal 5 V. The logic input and output levels scale to the voltage supplied to the V_{IO} pin. The isolated power from the V_{ISOOUT} pin must be supplied to the V_{ISOIN} pin to power the bus side digital isolator and transceiver.

STANDBY MODE

The STBY pin engages a reduced power standby mode that modifies the operation of both the CAN transceiver and digital isolation channels. Standby mode disables the TXD signal isolation channel and sets the transmitter output to a high impedance state loosely biased to GND_2. While in standby mode, the receiver filters bus data and responds only after the remote wake-up sequence is received.

When entering or exiting standby mode, the TXD input must be kept high and the RXD output must be ignored for the full t_{STBY_ON} and t_{STBY_OFF} times. STBY does not control or modify behavior of the *iso*Power integrated dc-to-dc converter. The dc-to-dc converter continues to operate and provide the power to the bus side.

REMOTE WAKE UP

The ADM3055E and the ADM3057E respond to the remote wake-up sequence as defined in ISO 11898-2:2016. When CAN channels are presented with the defined slow speed high low high sequence within the low wake-up pattern detection reset time (t_{WUPR}), low speed data transmission is allowed.

Successful receipt of the remote wake-up pattern does not bring the ADM3055E and the ADM3057E out of standby mode. The ADM3055E STBY pin must be brought low externally to exit standby mode. After the ADM3055E or ADM3057E device receives the remote wake-up pattern, the transceiver continues to receive low speed data until standby mode is exited.

SILENT MODE

Asserting the SILENT pin disables the TXD digital isolation channel. Any inputs to the TXD pin are ignored in this mode, and the transceiver presents a recessive bus state. The operation of the RXD channel is unaffected. The RXD channel continues to output data received from the internal CAN transceiver monitoring the bus.

Silent mode is useful when paired with a CAN controller using automatic baud rate detection. A CAN controller must be set to the same data rate as all attached nodes. The CAN controller produces an error frame and ties up the bus with a dominant state when the received data rate is different from expected. Other CAN nodes then echo this error frame. While in silent mode, the error frames produced by the CAN controller are kept from interrupting bus traffic, and the controller can continue listening to bus traffic to tune.

RS PIN

The RS pin sets the transceiver in one of three different modes of operation: high speed, slope control, or standby. This pin cannot be left floating.

For high speed mode, connect the RS pin directly to GND_2. Ensure that the transition time of the CAN bus signals are as short as possible to allow higher speed signaling. A shielded cable is recommended to avoid electromagnetic interference (EMI) problems in high speed mode.

Slope control mode allows the use of unshielded twisted pair wires or parallel pair wires as bus lines. Slow the signal rise and fall transition times to reduce EMI and ringing in slope control mode. Adjust the rise and fall slopes by adding a resistor (R_{SLOPE}) connected from RS to GND_2. The slope is proportional to the current output at the RS pin.

The RS pin can also set the CAN transceiver to standby mode, which occurs when the pin is driven to a voltage above V_{STB}. In standby mode, high speed data is filtered, and the CANH and CANL lines are biased to GND_2.

The RS pin can only set the CAN transceiver to standby mode. The state of the RS pin does not modify the operation of digital isolation channels or the auxiliary channel.

AUXILIARY CHANNEL

The auxiliary channel is available for low speed data transmission at up to 20 kHz (or 40 kbps nonreturn-to-zero format) when STBY is not asserted. The data rate limit of the channel allows the data channel to be shared by the STBY signal.

In standby mode, or when STBY is driven high, the operation of the channel is modified to share the multiplexed signal path with the STBY signal (see Figure 1). The AUX_{OUT} pin remains latched in the state when STBY is asserted. Periodic pulses (<25 µs wide) are sent to indicate that the logic side is powered and remains in standby mode.

In applications where AUX_{OUT} may be shorted to GND_2 or V_{DD2}, add a series resistance to the output channel.

An example of using this auxiliary channel to control a switchable termination from the logic side is demonstrated on the EVAL-ADM3055EEBZ evaluation board.

INTEGRATED AND CERTIFIED IEC EMC SOLUTION

Typically, designers must add protections against harsh operating environments while also making the product as small as possible. To reduce board space and the design effort needed to meet system level ESD standards, the ADM3055E and the ADM3057E include robust protection circuitry on chip for the CANH and CANL lines.

FAULT PROTECTION

Miswire events commonly occur when the system power supply is connected directly to the CANH and CANL bus lines during assembly. The ADM3055E and the ADM3057E CAN bus pins are protected against such high voltage miswire events. The ADM3055E and the ADM3057E CANH and CANL signal lines can withstand continuous ±40 V with respect to GND_2 or +40 V between the CAN bus lines without damage. This level of protection applies when the device is either powered or unpowered.

The ADM3055E provides IEC 61000-4-2 Level 4 ESD protection, but some applications may require further system level protection. The symmetrical nature of the ADM3055E ±40 V bus fault protection and the ±25 V CMR makes the selection of bidirectional transient voltage suppressor (TVS) diodes easier.

FAIL-SAFE FEATURES

In cases where the TXD input pin is allowed to float, to prevent bus traffic interruption, the TXD input channel has an internal pull-up to the V_{IO} pin. The pull-up holds the transceiver in the recessive state.

The ADM3055E and the ADM3057E feature a dominant timeout (t_{DT} in Table 2). A TXD line shorted to ground or malfunctioning CAN controller are examples of how a single node can indefinitely prevent further bus traffic. The dominant timeout limits how long the dominant state can transmit to the CAN bus by the transceiver. When the TXD pin is presented with a logic high, normal TXD functionality is restored.

The t_{DT} minimum also inherently creates a minimum data rate. Under normal operation, the CAN protocol allows five consecutive bits of the same polarity before stuffing a bit of the opposite polarity into the transmitting bit sequence. When an error is detected, the CAN controller purposely violates the bit stuffing rules by producing six consecutive dominant bits. At any given data rate, the CAN controller must transmit as many as 11 consecutive dominant bits to effectively limit the ADM3055E and the ADM3057E minimum data rate to 9600 bps.

THERMAL SHUTDOWN

The ADM3055E and the ADM3057E contain thermal shutdown circuitry that protects the devices from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. The circuitry disables the driver outputs when the die temperature reaches 175°C. When the die has cooled, the drivers are enabled again.

APPLICATIONS INFORMATION

PCB LAYOUT

Power supply bypassing is required at the logic input supply, V_{IO}, and at the shared CAN transceiver and digital isolator input supply pin, V_{ISOIN}. Low equivalent series resistance (ESR) bypass capacitors are required and must be placed as close to the chip pads as possible. The ADM3055E and the ADM3057E signal and power isolated CAN transceivers do not require external interface circuitry for the logic interfaces.

The integrated dc-to-dc converter supply input pin, V_{CC}, requires parallel 10 µF and 0.1 µF bypass capacitors placed close to the pin. Noise suppression requires a low inductance, high frequency capacitor. Ripple suppression and proper regulation require a large value capacitor. Effective bypass capacitance is also required on the isolated output supply pin, V_{ISOOUT}, for proper operation of the integrated dc-to-dc converter. Note that the total trace length between the ends of the low ESR capacitors and the input power supply pins, V_{CC}, V_{IO}, V_{ISOIN}, and V_{ISOOUT}, must not exceed 2 mm.

RADIATED EMISSIONS AND PCB LAYOUT

The ADM3055E and the ADM3057E signal and power isolated CAN FD transceivers pass EN 55022 Class B by 6 dB on a 2-layer PCB design with ferrite beads. Neither PCB stitching capacitance nor high voltage surface-mounted technology (SMT) safety capacitors are required to meet this emissions level.

The ADM3055E and the ADM3057E have an internal split pad lead frame on the bus side to isolate noise generated by the dc-to-dc converter from the transceiver. For best noise suppression, filter both the V_{ISOOUT} power supply pin and GND_{ISO} power supply return pin for high frequency currents before routing power to the transceiver. Use surface-mount ferrite beads in series with the signals, as shown in Figure 33.

The *iso*Power integrated dc-to-dc converters of the ADM3055E and the ADM3057E produce a 180 MHz carrier frequency to transmit power through the chip scale transformer. The impedance of the ferrite bead must be approximately 2 kΩ between the 100 MHz and 1 GHz frequency range to reduce the emissions of the 180 MHz primary switching frequency and 360 MHz secondary side rectifying frequency. See Table 14 for examples of appropriate surface-mount ferrite beads. Although the ferrite beads are beneficial for emissions performance, the ferrite beads are not required for functionality.

Table 14. Surface-Mount Ferrite Beads Example

Manufacturer	Part No.
Taiyo Yuden	BKH1005LM182-T
Murata Electronics	BLM15HD182SN1

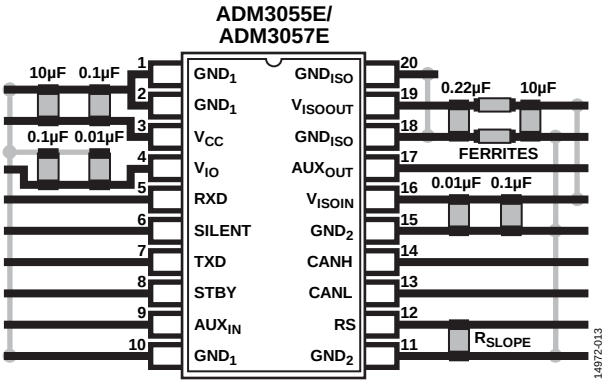


Figure 33. Recommended PCB Layout

THERMAL ANALYSIS

The ADM3055E and the ADM3057E consist of six internal die attached to a split lead frame with four die attach pads. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} value in Table 10. The θ_{JA} value is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADM3055E and the ADM3057E can operate at full load across the full temperature range without derating the output current.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and is the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, allowing the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and can therefore provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. See Table 3 for the material group and creepage information for the ADM3055E and the ADM3057E isolated CAN transceivers.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the thickness, material properties, and the voltage stress applied across the insulation. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation, causing incremental damage. The stress on the insulation can be divided into broad categories, such as dc stress and ac component, time varying voltage stress. DC stress causes little wear out because there is no displacement current, whereas ac component, time varying voltage stress causes wear out.

The ratings in certification documents are typically based on 60 Hz sinusoidal stress to reflect isolation from the line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier, as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ \ RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\ \ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 $V_{AC\ RMS}$, and a 400 V_{DC} bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages used to determine the creepage, clearance, and lifetime of a device, see Figure 34 and the equations that follow.

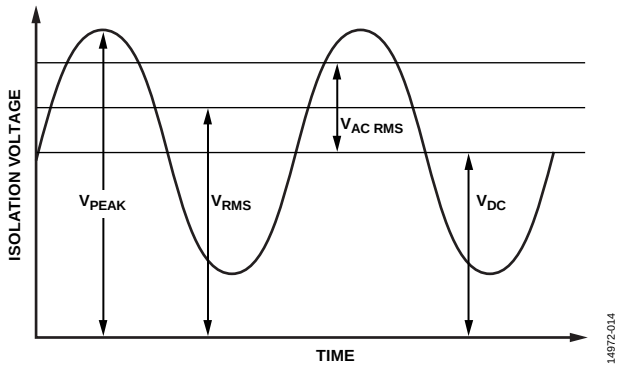


Figure 34. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ \ RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466\ \text{V}$$

Use this V_{RMS} value as the working voltage in conjunction with the material group and pollution degree to determine the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ \ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

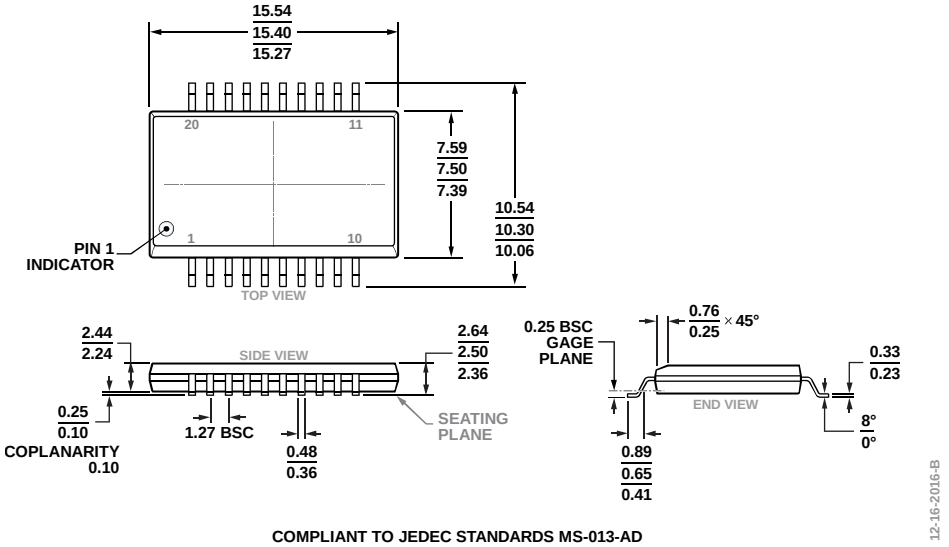
$$V_{AC\ \ RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC\ RMS} = 240\ \text{V}_{RMS}$$

In this case, the ac rms voltage is simply the line voltage of 240 V_{RMS}. This calculation is more relevant when the waveform is not sinusoidal. The calculated ac rms voltage is compared to the limits for the working voltage in Table 11 for the expected lifetime of the device, which is less than a 60 Hz sine wave, and is well within the limit for a 50-year service life.

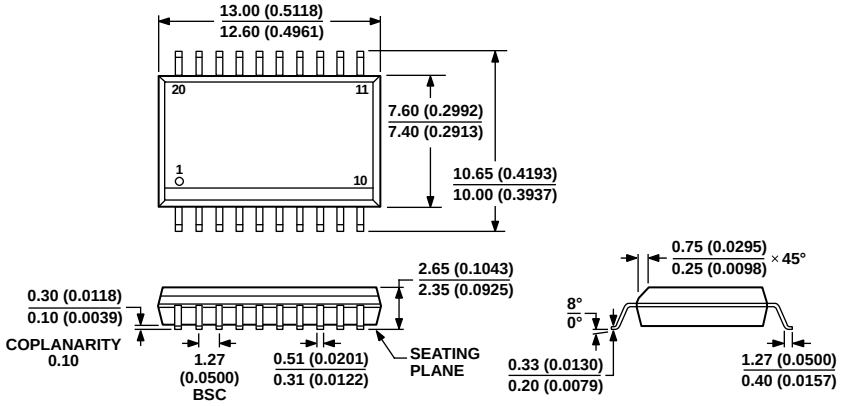
The dc working voltage limit is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AD

Figure 35. 20-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]
Wide Body,
(RI-20-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-013-AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body,
(RW-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADM3055EBRIZ	−40°C to +105°C	20-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]	RI-20-1
ADM3055EBRIZ-RL	−40°C to +105°C	20-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]	RI-20-1
EVAL-ADM3055EEBZ		ADM3055E Evaluation Board	
ADM3057EBRWZ	−40°C to +105°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADM3057EBRWZ-RL	−40°C to +105°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20

[1] Z = RoHS Compliant Part.
[2] Use the EVAL-ADM3055EEBZ evaluation board to evaluate the ADM3057E.

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