# Quad UV/OV Positive/Negative Voltage Supervisor

# ADM2914

## FEATURES

**Quad UV/OV positive/negative supervisor**
**Supervises up to 2 negative rails**
**Adjustable UV and OV input thresholds**
**High threshold accuracy over temperature: ±1.5%**
**1 V buffered reference output**
**Open-drain $\overline{UV}$ and $\overline{OV}$ reset outputs**
**Adjustable reset timeout with disable option**
**Outputs guaranteed down to $V_{CC}$ of 1 V**
**Glitch immunity**
**62 µA supply current**
**16-lead QSOP package**

## APPLICATIONS

**Server supply monitoring**
**FPGA/DSP core and I/O voltage monitoring**
**Telecommunications equipment**
**Medical equipment**

## FUNCTIONAL BLOCK DIAGRAM

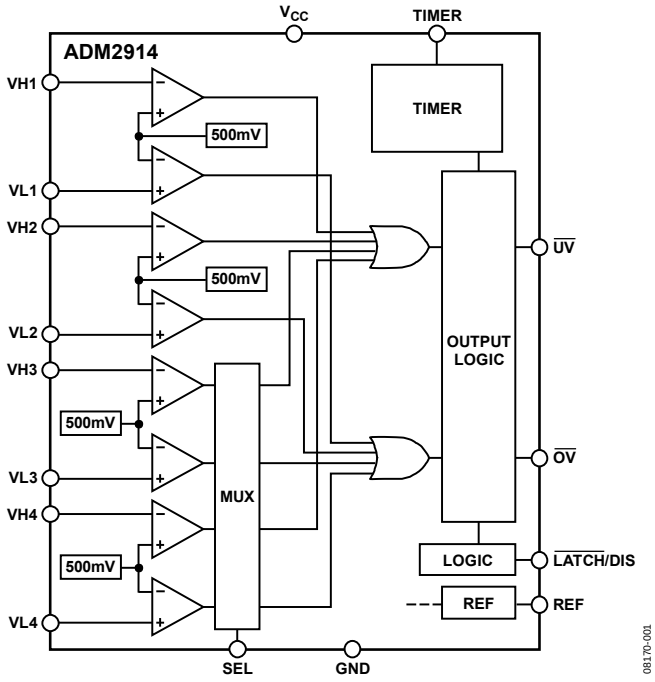



*Figure 1.*

## GENERAL DESCRIPTION

The ADM2914 is a quad voltage supervisory IC ideally suited for monitoring multiple rails in a wide range of applications.

Each monitored rail has two dedicated input pins, VHx and VLx, which allows each rail to be monitored for both overvoltage (OV) and undervoltage (UV) conditions. A common active low undervoltage ($\overline{UV}$) and overvoltage ($\overline{OV}$) pin is shared by each of the monitored voltage rails.

The ADM2914 includes a 1 V buffered reference output, REF, that acts as an offset when monitoring a negative voltage. The three-state SEL pin determines the polarity of the third and fourth inputs, that is, it configures the device to monitor positive or negative supplies.

The device incorporates an internal shunt regulator that enables the device to be used in higher voltage systems. This feature requires a resistor to be placed between the main supply rail and the $V_{CC}$ pin to limit the current flow into the $V_{CC}$ pin to no greater than 10 mA. The ADM2914 uses the internal shunt regulator to regulate $V_{CC}$ if the supply line exceeds the absolute maximum ratings.

The ADM2914 is available in two models. The ADM2914-1 offers a latching overvoltage output that can be cleared by toggling the $\overline{LATCH}$ input pin. The ADM2914-2 has a disable pin that can override and disable both the $\overline{OV}$ and $\overline{UV}$ output signals.

The ADM2914 is available in a 16-lead QSOP package. The device operates over the extended temperature range of −40°C to +125°C.

**Rev. B**
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## REVISION HISTORY

**2/10—Rev. A: Rev. B**
Changes to Figure 17 and Figure 18 ... 9

**12/09—Rev. 0: Rev. A**
Changes to Shunt Regulator Section ... 12

**5/09—Revision 0: Initial Version**

# SPECIFICATIONS

$T_A$ = −40°C to +85°C. Typical values at $T_A$ = 25°C, unless otherwise noted. $V_{CC}$ = 3.3 V, VLx = 0.45 V, VHx = 0.55 V, $\overline{LATCH}$ = $V_{CC}$, SEL = $V_{CC}$, DIS = open, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| SHUNT REGULATOR | | | | | |
| $V_{CC}$ Shunt Regulator Voltage, $V_{SHUNT}$ | 6.2 | 6.6 | 6.9 | V | $I_{CC}$ = 5 mA |
| | 6.2 | 6.6 | 7.0 | V | $T_A$ = −40°C to +125°C |
| $V_{CC}$ Shunt Regulator Load Regulation, $\Delta V_{SHUNT}$ | | 200 | 300 | mV | $I_{CC}$ = 2 mA to 10 mA |
| SUPPLY | | | | | |
| Supply Voltage, $V_{CC}$ [1] | 2.3 | | $V_{SHUNT}$ | V | |
| Minimum $V_{CC}$ Output Valid, $V_{CCR(MIN)}$ | | | 1 | V | DIS = 0 V |
| Supply Undervoltage Lockout, $V_{CC(UVLO)}$ | 1.9 | 2 | 2.1 | V | DIS = 0 V, $V_{CC}$ rising |
| Supply Undervoltage Lockout Hysteresis, $\Delta V_{CC(HYST)}$ | 5 | 25 | 50 | mV | DIS = 0 V |
| Supply Current, $I_{CC}$ | | 62 | 100 | µA | $V_{CC}$ = 2.3 V to 6 V |
| REFERENCE OUTPUT | | | | | |
| Reference Output Voltage, $V_{REF}$ | 0.985 | 1 | 1.015 | V | $I_{VREF}$ = ±1 mA |
| | 0.985 | 1 | 1.020 | V | $T_A$ = −40°C to +125°C |
| UNDERVOLTAGE/OVERVOLTAGE CHARACTERISTICS | | | | | |
| Undervoltage/Overvoltage Threshold, $V_{UOT}$ | 492.5 | 500 | 507.5 | mV | |
| Undervoltage/Overvoltage Threshold to Output Delay, $t_{UOD}$ | 50 | 125 | 500 | µs | VHx = $V_{UOT}$ − 5 mV or VLx = $V_{UOT}$ + 5 mV |
| VHx, VLx Input Current, $I_{VHL}$ | | | ±15 | nA | |
| | | | ±30 | nA | $T_A$ = −40°C to +125°C |
| $\overline{UV}/\overline{OV}$ Timeout Period, $t_{UOTO}$ | 6 | 8.5 | 12.5 | ms | $C_{TIMER}$ = 1 nF |
| | 6 | 8.5 | 14 | ms | $T_A$ = −40°C to +125°C |
| $\overline{OV}$ LATCH CLEAR INPUT (ADM2914-1) | | | | | |
| $\overline{OV}$ Latch Clear Threshold Input High, $V_{\overline{LATCH}(IH)}$ | 1.2 | | | V | |
| $\overline{OV}$ Latch Clear Threshold Input Low, $V_{\overline{LATCH}(IL)}$ | | | 0.8 | V | |
| $\overline{LATCH}$ Input Current, $I_{LATCH}$ | | | ±1 | µA | $V_{\overline{LATCH}}$ > 0.5 V |
| DISABLE INPUT (ADM2914-2) | | | | | |
| DIS Input High, $V_{DIS(IH)}$ | 1.2 | | | V | |
| DIS Input Low, $V_{DIS(IL)}$ | | | 0.8 | V | |
| DIS Input Current, $I_{DIS}$ | 1 | 2 | 3 | µA | $V_{DIS}$ > 0.5 V |
| TIMER CHARACTERISTICS | | | | | |
| TIMER Pull-Up Current, $I_{TIMER(UP)}$ | −1.3 | −2.1 | −2.8 | µA | $V_{TIMER}$ = 0 V |
| | −1.2 | −2.1 | −2.8 | µA | $T_A$ = −40°C to +125°C |
| TIMER Pull-Down Current, $I_{TIMER(DOWN)}$ | 1.3 | 2.1 | 2.8 | µA | $V_{TIMER}$ = 1.6 V |
| | 1.2 | 2.1 | 2.8 | µA | $T_A$ = −40°C to +125°C |
| TIMER Disable Voltage, $V_{TIMER(DIS)}$ | −180 | −270 | | mV | Referenced to $V_{CC}$ |
| OUTPUT VOLTAGE | | | | | |
| Output Voltage High, $\overline{UV}/\overline{OV}$, $V_{OH}$ | 1 | | | V | $V_{CC}$ = 2.3 V; $I_{\overline{UV}/\overline{OV}}$ = −1 µA |
| Output Voltage Low, $\overline{UV}/\overline{OV}$, $V_{OL}$ | | 0.1 | 0.3 | V | $V_{CC}$ = 2.3 V; $I_{\overline{UV}/\overline{OV}}$ = 2.5 mA |
| | | 0.01 | 0.15 | V | $V_{CC}$ = 1 V; $I_{\overline{UV}}$ = 100 µA |
| THREE-STATE INPUT SEL | | | | | |
| Low Level Input Voltage, $V_{IL}$ | | | 0.4 | V | |
| High Level Input Voltage, $V_{IH}$ | 1.4 | | | V | |
| Pin Voltage When Left in High-Z State, $V_Z$ | 0.7 | 0.9 | 1.1 | V | $I_{SEL}$ = ±10 µA |
| | 0.6 | 0.9 | 1.2 | V | $T_A$ = −40°C to +125°C |
| SEL High, Low Input Current, $I_{SEL}$ | | | ±25 | µA | |
| Maximum SEL Input Current, $I_{SEL(MAX)}$ | | | ±30 | µA | SEL tied to $V_{CC}$ or GND |

[1] The maximum voltage on the $V_{CC}$ pin is limited by the input current. The $V_{CC}$ pin has an internal 6.5 V shunt regulator and, therefore, a low impedance supply greater than 6 V may exceed the maximum allowed input current. When operating from a higher supply than 6 V, always use a dropper resistor.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| $V_{CC}$ | −0.3 V to +6 V |
| $\overline{UV}$, $\overline{OV}$ | −0.3 V to +16 V |
| TIMER | −0.3 V to ($V_{CC}$ + 0.3 V) |
| VLx, VHx, $\overline{LATCH}$, DIS, SEL | −0.3 V to +7.5 V |
| $I_{CC}$ | 10 mA |
| Reference Load Current ($I_{REF}$) | ±1 mA |
| $I_{\overline{UV}}$, $I_{\overline{OV}}$ | 10 mA |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 16-Lead QSOP | 104 | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

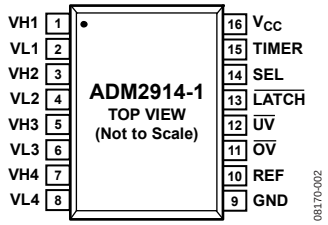



*Figure 2. ADM2914-1 Pin Configuration*

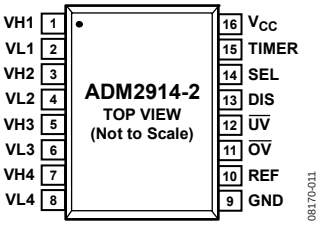



*Figure 3. ADM2914-2 Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic ADM2914-1 | Mnemonic ADM2914-2 | Description |
|---|---|---|---|
| 1 | VH1 | VH1 | Voltage High Input 1 and Voltage High Input 2. If the voltage monitored by VH1 or VH2 drops below 0.5 V, an undervoltage condition is detected. Connect to $V_{CC}$ when not in use. |
| 3 | VH2 | VH2 | |
| 2 | VL1 | VL1 | Voltage Low Input 1 and Voltage Low Input 2. If the voltage monitored by VL1 or VL2 rises above 0.5 V, an overvoltage condition is detected. Tie to GND when not in use. |
| 4 | VL2 | VL2 | |
| 5 | VH3 | VH3 | Voltage High Input 3 and Voltage High Input 4. The polarity of these inputs is determined by the state of the SEL pin (see Table 5). When the monitored input is configured as a positive voltage and the voltage monitored by VH3 or VH4 drops below 0.5 V, an undervoltage condition is detected. Conversely, when the input is configured as a negative voltage and the input drops below 0.5 V, an overvoltage condition is detected. Connect to $V_{CC}$ when not in use. |
| 7 | VH4 | VH4 | |
| 6 | VL3 | VL3 | Voltage Low Input 3 and Voltage Low Input 4. The polarity of these inputs is determined by the state of the SEL pin (see Table 5). When the monitored input is configured as a positive voltage and the voltage monitored by VL3 or VL4 rises above 0.5 V, an overvoltage condition is detected. Conversely, when the input is configured as a negative voltage and the input rises above 0.5 V, an undervoltage condition is detected. Tie to GND when not in use. |
| 8 | VL4 | VL4 | |
| 9 | GND | GND | Device Ground. |
| 10 | REF | REF | Buffered Reference Output. This pin is a 1 V reference that is used as an offset when monitoring negative voltages. This pin can source or sink 1 mA, and drive loads up to 1 nF. Larger capacitive loads may lead to instability. Leave unconnected when not in use. |
| 11 | $\overline{OV}$ | $\overline{OV}$ | Overvoltage Reset Output. $\overline{OV}$ is asserted low if a negative polarity input voltage drops below its associated threshold or if a positive polarity input voltage exceeds its threshold. The ADM2914-1 allows $\overline{OV}$ to be latched low. The ADM2914-2 holds $\overline{OV}$ low for an adjustable timeout period determined by the TIMER capacitor. This pin has a weak pull-up to VCC and can be pulled up to 16 V externally. Leave this pin unconnected when not in use. |
| 12 | $\overline{UV}$ | $\overline{UV}$ | Undervoltage Reset Output. $\overline{UV}$ is asserted low if a negative polarity input voltage exceeds its associated threshold or if a positive polarity input voltage drops below its threshold. $\overline{UV}$ is held low for an adjustable timeout period set by the external capacitor tied to the TIMER pin. The $\overline{UV}$ pin has a weak pull-up to $V_{CC}$ and can be pulled up to 16 V externally via an external pull-up resistor. Leave this pin unconnected when not in use. |
| 13 | $\overline{LATCH}$ | | $\overline{OV}$ Latch Bypass Input/Clear Pin. When pulled high, the $\overline{OV}$ latch is cleared. When held high, the $\overline{OV}$output has the same delay and output characteristics as the $\overline{UV}$ output. When pulled low, the $\overline{OV}$ output is latched when asserted. (Applies only to the ADM2914-1.) |
| | | DIS | $\overline{OV}$ and $\overline{UV}$ Disable Input. When pulled high, the $\overline{OV}$ and $\overline{UV}$ outputs are held high irrespective of the state of the VHx and VLx input pins. However, if a UVLO condition occurs, the $\overline{OV}$ and $\overline{UV}$ outputs are asserted. This pin has a weak internal pull-down (2 µA) to GND. Leave this pin unconnected when not in use. (Applies only to the ADM2914-2.) |
| 14 | SEL | SEL | Input Polarity Select. This three-state input pin allows the polarity of VH3, VL3, VH4, and VL4 to be configured. Connect to $V_{CC}$ or GND, or leave open to select one of three possible input polarity configurations (see Table 5). |
| 15 | TIMER | TIMER | Adjustable Reset Delay Timer. Connect an external capacitor to the TIMER pin to program the reset timeout delay. Refer to Figure 15 in the Typical Performance Characteristics section. Connect this pin to $V_{CC}$ to bypass the timer. |
| 16 | $V_{CC}$ | $V_{CC}$ | Supply Voltage. $V_{CC}$ operates as a direct supply for voltages up to 6 V. For voltages greater than 6 V, it operates as a shunt regulator. A dropper resistor must be used in this configuration to limit the current to less than 10 mA. When used without the resistor, the voltage at this pin must not exceed 6 V. A 0.1 µF bypass capacitor or greater should be used. |

# TYPICAL PERFORMANCE CHARACTERISTICS

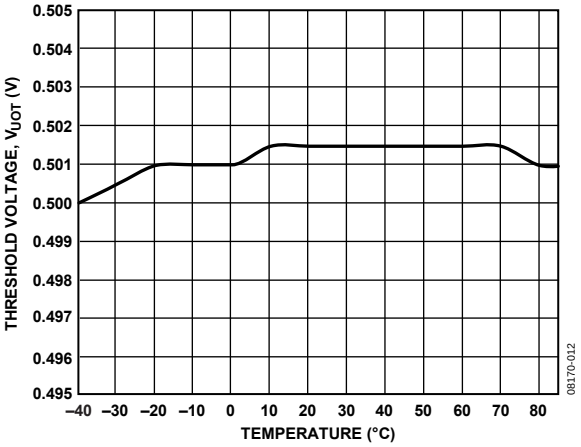



*Figure 4. Input Threshold Voltage vs. Temperature*

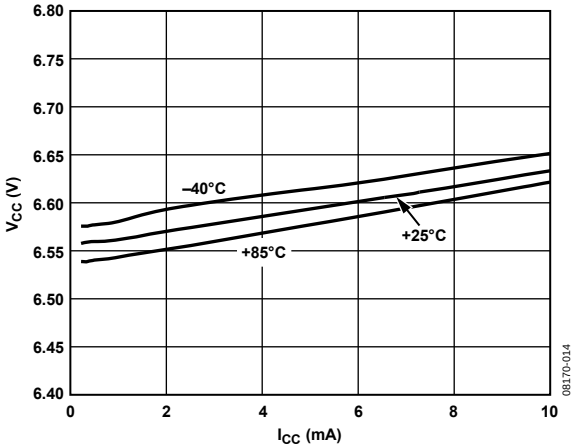



*Figure 7. $V_{CC}$ Shunt Voltage vs. $I_{CC}$*

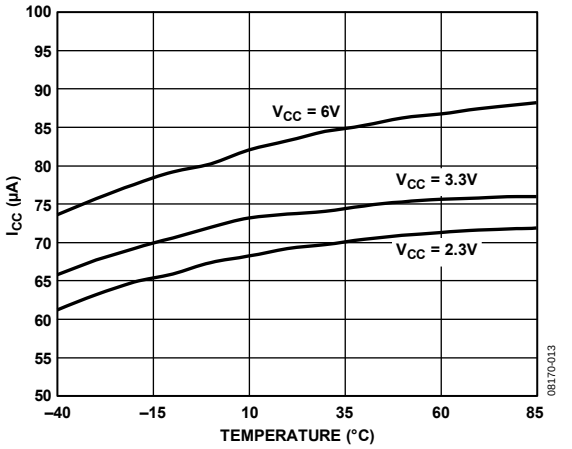



*Figure 5. Supply Current vs. Temperature*

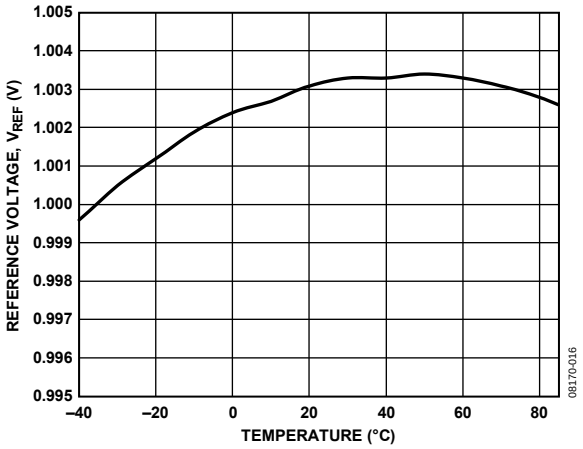



*Figure 8. Buffered Reference Voltage vs. Temperature*

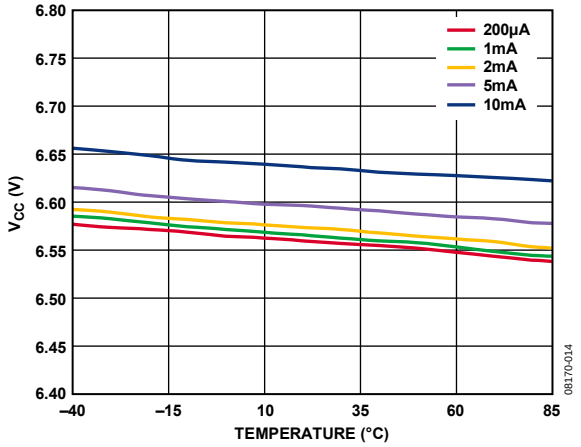



*Figure 6. $V_{CC}$ Shunt Voltage vs. Temperature*

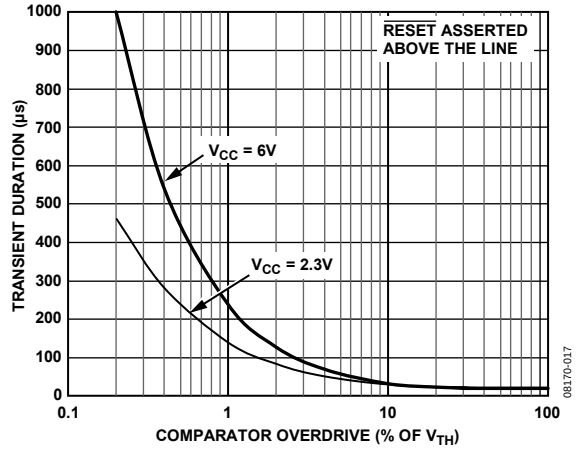



*Figure 9. Transient Duration vs. Comparator Overdrive*

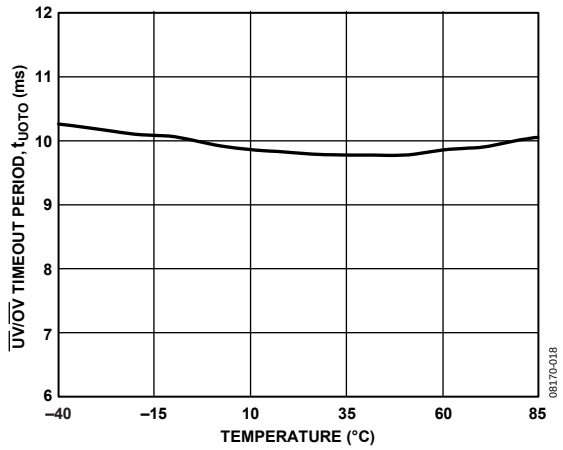



Figure 10. $\overline{UV}/\overline{OV}$ Timeout Period vs. Temperature

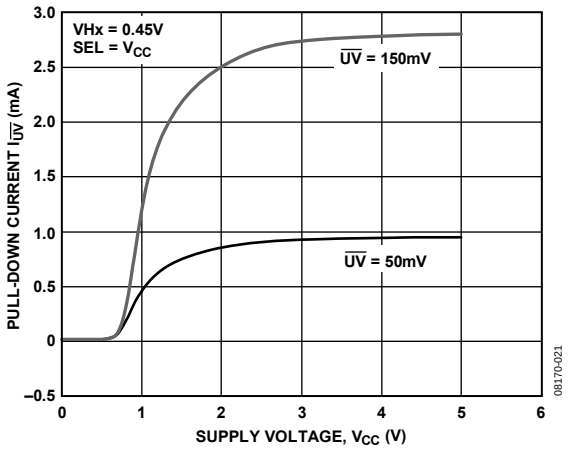



Figure 13. $I_{SINK}$, $I_{\overline{UV}}$ vs. $V_{CC}$

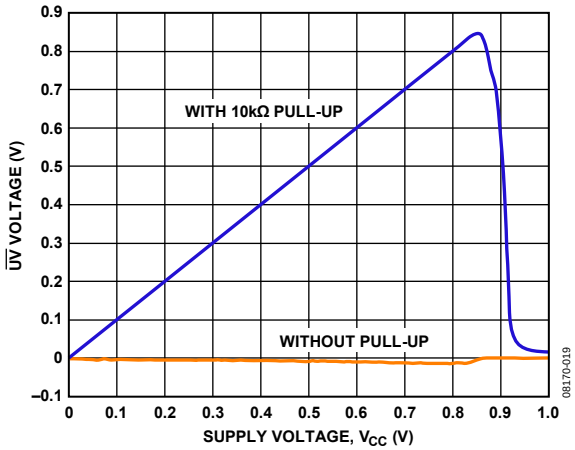



Figure 11. $\overline{UV}$ Output Voltage vs. $V_{CC}$

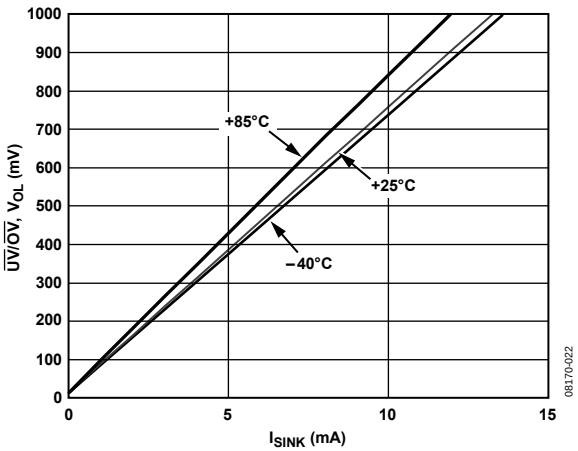



Figure 14. $\overline{UV}/\overline{OV}$ Voltage Output Low vs. Output Sink Current

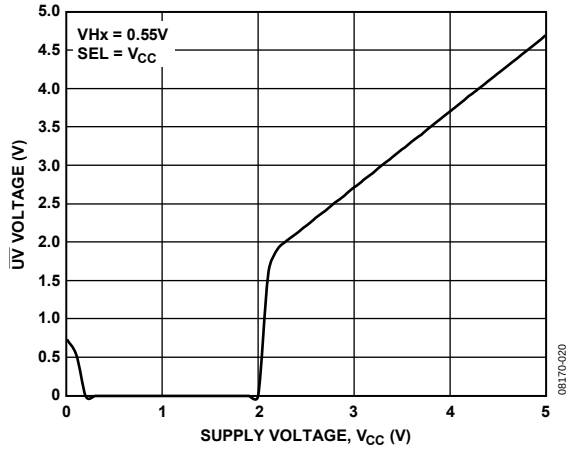



Figure 12. $\overline{UV}$ Output Voltage vs. $V_{CC}$

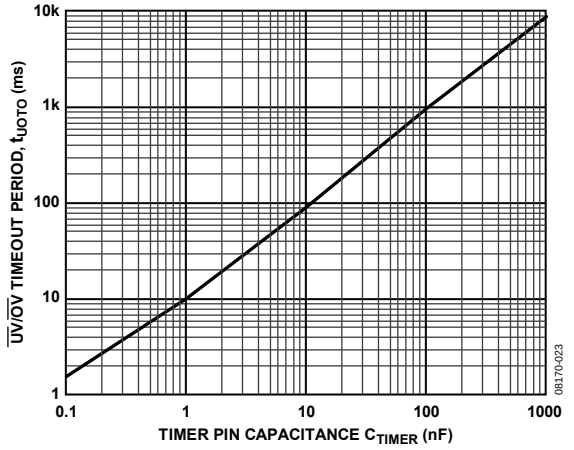



Figure 15. $\overline{UV}/\overline{OV}$ Timeout Period vs. Capacitance

# THEORY OF OPERATION

## VOLTAGE SUPERVISION

The ADM2914 supervises up to four voltage rails for overvoltage and undervoltage conditions. Two pins, VHx and VLx, are assigned to monitor each rail, one for overvoltage detection and the other for undervoltage detection. Each pin is connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 0.5 V voltage reference with accuracy of ±1.5%.

The output of each of the internal undervoltage comparators is tied to a common $\overline{UV}$ output pin. Likewise, the outputs of the internal overvoltage comparators are tied to a common $\overline{OV}$ output pin.

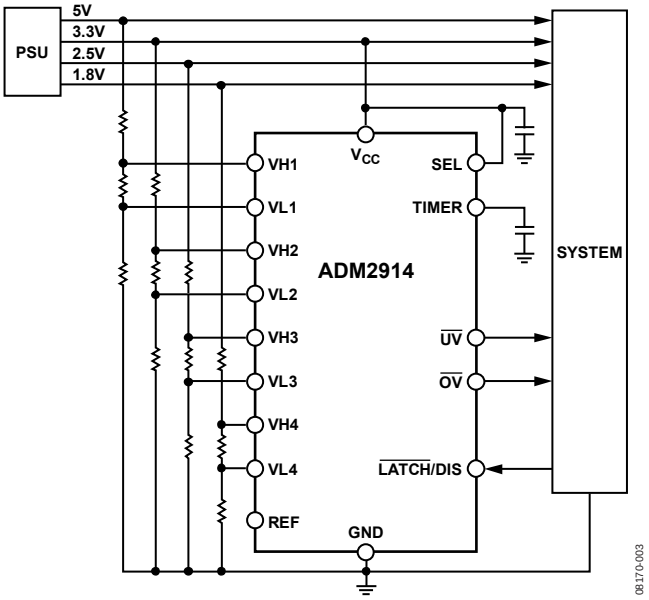



*Figure 16. Typical Applications Diagram*

## POLARITY CONFIGURATION

The ADM2914 is capable of monitoring supply voltages of both positive and negative polarities. The SEL pin is a three-state pin that determines the polarity of Input 3 and Input 4. As summarized in Table 5, the SEL pin is either connected to GND, $V_{CC}$, or left unconnected.

When an input is configured to monitor a positive voltage, using the three-resistor scheme shown in Figure 17, VHx is connected to the high-side tap of the resistor divider and VLx is connected to the low-side tap of the resistor divider.

Conversely, when an input is configured to monitor a negative voltage, UVx and OVx are swapped internally. The negative voltage for monitoring is then connected as shown in Figure 18. VHx is still connected to the high-side tap and VLx is still connected to the low-side tap. Within this configuration, an undervoltage condition occurs when the monitored voltage is less negative than the programmed threshold, and an overvoltage condition occurs when the monitored voltage is more negative than the configured threshold.

**Table 5. Polarity Configuration**

| | Input 3 | | | Input 4 | | |
|---|---|---|---|---|---|---|
| **SEL Pin** | **Polarity** | **UV Condition** | **OV Condition** | **Polarity** | **UV Condition** | **OV Condition** |
| Connected to $V_{CC}$ | Positive | VH3 < 0.5 V | VL3 > 0.5 V | Positive | VH4 < 0.5 V | VL4 > 0.5 V |
| Left Unconnected | Positive | VH3 < 0.5 V | VL3 > 0.5 V | Negative | VL4 > 0.5 V | VH4 < 0.5 V |
| Connected to GND | Negative | VL3 > 0.5 V | VH3 < 0.5 V | Negative | VL4 > 0.5 V | VH4 < 0.5 V |

## MONITORING PIN CONNECTIONS

### *Positive Voltage Monitoring Scheme*

When monitoring a positive supply, the desired nominal operating voltage for monitoring is denoted by $V_M$, $I_M$ is the nominal current through the resistor divider, $V_{OV}$ is the overvoltage trip point, and $V_{UV}$ is the undervoltage trip point.

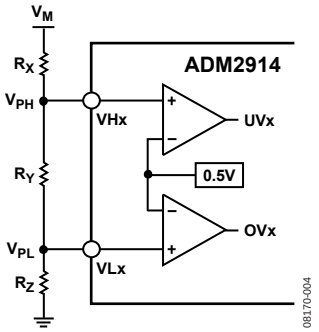



*Figure 17. Positive Undervoltage/Overvoltage Monitoring Configuration*

Figure 17 illustrates the positive voltage monitoring input connection. Three external resistors, $R_X$, $R_Y$, and $R_Z$, divide the positive voltage for monitoring, $V_M$, into high-side voltage, $V_{PH}$, and low-side voltage, $V_{PL}$. The high-side voltage is connected to the corresponding VHx pin, and the low-side voltage is connected to the corresponding VLx pin.

To trigger an overvoltage condition, the low-side voltage (in this case, $V_{PL}$) must exceed the 0.5 V threshold on the VLx pin. The low-side voltage, $V_{PL}$, is given by the following equation:

$$V_{PL} = V_{OV}\left(\frac{R_Z}{R_X + R_Y + R_Z}\right) = 0.5 \text{ V}$$

Also,

$$R_X + R_Y + R_Z = \frac{V_M}{I_M}$$

Therefore, $R_Z$, which sets the desired trip point for the overvoltage monitor, is calculated using the following equation:

$$R_Z = \frac{(0.5)(V_M)}{(V_{OV})(I_M)} \quad (1)$$

To trigger the undervoltage condition, the high-side voltage, $V_{PH}$, must exceed the 0.5 V threshold on the VHx pin. The high-side voltage, $V_{PH}$, is given by the following equation:

$$V_{PH} = V_{UV}\left(\frac{R_Y + R_Z}{R_X + R_Y + R_Z}\right) = 0.5 \text{ V}$$

Because $R_Z$ is already known, $R_Y$ can be expressed as follows:

$$R_Y = \frac{(0.5)(V_M)}{(V_{UV})(I_M)} - R_Z \quad (2)$$

When $R_Y$ and $R_Z$ are known, $R_X$ is calculated using the following equation:

$$R_X = \frac{(V_M)}{(I_M)} - R_Z - R_Y \quad (3)$$

If $V_M$, $I_M$, $V_{OV}$, or $V_{UV}$ changes, each step must be recalculated.

### *Negative Voltage Monitoring Scheme*

Figure 18 shows the circuit configuration for negative supply voltage monitoring. To monitor the negative voltage, a 1 V reference voltage is required to connect to the end node of the voltage divider circuit. This reference voltage is generated internally and is output through the REF pin.

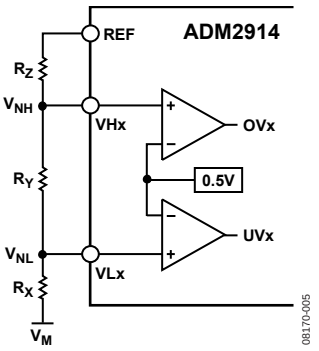



*Figure 18. Negative Undervoltage/Overvoltage Monitoring Configuration*

The equations described in the Positive Voltage Monitoring Scheme section need some minor modifications for use with negative voltage monitoring. The 1 V reference voltage is added to the overall voltage drop; it must therefore be subtracted from $V_M$, $V_{UV}$, and $V_{OV}$ before using each in the previous equations.

To monitor a negative voltage level, the resistor divider circuit divides the voltage differential level between the 1 V reference voltage and the negative supply voltage into high-side voltage, $V_{NH}$, and low-side voltage, $V_{NL}$. Similar to the positive voltage monitoring scheme, the high-side voltage, $V_{NH}$, is connected to the corresponding $VH_X$ pin, and the low-side voltage, $V_{NL}$, is connected to the corresponding $VL_X$ pin. Refer to the Voltage Monitoring Example section for more information.

## THRESHOLD ACCURACY

The reset threshold accuracy is fundamental, especially at lower voltage levels. Consider an FPGA application that requires a 1 V core voltage input with tolerance of ±5%, where the supply has a specified regulation, for example, ±1.5%. As shown in Figure 19, to ensure that the supply is within the FPGA input voltage requirement range, its voltage level must be monitored for UV and OV conditions. The voltage swing on the supply itself causes the voltage band available for setting the monitoring threshold to be quite narrow. In this example, the threshold voltages, including the tolerances, must fit within a monitor region of only 0.035 V. The ADM2914 device with 0.1% resistors can achieve this level of accuracy.

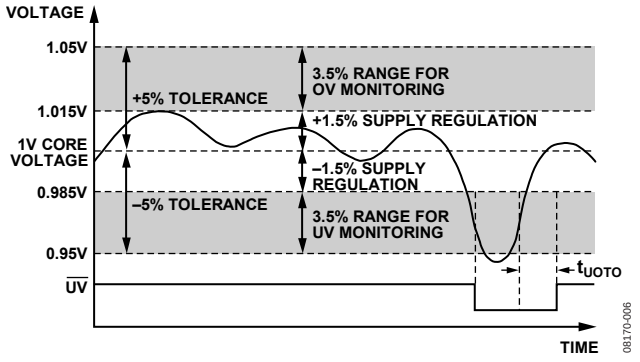



*Figure 19. Monitoring Threshold Accuracy Example*

## VOLTAGE MONITORING EXAMPLE

To illustrate how the ADM2914 device works in a real application, consider the 1 V input example shown in Figure 19, with the addition of a −12 V rail.

The first step is to choose the nominal current flow through both voltage divider circuits, for example, 5 μA.

For the 1 V ± 5% input, due to the specified ±1.5% regulation of the supply, the UV and OV thresholds should be set in the middle of the voltage monitoring band. In this case, on the ±3.25% points of the supply, the UV threshold is 0.9675 V and the OV threshold is 1.0325 V.

Input these values into Equation 1.

$$R_Z = \frac{(0.5)(1)}{(1.0325)(5\times10^{-6})} \approx 96.5\ \text{k}\Omega$$

Insert the value of $R_Z$ into Equation 2.

$$R_Y = \frac{(0.5)(1)}{(0.9675)(5\times10^{-6})} - 96.5\ \text{k}\Omega \approx 6.42\ \text{k}\Omega$$

Then substitute the calculated values for $R_Z$ and $R_Y$ into Equation 3.

$$R_X = \frac{1}{5\times10^{-6}} - 96.5\ \text{k}\Omega - 6.42\ \text{k}\Omega \approx 96.5\ \text{k}\Omega$$

This design approach meets the application specifications. As described previously, the 1 V rail is specified with an input requirement of ±5% and a supply tolerance of ±1.5%. This effectively means that the OV threshold of the monitoring device, including all the tolerance factors, must fit within the 1.015 V to 1.05 V range. Similarly, the UV threshold range must be between 0.95 V and 0.985 V.

The four worst-case scenarios of minimum and maximum undervoltage and overvoltage thresholds are calculated as follows:

Minimum overvoltage threshold

$$V_{OV_MIN} = (0.5\ \text{V} - 1.5\%)\left(1 + \frac{(R_X - 0.1\%) + (R_Y - 0.1\%)}{(R_Z + 0.1\%)}\right)$$

$$= 0.4925\left(1 + \frac{(96{,}500 + 6420)(0.999)}{(96{,}500)(1.001)}\right)$$

$$= 1.016\ \text{V} > 1.015\ \text{V}$$

Maximum overvoltage threshold

$$V_{OV_MAX} = (0.5\ \text{V} + 1.5\%)\left(1 + \frac{(R_X + 0.1\%) + (R_Y + 0.1\%)}{(R_Z - 0.1\%)}\right)$$

$$= 1.049\ \text{V} < 1.05\ \text{V}$$

The maximum and minimum overvoltage threshold values lie within the 1.015 V to 1.05 V range specified. The minimum and maximum undervoltage thresholds are calculated as follows:

Minimum undervoltage threshold

$$V_{UV_MIN} = (0.5\ \text{V} - 1.5\%)\left(1 + \frac{(R_X - 0.1\%)}{(R_Y + 0.1\%) + (R_Z + 0.1\%)}\right)$$

$$= 0.953\ \text{V} > 0.95\ \text{V}$$

Maximum undervoltage threshold

$$V_{UV_MAX} = (0.5\ \text{V} + 1.5\%)\left(1 + \frac{(R_X + 0.1\%)}{(R_Y - 0.1\%) + (R_Z - 0.1\%)}\right)$$

$$= 0.984\ \text{V} < 0.985\ \text{V}$$

Again, these values fit within the specified undervoltage monitoring range. All four worst-case scenarios satisfy the tolerance requirement; therefore, the design approach is valid.

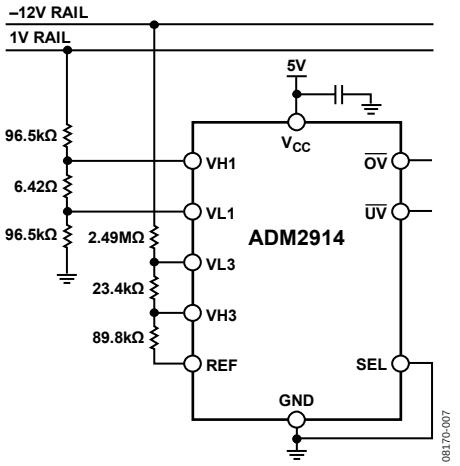



*Figure 20. Positive and Negative Supply Monitor Example*

Next, consider a −12 V input, which is specified with a ±20% input. The threshold accuracy required by the supply is chosen to be within ±5% of the −12 V rail. Therefore, the overvoltage threshold is set to −13.5 V, and the undervoltage threshold is −10.5 V. The negative voltage scheme configuration requires that the 1 V reference voltage be accounted for in Equation 1 to Equation 3. The 1 V reference voltage is subtracted from $V_M$, $V_{UV}$, and $V_{OV}$, and the absolute value of the result is taken.

Equation 1 becomes

$$R_Z = \frac{(0.5)(|-12-1|)}{(|-13.5-1|)(5\times10^{-6})} \approx 89.8\ \text{k}\Omega$$

Insert the value of $R_Z$ into Equation 2.

$$R_Y = \frac{(0.5)(|-12-1|)}{(|-10.5-1|)(5\times10^{-6})} - 89.8\ \text{k}\Omega \approx 23.4\ \text{k}\Omega$$

To calculate $R_X$, insert the value of $R_Z$ and $R_Y$ into Equation 3.

$$R_X = \frac{(|-12-1|)}{5\times10^{-6}} - (89.8\ \text{k}\Omega) - (23.4\ \text{k}\Omega) \approx 2.49\ \text{M}\Omega$$

## POWER-UP AND POWER-DOWN

On power-up, when $V_{CC}$ reaches 1 V, the active low $\overline{UV}$ output is asserted, and the $\overline{OV}$ output pulls up to $V_{CC}$. When the voltage on the $V_{CC}$ pin reaches 1 V, the ADM2914 is guaranteed to assert $\overline{UV}$ low and $\overline{OV}$ high. When $V_{CC}$ exceeds 1.9 V (minimum), the VHx and VLx inputs take control. When $V_{CC}$ and each of the VHx inputs are valid, an internal timer begins. Subsequent to an adjustable time delay, $\overline{UV}$ weakly pulls high.

## $\overline{UV}$/$\overline{OV}$ TIMING CHARACTERISTICS

$\overline{UV}$ is an active low output. It is asserted when any of the four monitored voltages is below its associated threshold. When the voltage on the $V_{CC}$ pin is above 2 V, an internal timer holds $\overline{UV}$ low for an adjustable period, $t_{UOTO}$, after the voltage on all the monitoring rails rises above their thresholds. This allows time for all monitored power supplies to stabilize after power-up. Similarly, any monitored voltage that falls below its threshold initiates a timer reset, and the timer starts again when all the monitoring rails rise above their thresholds.

The $\overline{UV}$ and $\overline{OV}$ outputs are held asserted after all faults have cleared for an adjustable timeout period, determined by the value of the external capacitor attached to the TIMER pin.

## TIMER CAPACITOR SELECTION

The $\overline{UV}$ and $\overline{OV}$ timeout period on the ADM2914 is programmable via the external timer capacitor, $C_{TIMER}$, placed between the TIMER pin and ground. The timeout period, $t_{UOTO}$, is calculated using the following equation:

$$C_{TIMER} = (t_{UOTO})(115)(10^{-9})\ \text{F/sec}$$

Refer to Figure 15 in the Typical Performance Characteristics section, which illustrates the delay time as a function of the timer capacitor value. A minimum capacitor value of 10 pF is required. The chosen timer capacitor must have a leakage current that is less than the 1.3 µA TIMER pin charging current. To bypass the timeout period, connect the TIMER pin to $V_{CC}$.

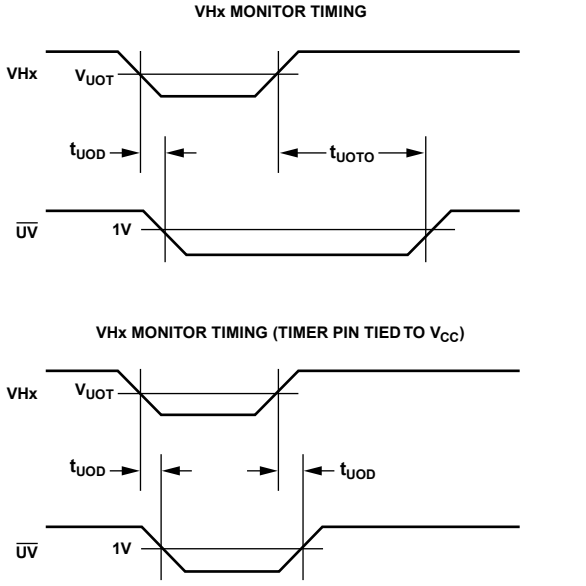



*Figure 21. VHx Positive Voltage Monitoring Timing Diagram*

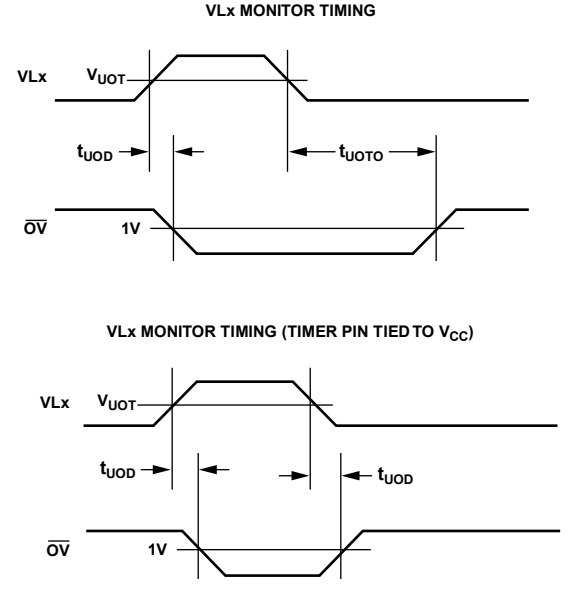



*Figure 22. VLx Positive Voltage Monitoring Timing Diagram*

## $\overline{UV}$ AND $\overline{OV}$ RISE AND FALL TIMES

The $\overline{UV}$ and $\overline{OV}$ output rise times (from 10% to 90%) can be approximated using the following formula:

$$t_R \approx 2.2(R_{PULL-UP})(C_{LOAD})$$

where:
$R_{PULL-UP}$ is the internal weak pull-up resistance with an approximate value of 400 kΩ at room temperature with $V_{CC}$ > 1 V.
$C_{LOAD}$ is the external load capacitance on the output pin.

When a fault occurs, the $\overline{UV}$ or $\overline{OV}$ output fall time can be expressed as

$$t_F \approx 2.2(R_{PULL-DOWN})(C_{LOAD})$$

where $R_{PULL-DOWN}$ is the internal pull-down resistance, which is approximately 50 Ω. Assuming a load capacitance of 150 pF, the fall time is 16.5 ns.

## $\overline{UV}$/$\overline{OV}$ OUTPUT CHARACTERISTICS

Both the $\overline{OV}$ and $\overline{UV}$ outputs have a strong pull-down to ground and a weak internal pull-up to $V_{CC}$. This permits the pins to behave as open-drain outputs. When the rise time on the pin is not critical, the weak pull-up removes the requirement for an external pull-up resistor. The open-drain configuration allows for wire-OR'ing of outputs, which is particularly useful when more than one signal needs to pull down on the output.

At $V_{CC}$ = 1 V, a maximum $V_{OL}$ = 0.15 V at $\overline{UV}$ is guaranteed. At $V_{CC}$ = 1 V, the weak pull-up current on $\overline{OV}$ is almost turned on. Consequently, if the state and pull-up strength of the $\overline{OV}$ pin are important at very low $V_{CC}$, an external pull-up resistor of no more than 100 kΩ is advised. By adding an external pull-up resistor, the pull-up strength on the $\overline{OV}$ pin is greater. Therefore, if it is connected in a wire-OR'ed configuration, the pull-down strength of any single device must account for this additional pull-up strength.

## GLITCH IMMUNITY

The ADM2914 is immune to short transients that may occur on the monitored voltage rails. The device contains internal filtering circuitry that provides immunity to fast transient glitches. Figure 9 illustrates glitch immunity performance by showing the maximum transient duration without causing a reset pulse. Glitch immunity makes the ADM2914 suitable for use in noisy environments.

## UNDERVOLTAGE LOCKOUT (UVLO)

The ADM2914 has an undervoltage lockout circuit that monitors the voltage on the $V_{CC}$ pin. When the voltage on $V_{CC}$ drops below 1.9 V (minimum), the circuit is activated. The $\overline{UV}$ output is asserted and the $\overline{OV}$ output is cleared and not allowed to assert. When $V_{CC}$ recovers, $\overline{UV}$ exhibits the same timing characteristics as if an undervoltage condition had occurred on the inputs.

## SHUNT REGULATOR

The ADM2914 is powered via the $V_{CC}$ pin. The $V_{CC}$ pin can be directly connected to a voltage rail of up to 6 V. In this mode, the supply current of the device does not exceed 100 µA. An internal shunt regulator allows the ADM2914 to operate at voltage levels greater than 6 V by simply placing a dropper resistor in series between the supply rail and the $V_{CC}$ pin to limit the input current to less than 10 mA.

Once the supply voltage, $V_{IN}$, has been established, an appropriate value for the dropper resistor can be calculated. Begin by determining the maximum supply current required, $I_{CCtotal}$, by adding the current drawn from the reference and/or the pull resistors between the outputs and the $V_{CC}$ pin to the maximum specified supply current. The minimum and maximum shunt regulator voltage specified in Table 1, $V_{SHUNT\,min}$ and $V_{SHUNT\,max}$, are also required in the following calculations.

Calculate the maximum and minimum dropper resistor values

$$R_{MAX} = \frac{V_{IN\,\min} - V_{SHUNT\,\max}}{I_{CCtotal}}$$

$$R_{MIN} = \frac{V_{IN\,\max} - V_{SHUNT\,\min}}{100\mu}$$

Based on these values, choose a real-world resistor value within this range. Then, given the specified accuracy of this resistor, calculate the minimum and maximum real resistor value variation, $R_{REALmin}$ and $R_{REALmax}$, respectively.

The maximum device power is calculated as follows:

$$P_{DeviceMax} = V_{SHUNTmax}\left[\frac{\left(V_{IN\,\max} - V_{SHUNTmax}\right)}{R_{REAL\,\min}} - Icc_{TOTAL}\right] + V_{SHUNTmax} I_{CCtotal}$$

To check that the calculated value of the resistor will be acceptable, calculate the maximum device temperature rise;

$$Temp_{RISEmax} = \theta_{JA} P_{DeviceMax}$$

Add this value to the ambient operating temperature. If the resistor value is acceptable, the result will lie within the specified operating temperature range of the device, –40°C to +85°C.

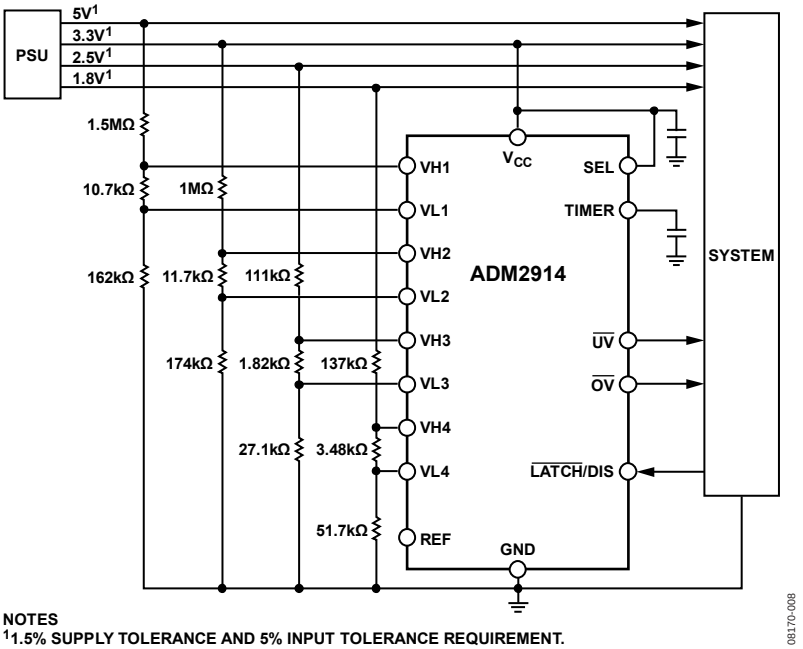
### $\overline{\text{OV}}$ LATCH (ADM2914-1)

If an overvoltage condition occurs when the $\overline{\text{LATCH}}$ pin is pulled low, the $\overline{\text{OV}}$ pin latches low. Pulling $\overline{\text{LATCH}}$ high clears the latch. If an $\overline{\text{OV}}$ condition clears while $\overline{\text{LATCH}}$ is high, the latch is bypassed and the $\overline{\text{OV}}$ pin behaves in the same way as the $\overline{\text{UV}}$ pin, with an identical timeout period. If the $\overline{\text{LATCH}}$ pin is pulled low while the timeout period is active, the $\overline{\text{OV}}$ pin latches low, as in normal operation.

### DISABLE (ADM2914-2)

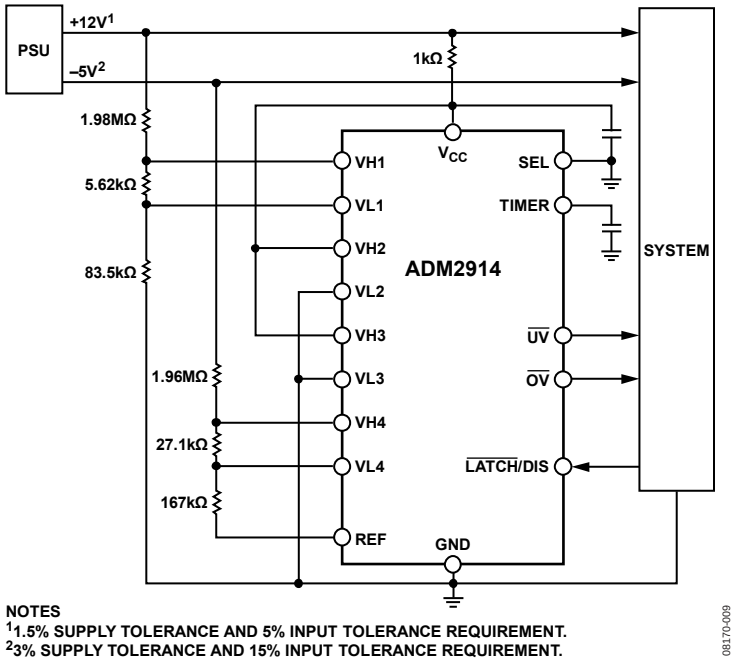
Pulling the DIS pin high disables both the $\overline{\text{UV}}$ and $\overline{\text{OV}}$ outputs, and forces both outputs to remain weakly pulled high, regardless of any faults that are detected at the inputs. If a UVLO condition is detected, the $\overline{\text{UV}}$ output is asserted and pulls low; however, the timeout function is bypassed. As soon as the UVLO condition clears, the $\overline{\text{UV}}$ output pulls high. To guarantee normal operation when the pin is left unconnected, DIS has a weak 2 µA internal pull-down current.

# TYPICAL APPLICATIONS



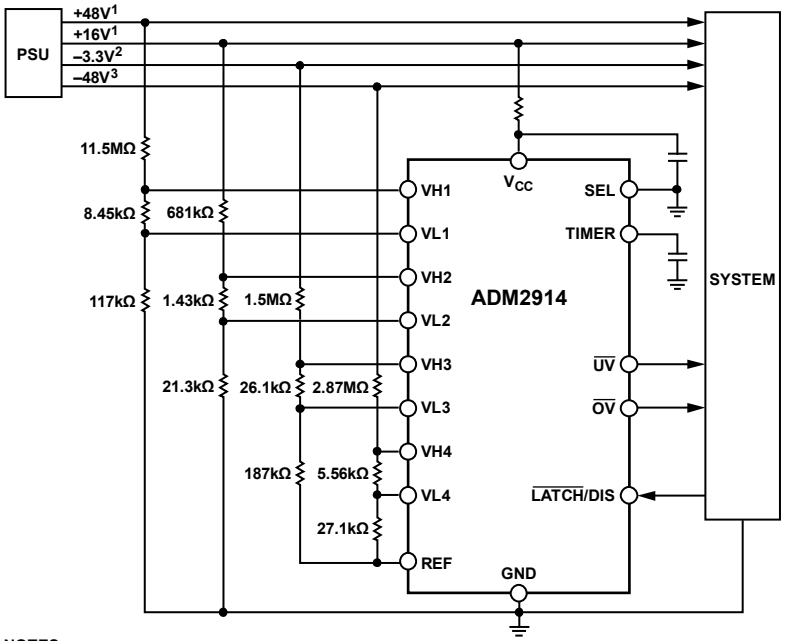

NOTES
[1]1.5% SUPPLY TOLERANCE AND 5% INPUT TOLERANCE REQUIREMENT.

*Figure 23. Typical Application Diagram for Monitoring 5 V, 3.3 V, 2.5 V, and 1.8 V*




NOTES
[1]1.5% SUPPLY TOLERANCE AND 5% INPUT TOLERANCE REQUIREMENT.
[2]3% SUPPLY TOLERANCE AND 15% INPUT TOLERANCE REQUIREMENT.

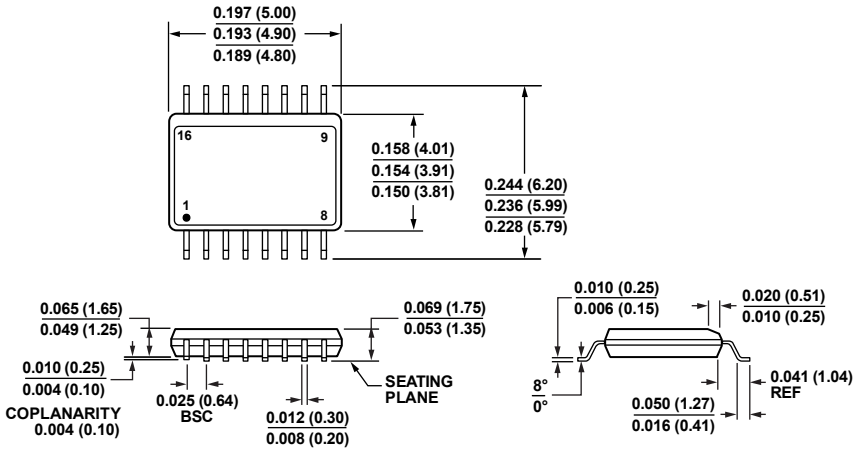
*Figure 24. Typical Application Diagram for Monitoring +12 V and −5 V*




NOTES
[1]1.5% SUPPLY TOLERANCE AND 10% INPUT TOLERANCE REQUIREMENT.
[2]2% SUPPLY TOLERANCE AND 15% INPUT TOLERANCE REQUIREMENT.
[3]4% SUPPLY TOLERANCE AND 15% INPUT TOLERANCE REQUIREMENT.

*Figure 25. Typical Application Diagram for Monitoring +48 V, +16 V, −3.3 V, and −48 V*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012808-A

*Figure 26. 16-Lead Shrink Small Outline Package [QSOP]*
*(RQ-16)*
*Dimensions shown in inches and (millimeters)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADM2914-1ARQZ | −40°C to +125°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 |
| ADM2914-1ARQZ-RL7 | −40°C to +125°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 |
| ADM2914-2ARQZ | −40°C to +125°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 |
| ADM2914-2ARQZ-RL7 | −40°C to +125°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 |
| EVAL-ADM2914EBZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

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D08170-0-2/10(B)