High Speed, Isolated RS-485 Transceiver with Integrated Transformer Driver

ADM2485

FEATURES

- Half-duplex, isolated RS-485 transceiver
- Integrated oscillator driver for external transformer
- PROFIBUS® compliant
- Complies with ANSI/TIA/EIA RS-485-A-98 and ISO 8482:1987(E)
- Data rate: 16 Mbps
- 5 V or 3.3 V operation (V_{DD1})
- 50 nodes on bus
- High common-mode transient immunity: >25 kV/µs
- Isolated DE OUT status output
- Thermal shutdown protection
- Safety and regulatory approvals
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - VDE Certificate of Conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - Reinforced insulation, V_{IORM} = 560 V peak
- Operating temperature range: –40°C to +85°C
- Wide-body, 16-lead SOIC package

APPLICATIONS

- Isolated RS-485/RS-422 interfaces
- PROFIBUS networks
- Industrial field networks
- Multipoint data transmission systems

FUNCTIONAL BLOCK DIAGRAM

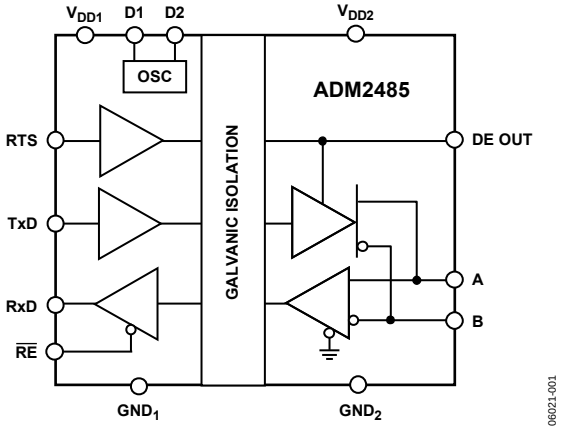


Figure 1.

GENERAL DESCRIPTION

The ADM2485 differential bus transceiver is an integrated, galvanically isolated component designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and complies with ANSI/TIA/EIA RS-485-A-98 and ISO 8482:1987(E).

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package. An on-chip oscillator outputs a pair of square waveforms that drive an external transformer to provide isolated power with an external transformer. The logic side of the device can be powered with either a 5 V or a 3.3 V supply, and the bus side is powered with an isolated 5 V supply.

The ADM2485 driver has an active high enable. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output port that imposes minimal loading on the bus when the driver is disabled or when V_{DD1} or V_{DD2} = 0 V. Also provided is an active high receiver disable that causes the receive output to enter a high impedance state.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention might cause excessive power dissipation. The part is fully specified over the industrial temperature range and is available in a 16-lead, wide-body SOIC package.

Rev. A
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
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REVISION HISTORY

12/07—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Features Section ... 1
Changes to Table 4 ... 6
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Changes to PCB Section and Figure 34 ... 16
Updated Outline Dimensions ... 17

1/07—Revision 0: Initial Version

SPECIFICATIONS

2.7 V ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Outputs					
Differential Output Voltage, V_{OD}			5	V	R = ∞, see Figure 21
	2.1		5	V	R = 50 Ω (RS-422), see Figure 21
	2.1		5	V	R = 27 Ω (RS-485), see Figure 21
	2.1		5	V	V_{TST} = −7 V to +12 V, V_{DD1} ≥ 4.75 V, see Figure 22
Δ|V_{OD}| for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 21
Common-Mode Output Voltage, V_{OC}			3	V	R = 27 Ω or 50 Ω, see Figure 21
Δ|V_{OC}| for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 21
Output Short-Circuit Current, V_{OUT} = High	60		200	mA	−7 V ≤ V_{OUT} ≤ +12 V
Output Short-Circuit Current, V_{OUT} = Low	60		200	mA	−7 V ≤ V_{OUT} ≤ +12 V
Bus Enable Output					
Output High Voltage	V_{DD2} − 0.1			V	I_{ODE} = 20 μA
	V_{DD2} − 0.3	V_{DD2} − 0.1		V	I_{ODE} = 1.6 mA
	V_{DD2} − 0.4	V_{DD2} − 0.2		V	I_{ODE} = 4 mA
Output Low Voltage			0.1	V	I_{ODE} = −20 μA
		0.1	0.3	V	I_{ODE} = −1.6 mA
		0.2	0.4	V	I_{ODE} = −4 mA
Logic Inputs					
Input High Voltage	0.7 V_{DD1}			V	TxD, RTS, $\overline{RE}$
Input Low Voltage			0.25 V_{DD1}	V	TxD, RTS, $\overline{RE}$
CMOS Logic Input Current (TxD, RTS, $\overline{RE}$)	−10	+0.01	+10	μA	TxD, RTS, $\overline{RE}$ = V_{DD1} or 0 V
RECEIVER					
Differential Inputs					
Differential Input Threshold Voltage, V_{TH}	−200		+200	mV	−7 V ≤ V_{CM} ≤ +12V
Input Hysteresis		70		mV	−7 V ≤ V_{CM} ≤ +12V
Input Resistance (A, B)	20	30		kΩ	−7 V ≤ V_{CM} ≤ +12V
Input Current (A, B)			0.6	mA	V_{IN} = +12 V
			−0.35	mA	V_{IN} = −7 V
RxD Logic Output					
Output High Voltage	V_{DD1} − 0.1			V	I_{OUT} = +20 μA, V_A − V_B = +0.2 V
	V_{DD1} − 0.4	V_{DD1} − 0.2		V	I_{OUT} = +1.5 mA, V_A − V_B = +0.2 V
Output Low Voltage			0.1	V	I_{OUT} = −20 μA, V_A − V_B = −0.2 V
		0.2	0.4	V	I_{OUT} = −4 mA, V_A − V_B = −0.2 V
Output Short-Circuit Current	7		85	mA	V_{OUT} = GND or V_{CC}
Tristate Output Leakage Current			±1	μA	0.4 V ≤ V_{OUT} ≤ 2.4 V
TRANSFORMER DRIVER					
Oscillator Frequency	400	500	600	kHz	V_{DD1} = 5.5 V
	230	330	430	kHz	V_{DD1} = 3.3 V
Switch-On Resistance		0.5	1.5	Ω	
Start-Up Voltage		2.2	2.5	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY CURRENT					
Logic Side			2.5	mA	RTS = 0 V, V_{DD1} = 5.5 V
		2.3		mA	2.5 Mbps, V_{DD1} = 5.5 V, see Figure 23
		5.0	6.5	mA	16 Mbps, V_{DD1} = 5.5 V, see Figure 23
		1.26		mA	RTS = 0 V, V_{DD1} = 3.3 V
		1.5		mA	2.5 Mbps, V_{DD1} = 3.3 V, see Figure 23
		2.9		mA	16 Mbps, V_{DD1} = 3.3 V, see Figure 23
Bus Side		1.7	2.5	mA	RTS = 0 V
		49.0		mA	2.5 Mbps, RTS = V_{DD1}, see Figure 23 for load conditions
		55.0	75.0	mA	16 Mbps, RTS = V_{DD1}, see Figure 23 for load conditions
COMMON-MODE TRANSIENT IMMUNITY[1]	25			kV/µs	Transient magnitude = 800 V, V_{CM} = 1 kV
HIGH FREQUENCY COMMON-MODE NOISE IMMUNITY		100		mV	V_{HF} = +5 V, −2 V < V_{TEST2} < +7 V, 1 MHz < f_{TEST} < 50 MHz, see Figure 24

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

2.7 V ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	16			Mbps	
Propagation Delay Input-to-Output					
t_{PLH}, t_{PHL}	25	45	55	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 25
RTS-to-DE OUT Propagation Delay	20	35	55	ns	See Figure 26
Driver Output-to-$\overline{\text{Output}}$, t_{SKEW}		2	5	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 2 and Figure 25
Rise/Fall Time, t_R, t_F		5	15	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 2 and Figure 25
Enable Time		43	53	ns	See Figure 4 and Figure 27
Disable Time		43	55	ns	See Figure 4 and Figure 27
Enable Skew, $\lvert t_{AZH} - t_{BZL}\rvert$, $\lvert t_{AZL} - t_{BZH}\rvert$		1	3	ns	See Figure 4 and Figure 27
Disable Skew, $\lvert t_{AHZ} - t_{BLZ}\rvert$, $\lvert t_{ALZ} - t_{BHZ}\rvert$		2	5	ns	See Figure 4 and Figure 27
RECEIVER					
Propagation Delay, t_{PLH}, t_{PHL}	25	45	55	ns	C_L = 15 pF, see Figure 3 and Figure 28
Differential Skew, t_{SKEW}			5	ns	C_L = 15 pF, see Figure 3 and Figure 28
Enable Time		3	13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 5 and Figure 29
Disable Time		3	13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 5 and Figure 29

Timing Diagrams

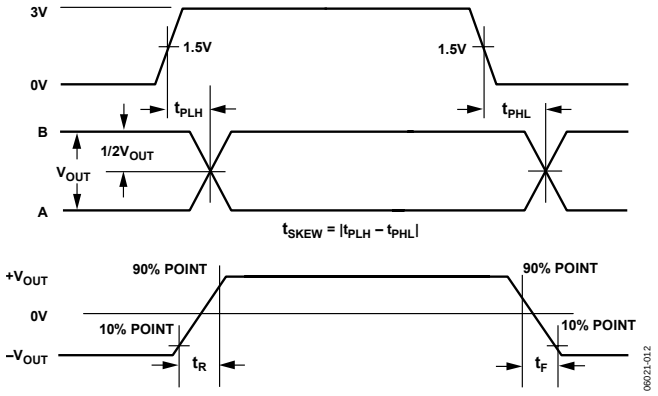


Figure 2. Driver Propagation Delay, Rise/Fall Timing

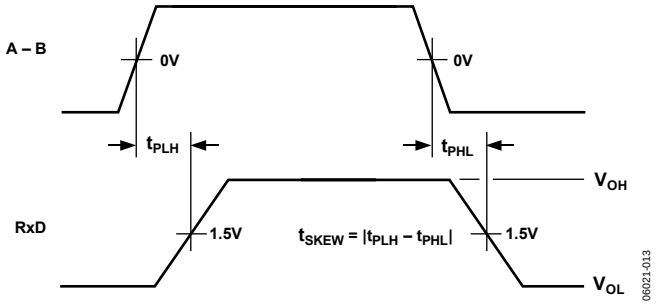


Figure 3. Receiver Propagation Delay

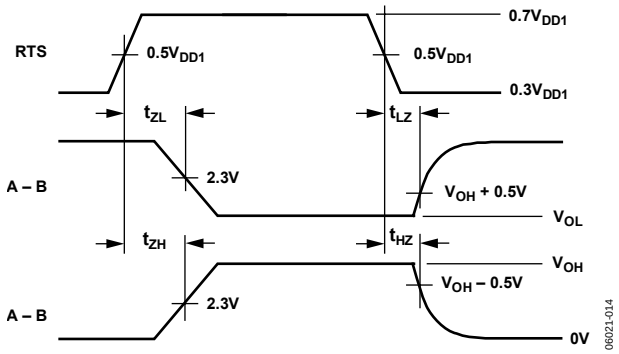


Figure 4. Driver Enable/Disable Timing

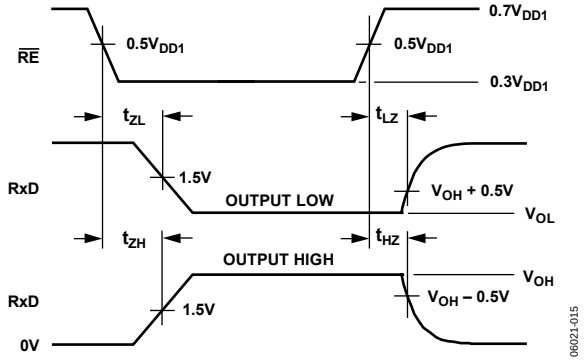


Figure 5. Receiver Enable/Disable Timing

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	Thermocouple located at center of package underside

[1] Device considered a 2-terminal device: Pin 1 to Pin 8 are shorted together and Pin 9 to Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Table 4. ADM2485 Approvals

Organization	Approval Type	Notes
UL	Recognized under the Component Recognition Program of Underwriters Laboratories, Inc.	In accordance with UL 1577, each ADM2485 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA).
VDE	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12	In accordance with DIN V VDE V 0884-10, each ADM2485 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (External Clearance)	L(I01)	5.15 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	5.5 min	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303-1
Isolation Group		IIIa		Material Group (DIN VDE 0110: 1989-01, Table 1)

VDE 0884-2 INSULATION CHARACTERISTICS

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on packages denotes DIN V VDE V 0884-10 approval.

Table 6.

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 for Rated Mains Voltage			
≤150 V rms		I to IV	
≤300 V rms		I to III	
≤400 V rms		I to II	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110: 1989-01, Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	V peak
Input-to-Output Test Voltage	V_{PR}		
Method B1: $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Tested, t_m = 1 sec, Partial Discharge < 5 pC		1050	V peak
Method A (After Environmental Tests, Subgroup 1): $V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, Partial Discharge <5 pC		896	V peak
Method A (After Input and/or Safety Test, Subgroup 2/3): $V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, Partial Discharge <5 pC		672	V peak
Highest Allowable Overvoltage[1]	V_{TR}	4000	V peak
Safety-Limiting Values[2]			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	265	mA
Output Current	$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S[3]	R_S	$>10^9$	Ω

[1] Transient overvoltage, t_{TR} = 10 sec.
[2] The safety-limiting value is the maximum value allowed in the event of a failure. See Figure 14 for the thermal derating curve.
[3] V_{IO} = 500 V.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective grounds.

Table 7.

Parameter	Rating
V_{DD1}	−0.5 V to +6 V
V_{DD2}	−0.5 V to +6 V
Digital Input Voltage (RTS, $\overline{RE}$, TxD)	−0.5 V to V_{DD1} + 0.5 V
Digital Output Voltage	
RxD	−0.5 V to V_{DD1} + 0.5 V
DE OUT	−0.5 V to V_{DD2} + 0.5 V
D1, D2	13 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
Average Output Current per Pin	−35 mA to +35 mA
θ_{JA} Thermal Impedance	73°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

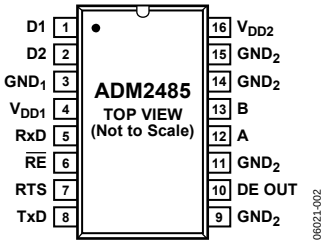


Figure 6. Pin Configuration

Table 8. Pin Function Description

Pin No.	Mnemonic	Function
1	D1	Transformer Driver Terminal 1.
2	D2	Transformer Driver Terminal 2.
3	GND_1	Ground, Logic Side.
4	V_{DD1}	Power Supply, Logic Side (3.3 V or 5 V). Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 µF and 0.1 µF.
5	RxD	Receiver Output Data. This output is high when (A − B) > 200 mV and low when (A − B) < −200 mV. The output is tristated when the receiver is disabled, that is, when $\overline{RE}$ is driven high.
6	$\overline{RE}$	Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver; driving it high disables the receiver.
7	RTS	Driver Enable Input. Driving this input high enables the driver; driving it low disables the driver.
8	TxD	Driver Input. Data to be transmitted by the driver is applied to this input.
9, 11, 14, 15	GND_2	Ground, Bus Side.
10	DE OUT	Driver Enable Status Output.
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled or V_{DD1} or V_{DD2} is powered down, Pin A is put in a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled or V_{DD1} or V_{DD2} is powered down, Pin B is put in a high impedance state to avoid overloading the bus.
16	V_{DD2}	Power Supply, Bus Side (Isolated 5 V Supply). Decoupling capacitor to GND_2 required; capacitor value should be between 0.01 µF and 0.1 µF.

TYPICAL PERFORMANCE CHARACTERISTICS

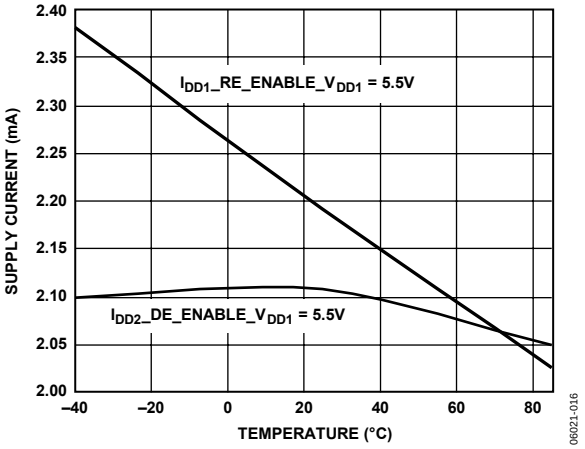


Figure 7. Unloaded Supply Current vs. Temperature

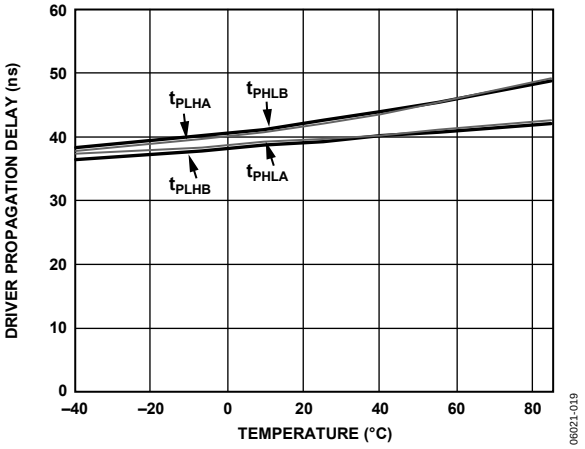


Figure 10. Driver Propagation Delay vs. Temperature

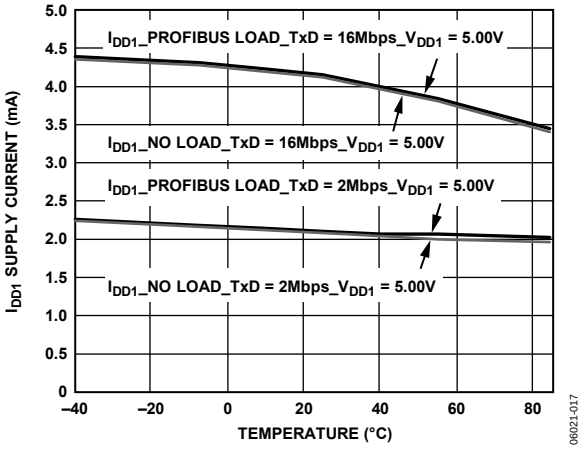


Figure 8. Logic Side Supply Current (I_{DD1} = 1 mA) vs. Temperature

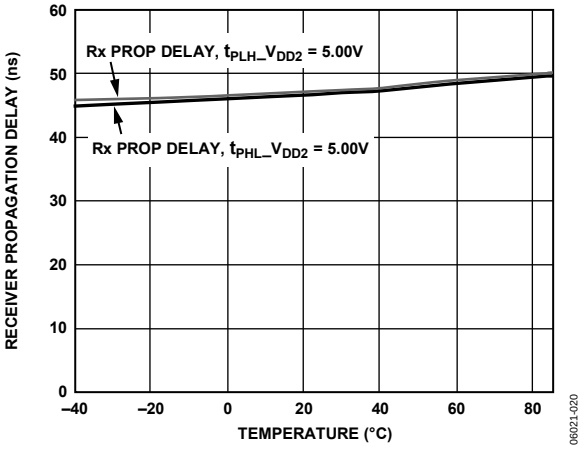


Figure 11. Receiver Propagation Delay vs. Temperature

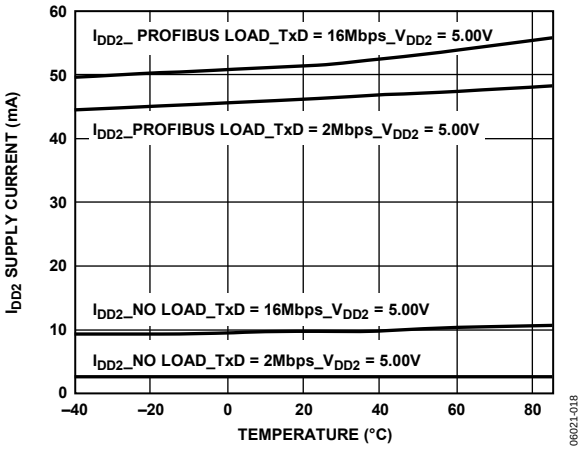


Figure 9. Bus Side Supply Current (I_{DD2} = 2 mA) vs. Temperature

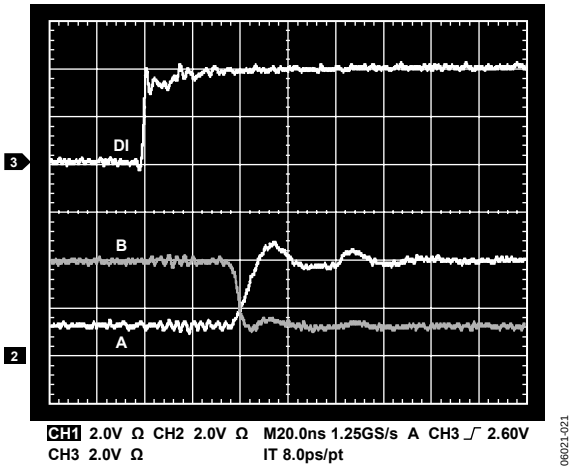


Figure 12. Driver/Receiver Propagation Delay, Low to High (R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

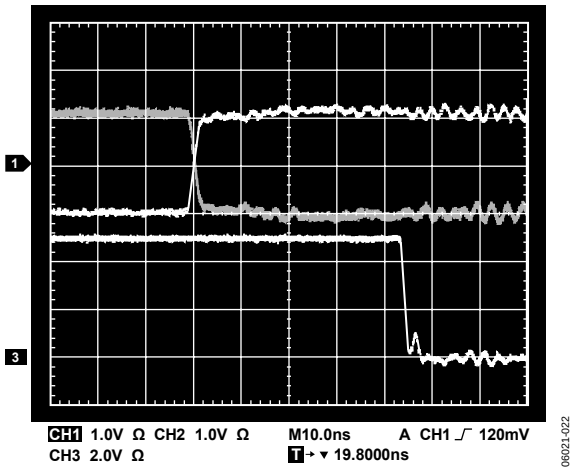


Figure 13. Driver/Receiver Propagation Delay, High to Low (R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

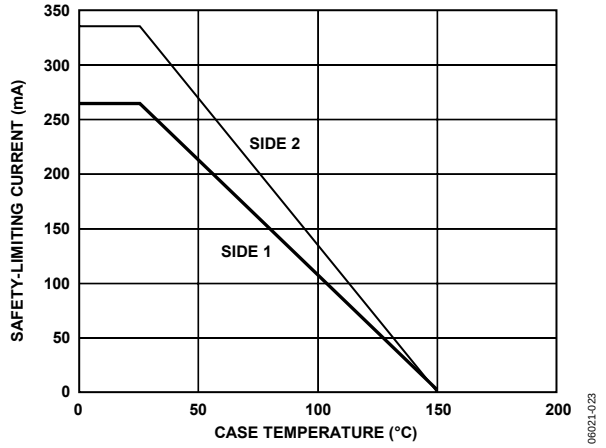


Figure 14. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884-2

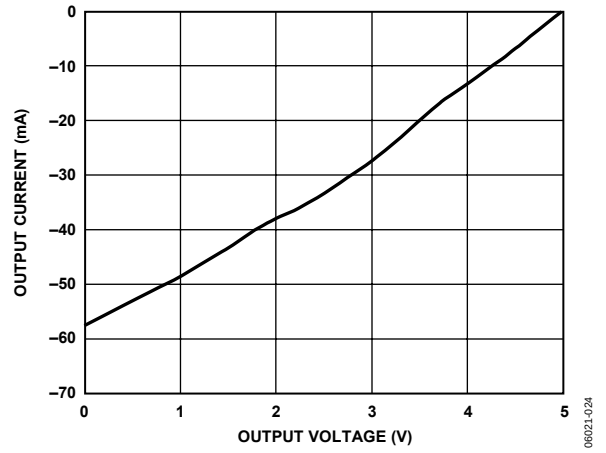


Figure 15. Output Current vs. Receiver Output High Voltage

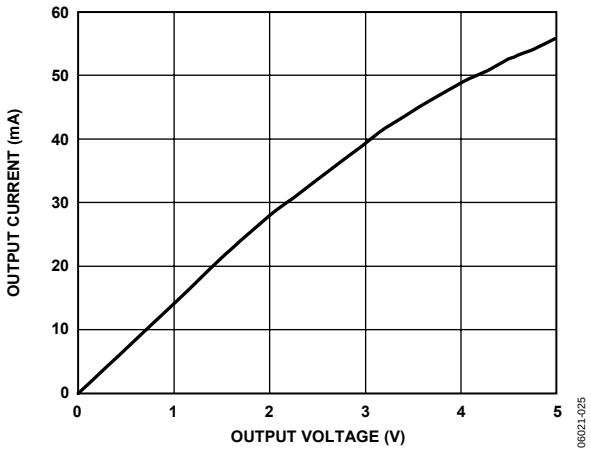


Figure 16. Output Current vs. Receiver Output Low Voltage

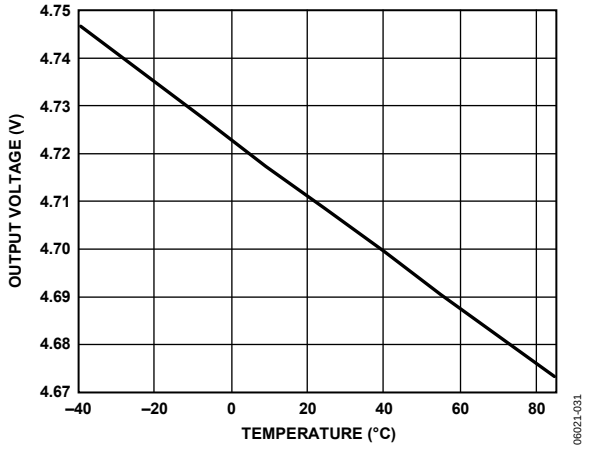


Figure 17. Receiver Output High Voltage vs. Temperature (I_{DD2} = –4 mA)

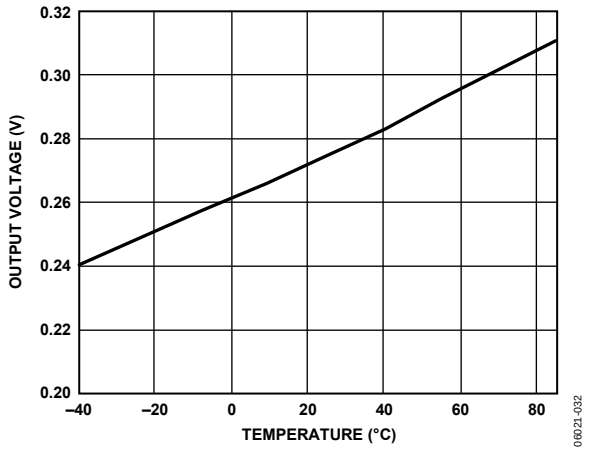


Figure 18. Receiver Output Low Voltage vs. Temperature (I_{DD2} = –4 mA)

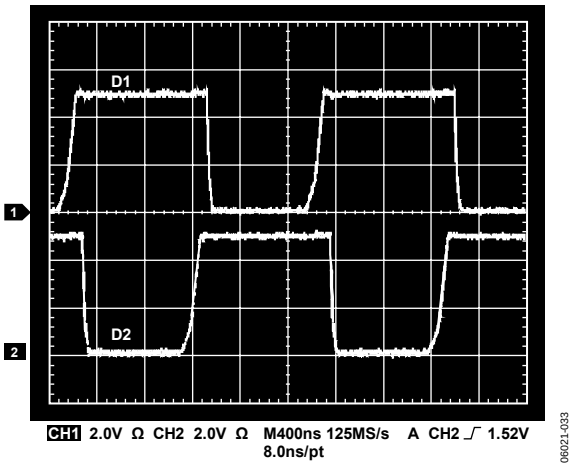


Figure 19. Switching Waveforms
(50 Ω Pull-Up to V_{DD1} on D1 and D2)

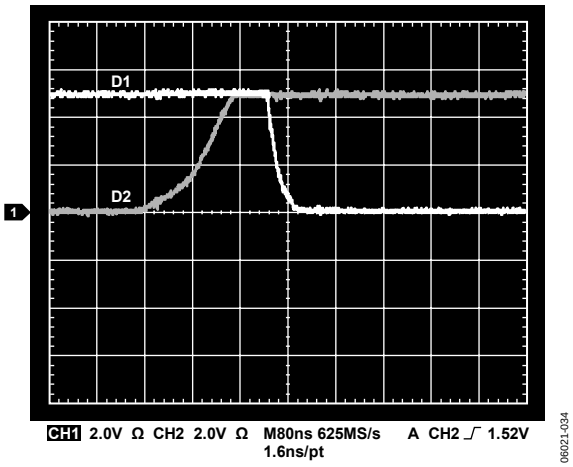


Figure 20. Switching Waveforms
(Break-Before-Make, 50 Ω Pull-Up to V_{DD1} on D1 and D2)

TEST CIRCUITS

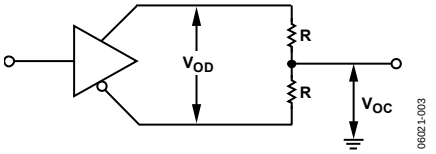


Figure 21. Driver Voltage Measurement

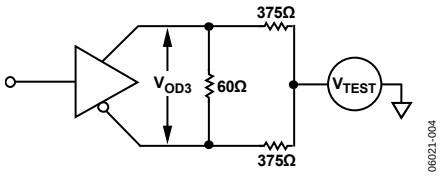


Figure 22. Driver Voltage Measurement

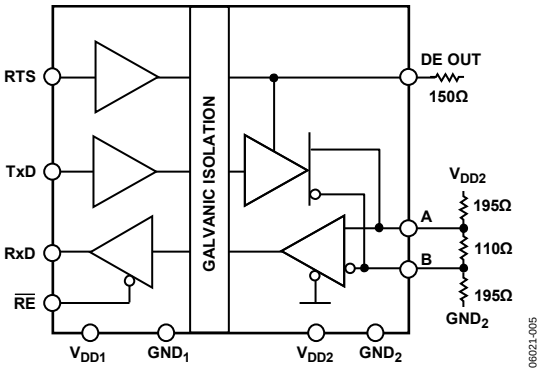


Figure 23. Supply-Current Measurement Test Circuit

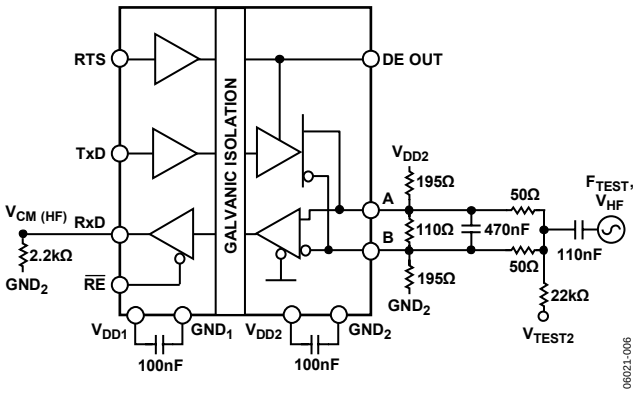


Figure 24. High Frequency, Common-Mode Noise Test Circuit

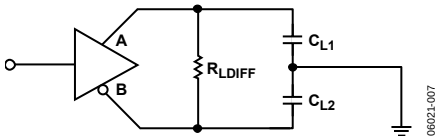


Figure 25. Driver Propagation Delay

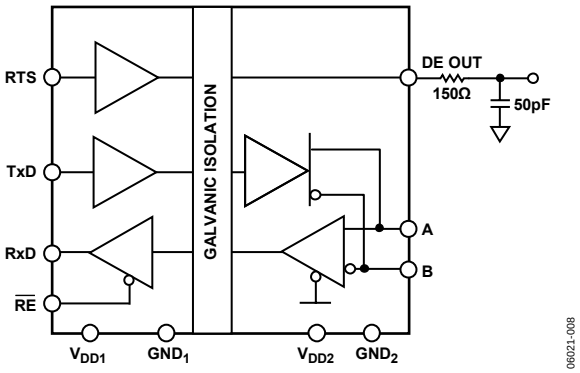


Figure 26. RTS to DE OUT Propagation Delay

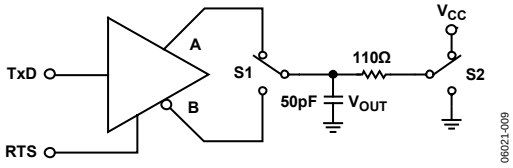


Figure 27. Driver Enable/Disable

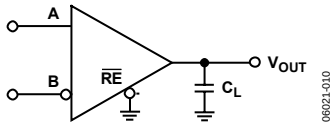


Figure 28. Receiver Propagation Delay

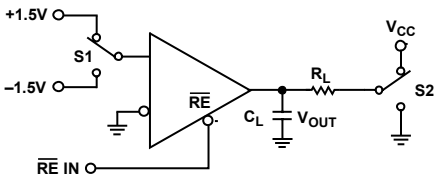


Figure 29. Receiver Enable/Disable

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2485, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 30). Driver input and data enable, applied to the TxD and RTS pins, respectively, and referenced to logic ground (GND_1), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

iCoupler Technology

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. This technique uses chip-scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

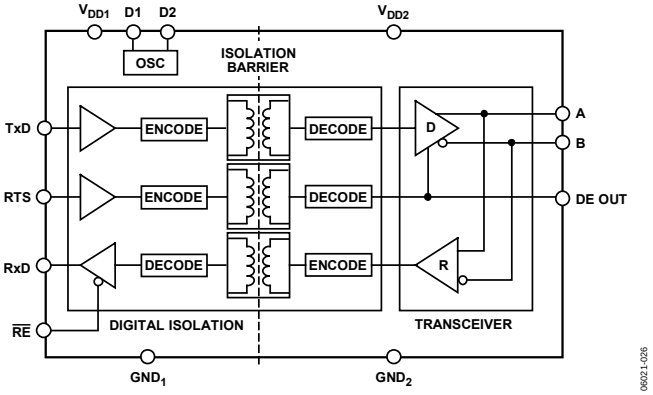


Figure 30. ADM2485 Digital Isolation and Transceiver Sections

TRUTH TABLES

Table 10 and Table 11 use the abbreviations found in Table 9.

Table 9. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 10. Transmitting

Supply Status		Inputs		Outputs		
V_{DD1}	V_{DD2}	RTS	TxD	A	B	DE OUT
On	On	H	H	H	L	H
On	On	H	L	L	H	H
On	On	L	X	Z	Z	L
On	Off	X	X	Z	Z	L
Off	On	X	X	Z	Z	L
Off	Off	X	X	Z	Z	L

Table 11. Receiving

Supply Status		Input	Outputs	
V_{DD1}	V_{DD2}	A – B	$\overline{RE}$	RxD
On	On	>+0.2 V	L or NC	H
On	On	<–0.2 V	L or NC	L
On	On	–0.2 V < A – B < +0.2 V	L or NC	I
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	On	X	L or NC	H
Off	Off	X	L or NC	L

THERMAL SHUTDOWN

The ADM2485 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

RECEIVER FAIL-SAFE INPUTS

The receiver input includes a fail-safe feature that guarantees a Logic high RxD output when the A and B inputs are floating or open-circuited.

MAGNETIC FIELD IMMUNITY

Because *i*Couplers use a coreless technology, no magnetic components are present and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Couplers have essentially infinite dc field immunity. The following analysis defines the conditions under which this can occur. The ADM2485 3.3 V operating condition is examined because it represents the most susceptible mode of operation.

The limitation on the *i*Coupler ac magnetic field immunity is set by the condition in which the induced error voltage in the receiving coil (the bottom coil, in this case) is made sufficiently large, either to falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left(\frac{-d\beta}{dt}\right) \sum \pi r_n^2 \; ; \; n = 1, 2 \ldots N \qquad (1)$$

where, if the pulses at the transformer output are greater than 1.0 V in amplitude:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of nth turn in the receiving coil (cm).

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin where induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 31.

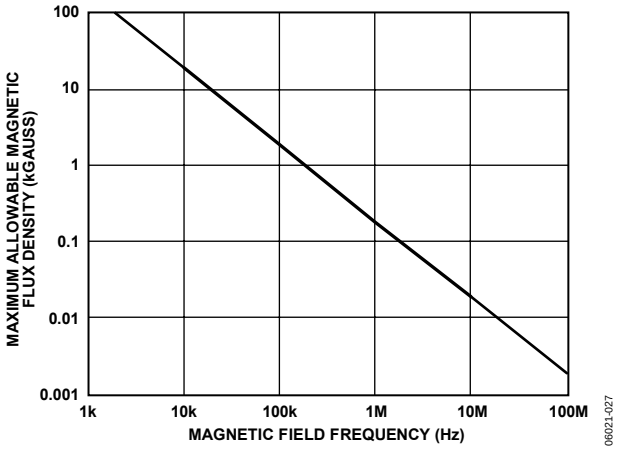


Figure 31. Maximum Allowable External Magnetic Flux Density vs. Magnetic Field Frequency

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil, which is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and it is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

Figure 32 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow at given distances from the ADM2485 transformers.

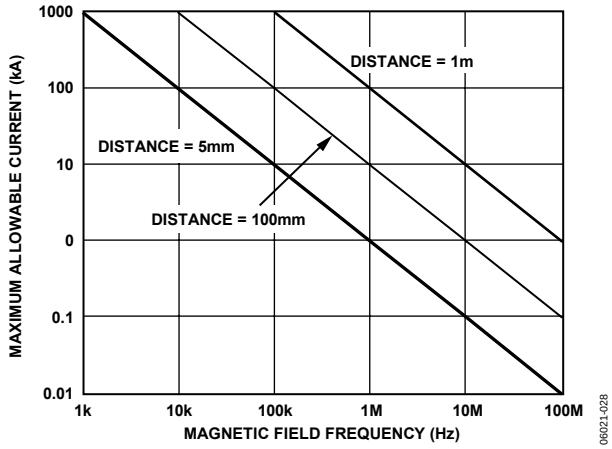


Figure 32. Maximum Allowable Current for Various Current-to-ADM2485 Spacings

At combinations of strong magnetic field and high frequency, any loops formed by printed circuit board (PCB) traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care must be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

PCB LAYOUT

The ADM2485 isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 33).

Bypass capacitors are most conveniently connected between Pin 3 and Pin 4 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value must be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

Bypassing between Pin 9 and Pin 16 is also recommended unless the ground wires on the V_{DD2} side are connected close to the package.

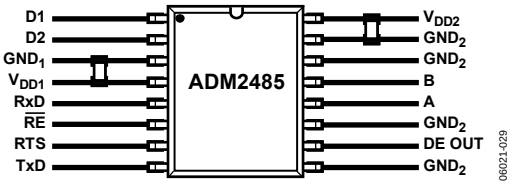


Figure 33. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care must be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout must be designed such that any coupling that does occur equally affects all pins on a given component side.

Failure to ensure this can cause voltage differentials between pins exceeding the device absolute maximum ratings, thereby leading to latch-up or permanent damage.

TRANSFORMER SUPPLIERS

The transformer primarily used with the ADM2485 must be a center-tapped transformer winding. The turns ratio of the transformer must be set to provide the minimum required output voltage at the maximum anticipated load with the minimum input voltage. Table 12 shows ADM2485 transformer suppliers.

Table 12. Transformer Suppliers

Manufacturer	Primary Voltage 3.3 V	Primary Voltage 5 V
Coilcraft	DA2304-AL	DA2303-AL
C&D Technologies	782485/35C	782485/55C

APPLICATIONS DIAGRAM

The ADM2485 integrates a transformer driver that, when used with an external transformer and LDO, generates an isolated 5 V power supply, to be supplied between V_{DD2} and GND_2.

D1 and D2 of the ADM2485 drive the center-tapped Transformer T1. A pair of Schottky diodes and a smoothing capacitor is used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated 5 V power supply to the ADM2485 bus-side circuitry (V_{DD2}), as shown in Figure 34.

When the ADM2485 is powered by 3.3 V on the logic side, a 1CT:2.2CT Transformer T1 is required to step up the 3.3 V to 6 V, ensuring enough headroom for the ADP3330 LDO to output a regulated 5 V output.

If ADM2485 is powered by 5 V on the logic side, a 1CT:1.5CT Transformer T1 is required, ensuring enough headroom for the ADP3330 LDO to output a regulated 5 V output.

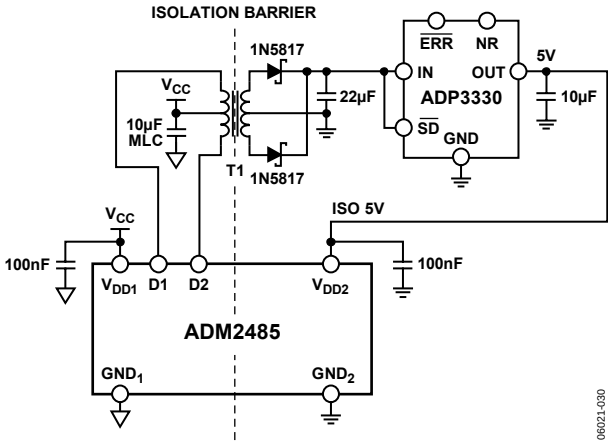
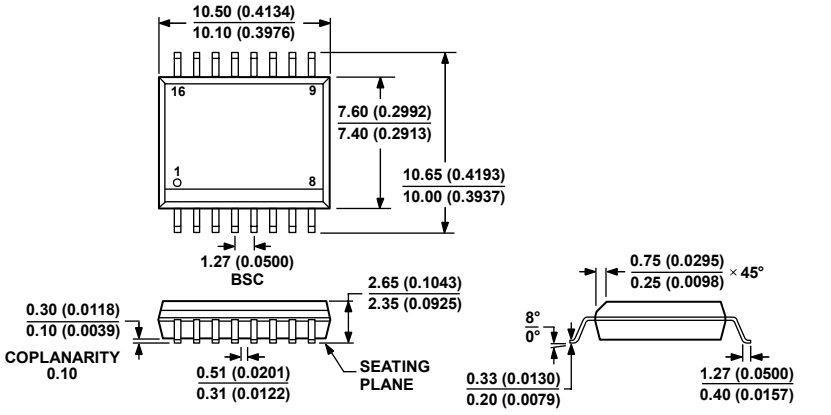


Figure 34. Applications Diagram

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 35. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADM2485BRWZ[1]	16	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADM2485BRWZ-REEL7[1]	16	−40°C to +85°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.

NOTES

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