High Voltage Positive Hot Swap Controller and Digital Power Monitor with PMBus

Data Sheet

ADM1272

FEATURES

- Controls supply voltages from 16 V to 80 V (absolute maximum 120 V)
- High voltage (80 V) IPC-9592 compliant packaging
- <500 ns response time to short circuit
- FET energy monitoring for adaptable FET SOA protection
- Gate boost mode for fast recovery from OC transients
- Programmable random start mode to stagger power-on
- FET fault detection
- Remote temperature sensing with programmable warning and shutdown thresholds
- Programmable 2.5 mV to 30 mV system current-limit setting range
- ±0.85% accurate current measurement with 12-bit ADC
- I_{LOAD}, V_{IN}, V_{OUT}, temperature, power, and energy telemetry
- Programmable start-up current limit
- Programmable linear output voltage soft start
- 1% accurate UV and OV thresholds
- Programmable hot swap restart function
- 2 programmable GPIO pins
- Reports power and energy consumption
- Peak detect registers for current, voltage, and power
- PMBus fast mode compliant interface
- 48-lead 7 mm × 8 mm LFCSP

APPLICATIONS

- 48 V/54 V systems
- Servers
- Power monitoring and control/power budgeting
- Central office equipment
- Telecommunication and data communication equipment
- Industrial applications

GENERAL DESCRIPTION

The ADM1272 is a hot swap controller that allows a circuit board to be removed from or inserted into a live backplane. It also features current, voltage, and power readback via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus™ interface. This device is able to withstand up to 120 V, which makes it very robust in surviving surges and transients commonly associated with high voltage systems, usually clamped using protection devices such as transient voltage suppressors (TVSs) that can often exceed 100 V.

The load current, I_{LOAD}, is measured using an internal current sense amplifier that measures the voltage across a sense resistor in the power path via the SENSE+ and SENSE− pins. A default current limit sense voltage of 30 mV is set, but this limit can be adjusted down, if required, using a resistor divider network from the VCAP regulator output voltage to the ISET pin. An additional resistor can also be placed from ISET to V_{IN} (or V_{OUT}) to allow the current limit to track inversely with the rail voltage. This resistor allows an approximate system power limit to be used.

The ADM1272 limits the current through the sense resistor by controlling the gate voltage of an external N channel field effect transistor (FET) in the power path. The sense voltage, and therefore the load current, is maintained below the preset maximum. The ADM1272 protects the external FET by monitoring and limiting the energy transfer through the FET while the current is being controlled. This energy limit is set by the choice of components connected to the EFAULT pin (for fault protection mode) and the ESTART pin during startup. Therefore, different energy limits can be set for start-up and normal fault conditions. During startup, inrush currents are maintained very low and different areas of the safe operating area (SOA) curve are of interest, whereas during fault conditions, the currents can be much higher.

The controller uses the drain to source voltage (V_{DS}) across the FET to set the current profile of the EFAULT and ESTART pins and, therefore, the amount of much energy allowed to be transferred in the FET. This energy limit ensures the MOSFET remains within the SOA limits. Optionally, use a capacitor on the DVDT pin to set the output voltage ramp rate, if required. In case of a short-circuit event, a fast internal overcurrent detector responds in hundreds of ns and signals the gate to shut down. A 1.5 A pull-down device ensures a fast FET response. The gate then recovers control within 50 µs to ensure minimal disruption during conditions, such as line steps and surges. The ADM1272 features overvoltage (OV) and undervoltage (UV) protection, programmed using external resistor dividers on the UVH, UVL, and OV pins. The use of two pins for undervoltage allows independent accurate rising and falling thresholds. The PWRGD output pin signals when the output voltage is valid and the gate is sufficiently enhanced. The validity of VOUT is determined using the PWGIN pin.

The 12-bit ADC measures the voltage across the sense resistor, the supply voltage on the SENSE+ pin, the output voltage, and the temperature using an external NPN/PNP device. A PMBus interface allows a controller to read data from the ADC. As many as 16 unique I^2C addresses can be selected, depending on how the two ADRx pins are connected. The ADM1272 is available in a custom 48-lead LFCSP (7 mm × 8 mm) with a pinstrap mode that allows the device to be configured for automatic retry or latchoff when an overcurrent (OC) fault occurs.

Rev. B
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REVISION HISTORY

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5/2019—Rev. 0 to Rev. A

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4/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

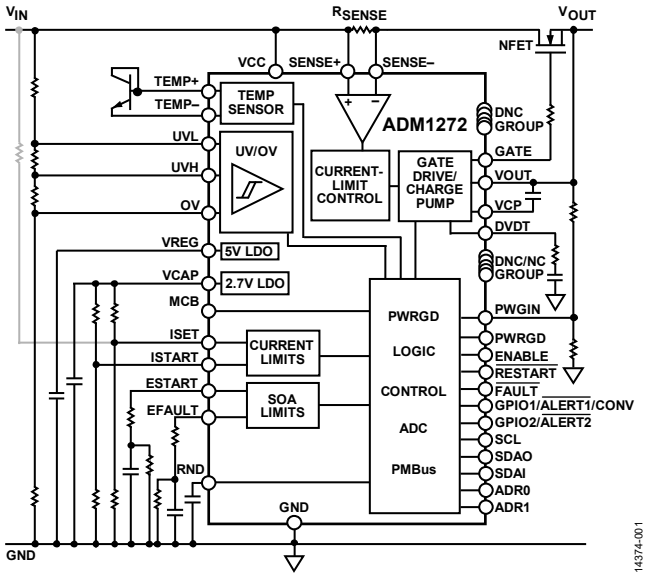


Figure 1.

SPECIFICATIONS

V_{CC} = 16 V to 80 V, $V_{CC} \geq V_{SENSE+}$, V_{SENSE+} = 16 V to 80 V, $V_{\Delta SENSE} = (V_{SENSE+} - V_{SENSE-})$ = 0 V, T_J= −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Operating Voltage Range[1]	V_{CC}	16		80	V	
Undervoltage Lockout	V_{CCUV}	13		16	V	V_{CC} rising
Undervoltage Hysteresis	$V_{CCUVHYS}$		70	115	mV	
Quiescent Current	I_{CC}			6	mA	GATE on and power monitor running
Power-On Reset (POR)	t_{POR}		27		ms	
UVL AND UVH PINS						
Input Current	I_{UV}		1	50	nA	UVL ≤ 3.6 V, when UVL and UVH are tied together
UVH Threshold	UVH_{TH}	0.99	1.0	1.01	V	UV rising
UVL Threshold	UVL_{TH}	0.887	0.9	0.913	V	UV falling
UVx Threshold Hysteresis	UV_{HYST}		100		mV	When UVL and UVH are tied together
UVx Glitch Filter	UV_{GF}	3.5		7.5	µs	50 mV overdrive
UVx Propagation Delay	UV_{PD}		5	8	µs	UVx low to GATE pull-down active
OV PIN						
Input Current	I_{OV}			50	nA	OV ≤ 3.6 V
OV Threshold	OV_{TH}	0.99	1.0	1.01	V	OV rising
OV Hysteresis Current	I_{OVHYST}	4.5	5.25	6	µA	
OV Glitch Filter	OV_{GF}	1.75		3.75	µs	50 mV overdrive
OV Propagation Delay	OV_{PD}		3	4.5	µs	OV high to GATE pull-down active
SENSE+ AND SENSE− PINS						
Current-Limit Setting Range	$V_{SENSECL}$	2.5		30	mV	Adjustable using ISET and ISTART pins
Input Current	I_{SENSEx}		130	170	µA	Per individual pin
Input Imbalance	$I_{\Delta SENSE}$			5	µA	$I_{\Delta SENSE} = (I_{SENSE+}) - (I_{SENSE-})$
VREG PIN						
Internally Regulated Voltage	V_{VREG}	4.5	5	5.5	V	0 µA ≤ I_{VREG} ≤ 100 µA; C_{VREG} = 1 µF
VCAP PIN						
Internally Regulated Voltage	V_{VCAP}	2.68	2.7	2.72	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET PIN						
Reference High Limit[1]	V_{CLREF_HI}		1.2		V	V_{CLREF}[2] = $V_{VCAP} - V_{ISET}$; $V_{SENSECL}$ = 30 mV; internally clamped with falling V_{ISET}
Reference Low Limit[1]	V_{CLREF_LO}		100		mV	Internally clamped with rising V_{ISET} or V_{ISTART} < 100 mV, $V_{CLREF} = V_{VCAP} - V_{ISET}$; $V_{SENSECL}$ = 2.5 mV
Gain of Current Sense Amplifier[1]	AV_{CSAMP}		40		V/V	
Input Current	I_{ISET}			100	nA	$V_{ISET} \leq V_{VCAP}$
ISTART PIN						
Reference Select Threshold	$V_{ISTARTRSTH}$	1.35	1.5	1.65	V	If $V_{ISTART} > V_{ISTARTRSTH}$, internal 1 V reference ($V_{CLREF1V}$) is used
Internal Reference[1]	$V_{CLREF1V}$		1		V	
Input Current	I_{ISTART}			100	nA	$V_{ISTART} \leq V_{VCAP}$
GATE PIN[3]						
Gate Drive Voltage	ΔV_{GATE}					$\Delta V_{GATE} = V_{GATE} - V_{OUT}$
		10	12	14	V	80 V ≥ V_{CC} ≥ 20 V; I_{GATE} ≤ 5 µA
		4.5			V	20 V ≥ V_{CC} ≥ 16 V; I_{GATE} ≤ 5 µA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Gate Pull-Up Current	I_{GATEUP}	−20		−30	µA	ΔV_{GATE} = 0 V
Gate Recovery Rate			0.12		V/µs	Following severe OC shutdown
Gate Pull-Down Current						
Regulation	I_{GATEDN_REG}	35	60	75	µA	4 V > ΔV_{GATE} ≥ 2 V; V_{ISET} = 1.7 V; $V_{\Delta SENSE}$ = 30 mV
		50	70	90		ΔV_{GATE} ≥ 4 V; V_{ISET} = 1.7 V; $V_{\Delta SENSE}$ = 30 mV
Slow	I_{GATEDN_SLOW}	8	15	25	mA	ΔV_{GATE} ≥ 2 V; V_{ENABLE} = 0 V
Fast	I_{GATEDN_FAST}	1.1	1.5	1.9	A	ΔV_{GATE} ≥ 10 V
VCP PIN						
VCP Capacitor Ratio			10			C_{VCP} must be 10 times larger than C_{DVDT} + $C_{GATETOTAL}$
DVDT PIN						
Switch Resistance	$DVDT_{SWG}$		40		Ω	V_{GATE} − V_{DVDT} = 100 mV; V_{GATE} ≤ (V_{VOUT} + 5 V); V_{CC} > 20 V
	$DVDT_{SWVO}$		40		Ω	V_{DVDT} − V_{OUT} = 100 mV
HOT SWAP SENSE VOLTAGE						
Hot Swap Sense Voltage Current Limit						ΔV_{GATE} = 3 V; I_{GATE} = 0 µA
	$V_{SENSECL}$	29.4	30	30.3	mV	V_{ISET} < 1 V; internally clamped
		24.3	25	25.4	mV	V_{ISET} = 1.7 V
		19.3	20	20.4	mV	V_{ISET} = 1.9 V
		14.3	15	15.4	mV	V_{ISET} = 2.1 V
		9.3	10	10.4	mV	V_{ISET} = 2.3 V
Start-Up Current Limit	$V_{SENSECL}$	29.4	30	30.4	mV	V_{ISTART} = 1.2 V; STRT_UP_IOUT_LIM = Code 0x0F
		24.4	25	25.4	mV	V_{ISTART} = 1 V, or V_{ISTART} > 1.65 V
		19.4	20	20.4	mV	V_{ISTART} = 0.8 V
		14.4	15	15.4	mV	V_{ISTART} = 0.6 V
		4.4	5	5.4	mV	V_{ISTART} = 0.2 V
Minimum $V_{SENSECL}$ Clamp	V_{CLAMP}	1.9	2.4	2.9	mV	V_{ISTART} = 0 V or V_{ISET} =2.7 V or STRT_UP_IOUT_LIM = 0x00
Circuit Breaker Offset	V_{CBOS}	0.9	1.1	1.31	mV	Circuit breaker trip voltage, V_{CB} = $V_{SENSECL}$ − V_{CBOS}
SEVERE OVERCURRENT (SOC)						
Voltage Threshold	$V_{SENSEOC}$	43	45	47	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 11 (1.5×)
		58	60	62	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 10 (2×, default at power-up)
		88	90	92	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 01 (3×)
		118	120	122	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 00 (4×)
Glitch Filter Duration		80		280	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 00
		500		880	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 01
		2.2		5.5	µs	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT =10
		6.8		10.8	µs	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 11
Response Time	t_{SOC}					To gate pull-down current active
			330	500	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 00 (default)
			860	1070	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 01
			6500	9000	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 10
			11500	15000	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 11
ESTART PIN						
Pull-Up Current[4]	$I_{ESTARTUP}$	−88	−100	−113	µA	V_{CC} − V_{OUT} = 100 V; V_{ISTART} >1.65 V; $V_{\Delta SENSE}$ = 25 mV
		−8.4	−10	−11.3	µA	V_{CC} − V_{OUT} = 10 V; V_{ISTART} >1.65 V; $V_{\Delta SENSE}$ = 25 mV
		−0.8	−1	−1.2	µA	V_{CC} − V_{OUT} = 0 V; V_{ISTART} >1.65 V; $V_{\Delta SENSE}$ = 25 mV
Pull-Down Current	$I_{ESTARTDN}$	350	500	680	nA	V_{CC} − V_{OUT} = 0 V
High Threshold	$V_{ESTARTH}$	0.98	1.0	1.02	V	
Low Threshold	$V_{ESTARTL}$	35	50	65	mV	
Glitch Filter	$V_{ESTARTGF}$		10		µs	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EFAULT						
Pull-Up Current[4]	$I_{EFAULTUP}$	−88	−100	−113	µA	$V_{CC} - V_{OUT}$ = 100 V; V_{ISET} = 0 V; $V_{\Delta SENSE}$ = 30 mV
		−8.4	−10	−11.3	µA	$V_{CC} - V_{OUT}$ = 10 V; V_{ISET} = 0 V; $V_{\Delta SENSE}$ = 30 mV
		−0.8	−1	−1.2	µA	$V_{CC} - V_{OUT}$ = 0 V; V_{ISET} < 1 V; $V_{\Delta SENSE}$ = 30 mV
Pull-Down Current	$I_{EFAULTDN}$	350	500	680	nA	Always present on active pin when pull-up currents are not active
High Threshold	$V_{EFAULTH}$	0.98	1.0	1.02	V	
Low Threshold	$V_{EFAULTL}$	35	50	65	V	
Glitch Filter	$V_{EFAULTGF}$		10		µs	
MCB PIN						Mask severe OC shutdown
Input Current	I_{MCB}			4.4	µA	MCB ≤ 3.6 V (internal 1 MΩ pull-down resistor)
MCB Threshold	V_{MCB_TH}	0.58	0.6	0.62	V	MCB rising
MCB Threshold Hysteresis	V_{MCB_HYST}	10	25	40	mV	
MCB masking window	t_{MCB}					Must exceed V_{MCB_TH} within t_{MCB} of severe over current event
		150			ns	OC_FILT_SELECT = 00
		600			ns	OC_FILT_SELECT = 01
		4.5			µs	OC_FILT_SELECT = 10
		9.0			µs	OC_FILT_SELECT = 11
VOUT PIN						
Input Current		20		200	µA	1 V ≤ VOUT ≤ 80 V
$\overline{\text{FAULT}}$ PIN						
Output Low Voltage	V_{OL_LATCH}			0.4	V	I_{FAULT} = 1 mA
				1.5	V	I_{FAULT} = 5 mA
Leakage Current				100	nA	V_{FAULT} ≤ 2 V; $\overline{\text{FAULT}}$ output high-Z
				1	µA	V_{FAULT} = 20 V; $\overline{\text{FAULT}}$ output high-Z
ENABLE PIN						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Glitch Filter			1		µs	
Leakage Current				100	nA	V_{ENABLE} ≤ 2 V
				1	µA	V_{ENABLE} = 18 V
RND PIN						
Pull-Up Current		−3.6	−4.2	−4.9	µA	V_{RND} = 0.5 V
High Threshold		0.93	1	1.07	V	
Delay Range[5]		0.28		38.9	ms	RND pin not connected
		16.6		2274	ms	C_{RND} = 100 nF
Timeout				3.63	sec	If pin fails to cycle, power-up continues following this timeout
Maximum External Capacitance				220	nF	
$\overline{\text{RESTART}}$ PIN						
Input Voltage High	V_{IH}	1.1			V	
Input Voltage Low	V_{IL}			0.8	V	
Glitch Filter			10		µs	
Internal Pull-Up Current			−16		µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
GPIO1/$\overline{\text{ALERT1}}$/CONV AND GPIO2/$\overline{\text{ALERT2}}$ PINS						
Output Low Voltage	V_{OL_GPIO}			0.4	V	I_{GPIO1} = 1 mA
				1.5	V	I_{GPIO1} = 5 mA
Leakage Current	I_{LKG_GPIO}			100	nA	$V_{GPIO1} \leq 2$ V; GPIO output high-Z
				1	µA	V_{GPIO1} = 20 V; GPIO output high-Z
Input High Voltage	V_{GPIOIH}	1.1			V	
Input Low Voltage	V_{GPIOIL}			0.8	V	
Glitch Filter			1		µs	
PWRGD PIN						
Output Low Voltage	V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
				1.5	V	I_{PWRGD} = 5 mA
VCC That Guarantees Valid Output		1.9			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current				100	nA	$V_{PWRGD} \leq 2$ V; PWRGD output high-Z
				1	µA	V_{PWRGD} = 20 V; PWRGD output high-Z
PWGIN PIN						
Input Current	I_{PWGIN}			50	nA	PWGIN ≤ 3.6 V
PWGIN Threshold	V_{PWGIN_TH}	0.99	1.0	1.01	V	PWGIN falling
PWGIN Threshold Hysteresis	V_{PWGIN_HYST}	45	60	75	mV	
Glitch Filter			2		µs	Asserting and deasserting of PWRGD pin
ADC						
Conversion Time						Includes time for power multiplication
			144	160	µs	One sample of I_{OUT}; from command received to valid data in register
			78	87	µs	One sample of V_{IN}; from command received to valid data in register
			78	87	µs	One sample of V_{OUT}; from command received to valid data in register
ADR0/ADR1 PINS						
Address Set to 00		0		0.8	V	Connect to GND
Input Current for Address Set to 00		−40	−22		µA	V_{ADRx} = 0 V to 0.8 V
Address Set to 01		135	150	165	kΩ	Resistor to GND
Address Set to 10		−1		+1	µA	No connect state; maximum leakage current allowed
Address Set to 11		2			V	Connect to VCAP or alternative supply within ratings
Input Current for Address Set to 11			3	10	µA	V_{ADRx} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
TEMP± PINS						External transistor is 2N3904
Operating Range		−55		+150	°C	Limited by external diode
Accuracy			±1	±7	°C	$T_A = T_{DIODE}$ = −40°C to +125°C
Resolution			0.25		°C	LSB size
Low Level Output Current Source[6]			5		µA	
Medium Level Output Current Source[6]			30		µA	
High Level Output Current Source[6]			105		µA	
Maximum Series Resistance for External Diode[6]	R_{STEMP}			100	Ω	For <±0.5°C additional error, C_P = 0 pF
Maximum Parallel Capacitance for External Diode[6]	C_{PTEMP}			1	nF	R_{STEMP} = 0 Ω

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS DIGITAL INPUTS (SDAI/SDAO, SCL)						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Input Leakage	I_{LEAK_PIN}	−10		+10	µA	
		−5		+5	µA	Device is not powered
Nominal Bus Voltage	V_{DD}	2.7		5.5	V	3 V to 5 V ± 10%
Capacitive Load per Bus Segment	C_{BUS}			400	pF	
Capacitance for SDAI, SDAO, or SCL Pin	C_{PIN}		5		pF	
Input Glitch Filter, t_{SP}	t_{SP}	0		50	ns	

[1] Tolerances included in the total sense voltage tolerances.
[2] V_{CLREF} is the active current-limit reference. $V_{CLREF} = V_{SENSECL} \times AV_{CSAMP}$, where $V_{SENSECL}$ is the current limit at the SENSE± pins.
[3] Maximum voltage on the gate with respect to VOUT is always clamped to ≤14 V.
[4] Pull-up current is (VCC − VOUT − V_{TH})/R, where V_{TH} is approximately 1 V and R = 1 MΩ (±10%).
[5] Guaranteed by design, but not production tested.
[6] Sampled during initial release to ensure compliance, but not subject to production testing.

POWER MONITORING ACCURACY SPECIFICATIONS

V_{CC} = 16 V to 80 V, $V_{CC} \geq V_{SENSE+}$, V_{SENSE+} = 16 V to 80 V, $V_{\Delta SENSE} = (V_{SENSE+} - V_{SENSE-})$, T_J = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT SENSE ABSOLUTE ERROR					128-sample averaging (unless otherwise noted)
			±1.2	%	$V_{\Delta SENSE}$ = 30 mV
			±0.85	%	$V_{\Delta SENSE}$ = 30 mV, T_J = 25°C to 85°C
			±1.5	%	$V_{\Delta SENSE}$ = 25 mV
			±1.0	%	$V_{\Delta SENSE}$ = 25 mV, T_J = 25°C to 85°C
			±1.8	%	$V_{\Delta SENSE}$ = 20 mV
			±1.25	%	$V_{\Delta SENSE}$ = 20 mV, T_J = 25°C to 85°C
			±1.85	%	$V_{\Delta SENSE}$ = 20 mV, 16-sample averaging
			±1.9	%	$V_{\Delta SENSE}$ = 20 mV, 1-sample averaging
			±2.4	%	$V_{\Delta SENSE}$ = 15 mV
			±1.7	%	$V_{\Delta SENSE}$ = 15 mV, T_J = 25°C to 85°C
			±3.6	%	$V_{\Delta SENSE}$ = 10 mV
			±2.6	%	$V_{\Delta SENSE}$ = 10 mV, T_J = 25°C to 85°C
			±7	%	$V_{\Delta SENSE}$ = 5 mV
			±5	%	$V_{\Delta SENSE}$ = 5 mV, T_J = 25°C to 85°C
			±14.1	%	$V_{\Delta SENSE}$ = 2.5 mV
			±10	%	$V_{\Delta SENSE}$ = 2.5 mV, T_J = 25°C to 85°C
SENSE+/VOUT ABSOLUTE ERROR			±0.4	%	V_{SENSE+}/V_{OUT} = 40 V to 80 V
POWER ABSOLUTE ERROR			±1.9	%	$V_{\Delta SENSE}$ = 20 mV, V_{CC} = 54 V
			±1.3	%	$V_{\Delta SENSE}$ = 20 mV, V_{CC} = 54 V, T_J = 25°C to 85°C

SERIAL BUS TIMING CHARACTERISTICS

Table 3.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
f_{SCLK}	Clock frequency			400	kHz	
t_{BUF}	Bus free time	1.3			µs	
$t_{HD;STA}$	Start hold time	0.6			µs	
$t_{SU;STA}$	Start setup time	0.6			µs	
$t_{SU;STO}$	Stop setup time	0.6			µs	
$t_{HD;DAT}$	SDAO/SDAI hold time	300		900	ns	
$t_{SU;DAT}$	SDAO/SDAI setup time	100			ns	
t_{LOW}	SCL low time	1.3			µs	
t_{HIGH}	SCL high time	0.6			µs	
t_R[1]	SCL, SDAO/SDAI rise time	20		300	ns	
t_F	SCL, SDAO/SDAI fall time	20		300	ns	

[1] $t_R = (V_{IL(MAX)} - 0.15)$ to (2.1 + 0.15) and $t_F = 0.9\ V_{DD}$ to $(V_{IL(MAX)} - 0.15)$; where $V_{IH3V3} = 2.1$ V, and $V_{DD} = 3.3$ V.

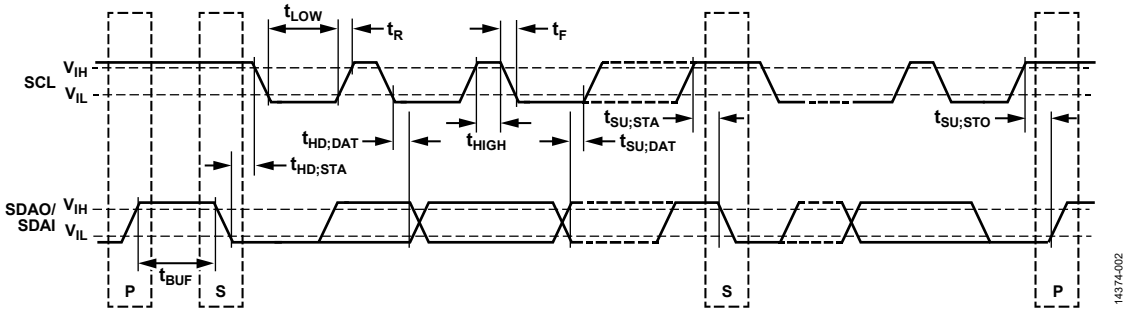


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VCC, SENSE± to GND	−0.3 V to +120 V
$V_{\Delta SENSE}$ (SENSE+ − SENSE−)	−1 V to +1 V
VOUT to GND	−5 V to +120 V
VCP to GND	−0.3 V to (VOUT + 12 V) or (VCC + 15 V), whichever is lower
GATE (Internal Supply Only)[1] to GND	(VOUT − 0.3 V) to (VCP + 0.3 V)
DVDT to GND	(VOUT − 0.3 V) to (GATE + 0.3 V)
UVH, UVL, OV, MCB to GND	−0.3 V to +6.5 V
ISTART, ISET, VCAP to GND	−0.3 V to +4 V
ESTART, EFAULT, TEMP+ to GND	−0.3 V to VCAP + 0.3 V
VREG (Internal Supply Only) to GND	−0.3 V to +5.5 V
$\overline{\text{FAULT}}$, $\overline{\text{RESTART}}$ to GND	−0.3 V to +20 V
PWGIN, SCL, SDAO, SDAI, ADR0, ADR1 to GND	−0.3 V to +6.5 V
RND to GND	−0.3 V to VCAP + 0.3 V
ENABLE, GPIO1/$\overline{\text{ALERT1}}$/CONV, GPIO2/$\overline{\text{ALERT2}}$, PWRGD to GND	−0.3 V to +20 V
TEMP− Pin to GND (Internally Connected to GND)	0 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	125°C

[1] The GATE pin has internal clamping circuits to prevent the GATE pin voltage from exceeding the maximum ratings of a MOSFET with a gate to source voltage (V_{GSMAX}) = 20 V and internal process limits. Applying a voltage source to this pin externally may cause irreversible damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-48-18[1]			
Still Air	50	0.5	°C/W
2 m/sec Air Flow	40	1	°C/W

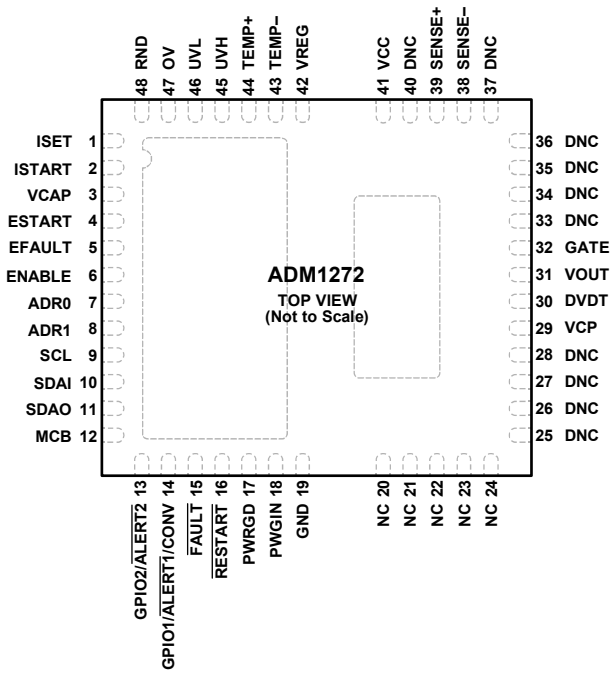
[1] The thermal resistance values are based on JEDEC 2S2P test conditions.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. THE NC PINS ARE NOT REQUIRED TO BE CONNECTED, BUT DO HAVE INTERNAL CONNECTIONS. THEY SHARE THE SAME ELECTRICAL NODE INTERNALLY TO THE EPVCC PAD AND CAN THEREFORE BE USED AS A THERMAL EXIT ROUTE FROM EPVCC ON THE SAME OUTER LAYER AND SAME ELECTRICAL CONNECTION AS EPVCC.
2. DNC = DO NOT CONNECT. THE DNC PINS MUST NOT BE CONNECTED TO ANY ELECTRICAL SIGNAL, GND, OR SUPPLY VOLTAGE. ANY CONNECT COPPER MUST BE ELECTRICALLY ISOLATED AND APPROPRIATELY SPACED FROM OTHER NODES, WHICH ALLOWS COMPLIANCE WITH IPC-9592 RECOMMENDATIONS FOR 80V.
3. EXPOSED PAD. ALWAYS CONNECT TO GND. THE EXPOSED PAD IS LOCATED ON THE UNDERSIDE OF THE LFCSP PACKAGE AND IS THE LARGER OF THE TWO PADS. SOLDER THE EXPOSED PAD TO THE PCB FOR OPTIMAL THERMAL DISSIPATION.
4. EXPOSED PAD. INTERNALLY CONNECTED TO VCC. THE EXPOSED PAD IS LOCATED ON THE UNDERSIDE OF THE LFCSP PACKAGE AND IS THE SMALLER OF THE TWO PADS. SOLDER THE EXPOSED PAD TO THE PCB FOR OPTIMAL THERMAL DISSIPATION. ALWAYS ELECTRICALLY CONNECT EPVCC TO THE SAME POTENTIAL AS VCC. MOST OF THE DEVICE POWER IS DISSIPATED THROUGH THIS PAD; THEREFORE, CONSIDER A STRONG THERMAL CONNECTION TO AVAILABLE COPPER.

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ISET	Current-Limit Setting. This pin allows the current-limit threshold to be programmed. The default limit of 30 mV is set when this pin is connected directly to 0 V. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used. The voltage used internally to set the current limit is the voltage between VCAP and ISET. An optional additional resistor from ISET to V_{IN} (or V_{OUT}) can be used to allow the current limit to inversely track V_{IN} (or V_{OUT}), providing an approximate system power limit.
2	ISTART	Start-Up Current limit. This pin allows a separate start-up current limit to be set for power-up modes. When powering up into large capacitive loads, it is desirable to keep the inrush current low and constant to minimize the SOA stress in the MOSFET. The ESTART pin limits the energy when using this mode. The ISTART pin sets the start-up current limit by using a divider from the VCAP pin, $V_{SENSECL} = V_{ISTART}/AV_{CSAMP}$, or if pulled up to VCAP with a 10 kΩ resistor, an internal 1 V threshold is used (25 mV). The start-up current limit is only active prior to PWGDIN being valid. The start-up current limit can also be lowered from the hardware setting over the PMBus with the STRT_UP_IOUT_LIM register. The start-up current limit = $V_{ISTART} \times$ (STRT_UP_IOUT_LIM/16). When using the DVDT pin to set the output voltage ramp, the ISTART pin can also be used as a backup protection feature, but it must be set to a current limit higher than the expected DVDT inrush.
3	VCAP	Internal Regulated 2.7 V Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain optimal voltage regulation. This pin can be used as a reference to program the ISET pin voltage. To guarantee accuracy specifications, do not load the VCAP pin by more than 100 µA.

Pin No.	Mnemonic	Description
4	ESTART	FET Energy Tracking During Power-Up. This pin approximates the energy in the FET during power-up. The user can place a component network between the ESTART pin and ground that allows the pin voltage to be proportional to the predicted MOSFET junction temperature. If the voltage on the pin exceeds a threshold (1 V), the FET is deemed to be running too close to its SOA and is turned off. This setting assumes lower current limits and greater SOA capability.
5	EFAULT	FET Energy Tracking During Normal Operation. This pin approximates the energy in the FET when faults occur during normal operation. The user can place a component network between the EFAULT pin and ground that allows the pin voltage to be proportional to the predicted MOSFET junction temperature. If the voltage on the pin exceeds a threshold (1 V), the FET is deemed to be running too close to its SOA and is turned off. This setting assumes higher current limits and lesser SOA capability. Considerations must be made if varying ISET with V_{IN}/V_{OUT} when assuming constant current limits.
6	ENABLE	Enable Input. This pin is a digital logic input. This input must be high to allow the ADM1272 hot swap controller to begin a power-up sequence. If this pin is held low, the ADM1272 is prevented from powering up.
7, 8	ADR0, ADR1	PMBus Address. These pins can be tied to GND, tied to VCAP, left floating, or tied low through a resistor for a total of 16 unique PMBus device addresses (see the Device Addressing section).
9	SCL	Serial Clock Pin. SCL is an open-drain input. It requires an external pull-up resistor.
10	SDAI	PMBus Serial Data Input. The serial data is split into an input and an output for easy use with isolators.
11	SDAO	PMBus Serial Data Output. The serial data is split into an input and an output for easy use with isolators.
12	MCB	Mask Circuit Breaker. When the voltage on this pin is greater than the threshold, the SOC shutdown is disabled. The function returns immediately after the voltage returns below this threshold.
13	GPIO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Input/Output 2 (GPIO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. It is also possible to read the state of this pin on the PMBus. This pin defaults to an alert output at power-up. There is no internal pull-up circuit.
14	GPIO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Input/Output 1 (GPIO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. It is also possible to read the state of this pin on the PMBus. This pin defaults to an alert output at power-up. There is no internal pull-up circuit on this pin.
15	$\overline{\text{FAULT}}$	Fault. This pin asserts low and latches when a fault occurs. The faults that can trigger this pin are an OC fault resulting in the EFAULT/ESTART threshold, an overtemperature fault, or a FET health fault.
16	$\overline{\text{RESTART}}$	Falling Edge Triggered Automatic Restart. The gate remains off for 10 sec by default, and then powers back on. The device has an internal weak pull-up circuit to VCAP. This pin is also used to configure the desired retry scheme. See the Hot Swap Retry section for additional details. The default time for this function is 10 sec. However, this time can be adjusted from 0.1 sec to 25.6 sec by writing to the RESTART_TIME register.
17	PWRGD	Power-Good Signal. This pin indicates that the supply is within tolerance (PWGIN input), no faults are detected, and the ADM1272 hot swap is enabled with the gate fully enhanced.
18	PWGIN	Power-Good Input Threshold. This pin sets the power-good input threshold. The user can set an accurate power-good threshold with a resistor divider from the source of the FET (VOUT). The PWRGD output signal is not asserted until the output voltage is above the threshold set by PWGIN.
19	GND	Ground.
20 to 24	NC	No Connect. The NC pins are not required to be connected, but do have internal connections. They share the same electrical node internally to the EPVCC pad and can therefore be used as a thermal exit route from EPVCC on the same outer layer and same electrical connection as EPVCC.
25 to 28, 33 to 37, 40	DNC	Do Not Connect. The DNC pins must not be connected to any electrical signal, GND, or supply voltage. Any connect copper must be electrically isolated and appropriately spaced from other nodes, which allows compliance with IPC-9592 recommendations for 80 V.

Pin No.	Mnemonic	Description
29	VCP	Internal Charge Pump Voltage Reservoir Capacitor. Connect a capacitor to VOUT to store energy required in the fast gate recovery mode. Ensure that the size of C_{VCP} is at least 10 times that of the parasitic gate capacitance. If C_{VCP} is greater than 500 nF, add additional delays to the initial power-on delay. See the FET Gate Drive section.
30	DVDT	Output Voltage Ramp Rate Setting. The DVDT pin sets a linear output voltage ramp rate. During power-up events, this pin is internally connected to the GATE pin. This internal connection allows the output voltage ramp to be predominately determined by I_{GATEUP} and C_{DVDT}. When the power-up is complete, the DVDT pin is disconnected from the GATE pin and connected to VOUT to prevent impeding the GATE shutdown time. A 20 kΩ resistor must be used in series with the capacitor to limit pin currents during fast transients on VOUT. Use a high voltage capacitor.
31	VOUT	Output Voltage. Connect this pin directly to the source of the MOSFET (output voltage). The GATE pin is referenced from this node and pull-down currents flow through this pin. PCB routing must be sized accordingly to allow all GATE shutdown currents. This pin is also used to read back the output voltage using the internal ADC. It also enables V_{DS} monitoring across the MOSFET to feed back to the SOA protection scheme.
32	GATE	Gate Driver. This pin is the high-side gate drive of an external N channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held to the VOUT pin when the supply is below the UVLO threshold.
38	SENSE−	Negative Current Sense Input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1272 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.
39	SENSE+	Positive Current Sense Input. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1272 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also measures the supply input voltage using the ADC.
41	VCC	Positive Supply Input. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, the voltage on this pin must remain greater than or equal to SENSE+ to ensure that specifications are adhered to. No sequencing is required.
42	VREG	Internal Regulated 5 V Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain optimal regulation. Do not load this pin externally.
43	TEMP−	Temperature Input GND. Connect this pin directly to the low side of the NPN device.
44	TEMP+	Temperature Input. An external NPN device can be placed close to the MOSFETs and connected back to this pin to report the temperature. The voltage at the TEMP+ pin is measured by the ADC.
45	UVH	Undervoltage Rising Input. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UVH limit.
46	UVL	Undervoltage Falling Input. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UVL limit.
47	OV	Overvoltage Input. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
48	RND	Random Delay. A capacitor on this pin sets the minimum and maximum power-up delay time range. With no capacitor on this pin, the system delay is from 0.43 ms to 27.5 ms. With a maximum of 220 nF, the delay can be from 54.3 ms to 3.0 sec. This delay is active only after VCC comes out of UVLO and, therefore, is only present at each power cycle.
	EPGND	Exposed Pad. Always connect to GND. The exposed pad is located on the underside of the LFCSP package and is the larger of the two pads. Solder the exposed pad to the PCB for optimal thermal dissipation.
	EPVCC	Exposed Pad. Internally connected to VCC. The exposed pad is located on the underside of the LFCSP package and is the smaller of the two pads. Solder the exposed pad to the PCB for optimal thermal dissipation. Always electrically connect EPVCC to the same potential as VCC. Most of the device power is dissipated through this pad; therefore, consider a strong thermal connection to available copper.

TYPICAL PERFORMANCE CHARACTERISTICS

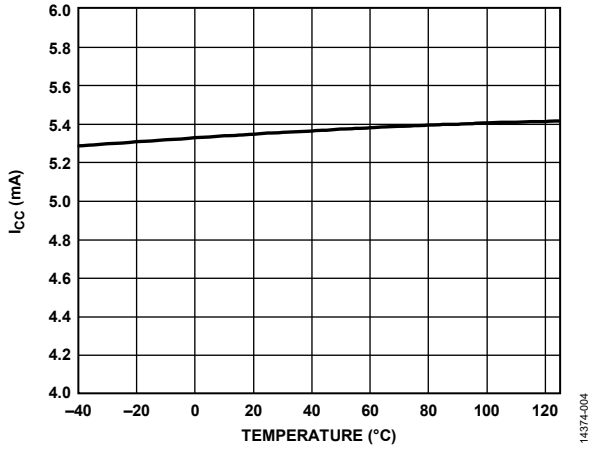


Figure 4. Supply Current (I_{CC}) vs. Temperature

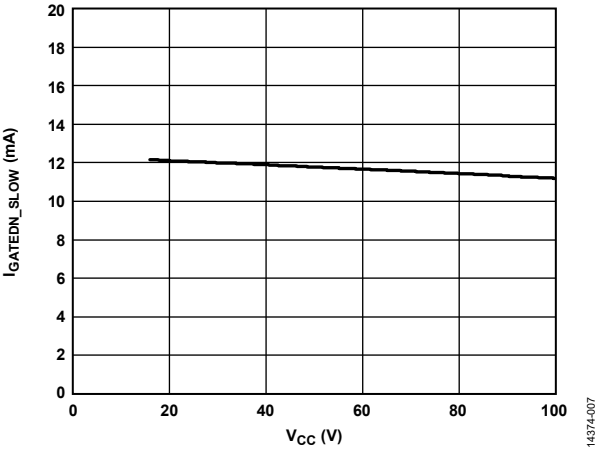


Figure 7. GATE Slow Pull-Down Current (I_{GATEDN_SLOW}) vs. V_{CC}

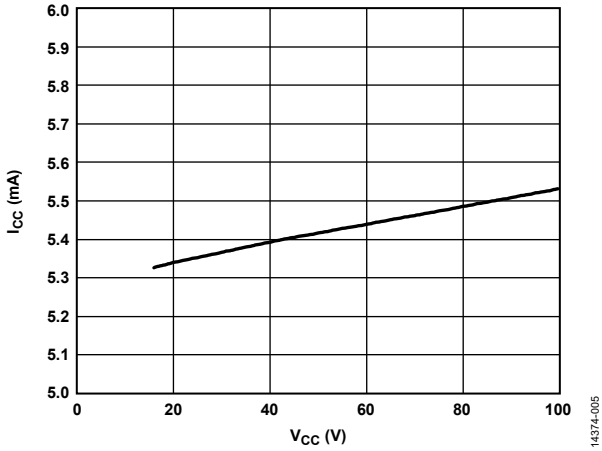


Figure 5. Supply Current (I_{CC}) vs. V_{CC}

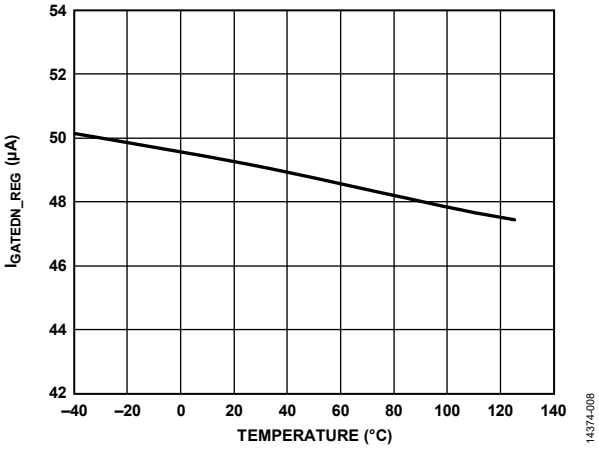


Figure 8. GATE Regulation Pull-Down Current (I_{GATEDN_REG}) vs. Temperature

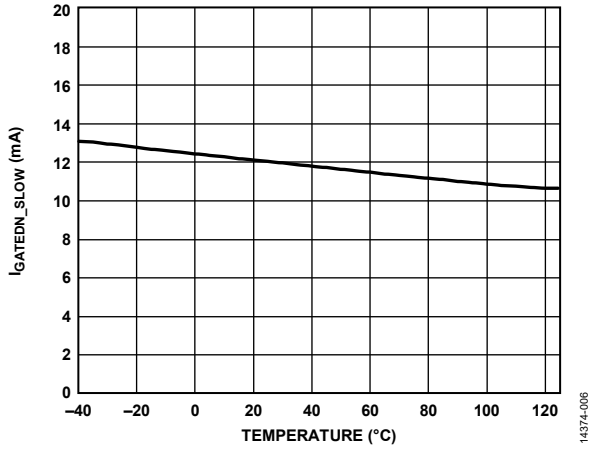


Figure 6. GATE Slow Pull-Down Current (I_{GATEDN_SLOW}) vs. Temperature

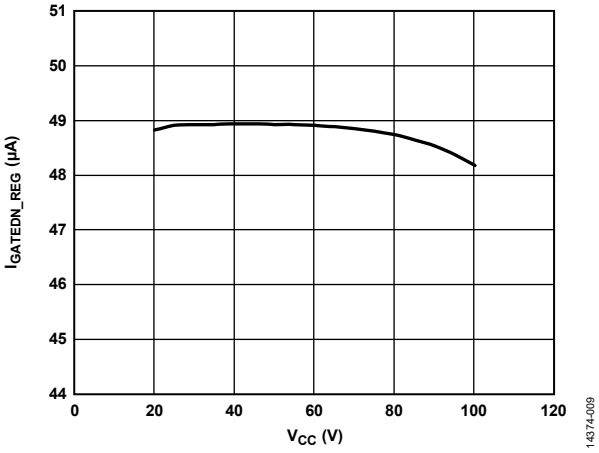


Figure 9. GATE Regulation Pull-Down Current (I_{GATEDN_REG}) vs. V_{CC}

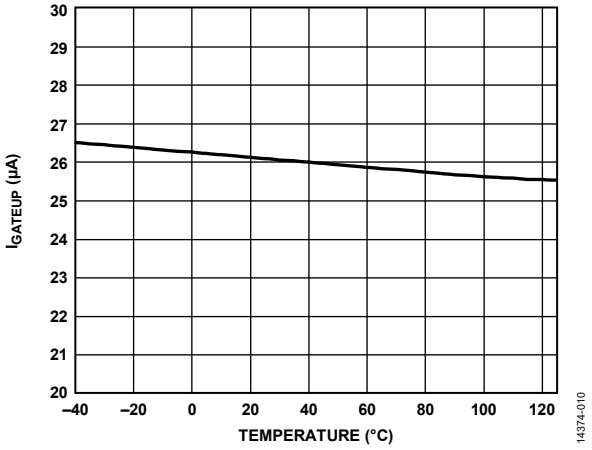


Figure 10. GATE Pull-Up Current (I_{GATEUP}) vs. Temperature

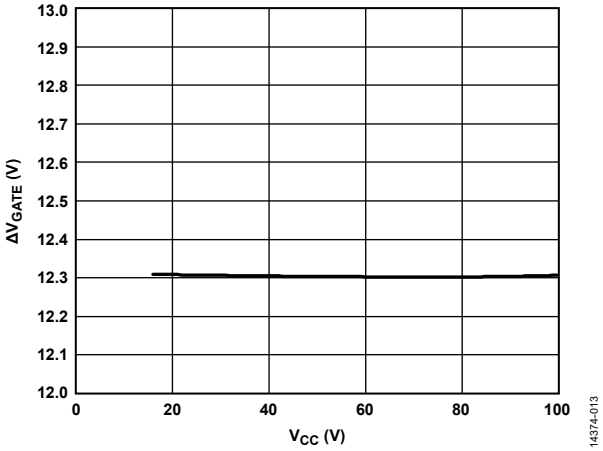


Figure 13. V_{GATE} (5 µA Load) vs. V_{CC}

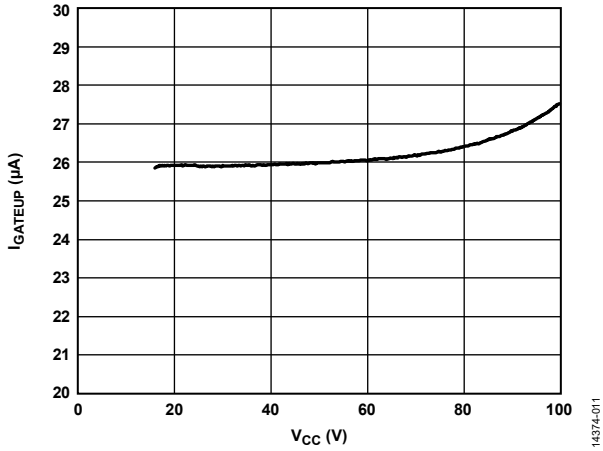


Figure 11. GATE Pull-Up Current (I_{GATEUP}) vs. V_{CC}

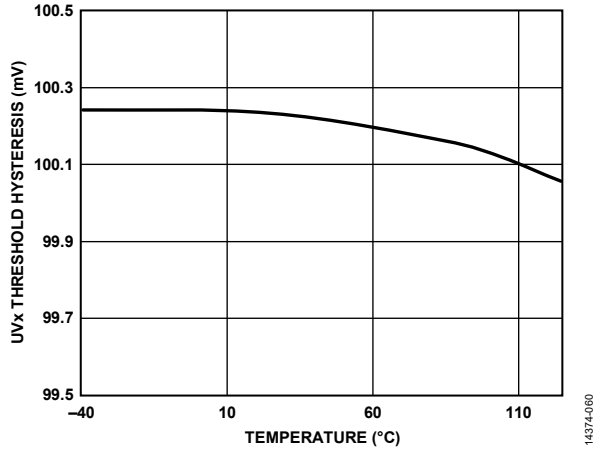


Figure 14. UVx Threshold Hysteresis vs. Temperature

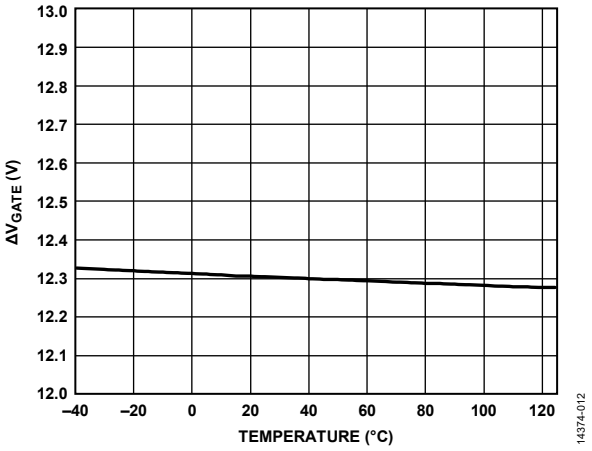


Figure 12. ΔV_{GATE} (5 µA Load) vs. Temperature

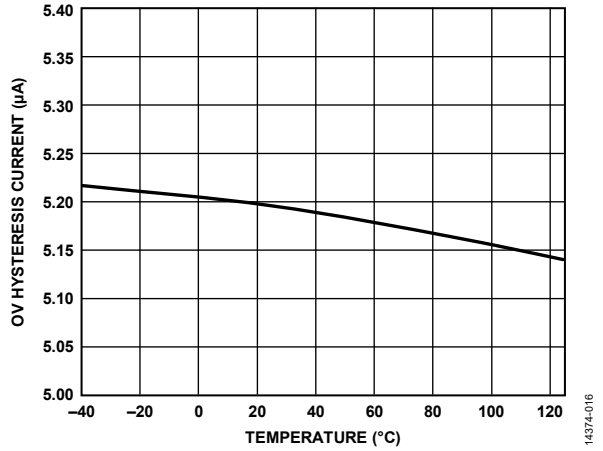


Figure 15. OV Hysteresis Current vs. Temperature

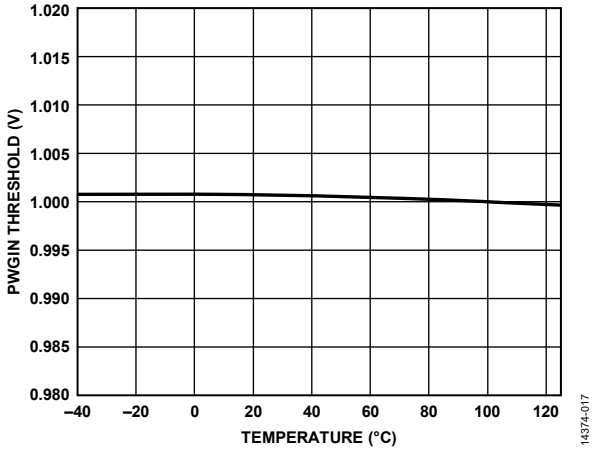


Figure 16. PWGIN Threshold vs. Temperature

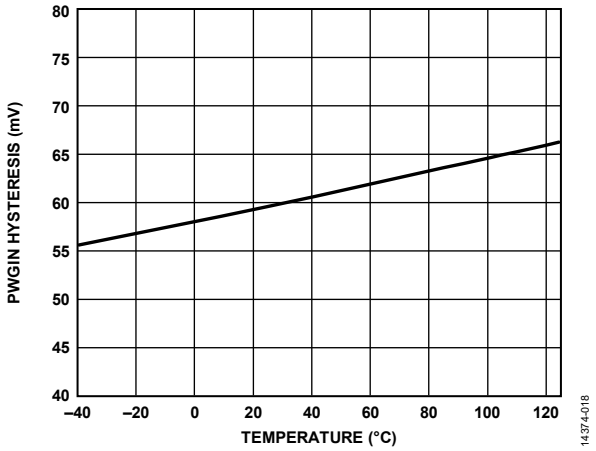


Figure 17. PWGIN Hysteresis vs. Temperature

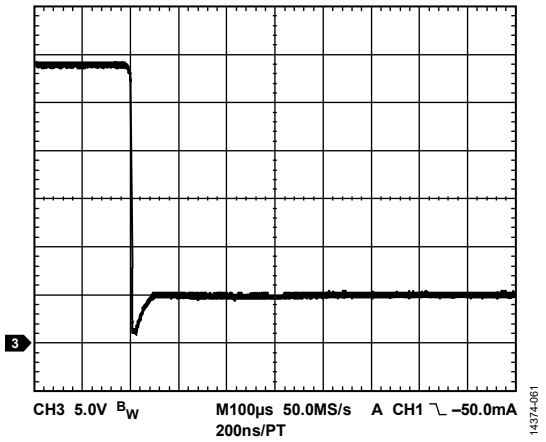


Figure 18. VGATE Response to Severe Overcurrent Event (GATE Fast Pull-Down)

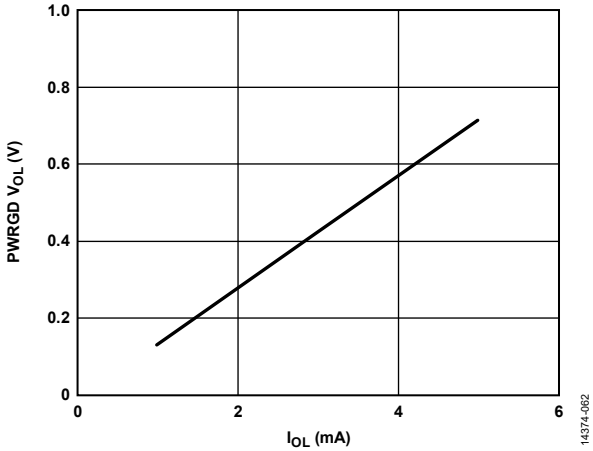


Figure 19. PWRGD V_{OL} vs. I_{OL}

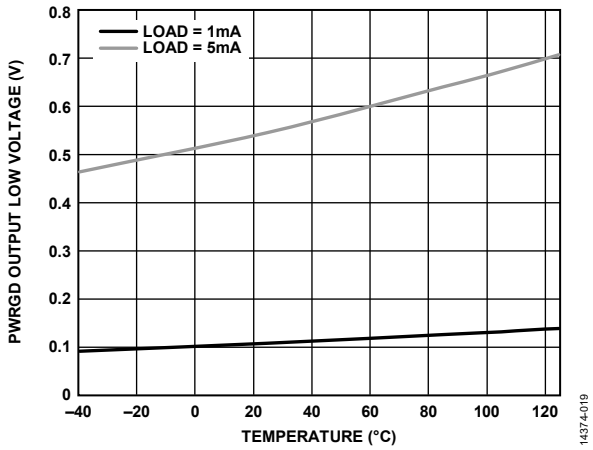


Figure 20. PWRGD Output Low Voltage (V_{OL}) vs. Temperature

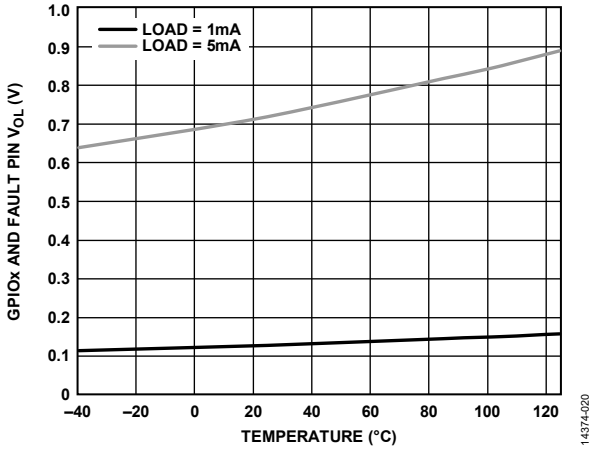


Figure 21. GPIOx and Fault Pin V_{OL} vs. Temperature

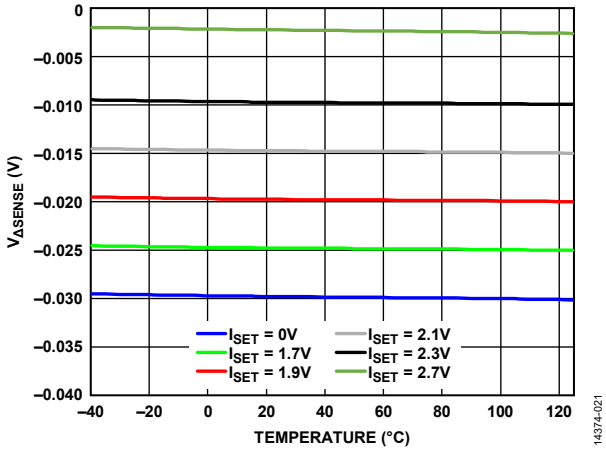


Figure 22. $V_{\Delta SENSE}$ vs. Temperature, V_{ISET} with 1 Ω Sense Resistor

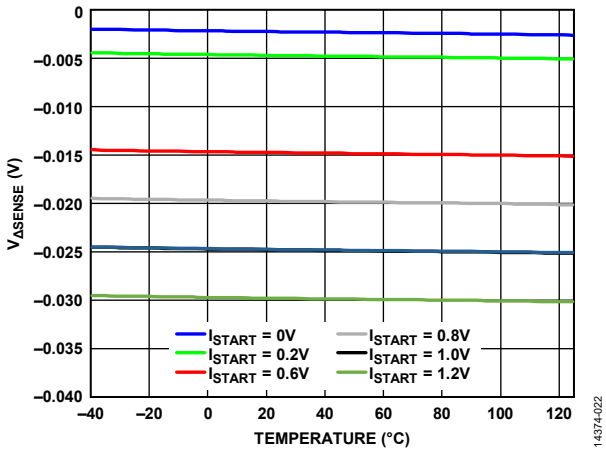


Figure 23. $V_{\Delta SENSE}$ vs. Temperature, V_{ISTART} with 1 Ω Sense Resistor

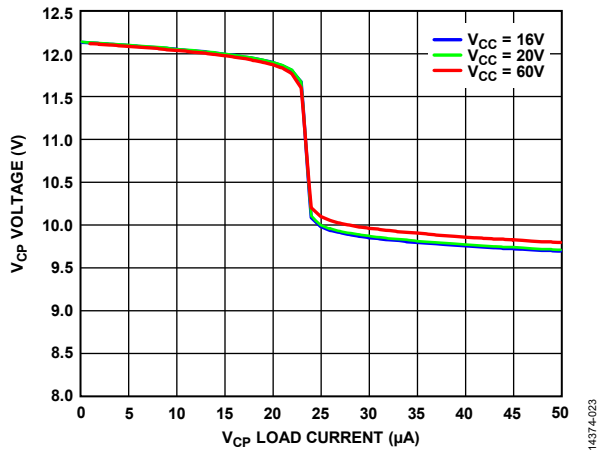


Figure 24 V_{CP} Load Regulation

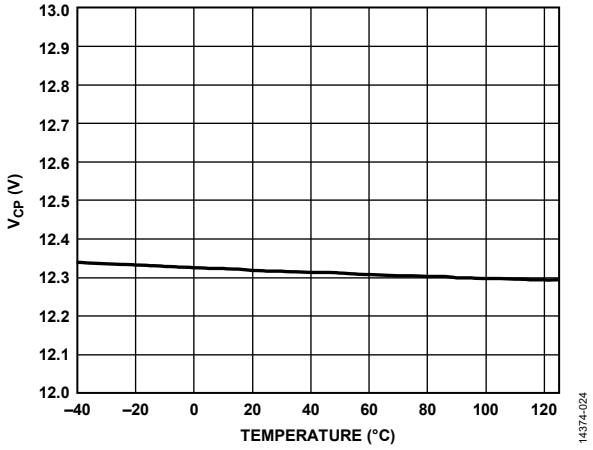


Figure 25. V_{CP} vs. Temperature

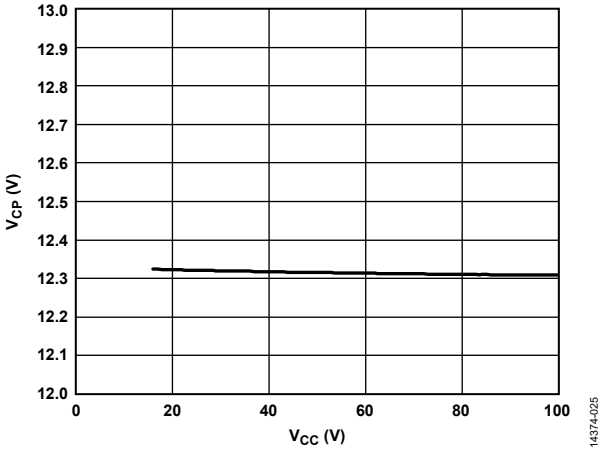


Figure 26. V_{CP} vs. V_{CC}

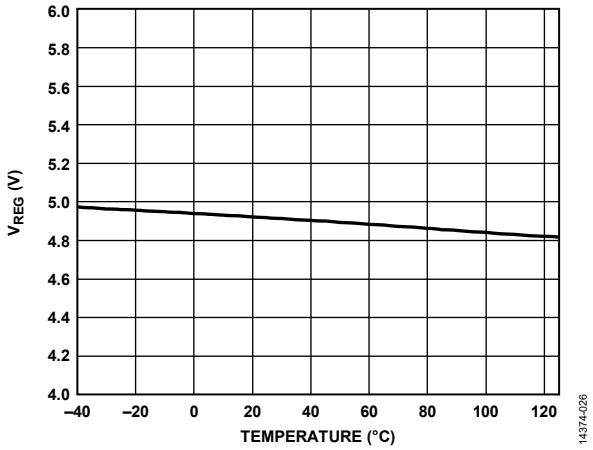


Figure 27. V_{REG} vs. Temperature

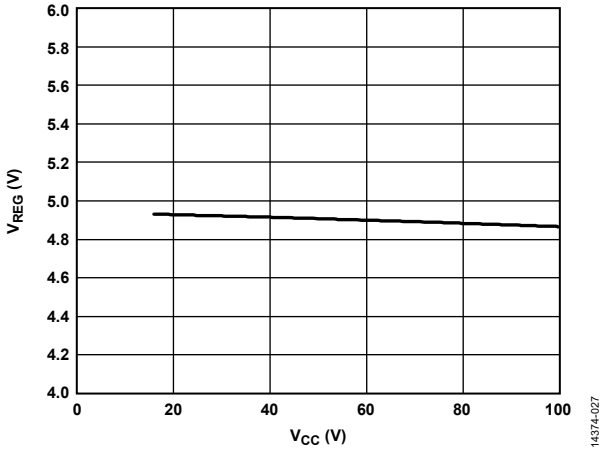


Figure 28. V_{REG} vs. V_{CC}

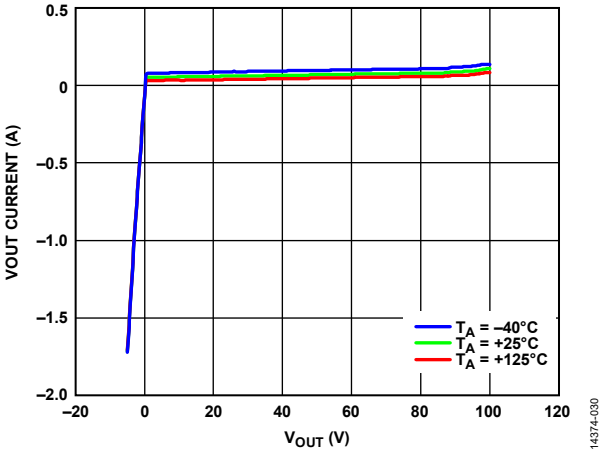


Figure 31. VOUT Current vs. V_{OUT}

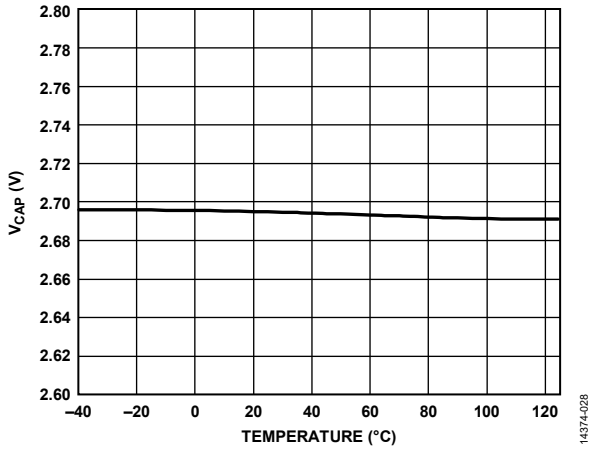


Figure 29. V_{CAP} vs. Temperature

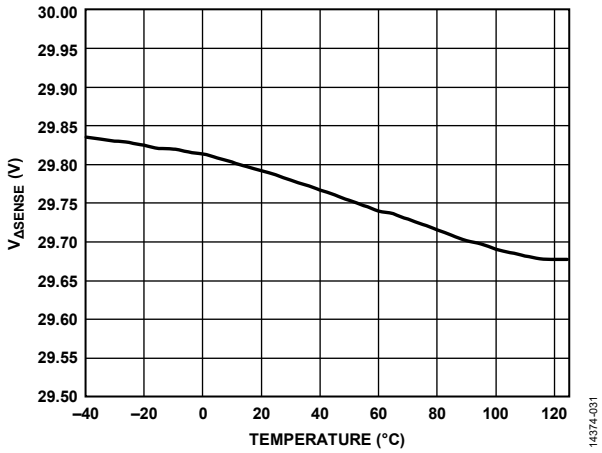


Figure 32. $V_{\Delta SENSE}$ vs. Temperature at ISET = 0

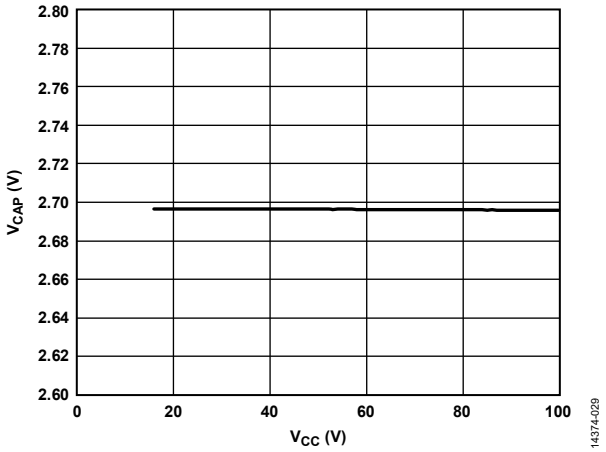


Figure 30. V_{CAP} vs. V_{CC}

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1272 is designed to manage the powering on and off of a system in a controlled manner, allowing a board to be removed from, or inserted into, a live backplane by protecting it from excess currents. After power-up is complete, the ADM1272 continues to protect the system from faults. These faults include overcurrent, short circuit, overvoltage, undervoltage, and transient disturbances on the backplane, and some FET fault issues. The ADM1272 is usually placed on a system/board that is removable. However, it also can be placed on the backplane in some cases. The ADM1272 also has the capability of measuring and reporting power and energy telemetry.

POWERING THE ADM1272

A supply voltage from 16 V to 80 V is required to power the ADM1272 via the VCC pin. An internal regulator provides a 5 V rail, which is presented on the VREG pin, to supply the digital section of the ADM1272 (for internal use only), and must be decoupled according to the VREG pin description in Table 6.

The VCC pin provides the majority of the bias current for the device; however, some bias currents are supplied through the SENSE± pins. Both the VCC and SENSE+ pins can be connected to the same voltage node, but in most applications, it is recommended to connect an RC filter to the VCC pin to avoid resets due to very fast transients on the input rail (see Figure 33).

Choose the values of these components such that a time constant is provided that can filter any expected glitches. However, use a resistor that is small enough to keep voltage drops caused by quiescent current to a minimum. Do not place a supply decoupling capacitor on the rail before the FET, unless a series resistor is used to limit the inrush current.

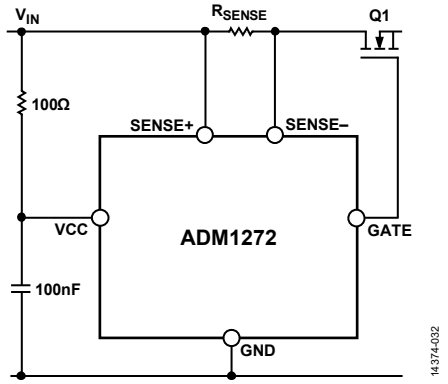


Figure 33. Reinforced Transient Glitch Protection Using an RC Network

UV AND OV

The ADM1272 monitors the supply voltage for UV and OV conditions. The OV pin is connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 1 V voltage reference. The user can program the value of the OV hysteresis by varying the top resistor of the resistor divider on the pin. This impedance in combination with the 5 µA OV hysteresis current (current turned on after OV triggers) sets the OV hysteresis voltage.

$$OV_{RISING} = OV_{THRESHOLD} \times \frac{R_{TOP} + R_{BOTTOM}}{R_{BOTTOM}}$$

$$OV_{FALLING} \approx OV_{RISING} - (R_{TOP} \times 5\ \mu A)$$

The UV detector is split into two separate pins, UVH and UVL. The voltage on the UVH pin is compared internally to a 1 V reference, whereas the UVL pin is compared to a 0.9 V reference. Therefore, if the pins are tied together, the UV hysteresis is 100 mV. The hysteresis can be adjusted by placing a resistor between UVL and UVH.

Figure 1 shows the voltage monitoring input connection. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UVL pin falls below 0.9 V, and the gate is shut down using the 10 mA pull-down device. The fault is cleared after the UVH pin rises above 1.0 V.

Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the gate is shut down using the 10 mA pull-down device.

For the maximum rating on the UVx and OV pins, see Table 4. If transients are expected on the main input line, use external protection circuitry to protect the inputs and to allow these pin voltages to exceed their rating.

HOT SWAP CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE}. An internal current sense amplifier provides a gain of 40 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and used by the hot swap control logic to detect when an overcurrent condition occurs.

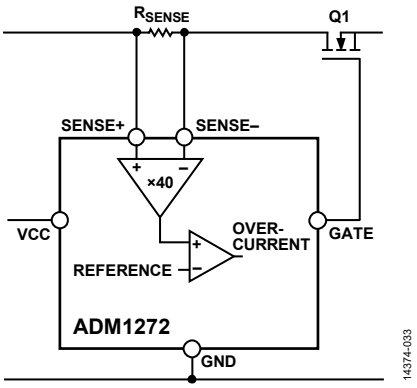


Figure 34. Hot Swap Current Sense Amplifier

The SENSE± inputs can be connected to multiple parallel sense resistors. The way the sense points of these resistors are combined has a significant effect on the accuracy of the voltage drop detected by the ADM1272.

To achieve better accuracy, averaging resistors can be used to sum the voltages from the nodes of each sense resistor, as shown in Figure 35. A typical value for the averaging resistors is 10 Ω, enough to be significantly greater than the trace resistance. The input current to each sense pin is matched to within 5 μA. This matching ensures that the same offset is observed by both sense inputs, reducing differential errors.

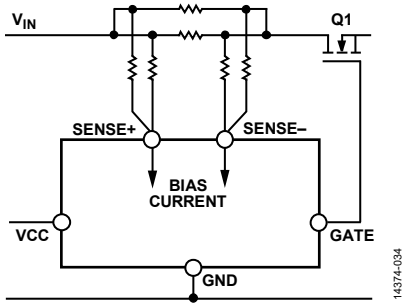


Figure 35. Connection of Multiple Sense Resistors to the SENSE± Pins

CURRENT-LIMIT MODES

The ADM1272 features dual current limits, one for startup (ISTART) and one for normal operation (ISET). At startup, the ISTART pin determines the current limit used during power-up. This dual current limit allows users to program an independent current limit at startup, specific to the conditions of the start-up profile and expectations. After startup is complete, the system switches to the main current limit determined by ISET. The conditions that must be satisfied for this switch to occur are as follows:

- The system is not in current limit.
- (V_{OUT} − V_{IN}) < 2 V.
- The gate voltage is fully enhanced (V_{GS} > 10 V).

The system remains at the normal current limit (ISET) unless there is an interruption triggered by an OV, UV, or manual shutdown (enable, restart, or PMBus command) and this interruption results in V_{DS} > 2 V and inactive PWRGD. If this interruption occurs, the system resets to ISTART and assumes a full system restart. For this reset to happen, a shutdown must be signaled with enough time to allow the gate to disable the FETs and the output to discharge. However, the system remains in ISET current limit following an OC fault to allow a recovery attempt. If the system cannot recover, a latchoff occurs and ISTART assumes control at the next startup.

SETTING THE CURRENT LIMITS (ISET/ISTART)

The current limit is typically determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor requirements become smaller, and resolution can be difficult to achieve when selecting the appropriate sense resistor or combination thereof. The ADM1272 provides adjustable current sense voltage limits to manage this issue. The device allows the user to program the required current sense voltage limits independently up to 30 mV. The recommended range is 2.5 mV to 30 mV, although tolerances and errors increase as $V_{SENSECL}$ decreases.

In conjunction with the sense resistor, the current-limit reference voltage determines the load current level to which the ADM1272 limits the current during an overcurrent event. This reference voltage is compared to the amplified current sense voltage to determine whether the limit is reached.

The active current-limit reference voltage input to the internal comparator is clamped to a minimum level of 100 mV (that is, $V_{SENSECL}$ = 2.5 mV) to prevent current limits being set too low, which may result in zero current flow across all conditions.

The current limit set by the ISET/ISTART pins is the current at which the ADM1272 tries to regulate when the load requires more current. This current limit, defined by the reference to the current control loop, is the regulation current limit or I_{REG} ($V_{SENSECL}$ at the sense voltage).

Another current-limit threshold just below I_{REG} that alerts the ADM1272 when the current limit is reached and is active, is the circuit breaker current limit or I_{CB} (V_{CB} at sense voltage). V_{CB} can be expressed at the sense pins (in mV) as follows:

$$V_{CB} = V_{SENSECL} - V_{CBOS}$$

where V_{CBOS} is the circuit breaker offset and is listed in Table 1 as 1.1 mV (typical).

ISTART

The ISTART pin sets the start-up current limit in start-up mode using a divider from the VCAP pin, or if pulled up to VCAP with a 10 kΩ resistor, an internal 1 V threshold is used (25 mV).

The VCAP pin has a 2.7 V internal regulated voltage that can be used as a reference to set a voltage at the ISTART pin. Assuming that V_{ISTART} equals the voltage on the ISTART pin, size the resistor divider to set the ISTART voltage as follows:

$$V_{ISTART} = V_{SENSECL} \times 40$$

where $V_{SENSECL}$ is the current sense voltage limit.

The default value of 25 mV is achieved by connecting the ISTART pin directly to the VCAP pin (or V_{ISTART} > 1.65 V). This connection configures the device to use an internal 1 V reference, which equates to 25 mV at the sense inputs (see Figure 36).

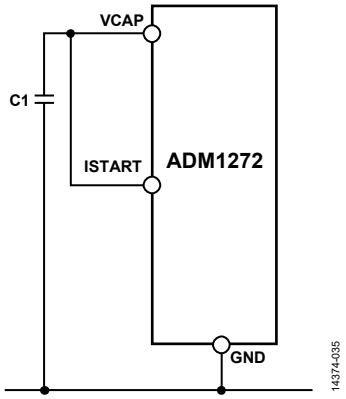


Figure 36. Fixed 25 mV ISTART Current Sense Limit

To program the sense voltage from 10 mV to 30 mV, a resistor divider sets the reference voltage on the ISTART pin (see Figure 37).

When using the DVDT pin to set the output voltage ramp, set the ISTART pin high enough to prevent the inrush current from reaching the current limit.

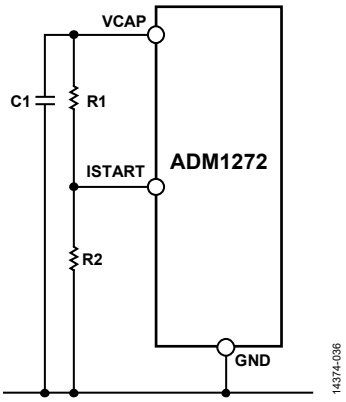


Figure 37. Adjustable 5 mV to 30 mV Current Sense Limit

The start-up current limit can be programmed via the ISTART pin or reduced via the PMBus register, STRT_UP_IOUT_LIM (Register 0xF6). If both are configured, the lowest current limit is selected as the active current limit. The clamp level in both cases is a 2.5 mV $V_{\Delta SENSE}$ current limit.

The start-up current limit PMBus register is set to the maximum value at power-on reset; therefore, the ADM1272 uses the ISTART pin setting by default.

If configuring the start-up current limit with the PMBus register, the start-up current limit is set as a fraction of the effective ISTART current limit. There are four register bits so that the start-up current limit can be set from 1/16th to 16/16th of the normal current limit. The effective ISTART voltage can be calculated as

$$V_{ISTART} = (V_{VCAP} - V_{ISET}) \times \left(\frac{STRT_UP_IOUT_LIM + 1}{16} \right)$$

The start-up circuit breaker and current limits can then be calculated from this effective ISTART voltage.

ISET

The ISET pin sets the system current limit during normal operation using a divider from the VCAP pin or pulled down to GND. The ISET pin differs from ISTART in that the resulting current-limit reference voltage is not the voltage presented on the pin, but the difference between VCAP and ISET. This relationship is presented as follows:

$$V_{VCAP} - V_{ISET} = V_{SENSECL} \times 40$$

where $V_{SENSECL}$ is the current sense voltage limit.

This configuration allows a third optional resistor (from ISET to V_{IN}) to be used to allow the current limit to inversely track the input voltage. This feature is useful to avoid overdesigning the system current limit and allows the maximum current demand to output load at low V_{IN}, which results in an unnecessarily high current limit for maximum V_{IN}. The high current limit may even exceed input power limitations.

The default value of 30 mV is achieved by pulling the ISET pin directly to GND (or V_{ISET} < 1.5 V). Although the ISET pin may be at 0 V, the internal buffered ISET voltage does not drop below 1.5 V. This configuration clamps the current-limit reference voltage to 1.2 V ($V_{VCAP} - V_{ISET}$), which equates to 30 mV at the sense inputs (see Figure 38).

For information about the protection of the FET SOA, see the Safe Operating Area Protection (ESTART/EFAULT) section.

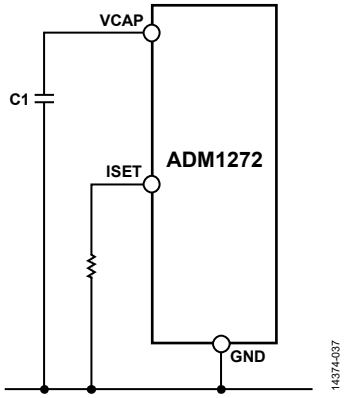


Figure 38. Fixed 30 mV ISET Current Sense Limit

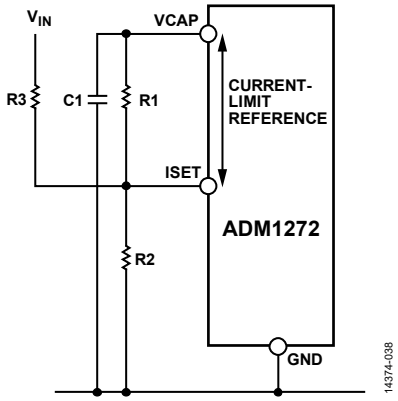


Figure 39. Programming the Variable Current Sense Limit (R3 for Power Limit Setting)

SETTING A LINEAR OUTPUT VOLTAGE RAMP AT POWER-UP (DVDT)

The most common method of power-up in a typical application is to configure a single linear voltage ramp on the output, which allows a constant inrush current into the load capacitance. This method has the advantage of setting slow ramp times, which result in low inrush currents. This method is often required to limit supply inrush demand and to prevent high capacitive loads from stressing the FET SOA.

This design allows a linear monotonic power-up event without the restrictions of the system current limit or fault timer. A power-up ramp is set such that the inrush is low enough not to reach the active circuit breaker current limit, which allows the power-up to continue without any closed-loop interaction but still uses the active current limit to protect against fault conditions. A capacitor on the DVDT pin sets the dv/dt ramp rate of the output voltage. However, the parasitic FET gate capacitances also contribute to the total gate capacitance and must be considered.

The DVDT pin is internally connected to the GATE pin only during start-up mode. When the startup is complete, the DVDT pin is disconnected from the GATE pin and connected internally to VOUT. This configuration prevents unnecessary capacitive loading of GATE, which can slow shutdown responses to faults and impede recovery from transient conditions. The DVDT pin is reconnected to GATE prior to any subsequent start-up events.

To ensure that the inrush current does not approach or exceed the active current-limit level, the output voltage ramp can be set by selecting the appropriate value for C_{DVDT}, as follows:

$$C_{DVDT} = (I_{GATEUP}/I_{INRUSH}) \times C_{LOAD}$$

where:
C_{DVDT} is the total gate capacitance (including FET parasitics).
I_{GATEUP} is the specified gate pull-up current.
C_{LOAD} is the load capacitance.

Add margin and tolerance as necessary to ensure a robust design. Subtract any parasitic gate drain capacitance, C_{GD}, of the MOSFETs from the total to determine the additional external capacitance required.

Next, the power-up ramp time can be approximated by

$$t_{RAMP} = (V_{IN} \times C_{LOAD})/I_{INRUSH} = (V_{IN} \times C_{DVDT})/I_{GATEUP}$$

Check the SOA of the MOSFET for conditions and the duration of this power-up ramp. For more information about protection of the FET SOA during start-up faults, see the information about the protection of the FET SOA, see the Safe Operating Area Protection (ESTART/EFAULT) section.

The diagram in Figure 40 shows a typical hot swap power-up with a DVDT capacitor configured for a linear output voltage ramp.

The ISTART current limit can also be used to provide a constant current instead of using the DVDT pin. However, if linear output voltage ramps are preferred, use of the DVDT function is recommended with an ISTART level above any expected inrush current profiles as protection. Loads can often require dynamic currents, which may result in nonlinear profiles when using a constant current control at startup. In addition, if very low current limits are required (in comparison to the main current limit), using a closed-loop system may result in wide tolerance and/or current limits below the recommended range of V_{SENSE}.

When configuring with the ISTART pin, calculate the circuit breaker (CB) level using the following equation:

$$Start\text{–}Up\ CB = \frac{\left(\frac{V_{ISTART}}{40} - 1.1\,\text{mV}\right)}{R_{SENSE}}$$

To prevent the start-up current limit from being triggered during a normal slew rate controlled power-up, set the circuit breaker level above the maximum expected inrush current.

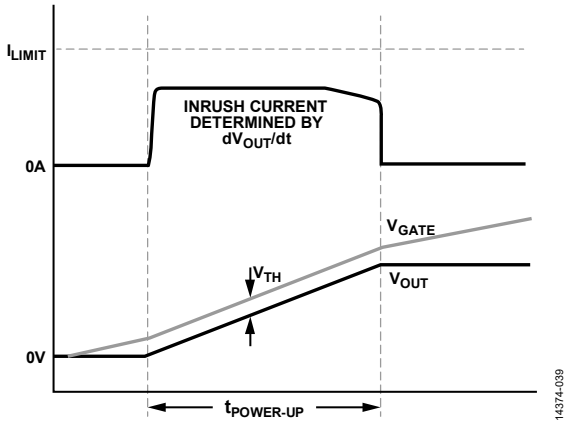


Figure 40. Linear Voltage Ramp Power-Up

SAFE OPERATING AREA PROTECTION (ESTART/EFAULT)

The ADM1272 features an FET protection scheme that offers increased flexibility for managing various system conditions while still protecting the FET from SOA stress.

Traditional timer schemes uses a single fault timer to protect the FET when regulating current or when current limits are exceeded. This approach requires the timers to be set to worst case conditions like short circuits, which limits the robustness of the solution to various system conditions/faults.

For short circuits, the SOA requires the setting of a short timer because the FET V_{DS} is very high. However, for a load fault that results in only a few volts across the FET V_{DS}, because the timer is optimized for worst case conditions, the timer setting remains very short. If a transient fault occurs, resulting in a momentary active current limit but only a few volts of V_{DS}, the system is likely to shut down quickly even though the FET SOA is not exceeded because V_{DS} is low and can operate longer. This condition is problematic during common scenarios such as input line steps and disturbances.

To accommodate these conditions and ensure there are no unnecessary shutdowns, the ADM1272 monitors and uses the FET V_{DS} to optimize how long the FET is allowed to remain in regulation. The ESTART and EFAULT pins control this regulation time for start-up mode and normal mode, respectively. Each pin programs an independent setting for each mode of operation to allow SOA protection to be optimized for its respective current limit. As the system transitions from one mode to another, the ADM1272 retains any potential recent SOA stress history by copying the same voltage from the ESTART pin to the EFAULT pin at transitions and vice versa.

The assumption is that, although there is a significant level of V_{DS} across the FET, its drain current, I_D, is being held constant (at the limit); thus, the FET power is proportional to V_{DS}. The SOA curve of the FET indicates the amount the FET can dissipate, for a given time, before the junction temperature reaches its maximum and SOA is breached. A current source (I_{VDS}) equivalent to 1 µA per 1 V V_{DS} is sourced from EFAULT/ESTART. Through analysis and manipulations of the SOA curves, for a given fixed current, an RC configuration from EFAULT/ESTART to GND can provide a solution to ensure the voltage on the pin reaches 1 V before the SOA is exceeded. This configuration presents a profile on the EFAULT/ESTART pin that is representative of the FET junction temperature. Upon reaching 1 V, the device deems the FET to be at the SOA limit and latches off. This solution results in fault on times that are proportional to V_{DS} and allows low V_{DS} faults to recover without latching off, while ensuring high V_{DS} faults are latched off immediately.

Although the EFAULT and ESTART pins provide the same function for their respective operation mode, there is one subtle difference: the ESTART pin enables I_{VDS} only when the current exceeds I_{CB}, whereas the EFAULT I_{VDS} is solely dependent on V_{DS}.

A pull-down current of 500 nA discharges the RC network, which allows a single capacitor on each pin to be used at the expense of being able to use less of the SOA. When the current control loop is near regulation, this 500 nA pull-down current is disabled and a 1 µA pull-up current enabled. The 1 µA current ensures that the EFAULT and ESTART pins run current even if there is a very small V_{DS}, thus allowing the system to power down if this condition lasts for an extended period. If conditions prevent the pins from reaching 1 V while at a low V_{DS} (where the SOA may indicate dc), there is an internal 100 ms limit, after which the system returns a fault and latches off. This backup limit prevents overheating in a steady state in the MOSFET. The 100 ms timer runs when V_{GS} is <10 V and the current is in regulation.

FET GATE DRIVE

The ADM1272 is designed to control a high-side gate drive of an external N channel FET. The GATE pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held to the VOUT pin when the supply is below the UVLO limit.

The GATE pin features a G_M amplifier output that sources and sinks the GATE node to regulate the current. When a shutdown is requested, the GATE pin uses a 10 mA pull-down device to disable the FET and this pull-down device remains active when the FET is disabled.

The charge pump used on the GATE pin is capable of driving V_{GS} to >10 V, but it is clamped to less than 14 V above VOUT. These clamps ensure that the maximum V_{GS} rating of the FET is not exceeded.

FAST RESPONSE TO SEVERE OVERCURRENT

The ADM1272 features a separate high bandwidth current sense amplifier that detects a severe overcurrent indicative of a short-circuit condition. A fast response time allows the ADM1272 to handle events of this type that may otherwise cause catastrophic damage if not detected and prevented quickly. The fast response circuit ensures that the ADM1272 can detect an overcurrent event at approximately 150% to 400% (default 200%) of the normal current limit set by the ISET pin, and can respond to and control the current within 1 µs in most cases.

There are four severe overcurrent threshold options and four severe overcurrent glitch filter options selectable via the PMBus registers as follows:

- Thresholds: 150%, 200%, 300%, 400%
- Glitch filters: 500 ns, 1 µs, 5 µs, 10 µs

The GATE pin of the ADM1272 is pulled down with ~1.5 A for a maximum duration of 10 µs. Following a severe OC shutdown, by default, the device attempts to regain control of the FET one time. To expedite recovery after sudden shutdown events, a gate boost circuit is enabled to bring the gate voltage back to

the FET V_{TH} threshold within ~50 µs. After the current sense amplifier detects 2 mV at the sense pins, this circuit is disabled and the normal gate drive resumes.

MCB

The MCB pin (mask circuit breaker) is designed to mask the severe overcurrent circuit, when enabled. If the voltage on this pin exceeds the threshold, the severe OC detector is disabled for the duration, which disables the large GATE pull-down circuit while the pin is high. All other protection features remain intact.

RND

The RND pin allows the user to insert a random delay into the start-up routing, which allows staggered distribution of power-up on multiple systems, when commanded simultaneously. Allow this pin to float when not in use. There is a maximum timeout feature of 3 sec to prevent faulty capacitors from impeding a startup.

Table 7. Typical Delay Time with External Capacitor

RND Capacitor	Minimum Time	Maximum Time
None (~10 pF)	0.43 ms	27.5 ms
4.7 nF	1.58 ms	101 ms
10 nF	2.88 ms	184 ms
22 nF	5.82 ms	372 ms
47 nF	11.9 ms	764 ms
100 nF	24.9 ms	1.59 sec
220 nF	54.3 ms	3.0 sec[1, 2]

[1] The discharge time is fixed; capacitors larger than 220 nF may not be fully discharged during the discharge cycle. Therefore, the delay time is not proportional to the capacitance for capacitors larger than this value.
[2] Limited by internal timeout of 3 sec to prevent faulty capacitors on the RND pin from impeding a startup.

VOLTAGE TRANSIENTS

System backplanes are subject to transients. Transients commonly occur following a fast shutdown on a system running high currents. The source inductance results in a fast dv/dt on the input and the load inductance may result in a negative voltage transient at VOUT. It is critical to use appropriately rated TVS diodes on the input and Schottky diodes on the output. The ADM1272 can tolerate 120 V at the input pins and −5 V at the VOUT pin.

SURGE AND TRANSIENT RECOVERY

Surges, line steps, and backplane disturbances are sometimes unavoidable in a system chassis backplane. Usually such events result in a fast dv/dt on the input supply, which in turn causes a sudden inrush current demand on the positive edge. This sudden inrush current is almost identical to a current spike seen during an output fault condition and is therefore always difficult to differentiate and manage without resulting in a system reset.

The ADM1272 uses a number of features designed to address this issue. Many existing solutions rely on masking the severe overcurrent feature and allowing the inrush current to pass. The ADM1272 features an MCB pin for just that function. However, using the MCB pin is not the preferred course of action because it often results in very high currents flowing uninterrupted in the system, which can lead to other issues.

The primary features to address such power line disturbances are as follows:

- Fast recovery allows the inrush current to trigger the severe overcurrent and shuts down the FET quickly to limit the high peak currents from flowing in the system. However, after shutdown, recover the current control quickly so that the output load capacitors do not discharge with the load demand. This recovery is achieved via a gate drive boost circuit designed to deliver extra charge into GATE until the FET is reenabled.
- Isolated DVDT capacitor that controls the gate ramp voltage is disconnected during this recovery, allowing the FET to recover faster.
- No current foldback. If the load is demanding full current during this event, the current limit cannot be reduced without impeding recovery. Instead, the FET on time is managed to ensure SOA protection.
- EFAULT function. This feature replaces the typical timer function. It can be optimized to allow the FET to remain on for longer with lower V_{DS} faults, which is typical in these scenarios.

The combination of these features allows the ADM1272 to maintain the output voltage and prevent system resets during these transients events, while still protecting the MOSFETs.

POWER GOOD

The power-good (PWRGD) output indicates whether the output voltage is above a user defined threshold and can, therefore, be considered good. A resistor divider on the PWGIN pin sets an accurate power-good threshold on the output voltage.

The PWRGD pin is an open-drain output that pulls low when the voltage at the PWGIN pin is lower than 1.0 V (power bad). When the voltage at the PWGIN pin is above this threshold plus a fixed hysteresis of 60 mV, the output power is considered to be good.

However, PWRGD asserts only when the following conditions are met:

- PWGIN is above the rising threshold voltage.
- Hot swap is enabled, that is, the ENABLE pin is high and the UVx and OV pins are within range.
- There is no active fault condition, that is, the $\overline{\text{FAULT}}$ pin is cleared following any fault condition.
- The MOSFET is fully enhanced (V_{GS} > 10 V).

After these conditions are met, the open-drain pull-down current is disabled, allowing PWRGD to be pulled high. PWRGD is guaranteed to be in a valid state for VCC ≥ 1 V. An external pull-up circuit is required.

If the gate voltage drops below 10 V (that is, no longer meets MOSFET fully enhanced condition), PWRGD still remains asserted for 100 ms. If the condition persists for longer than 100 ms, PWRGD is deasserted and an FET health fault is signaled.

If any of the other conditions for PWRGD are no longer met, PWRGD is deasserted immediately.

Additional hysteresis can be added by simply placing a resistor from PWRGD to PWGIN.

The PWRGD polarity can be changed through the PMBus.

FAULT PIN

The $\overline{\text{FAULT}}$ pin asserts when one of the following faults causes the hot swap to shut down:

- FET health fault
- Overcurrent fault
- Overtemperature fault

The $\overline{\text{FAULT}}$ pin is latched, and it can only be cleared by a rising edge on the ENABLE pin, a PMBus OPERATION on command from the off state, or a POWER_CYCLE command, assuming no faults are still active. The fault registers are not cleared by the ENABLE pin or the POWER_CYCLE command; they can only be cleared by a PMBus OPERATION off to on command or a CLEAR_FAULTS command.

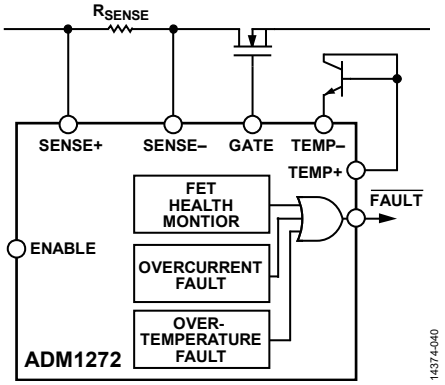


Figure 41. $\overline{\text{FAULT}}$ Pin Operation

RESTART PIN

The $\overline{\text{RESTART}}$ pin is a falling edge triggered input that allows the user to command a 10 sec automatic restart. When this input is set low, the gate turns off for 10 sec, and then powers back up. The pin is falling edge triggered; therefore, holding $\overline{\text{RESTART}}$ low for more than 10 sec generates only one restart. This pin has an internal pull-up current of approximately 16 µA, allowing it to be driven by an open-drain pull-down output or a push/pull output. The input threshold is ~1 V. The restart function can also be triggered from a PMBus command. In all cases, the restart time can be programmed from 2 sec to 25 sec on the PMBus, but defaults back to 10 sec after the device POR.

This pin is also used to configure the desired retry scheme. See the Hot Swap Retry section for additional details.

HOT SWAP RETRY

The ADM1272 can be configured to latch off or autoretry mode. The default is latchoff mode. To configure autoretry, connect the $\overline{\text{FAULT}}$ pin to $\overline{\text{RESTART}}$. As $\overline{\text{FAULT}}$ goes low, the restart command triggers. This cycle continues unless interrupted or the device is disabled.

ENABLE INPUT

The ADM1272 provides a dedicated ENABLE digital input pin. The ENABLE pin allows the ADM1272 to remain off by using a hardware signal, even when the voltage on the UV pin is greater than 1.0 V and the voltage on the OV pin is less than 1.0 V. Although the UV pin can be used to provide a digital enable signal, using the ENABLE pin for this purpose means that the ability to monitor for undervoltage conditions is not lost.

In addition to the conditions for the UVx and OV pins, the ADM1272 ENABLE input pin must be asserted for the device to begin a power-up sequence.

REMOTE TEMPERATURE SENSING

The ADM1272 provides the capability to measure temperature at a remote location with a single discrete NPN or PNP transistor. The temperature measurements can be read back over the PMBus interface. Warning and fault thresholds can also be set on the temperature measurement. Exceeding a fault threshold causes the controller to turn off the pass MOSFET, deassert the PWRGD pin, and assert the $\overline{\text{FAULT}}$ pin.

The external transistor is typically placed close to the main pass MOSFETs to provide an additional level of protection. The controller can then monitor and respond to an elevated MOSFET operating temperature. It is not possible to measure temperature at more than one location on the board.

Place the transistor close to the MOSFET for best accuracy. If the transistor is placed on the opposite side of the PCB, use multiple vias to ensure the optimum transfer of heat from the MOSFET to the transistor.

Temperature Measurement Method

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode by measuring the base emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the ADM1272 is to measure the change in V_{BE} when the device is operated at three different currents. The use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

The temperature sensor takes control of the ADC for 64 µs (typical) every 6 ms. It takes 12 ms to obtain a new temperature measurement from the ADC.

Remote Sensing Diode

The ADM1272 is designed to work with discrete transistors. The transistor can be either a PNP or NPN connected as a diode (base shorted to the collector). If an NPN transistor is used, the collector and base are connected to the TEMP+ pin and the emitter to TEMP−. If a PNP transistor is used, the collector and base are connected to TEMP− and the emitter to TEMP+.

The best accuracy is obtained by choosing devices according to the following criteria:

- Base emitter voltage greater than 0.25 V at 6 µA, at the highest operating temperature.
- Base emitter voltage less than 0.95 V at 100 µA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in transistor current gain, h_{FE} (50 to 150), that indicates tight control of V_{BE} characteristics.

Transistors, such as the 2N3904, 2N3906, or equivalent in SOT-23 packages are suitable devices to use.

Noise Filtering

For temperature sensors operating in noisy environments, the industry-standard practice is to place a capacitor across the temperature pins to mitigate the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. Although this capacitor reduces the noise, it does not eliminate it, making the use of the sensor in a noisy environment difficult.

The ADM1272 has a major advantage over other devices for eliminating the effects of noise on the external sensor. The series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the device. The effect of any filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADM1272 and the remote temperature sensor to operate in noisy environments. Figure 42 shows a low-pass filter using 100 Ω resistors and a 1 nF capacitor. This filtering reduces both common-mode noise and differential noise.

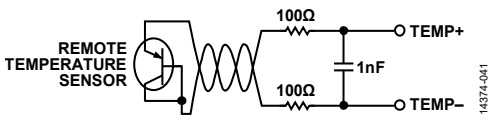


Figure 42. Filter Between Remote Sensor and ADM1272

FET HEALTH

The ADM1272 provides a comprehensive method of detecting a faulty pass MOSFET. When a faulty FET is detected, the following events occur simultaneously:

- PWRGD is deasserted.
- FAULT is asserted and latched low.
- FET health PMBus status bits are asserted and latched.

This detection feature ensures that any downstream dc-to-dc converters are disabled, limiting the power dissipation in any faulty or overheating FETs until the user clears the fault, which can be critical to avoid any catastrophic events due to faulty FETs.

A gate to source or gate to drain short is a common type of FET failure. This type of failure is detected by the ADM1272 at any time during operation.

A less common failure is a drain to source short. This normally occurs due to a board manufacturing defect such as a solder short. This type of failure is detected during the initial power-on reset cycle after power-up or after a 10 sec autoretry attempt.

There is also an option to disable FET health detection via the PMBus.

POWER MONITOR

The ADM1272 features an integrated ADC that accurately measures the current sense voltage, the input voltage, and optionally, the output voltage and temperature at an external transistor. The measured input voltage and current being delivered to the load are multiplied together to give a power value that can be read back. Each power value is also added to an energy accumulator that can be read back to allow an external device to calculate the energy consumption of the load.

The ADM1272 reports the measured current, input voltage, output voltage, and temperature. The PEAK_IOUT, PEAK_VIN, PEAK_VOUT, PEAK_PIN, and PEAK_TEMPERATURE commands can be used to read the highest readings since the value was last cleared.

An averaging function is provided for voltage, current, and power that allows a number of samples to be averaged together by the ADM1272. This function reduces the need for postprocessing of sampled data by the host processor. The number of samples that can be averaged is 2^N, where N is in the range of 0 to 7.

The power monitor current sense amplifier is bipolar and measures both positive and negative currents. The power monitor amplifier has an input range of ±25 mV.

The two basic modes of operation for the power monitor are single shot and continuous. In single-shot mode, the ADC samples the input voltage and current a number of times, depending on the averaging value selected by the user. The ADM1272 returns a single value corresponding to the average voltage and current measured. When configured for continuous mode, the power monitor continuously samples the voltage and current, making the most recent sample available to be read.

The single-shot mode can be triggered in a number of ways. The simplest method is by selecting the single shot mode using the PMON_CONFIG command and writing to the convert bit using the PMON_CONTROL command. The convert bit can also be written as part of a PMBus group command. Using a group command allows multiple devices to be written to as part of the same I^2C bus transaction, with all devices executing the

command when the stop condition appears on the bus. In this way, several devices can be triggered to sample at the same time.

Each time current sense and input voltage measurements are taken, a power calculation is performed, multiplying the two measurements together. This result can be read from the device using the READ_PIN command, returning the input power.

At the same time, the calculated power value is added to a power accumulator register that may increment a rollover counter if the value exceeds the maximum accumulator value. The power accumulator register also increments a power sample counter.

The power accumulator and power sample counter are read using the same READ_EIN command to ensure that the accumulated value and sample count are from the same point in time. The bus host reading the data assigns a time stamp when the data is read. By calculating the time difference between consecutive uses of READ_EIN and determining the delta in power consumed, it is possible for the host to determine the total energy consumed over that period.

PMBus INTERFACE

The I²C bus is a common, simple serial bus used by many devices to communicate. It defines the electrical specifications, the bus timing, the physical layer, and some basic protocol rules.

SMBus is based on I²C and provides a more robust and fault tolerant bus. Functions such as bus timeout and packet error checking (PEC) are added to help achieve this robustness, together with more specific definitions of the bus messages used to read and write data to devices on the bus.

PMBus is layered on top of SMBus and, in turn, on I²C. Using the SMBus defined bus messages, PMBus defines a set of standard commands that can be used to control a device that is part of a power chain.

The ADM1272 command set is based on the *PMBus™ Power System Management Protocol Specification*, Part I and Part II, Revision 1.2. This version of the standard is intended to provide a common set of commands for communicating with dc-to-dc type devices. However, many of the standard PMBus commands can be mapped directly to the functions of a hot swap controller.

Part I and Part II of the PMBus standard describe the basic commands and their use in a typical PMBus setup. The following sections describe how the PMBus standard and the ADM1272 specific commands are used.

DEVICE ADDRESSING

The PMBus device address is seven bits in size. There are no default addresses for any of the models; any device can be programmed to any of 16 possible addresses. Two quad-level ADRx pins map to the 16 possible device addresses.

Table 8. ADRx Pin Connections

ADRx State	ADRx Pin Connection
Low	Connect to GND
Resistor	150 kΩ resistor to GND
High-Z	No connection (floating)
High	Connect to VCAP

Table 9. PMBus Address Decode (7-Bit Address)

ADR2 State	ADR1 State	Device Address (Hex)
Low	Low	0x10
Low	Resistor	0x11
Low	High-Z	0x12
Low	High	0x13
Resistor	Low	0x14
Resistor	Resistor	0x15
Resistor	High-Z	0x16
Resistor	High	0x17
High-Z	Low	0x18
High-Z	Resistor	0x19
High-Z	High-Z	0x1A
High-Z	High	0x1B
High	Low	0x1C
High	Resistor	0x1D
High	High-Z	0x1E
High	High	0x1F

SMBUS PROTOCOL USAGE

All I²C transactions on the ADM1272 are performed using SMBus defined bus protocols. The following SMBus protocols are implemented by the ADM1272:

- Send byte
- Receive byte
- Write byte
- Read byte
- Write word
- Read word
- Block read

PACKET ERROR CHECKING

The ADM1272 PMBus interface supports the use of the PEC byte that is defined in the SMBus standard. The PEC byte is transmitted by the ADM1272 during a read transaction or sent by the bus host to the ADM1272 during a write transaction. The ADM1272 supports the use of PEC with all the SMBus protocols that it implements.

The use of the PEC byte is optional. The bus host can decide whether to use the PEC byte with the ADM1272 on a message by message basis. There is no need to enable or disable PEC in the ADM1272.

The PEC byte is used by the bus host or the ADM1272 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the ADM1272 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag.

Within a group command, the host can choose whether to send a PEC byte as part of the message to the ADM1272.

PARTIAL TRANSACTIONS ON I²C BUS

If there is a partial transaction on the I²C bus (for example, spurious data is interpreted as a start command), the ADM1272 I²C bus does not lock up, because it assumes it is in the middle of an I²C transaction. A new start command is recognized even in the middle of another transaction.

SMBus MESSAGE FORMATS

Figure 43 to Figure 51 show all the SMBus protocols supported by the ADM1272, along with the PEC variant. In these figures, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the ADM1272 is driving the bus.

Figure 43 to Figure 51 use the following abbreviations:

- S is the start condition.
- Sr is the repeated start condition.
- P is the stop condition.
- R is the read bit.
- $\overline{W}$ is the write bit.
- A is the acknowledge bit (0).
- $\overline{A}$ is the acknowledge bit (1).

A, the acknowledge bit, is typically active low (Logic 0) when the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a Logic 1, indicated by $\overline{A}$.

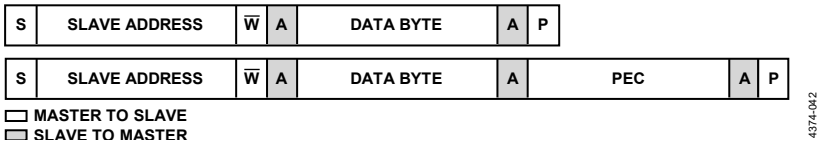


Figure 43. Send Byte and Send Byte with PEC

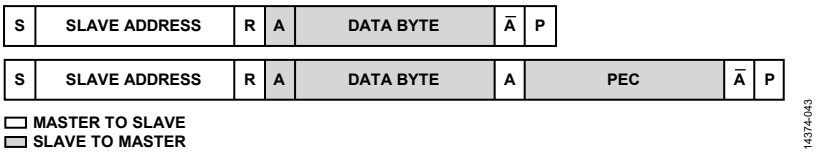


Figure 44. Receive Byte and Receive Byte with PEC

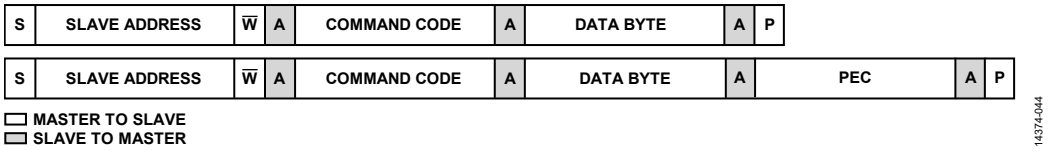


Figure 45. Write Byte and Write Byte with PEC

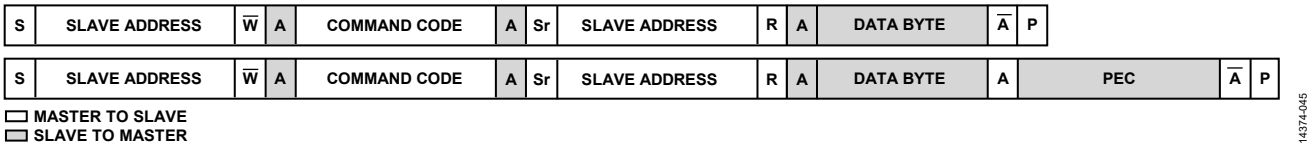


Figure 46. Read Byte and Read Byte with PEC

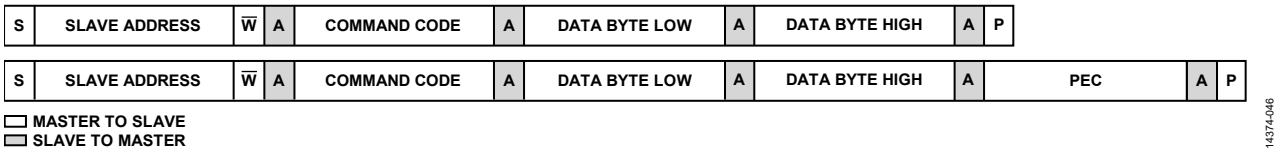


Figure 47. Write Word and Write Word with PEC

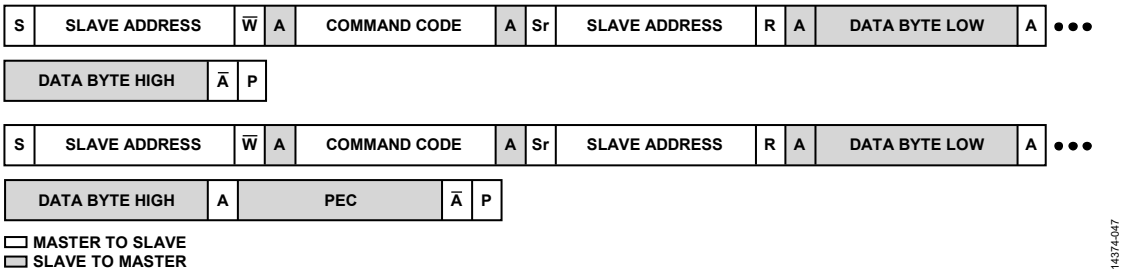


Figure 48. Read Word and Read Word with PEC

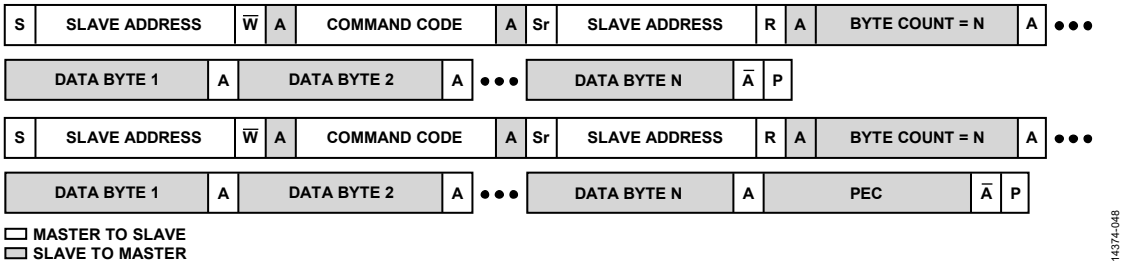


Figure 49. Block Read and Block Read with PEC

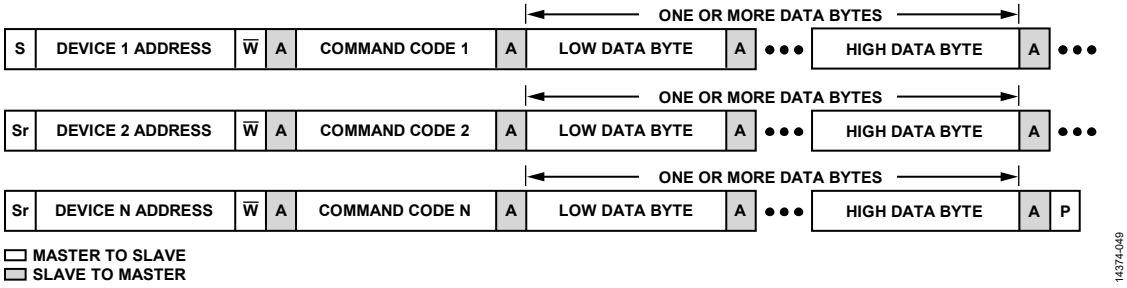


Figure 50. Group Command

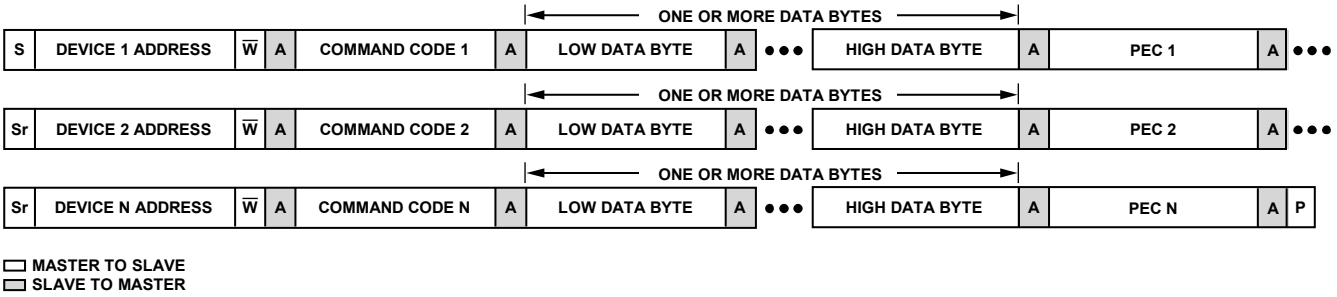


Figure 51. Group Command with PEC

GROUP COMMANDS

The PMBus standard defines what are known as group commands. Group commands are single bus transactions that send commands or data to more than one device at the same time. Each device is addressed separately, using its own address; there is no special group command address. A group command transaction can contain only write commands that send data to a device. It is not possible to use a group command to read data from devices.

From an I²C protocol point of view, a normal write command consists of the following:

- I²C start condition.
- Slave address bits and a write bit (followed by an acknowledge from the slave device).
- One or more data bytes (each of which is followed by an acknowledge from the slave device).
- I²C stop condition to end the transaction.

A group command differs from a nongroup command in that, after the data is written to one slave device, a repeated start condition is placed on the bus followed by the address of the next slave device and data. This process continues until all of the devices are written to, at which point the stop condition is placed on the bus by the master device.

The format of a group command and a group command with PEC is shown in Figure 50 and Figure 51, respectively.

Each device that is written to as part of the group command does not immediately execute the command written. The device must wait until the stop condition appears on the bus. At that point, all devices execute their commands at the same time.

Using a group command, it is possible, for example, to turn multiple PMBus devices on or off simultaneously. In the case of the ADM1272, it is also possible to issue a power monitor command that initiates a conversion, causing multiple ADM1272 devices to sample together at the same time.

HOT SWAP CONTROL COMMANDS

OPERATION Command

The GATE pin that drives the FET is controlled by a dedicated hot swap state machine. The UVx and OV input pins, the EFAULT, ESTART, PWGIN, and ENABLE pins, and the current sense all feed into the state machine, and they control when and with which pull-down current the gate is turned off.

It is also possible to control the hot swap GATE output using commands over the PMBus interface. Use the OPERATION command to request the hot swap output to turn on. However, if the UVx pin indicates that the input supply is less than required, the hot swap output is not turned on, even if the OPERATION command requests that the output be enabled.

If the OPERATION command is used to disable the hot swap output, the GATE pin is held low, even if all hot swap state machine control inputs indicate that it can be enabled.

The default state of Bit 7 (also named the on bit) of the OPERATION command is 1; therefore, the hot swap output is always enabled when the ADM1272 emerges from UVLO. If the on bit is never changed, the UVx input or the ENABLE/$\overline{\text{ENABLE}}$ input is the hot swap master on/off control signal.

If the on bit is set to 0 while the UVx signal is high, the hot swap output is turned off. If the UVx signal is low or if the OV signal is high, the hot swap output is already off and the status of the on bit has no effect.

If the on bit is set to 1, the hot swap output is requested to turn on. If the UVx signal is low or if the OV signal is high, setting the on bit to 1 has no effect, and the hot swap output remains off.

It is possible to determine at any time whether the hot swap output is enabled using the STATUS_BYTE or the STATUS_WORD command (see the Status Commands section).

The OPERATION command can also clear any latched faults in the status registers. To clear latched faults, set the on bit to 0 and then reset it to 1. This action also clears the latched $\overline{\text{FAULT}}$ pin.

DEVICE_CONFIG Command

The DEVICE_CONFIG command configures certain settings within the ADM1272, for example, enabling or disabling FET health detection, general-purpose output (GPO) pin configuration, and modifying the duration of the severe overcurrent settings.

POWER_CYCLE Command

Use the POWER_CYCLE command to request that the ADM1272 be turned off for approximately 11 sec and then turned back on. This command is useful if the processor that controls the ADM1272 is also powered off when the ADM1272 is turned off. This command allows the processor to request that the ADM1272 turn off and on again as part of a single command.

ADM1272 INFORMATION COMMANDS

CAPABILITY Command

The host processors can use the CAPABILITY command to determine the I²C bus features that are supported by the ADM1272. The features that are reported include the maximum bus speed, whether the device supports the PEC byte, and the SMBus alert reporting function.

PMBUS_REVISION Command

The PMBUS_REVISION command reports the version of Part I and Part II of the PMBus standard.

MFR_ID, MFR_MODEL, and MFR_REVISION Commands

The MFR_ID, MFR_MODEL, and MFR_REVISION commands return ASCII strings that can be used to facilitate detection and identification of the ADM1272 on the bus.

These commands are read using the SMBus block read message type. This message type requires that the ADM1272 return a byte count corresponding to the length of the string data that is to be read back.

STATUS COMMANDS

The ADM1272 provides a number of status bits to report faults and warnings from the hot swap controller and the power monitor. These status bits are located in six different registers arranged in a hierarchy. The STATUS_BYTE and STATUS_WORD commands provide 8 bits and 16 bits of high level information, respectively. The STATUS_BYTE and STATUS_WORD commands contain the most important status bits, as well as pointer bits that indicate whether any of the five other status registers must be read for more detailed status information.

In the ADM1272, a particular distinction is made between faults and warnings. A fault is always generated by the hot swap controller and is typically defined by hardware component values. Events that can generate a fault are

- Overcurrent condition that causes the hot swap timer to time out
- Overvoltage condition on the OV pin
- Undervoltage condition on the UV pin
- Overtemperature condition
- FET health issue detected

When a fault occurs, the hot swap controller always takes an action, usually to turn off the GATE pin, which is driving the FET. The $\overline{\text{FAULT}}$ pin is asserted, and the PWRGD pin is deasserted. A fault can also generate an SMBus alert on the GPO2/$\overline{\text{ALERT2}}$ pin.

All warnings in the ADM1272 are generated by the power monitor, which samples the voltage, current, and temperature and then compares these measurements to the threshold values set by the various limit commands. A warning has no effect on the hot swap controller, but it may generate an SMBus alert on one or both of the GPOx/$\overline{\text{ALERTx}}$ output pins.

When a status bit is set, it always means that the status condition—fault or warning—is active or was active at some point in the past. When a fault or warning bit is set, it is latched until it is explicitly cleared using either the OPERATION or the CLEAR_FAULTS command. Some other status bits are live, that is, they always reflect a status condition and are never latched.

STATUS_BYTE and STATUS_WORD Commands

The STATUS_BYTE and STATUS_WORD commands obtain a snapshot of the overall device status. These commands indicate whether it is necessary to read more detailed information using the other status commands.

The low byte of the word returned by the STATUS_WORD command is the same byte returned by the STATUS_BYTE command. The high byte of the word returned by the STATUS_WORD command provides a number of bits that determine which of the other status commands must be issued to obtain all active status bits. The status bits for FET health and power good are also found in the high byte of STATUS_WORD.

STATUS_INPUT Command

The STATUS_INPUT command returns a number of bits relating to voltage faults and warnings on the input supply as well as the overpower warning.

STATUS_VOUT Command

The STATUS_VOUT command returns a number of bits relating to voltage warnings on the output supply.

STATUS_IOUT Command

The STATUS_IOUT command returns a number of bits relating to current faults and warnings on the output supply.

STATUS_TEMPERATURE Command

The STATUS_TEMPERATURE command returns a number of bits relating to temperature faults and warnings at the external transistor.

STATUS_MFR_SPECIFIC Command

The STATUS_MFR_SPECIFIC command is a standard PMBus command, but the contents of the byte returned are specific to the ADM1272.

CLEAR_FAULTS Command

The CLEAR_FAULTS command clears fault and warnings bits when they are set. Fault and warnings bits are latched when they are set. In this way, a host can read the bits any time after the fault or warning condition occurs and determine which problem actually occurred.

If the CLEAR_FAULTS command is issued and the fault or warning condition is no longer active, the status bit is cleared. If the condition is still active—for example, if an input voltage is below the undervoltage threshold of the UVx pin—the CLEAR_FAULTS command attempts to clear the status bit, but that status bit is immediately set again.

GPO AND ALERT PIN SETUP COMMANDS

Two multipurpose pins are provided on the ADM1272: GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$.

These pins can be configured over the PMBus in one of three output modes, as follows:

- General-purpose digital output
- Output for generating an SMBus alert when one or more fault/warning status bits become active in the PMBus status registers
- Digital comparator

In digital comparator mode, the current, voltage, power, and temperature warning thresholds are compared to the values read or calculated by the ADM1272. The comparison result sets the output high or low according to whether the value is greater or less than the warning threshold that is set.

For an example of how to configure these pins to generate an SMBus alert and how to respond and clear the condition, see the Example Use of SMBUS ARA section.

ALERT1_CONFIG and ALERT2_CONFIG Commands

Using combinations of bit masks, the ALERT1_CONFIG and ALERT2_CONFIG commands select the status bits that, when set, generate an SMBus alert signal to a processor, or control the digital comparator mode. Pin 14 and Pin 13 (GPO1/ALERT1/CONV and GPO2/ALERT2) must be configured in SMBus alert or digital comparator mode in the DEVICE_CONFIG register.

When Pin 13 or Pin 14 is configured in GPO mode, the pin is under software control. If this mode is set, the SMBus alert masking bits are ignored.

POWER MONITOR COMMANDS

The ADM1272 provides a high accuracy, 12-bit current, voltage, and temperature power monitor. The power monitor can be configured in a number of different modes of operation and can run in either continuous mode or single-shot mode with different sample averaging options.

The power monitor can measure the following quantities:

- Input voltage (V_{IN})
- Output voltage (V_{OUT})
- Output current (I_{OUT})
- External temperature

The following quantities are then calculated:

- Input power (P_{IN})
- Input energy (E_{IN})

PMON_CONFIG Command

The power monitor can run in a variety of modes. The PMON_CONFIG command sets up the power monitor.

The settings that can be configured are as follows:

- Single-shot or continuous sampling
- V_{IN}/V_{OUT}/temperature sampling enable/disable
- Current and voltage sample averaging
- Power sample averaging
- Simultaneous sampling enable/disable
- Temperature sensor filter enable/disable

Modifying the power monitor settings while the power monitor is sampling is not recommended. To ensure correct operation of the device and to avoid any potential spurious data or the generation of status alerts, stop the power monitor before any of these settings are changed.

PMON_CONTROL Command

Power monitor sampling can be initiated via hardware or via software using the PMON_CONTROL command. This command can be used with single-shot or continuous mode.

READ_VIN, READ_VOUT, and READ_IOUT Commands

The ADM1272 power monitor always measures the voltage developed across the sense resistor to provide a current measurement. The input voltage measurement from the SENSE+ pin is also enabled by default. The output voltage present on the VOUT pin is available if enabled with the PMON_CONFIG command.

READ_TEMPERATURE_1 Command

Temperature measurement at an external transistor can also be enabled with the PMON_CONFIG command. If enabled, the temperature sensor takes over the ADC for 64 µs every 6 ms and returns a measurement every 12 ms.

READ_PIN, READ_PIN_EXT, READ_EIN, and READ_EIN_EXT Commands

The 12-bit input voltage (V_{IN}) and 12-bit current (I_{OUT}) measurement values are multiplied by the ADM1272 to obtain the input power value. This multiplication is accomplished by using fixed point arithmetic, and produces a 24-bit value. It is assumed that the numbers are in the 12.0 format, meaning that there is no fractional part. Note that only positive I_{OUT} values are used to avoid returning a negative power.

This 24-bit value can be read from the ADM1272 using the READ_PIN_EXT command, where the most significant bit (MSB) is always a zero because PIN_EXT is a twos complement binary value that is always positive.

The 16 most significant bits of the 24-bit value are used as the value for P_{IN}. The MSB of the 16-bit P_{IN} word is always zero, because P_{IN} is a twos complement binary value that is always positive.

Each time a power calculation is completed, the 24-bit power value is added to a 24-bit energy accumulator register. This is a twos complement representation as well; therefore, the MSB is always zero. Each time this energy accumulator register rolls over from 0x7FFFFF to 0x000000, a 16-bit rollover counter is incremented. The rollover counter is straight binary, with a maximum value of 0xFFFF before it rolls over.

A 24-bit straight binary power sample counter is also incremented by 1 each time a power value is calculated and added to the energy accumulator.

These registers can be read back using one of two commands, depending on the level of accuracy required for the energy accumulator and the desire to limit the frequency of reads from the ADM1272.

A bus host can read these values, and by calculating the delta in the energy accumulated, the delta in the number of samples, and the time delta since the last read, the host can calculate the average power since the last read, as well as the energy consumed since then.

The time delta is calculated by the bus host based on when it sends its commands to read from the device, and is not provided by the ADM1272.

To avoid loss of data, the bus host must read at a rate that ensures the rollover counter does not wrap around more than once, and if the counter does wrap around, that the next value read for P_{IN} is less than the previous one.

The READ_EIN command returns the top 16 bits of the energy accumulator, the lower 8 bits of the rollover counter, and the full 24 bits of the sample counter.

The READ_EIN_EXT command returns the full 24 bits of the energy accumulator, the full 16 bits of the rollover counter, and the full 24 bits of the sample counter. The use of the longer rollover counter means that the time interval between reads of the device can be increased from seconds to minutes without losing any data.

PEAK_IOUT, PEAK_VIN, PEAK_VOUT, PEAK_PIN, and PEAK_TEMPERATURE Commands

In addition to the standard PMBus commands for reading voltage and current, the ADM1272 provides commands that can report the maximum peak voltage, current, power, or temperature value since the peak value was last cleared.

The peak values are updated only after the power monitor samples and averages the current and voltage measurements. Individual peak values are cleared by writing a 0 value with the corresponding command.

WARNING LIMIT SETUP COMMANDS

The ADM1272 power monitor can monitor a number of different warning conditions simultaneously and report any current, voltage, power, or temperature values that exceed the user defined thresholds using the status commands.

All comparisons performed by the power monitor require the measured value to be strictly greater or less than the threshold value.

At power-up, all threshold limits are set to either minimum scale (for undervoltage or undercurrent conditions) or to maximum scale (for overvoltage, overcurrent, overpower, or overtemperature conditions). This requirement effectively disables the generation of any status warnings by default; warning bits are not set in the status registers until the user explicitly sets the threshold values.

VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT Commands

The VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT commands set the OV and UV thresholds on the input voltage, as measured at the SENSE+ pin.

VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT Commands

The VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_ LIMIT commands set the OV and UVx thresholds on the output voltage, as measured at the VOUT pin.

IOUT_OC_WARN_LIMIT Command

The IOUT_OC_WARN_LIMIT command sets the OC threshold for the current flowing through the sense resistor.

OT_WARN_LIMIT Command

The OT_WARN_LIMIT command sets the overtemperature threshold for the temperature measured at the external transistor.

PIN_OP_WARN_LIMIT Command

The PIN_OP_WARN_LIMIT command sets the overpower threshold for the power delivered to the load.

PMBUS DIRECT FORMAT CONVERSION

The ADM1272 uses the PMBus direct format to represent real-world quantities such as voltage, current, and power values. A direct format number takes the form of a 2-byte, twos complement, binary integer value.

It is possible to convert between direct format value and real-world quantities using the following equations. Equation 1 converts from real-world quantities to PMBus direct values, and Equation 2 converts PMBus direct format values to real-world values.

$$Y = (mX + b) \times 10^{R} \quad (1)$$

$$X = 1/m \times (Y \times 10^{-R} - b) \quad (2)$$

where:
Y is the value in PMBus direct format.
m is the slope coefficient, a 2-byte, twos complement integer.
X is the real-world value.
b is the offset, a 2-byte, twos complement integer.
R is a scaling exponent, a 1-byte, twos complement integer.

The same equations are used for voltage, current, power, and temperature conversions. The only difference is the values of the m, b, and R coefficients that are used. Table 10 lists all the coefficients required for the ADM1272.

Example 1

IOUT_OC_WARN_LIMIT requires a current-limit value expressed in direct format.

If the required current limit is 10 A, R_{SENSE} = 1 mΩ and IRANGE is 15 mV. Using Equation 1, and expressing X in units of amperes,

$$Y = ((1326 \times 10) + 20{,}480) \times 10^{-1}$$

$$Y = 3374$$

Writing a value of 6026 with the IOUT_OC_WARN_LIMIT command sets an overcurrent warning at 10 A.

Example 2

The READ_IOUT command returns a direct format value of 4000 representing the current flowing through the sense resistor.

To convert this value to the current, use Equation 2, with R_{SENSE} = 1 mΩ and IRANGE = 30 mV.

$$X = 1/663 \times (4000 \times 10^{1} - 20{,}480)$$

$$X = 29.44 \text{ A}$$

This means that, when READ_IOUT returns a value of 4000, 29.44 A is flowing in the sense resistor.

Note that the same calculations that are used to convert power values also apply to the energy accumulator value returned by the READ_EIN command because the energy accumulator is a summation of multiple power values.

The READ_PIN_EXT and READ_EIN_EXT commands return 24-bit extended precision versions of the 16-bit values returned by READ_PIN and READ_EIN. The direct format values must be divided by 256 prior to being converted with the coefficients shown in Table 10.

Example 3

The PIN_OP_WARN_LIMIT command requires a power limit value expressed in direct format.

If the required power limit is 1200 W and IRANGE and VRANGE are 30 mV and 60 V, respectively, using Equation 1,

$$Y = (17561 \times 1200) \times 10^{-3}$$

$$Y = 42{,}144$$

Writing a value of 42,144 with the PIN_OP_WARN_LIMIT command sets an overpower warning at 1200 W.

VOLTAGE AND CURRENT CONVERSION USING LSB VALUES

The direct format voltage and current values returned by the READ_VIN, READ_VOUT, and READ_IOUT commands and the corresponding peak versions are the data output directly by the ADM1272 ADC. Because the voltages and currents are 12-bit ADC output codes, they can also be converted to real-world values when there is knowledge of the size of the LSB on the ADC.

The m, b, and R coefficients defined for the PMBus conversion are required to be whole integers by the standard and have therefore been rounded slightly. Using this alternative method, with the exact LSB values, can provide somewhat more accurate numerical conversions.

Converting ADC Code to Current

To convert an ADC code to current in amperes, use Equation 3 and Equation 4.

$$V_{\Delta SENSE} = LSB_{CURRENT} \times (I_{ADC} - 2048) \quad (3)$$

where:
$V_{\Delta SENSE} = (V_{SENSE+}) - (V_{SENSE-})$.
$LSB_{CURRENT}$ = 7.53 µV with the 15 mV range and 15.06 µV with the 30 mV range
I_{ADC} is the 12-bit ADC code.

$$I_{OUT} = V_{\Delta SENSE}/R_{SENSE} \quad (4)$$

where:
I_{OUT} is the measured current value in amperes.
R_{SENSE} is the value of the sense resistor in milliohms.

For example, for a 30 mV range, Code 4000 results in $V_{\Delta SENSE}$ = 29.397 mV.

ADC Code to Voltage

To convert an ADC code to voltage, use the following formula:

$$V_M = LSB_{VOLTAGE} \times V_{ADC}$$

where:
V_M is the measured value in volts.
$LSB_{VOLTAGE}$ = 14.77 mV with the 0 V to 60 V range and 24.62 mV with the 0 V to 100 V range.
V_{ADC} is the 12-bit ADC code.

For example, for a 100 V range, Code 4000 results in V_M = 98.48 V.

Converting ADC Code to Power

To convert an ADC code to power in watts, use the following formula:

$$P_M = LSB_{POWER} \times P_{ADC}/R_{SENSE}$$

where:
P_M is the measured value in watts.
LSB_{POWER} is shown in Table 10 as the power for the LSB coefficient, and expressed in the order of 10^{-6}.
P_{ADC} is the 16-bit ADC code.

For example, for a 0 V to 100 V range and a 0 V to 30 mV range, Code 10000 results in P_M = 949.2 W.

Converting Current to 12-Bit Value

To convert a current in amperes to a 12-bit value, use Equation 5 and Equation 6 (round the result to the nearest integer).

$$V_{\Delta SENSE} = I_A \times R_{SENSE} \quad (5)$$

where:
$V_{\Delta SENSE} = (V_{SENSE+}) - (V_{SENSE-})$.
I_A is the current value in amperes.
R_{SENSE} is the value of the sense resistor in milliohms.

$$I_{CODE} = 2048 + (V_{\Delta SENSE}/LSB_{CURRENT}) \quad (6)$$

I_{CODE} is the 12-bit ADC code.
$LSB_{CURRENT}$ = 7.53 µV with the 0 V to 15 mV range and 15.06 µV with the 0 V to 30 mV range.

Converting Voltage to 12-Bit Value

To convert a voltage to a 12-bit value, use the following formula (round the result to the nearest integer):

$$V_{CODE} = V_A/LSB_{VOLTAGE}$$

where:
V_{CODE} is the 12-bit ADC code.
$LSB_{VOLTAGE}$ = 14.77 mV with the 0 V to 60 V range and 24.62 mV with the 0 V to 100 V range.

To convert power to a 16-bit value, use the following formula (round the result to the nearest integer):

$$P_{CODE} = P_A \times R_{SENSE}/LSB_{POWER}$$

where:
P_{CODE} is the 16-bit ADC code.
P_A is the power value in watts.
R_{SENSE} is the value of the sense resistor in milliohms.
LSB_{POWER} is shown in Table 10 as the power for the LSB coefficient, and expressed in the order of 10^{-6}.

Table 10. Required Coefficients for Voltage, Current, Power, and Temperature Conversion

	Voltage		Current		Power				
Coefficient	**0 V to 60 V Range**	**0 V to 100 V Range**	**0 V to 15 mV Range**	**0 V to 30 mV Range**	**0 V to 15 mV and 0 V to 60 V Ranges**	**0 V to 15 mV and 0 V to 100 V Ranges**	**0 V to 30 mV and 0 V to 60 V Ranges**	**0 V to 30 mV and 0 V to 100 V Ranges**	**Temperature**
m	6770	4062	1326 × R_{SENSE}	663 × R_{SENSE}	3512 × R_{SENSE}	21071 × R_{SENSE}	17561 × R_{SENSE}	10535 × R_{SENSE}	42
b	0	0	20480	20480	0	0	0	0	31871
R	−2	−2	−1	−1	−2	−3	−3	−3	−1
LSB	14.77	24.62	7.53	15.06	28.47	47.46	56.94	94.92	Not applicable

APPLICATIONS INFORMATION

GENERAL-PURPOSE OUTPUT PIN BEHAVIOR

The ADM1272 provides a flexible alert system, whereby one or more fault/warning conditions can be indicated on an external device.

FAULTS AND WARNINGS

A PMBus fault on the ADM1272 is typically generated due to an analog event (the exception being a temperature fault) and causes a change in state in the hot swap output, turning it off. The defined fault sources are as follows:

- Undervoltage (UV) event detected on the UVx pin.
- Overvoltage (OV) event detected on the OV pin.
- Overcurrent (OC) event that causes a hot swap timeout.
- Overtemperature (OT) event detected at the external transistor.
- Fault detected with the pass MOSFET.

Faults are continuously monitored, and, as long as power is applied to the device, they cannot be disabled. When a fault occurs, a corresponding status bit is set in one or more STATUS_xxx registers.

A value of 1 in a status register bit field always indicates a fault or warning condition. Fault and warning bits in the status registers are latched when set to 1. To clear a latched bit to 0—provided that the fault condition is no longer active—use the CLEAR_FAULTS command or use the OPERATION command to turn the hot swap output off and then on again.

A warning is less severe than a fault and never causes a change in the state of the hot swap controller. The sources of a warning are defined as follows:

- CML: a communications error occurred on the I^2C bus.
- HS_INLIM_FAULT: the circuit breaker threshold was tripped and EFAULT/ESTART started ramping, but did not necessarily shut the system down.
- I_{OUT} OC warning from the ADC.
- V_{IN} UV warning from the ADC.
- V_{IN} OV warning from the ADC.
- V_{OUT} UV warning from the ADC.
- V_{OUT} OV warning from the ADC.
- P_{IN} overpower (OP) warning from the $V_{IN} \times I_{OUT}$ calculation.
- OT warning from the ADC.
- Hysteretic output warning from the ADC.

GENERATING AN ALERT

A host device can periodically poll the ADM1272 using the status commands to determine whether a fault/warning is active. However, this polling is very inefficient in terms of software and processor resources. The ADM1272 has two output pins (GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$) that generate interrupts to a host processor.

By default at power-up, the open-drain GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ outputs are high impedance; therefore, the pins can be pulled high through a resistor. The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins are disabled by default on the ADM1272.

Any one or more of the faults and warnings listed in the Faults and Warnings section can be enabled and cause an alert, making the corresponding GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin active. By default, the active state of the GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins are low.

For example, to use GPO2/$\overline{\text{ALERT2}}$ to monitor the V_{OUT} UV warning from the ADC, the followings steps must be performed:

1. Set a threshold level with the VOUT_UV_WARN_LIMIT command.
2. Set the VOUT_UV_WARN_EN2 bit in the ALERT2_CONFIG register.
3. Start the power monitor sampling on V_{OUT} (ensure the power monitor is configured to sample V_{OUT} in the PMON_CONFIG register).

If a V_{OUT} sample is taken that is below the configured V_{OUT} UV value, the GPO2/$\overline{\text{ALERT2}}$ pin is pulled low, signaling an interrupt to a processor.

HANDLING/CLEARING AN ALERT

When faults/warnings are configured on the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pins, the pin becomes active to signal an interrupt to the processor. (The pin is active low, unless inversion is enabled.) The GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ signal performs the functions of an SMBus alert.

Note that the GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins can become active independently but they are always made inactive together.

A processor can respond to the interrupt in one of two ways, depending on whether there is a single device or multiple devices on the bus.

Single Device on Bus

When there is only one device on the bus, the processor simply reads the status bytes and issues a CLEAR_FAULTS command to clear all the status bits, which causes the deassertion of the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ line. If there is a persistent fault (for example, an undervoltage on the input), the status bits remain set after the CLEAR_ FAULTS command is executed because the fault has not been removed. However, the GPO1/ $\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ line is not pulled low unless a new fault or warning becomes active. If the cause of the SMBus alert is a power monitor generated warning and the power monitor is running continuously, the next sample generates a new SMBus alert after the CLEAR_FAULTS command is issued.

Multiple Devices on Bus

When there are multiple devices on the bus, the processor issues an SMBus alert response address (ARA) command to find out which device asserted the SMBus alert line. The processor reads the status bytes from that device and issues a CLEAR_FAULTS command.

SMBUS ALERT RESPONSE ADDRESS

The SMBus ARA is a special address that can be used by the bus host to locate any devices that must communicate with the bus host. A host typically uses a hardware interrupt pin to monitor the SMBus alert pins of multiple devices. When the host interrupt occurs, the host issues a message on the bus using the SMBus receive byte or receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have an SMB alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device can have an active SMB alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its SMBus alert signal. If the host sees that the SMBus alert signal is still low, it continues to read addresses until all devices that must communicate have transmitted their addresses.

EXAMPLE USE OF SMBus ARA

The full sequence of steps that occurs when an SMBus alert is generated and cleared is as follows:

1. A fault or warning is enabled using the ALERT2_CONFIG command, and the corresponding status bit for the fault or warning changes from 0 to 1, indicating that the fault or warning has just become active.
2. The GPO2/$\overline{\text{ALERT2}}$ pin becomes active (set low) to signal that an SMBus alert is active.
3. The host processor issues an SMBus ARA command to determine which device has an active alert.
4. If there are no other active alerts from devices with lower I^2C addresses, this device makes the GPO2/$\overline{\text{ALERT2}}$ pin inactive (set high) during the no acknowledge bit period after it sends its address to the host processor.
5. If the GPO2/$\overline{\text{ALERT2}}$ pin stays low, the host processor must continue to issue SMBus ARA commands to devices to determine the addresses of all devices that require a status check.
6. The ADM1272 continues to operate with the GPO2/$\overline{\text{ALERT2}}$ pin inactive and the contents of the status bytes unchanged until the host reads the status bytes and clears them, or until a new fault occurs. If a status bit for a fault/warning that is enabled on the GPO2/$\overline{\text{ALERT2}}$ pin and that was not already active (equal to 1) changes from 0 to 1, a new alert is generated, causing the GPO2/$\overline{\text{ALERT2}}$ pin to become active again.

DIGITAL COMPARATOR MODE

The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins can be configured to indicate if a user defined threshold for voltage, current, power, or temperature is exceeded. In this mode, the output pin is live and is not latched when a warning threshold is exceeded. In effect, the pin acts as a digital comparator, where the threshold is set using the warning limit threshold commands.

The ALERTx_CONFIG command is used, similar to the SMBus alert configuration, to select the specific warning threshold to be monitored. The GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin.

REGISTER DETAILS

OPERATION REGISTER

Address: 0x01, Reset: 0x80, Name: OPERATION

This command requests the hot swap turn on and turn off. When turning the hot swap on, it clears status bits for any faults or warnings that are not active.

Table 11. Bit Descriptions for OPERATION

Bits	Bit Name	Settings	Description	Reset	Access
7	ON		Hot swap enable.	0x1	RW
		0	Hot swap output disabled.		
		1	Hot swap output enabled.		
[6:0]	RESERVED		Always reads as 0000000.	0x00	RESERVED

CLEAR FAULTS REGISTER

Address: 0x03, Reset: 0x, Name: CLEAR_FAULTS

This command clears fault and warning bits in all the status registers. Any faults that are still active are not cleared, and remain set. Any warnings and the OT_FAULT bit that are generated by the power monitor are cleared, but can be asserted again if still active following the next power monitor conversion cycle.

This command does not require any data.

PMBus CAPABILITY REGISTER

Address: 0x19, Reset: 0xB0, Name: CAPABILITY

This command allows the host system to determine the SMBus interface capabilities of the device.

Table 12. Bit Descriptions for CAPABILITY

Bits	Bit Name	Settings	Description	Reset	Access
7	PEC_SUPPORT		Packet error correction (PEC) support.	0x1	R
		1	Always reads as 1. PEC is supported.		
[6:5]	MAX_BUS_SPEED		Maximum bus interface speed.	0x1	R
		01	Always reads as 01. Maximum supported bus speed is 400 kHz.		
4	SMBALERT_SUPPORT		SMBus alert support.	0x1	R
		1	Always reads as 1. Device supports SMBus alert and alert response address (ARA).		
[3:0]	RESERVED		Always reads as 0000.	0x0	RESERVED

OUTPUT VOLTAGE OVERVOLTAGE WARNING LIMIT REGISTER

Address: 0x42, Reset: 0x0FFF, Name: VOUT_OV_WARN_LIMIT

This command sets the overvoltage warning limit for the voltage measured on the VOUT pin.

Table 13. Bit Descriptions for VOUT_OV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VOUT_OV_WARN_LIMIT		Overvoltage warning threshold for the VOUT pin measurement, expressed in direct format.	0xFFF	RW

OUTPUT VOLTAGE UNDERVOLTAGE WARNING LIMIT REGISTER

Address: 0x43, Reset: 0x0000, Name: VOUT_UV_WARN_LIMIT

This command sets the undervoltage warning limit for the voltage measured on the VOUT pin.

Table 14. Bit Descriptions for VOUT_UV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VOUT_UV_WARN_LIMIT		Undervoltage warning threshold for the VOUT pin measurement, expressed in direct format.	0x000	RW

OUTPUT CURRENT OVERCURRENT WARNING LIMIT REGISTER

Address: 0x4A, Reset: 0x0FFF, Name: IOUT_OC_WARN_LIMIT

This command sets the overcurrent warning limit for the current measured between the SENSE+ and the SENSE− pins.

Table 15. Bit Descriptions for IOUT_OC_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	IOUT_OC_WARN_LIMIT		Overcurrent warning threshold for the I_{OUT} measurement, expressed in direct format.	0xFFF	RW

OVERTEMPERATURE FAULT LIMIT REGISTER

Address: 0x4F, Reset: 0x0FFF, Name: OT_FAULT_LIMIT

This command sets the overtemperature fault limit for the temperature measured between the TEMP+ and TEMP− pins.

Table 16. Bit Descriptions for OT_FAULT_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	OT_FAULT_LIMIT		Over-temperature fault threshold for the measurement between the TEMP+ and TEMP− pins, expressed in direct format.	0xFFF	RW

OVERTEMPERATURE WARNING LIMIT REGISTER

Address: 0x51, Reset: 0x0FFF, Name: OT_WARN_LIMIT

This command sets the over-temperature warning limit for the temperature measured on the TEMP+ and TEMP− pins.

Table 17. Bit Descriptions for OT_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	OT_WARN_LIMIT		Overtemperature warning threshold for the measurement between TEMP+/TEMP− pins, expressed in direct format.	0xFFF	RW

INPUT VOLTAGE OVERVOLTAGE WARNING LIMIT REGISTER

Address: 0x57, Reset: 0x0FFF, Name: VIN_OV_WARN_LIMIT

This command sets the overvoltage warning limit for the V_{IN} voltage, measured on the SENSE+ pin.

Table 18. Bit Descriptions for VIN_OV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VIN_OV_WARN_LIMIT		Overvoltage warning threshold for the V_{IN} voltage, measured on the SENSE+ pin. Expressed in direct format.	0xFFF	RW

INPUT VOLTAGE UNDERVOLTAGE WARNING LIMIT REGISTER

Address: 0x58, Reset: 0x0000, Name: VIN_UV_WARN_LIMIT

This command sets the undervoltage warning limit for the V_{IN} voltage, measured on the SENSE+ pin.

Table 19. Bit Descriptions for VIN_UV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VIN_UV_WARN_LIMIT		Undervoltage warning threshold for the V_{IN} voltage, measured on the SENSE+ pin. Expressed in direct format.	0x000	RW

OVERPOWER WARNING LIMIT REGISTER

Address: 0x6B, Reset: 0x7FFF, Name: PIN_OP_WARN_LIMIT

This command sets the overpower warning limit for the power calculated based on $V_{IN} \times I_{OUT}$.

Table 20. Bit Descriptions for PIN_OP_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Always reads as 0.	0x0	RESERVED
[14:0]	PIN_OP_WARN_LIMIT		Overpower warning threshold for the $V_{IN} \times I_{OUT}$ power calculation, expressed in direct format.	0x7FFF	RW

STATUS BYTE REGISTER

Address: 0x78, Reset: 0x00, Name: STATUS_BYTE

This command provides status information for critical faults and certain top level status commands in the device. STATUS_BYTE is also the lower byte returned by STATUS_WORD. A bit set to 1 indicates a fault or warning occurred.

Table 21. Bit Descriptions for STATUS_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Always reads as 0.	0x0	RESERVED
6	HOTSWAP_OFF		Hot swap gate is off. This bit is live.	0x0	R
		0	The hot swap gate drive output is enabled.		
		1	The hot swap gate drive output is disabled, and the GATE pin is pulled down. This can be due to, for example, an overcurrent fault that causes the device to latch off, an undervoltage condition on the UV pin, or the use of the OPERATION command to turn the output off.		
5	RESERVED		Always reads as 0.	0x0	RESERVED
4	IOUT_OC_FAULT		I_{OUT} overcurrent fault. This bit is latched.	0x0	R
		0	No overcurrent output fault detected.		
		1	The hot swap controller determined that the FET may be overheating due to trying to current limit, causing the hot swap gate drive to shut down.		
3	VIN_UV_FAULT		V_{IN} fault. This bit is latched.	0x0	R
		0	No undervoltage input fault detected on the UVL/UVH pins.		
		1	An undervoltage input fault was detected on the UVL/UVH pins.		
2	TEMP_FAULT		Temperature fault or warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by STATUS_TEMPERATURE.		
		1	There are one or more active status bits to be read by STATUS_TEMPERATURE.		
1	CML_FAULT		None of the above. This bit is latched.	0x0	R
		0	No communications error detected on the I^2C/PMBus interface.		
		1	An error was detected on the I^2C/PMBus interface. Errors detected are unsupported command, invalid PEC byte, and incorrectly structured message.		

Bits	Bit Name	Settings	Description	Reset	Access
0	NONEABOVE_STATUS		None of the above. This bit is live, that is, the status of this bit is in real time.	0x0	R
		0	No other active status bit reported by any other status command.		
		1	Active status bits are waiting to be read by one or more status commands.		

STATUS WORD REGISTER

Address: 0x79, Reset: 0x0000, Name: STATUS_WORD

This command provides status information for critical faults and all top level status commands in the device. The lower byte is also returned by STATUS_BYTE.

Table 22. Bit Descriptions for STATUS_WORD

Bits	Bit Name	Settings	Description	Reset	Access
15	VOUT_STATUS		V_{OUT} warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by STATUS_VOUT.		
		1	There are one or more active status bits to be read by STATUS_VOUT.		
14	IOUT_STATUS		I_{OUT} fault or warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by STATUS_IOUT.		
		1	There are one or more active status bits to be read by STATUS_IOUT.		
13	INPUT_STATUS		Input warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by STATUS_INPUT.		
		1	There are one or more active status bits to be read by STATUS_INPUT.		
12	MFR_STATUS		Manufacture specific fault or warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by STATUS_MFR_SPECIFIC.		
		1	There are one or more active status bits to be read by STATUS_MFR_SPECIFIC.		
11	PGB_STATUS		Power is not good. This bit is live.	0x0	R
		0	Output power is good. The voltage on the PWGIN pin is above the threshold and the voltage on the GATE pin is higher than the voltage on the VCC pin.		
		1	Output power is bad. The voltage on the PWGIN pin is below the threshold.		
[10:9]	RESERVED		Reserved.	0x0	RESERVED
8	FET_HEALTH_FAULT		FET health fault. This bit is latched.	0x0	R
		0	No FET faults are detected.		
		1	A fault condition is detected on the FET.		
7	RESERVED		Always set to 0.	0x0	RESERVED
6	HOTSWAP_OFF		Duplicate of corresponding bit in STATUS_BYTE.	0x0	R
5	RESERVED		Always set to 0.	0x0	RESERVED
4	IOUT_OC_FAULT		Duplicate of corresponding bit in STATUS_BYTE.	0x0	R
3	VIN_UV_FAULT		Duplicate of corresponding bit in STATUS_BYTE.	0x0	R
2	TEMP_FAULT		Duplicate of corresponding bit in STATUS_BYTE.	0x0	R
1	CML_FAULT		Duplicate of corresponding bit in STATUS_BYTE.	0x0	R
0	NONEABOVE_STATUS		Duplicate of corresponding bit in STATUS_BYTE.	0x0	R

OUTPUT VOLTAGE STATUS REGISTER

Address: 0x7A, Reset: 0x00, Name: STATUS_VOUT

This command provides status information for warnings related to VOUT.

Table 23. Bit Descriptions for STATUS_VOUT

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Always reads as 0.	0x0	RESERVED
6	VOUT_OV_WARN		VOUT overvoltage warning.	0x0	R
		0	No overvoltage condition on the output supply detected by the power monitor.		
		1	An overvoltage condition on the output supply was detected by the power monitor. This bit is latched.		
5	VOUT_UV_WARN		VOUT UV warning.	0x0	R
		0	No undervoltage condition on the output supply detected by the power monitor.		
		1	An undervoltage condition on the output supply is detected by the power monitor. This bit is latched.		
[4:0]	RESERVED		Always reads as 00000.	0x00	RESERVED

OUTPUT CURRENT STATUS REGISTER

Address: 0x7B, Reset: 0x00, Name: STATUS_IOUT

This command provides status information for faults and warnings related to I_{OUT}.

Table 24. Bit Descriptions for STATUS_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
7	IOUT_OC_FAULT		I_{OUT} overcurent fault.	0x0	R
		0	No overcurrent output fault detected.		
		1	The hot swap controller detects an overcurrent condition and the limit set by the components on the EFAULT or ESTART pin is exceeded, causing the hot swap gate drive to shut down. This bit is latched.		
6	RESERVED		Always reads as 0.	0x0	RESERVED
5	IOUT_OC_WARN		I_{OUT} overcurrent warning.	0x0	R
		0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
		1	An overcurrent condition is detected by the power monitor using the IOUT_OC_WARN_LIMIT command. This bit is latched.		
[4:0]	RESERVED		Always reads as 00000.	0x00	RESERVED

INPUT STATUS REGISTER

Address: 0x7C, Reset: 0x00, Name: STATUS_INPUT

This command provides status information for faults and warnings related to V_{IN} and P_{IN}.

Table 25. Bit Descriptions for STATUS_INPUT

Bits	Bit Name	Settings	Description	Reset	Access
7	VIN_OV_FAULT		V_{IN} overvoltage fault.	0x0	R
		0	No overvoltage detected on the OV pin.		
		1	An overvoltage was detected on the OV pin. This bit is latched.		
6	VIN_OV_WARN		V_{IN} overvoltage warning fault.	0x0	R
		0	No overvoltage condition on the input supply detected by the power monitor.		
		1	An overvoltage condition on the input supply was detected by the power monitor. This bit is latched.		

Bits	Bit Name	Settings	Description	Reset	Access
5	VIN_UV_WARN		V_{IN} undervoltage warning.	0x0	R
		0	No undervoltage condition on the input supply detected by the power monitor.		
		1	An undervoltage condition on the input supply was detected by the power monitor. This bit is latched.		
4	VIN_UV_FAULT		V_{IN} undervoltage fault.	0x0	R
		0	No undervoltage detected on the UVH/UVL pins.		
		1	An undervoltage was detected on the UVH/UVL pins. This bit is latched.		
[3:1]	RESERVED		Always reads as 000.	0x0	RESERVED
0	PIN_OP_WARN		P_{IN} overpower warning.	0x0	R
		0	No overpower condition on the input supply detected by the power monitor.		
		1	An overpower condition on the input supply was detected by the power monitor. This bit is latched.		

TEMPERATURE STATUS REGISTER

Address: 0x7D, Reset: 0x00, Name: STATUS_TEMPERATURE

This command provides status information for faults and warnings related to temperature.

Table 26. Bit Descriptions for STATUS_TEMPERATURE

Bits	Bit Name	Settings	Description	Reset	Access
7	OT_FAULT		Overtemperature fault.	0x0	R
		0	No overtemperature fault detected by the ADC.		
		1	An overtemperature fault was detected by the ADC. This bit is latched.		
6	OT_WARNING		Overtemperature warning.	0x0	R
		0	No overtemperature warning detected by the ADC.		
		1	An overtemperature warning was detected by the ADC. This bit is latched.		
5	RESERVED		Always reads as 0.	0x0	RESERVED
4	RESERVED		Always reads as 0.	0x0	RESERVED
[3:0]	RESERVED		Always reads as 0000.	0x0	RESERVED

MANUFACTURER SPECIFIC STATUS REGISTER

Address: 0x80, Reset: 0x00, Name: STATUS_MFR_SPECIFIC

This command provides status information for manufacturer specific faults and warnings.

Table 27. Bit Descriptions for STATUS_MFR_SPECIFIC

Bits	Bit Name	Settings	Description	Reset	Access
7	FET_HEALTH_FAULT		FET health fault.	0x0	R
		0	No FET health problems detected.		
		1	A FET health fault is detected. This bit is latched.		
6	UV_CMP_OUT		UV input comparator fault output.	0x0	R
		0	Input voltage to UVL/UVH pins is above threshold.		
		1	Input voltage to UVL/UVH pin is below threshold. This bit is live.		
5	OV_CMP_OUT		OV input comparator fault output.	0x0	R
		0	Input voltage to OV pin is below threshold.		
		1	Input voltage to OV pin is above threshold. This bit is live.		
4	SEVERE_OC_FAULT		Severe overcurrent fault.	0x0	R
		0	A severe overcurent is not detected by the hot swap.		
		1	A severe overcurrent is detected by the hot swap. This bit is latched.		

Bits	Bit Name	Settings	Description	Reset	Access
3	HS_INLIM_FAULT		Hot swap in limit fault.	0x0	R
		0	The hot swap has not actively limited the current into the load.		
		1	The hot swap has actively limited current into the load. This bit differs from the IOUT_OC_FAULT bit in that the HS_INLIM_FAULT bit is set immediately, whereas the IOUT_OC_FAULT bit is not set unless the limit set by the components on the ESET and ESTART pins is exceeded. This bit is latched.		
[2:0]	HS_SHUTDOWN_CAUSE		Cause of last hot swap shutdown. This bit is latched until the status registers are cleared.	0x0	R
		000	The hot swap is either enabled and working correctly, or is shut down using the OPERATION command.		
		001	An OT_FAULT condition occurred that caused the hot swap to shut down.		
		010	An IOUT_OC_FAULT condition occurred that caused the hot swap to shut down.		
		011	A FET_HEALTH_FAULT condition occurred that caused the hot swap to shut down.		
		100	A VIN_UV_FAULT condition occurred that caused the hot swap to shut down.		
		110	A VIN_OV_FAULT condition occurred that caused the hot swap to shut down.		

READ ENERGY REGISTER

Address: 0x86, Reset: 0x000000000000, Name: READ_EIN

This command reads the energy metering registers in a single operation to ensure time consistent data.

Table 28. Bit Descriptions for READ_EIN

Bits	Bit Name	Settings	Description	Reset	Access
[47:24]	SAMPLE_COUNT		This is the total number of P_{IN} samples acquired and accumulated in the energy count accumulator. Byte 5 is the high byte, Byte 4 is the middle byte, and Byte 3 is the low byte. This is an unsigned, 24-bit binary value.	0x000000	R
[23:16]	ROLLOVER_COUNT		Number of times that the energy count has rolled over, from 0x7FFF to 0x0000. This is an unsigned 8-bit binary value.	0x00	R
[15:0]	ENERGY_COUNT		Energy accumulator value in direct format. Byte 1 is the high byte, and Byte 0 is the low byte. Internally, the energy accumulator is a 24-bit value, but only the most significant 16 bits are returned with this command, expressed in direct format. Use the READ_EIN_EXT to access the nontruncated version.	0x0000	R

READ INPUT VOLTAGE REGISTER

Address: 0x88, Reset: 0x0000, Name: READ_VIN

This command reads the input voltage, V_{IN}, from the device.

Table 29. Bit Descriptions for READ_VIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_VIN		Input voltage from the SENSE+ pin measurement after averaging, expressed in direct format.	0x000	R

READ OUTPUT VOLTAGE REGISTER

Address: 0x8B, Reset: 0x0000, Name: READ_VOUT

This command reads the output voltage, V_{OUT}, from the device.

Table 30. Bit Descriptions for READ_VOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_VOUT		Input voltage from the VOUT pin measurement after averaging, expressed in direct format.	0x000	R

READ OUTPUT CURRENT REGISTER

Address: 0x8C, Reset: 0x0000, Name: READ_IOUT

This command reads the output current, I_{OUT}, from the device.

Table 31. Bit Descriptions for READ_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_IOUT		Output current derived from the SENSE+ and SENSE− sense pin voltage measurement after averaging, expressed in direct format.	0x000	R

READ TEMPERATURE 1 REGISTER

Address: 0x8D, Reset: 0x0000, Name: READ_TEMPERATURE_1

This command reads the temperature measured by the device.

Table 32. Bit Descriptions for READ_TEMPERATURE_1

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_TEMPERATURE_1		Temperature from the TEMP+ and TEMP− measurement, after averaging, expressed in direct format.	0x000	R

READ POWER REGISTER

Address: 0x97, Reset: 0x0000, Name: READ_PIN

This command reads the calculated input power, P_{IN}, from the device.

Table 33. Bit Descriptions for READ_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	READ_PIN		Input power calculation. Power is calculated as the product of individual samples of V_{IN} and I_{OUT}. These power calculations can be averaged, according to the settings of the PWR_AVG bits in the PMON_CONFIG register, before being presented to the READ_PIN register. Expressed in direct format.	0x0000	R

PMBUS REVISION REGISTER

Address: 0x98, Reset: 0x22, Name: PMBUS_REVISION

This command allows the system host to read the PMBus revision that the device supports.

Table 34. Bit Descriptions for PMBUS_REVISION

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	PMBUS_P1_REVISION	0010	PMBus Part I Support. Revision 1.2.	0x2	R
[3:0]	PMBUS_P2_REVISION	0010	PMBus Part II Support. Revision 1.2.	0x2	R

MANUFACTURER ID REGISTER

Address: 0x99, Reset: 0x494441, Name: MFR_ID

This command returns a string identifying the manufacturer of the device.

Table 35. Bit Descriptions for MFR_ID

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	MFR_ID		String identifying manufacturer as ADI (as ASCII code).	0x494441	R

MANUFACTURER MODEL REGISTER

Address: 0x9A, Reset: 0x41312D323732314D4441, Name: MFR_MODEL

This command returns a string identifying the specific model of the device.

Table 36. Bit Descriptions for MFR_MODEL

Bits	Bit Name	Settings	Description	Reset	Access
[79:0]	MFR_MODEL		String identifying model as ADM1272-1A (as ASCII code).	0x41312D323732314D4441	R

MANUFACTURER REVISION REGISTER

Address: 0x9B, Reset: 0x3532, Name: MFR_REVISION

The most significant byte is the ASCII revision of the hot swap and the least significant byte is the revision of the power management feature.

Table 37. Bit Descriptions for MFR_REVISION

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	MFR_REVISION		The upper byte is an ASCII character indicating the numerical revision of the hot swap feature. The lower byte is an ASCII character indicating the numerical revision of the power management feature.	0x3532	R

MANUFACTURER DATE REGISTER

Address: 0x9D, Reset: 0x313033303631, Name: MFR_DATE

This command returns a string identifying the manufacturing date of the device.

Table 38. Bit Descriptions for MFR_DATE

Bits	Bit Name	Settings	Description	Reset	Access
[47:0]	MFR_DATE		String identifying manufacturing date, in the form of YYMMDD. Example reset code of 1st March 2016 is shown.	0x313033303631	R

PROGRAMMABLE RESTART TIME REGISTER

Address: 0xCC, Reset: 0x64, Name: RESTART_TIME

Table 39. Bit Descriptions for RESTART_TIME

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	RESTART_TIME		This byte controls the off time of the hot swap restart feature. Default value gives 10.1 sec.	0x64	RW
		0x00	0.1 sec.		
		0x01	0.2 sec.		
		0x64	10.1 sec.		
		0xFF	25.6 sec.		

PEAK OUTPUT CURRENT REGISTER

Address: 0xD0, Reset: 0x0000, Name: PEAK_IOUT

This command reports the peak output current, I_{OUT}. Writing 0x0000 with this command resets the peak value.

Table 40. Bit Descriptions for PEAK_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_IOUT		Peak output current measurement, I_{OUT}, expressed in direct format. If averaging has been enabled, the average values are used in this calculation.	0x000	R

PEAK INPUT VOLTAGE REGISTER

Address: 0xD1, Reset: 0x0000, Name: PEAK_VIN

This command reports the peak input voltage, V_{IN}, measured at the SENSE+ pin. Writing 0x0000 with this command resets the peak value.

Table 41. Bit Descriptions for PEAK_VIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_VIN		Peak input voltage measurement, V_{IN}, measured at the SENSE+ pin. Expressed in direct format. If averaging has been enabled, the average values are used in this calculation.	0x000	R

PEAK OUTPUT VOLTAGE REGISTER

Address: 0xD2, Reset: 0x0000, Name: PEAK_VOUT

This command reports the peak output voltage, V_{OUT}. Writing 0x0000 with this command resets the peak value.

Table 42. Bit Descriptions for PEAK_VOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_VOUT		Peak output voltage measurement, V_{OUT}, expressed in direct format. If averaging is enabled, the average values are used in this calculation.	0x000	R

POWER MONITOR CONTROL REGISTER

Address: 0xD3, Reset: 0x01, Name: PMON_CONTROL

This command is used to start and stop the power monitor.

Table 43. Bit Descriptions for PMON_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Always reads as 0000000.	0x00	RESERVED
0	CONVERT		Convert enable.	0x1	RWAS
		0	Power monitor is not running.		
		1	Power monitor is sampling. Default. In single-shot mode, this bit clears itself after one complete cycle. In continuous mode, this bit must be written to 0 to stop sampling. A rising edge on a conversion (CONV) input pin sets this bit to 1. During sampling, additional rising edges on CONV are ignored.		

POWER MONITOR CONFIGURATION REGISTER

Address: 0xD4, Reset: 0x3F35, Name: PMON_CONFIG

This command configures the power monitor. Different combinations of channels can be included in the sampling round robin, and averaging can be set for different measurements.

Table 44. Bit Descriptions for PMON_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	TSFILT		Temperature sensor filter enable.	0x0	RW
		0	Filter disabled. Data sheet specifications are given with the temperature sensor filter disabled.		
		1	Filter enabled.		
14	SIMULTANEOUS		Signals on V_{IN} and I_{OUT} are sampled simultaneously.	0x0	RW
		0	Disabled. Data sheet specifications are given with simultaneous sampling disabled.		
		1	Enabled. Power monitoring accuracy is slightly reduced.		
[13:11]	PWR_AVG		P_{IN} averaging.	0x7	RW
		000	Disables sample averaging for power.		
		001	Sets sample averaging for power to two samples.		
		010	Sets sample averaging for power to four samples.		
		011	Sets sample averaging for power to eight samples.		
		100	Sets sample averaging for power to 16 samples.		
		101	Sets sample averaging for power to 32 samples.		
		110	Sets sample averaging for power to 64 samples.		
		111	Sets sample averaging for power to 128 samples.		
[10:8]	VI_AVG		$V_{IN}/V_{OUT}/I_{OUT}$ averaging.	0x7	RW
		000	Disables sample averaging for current and voltage.		
		001	Sets sample averaging for current and voltage to two samples.		
		010	Sets sample averaging for current and voltage to four samples.		
		011	Sets sample averaging for current and voltage to eight samples.		
		100	Sets sample averaging for current and voltage to 16 samples.		
		101	Sets sample averaging for current and voltage to 32 samples.		
		110	Sets sample averaging for current and voltage to 64 samples.		
		111	Sets sample averaging for current and voltage to 128 samples.		
[7:6]	RESERVED		Always reads as 00.	0x0	RESERVED
5	VRANGE			0x1	RW
		0	Sets the input divider of V_{IN} (on SENSE+) to give a full scale at 60 V.		
		1	Sets the input divider of V_{IN} (on SENSE+) to give a full scale at 100 V.		

Bits	Bit Name	Settings	Description	Reset	Access
4	PMON_MODE		Conversion mode.	0x1	RW
		0	Single-shot sampling.		
		1	Continuous sampling.		
3	TEMP1_EN		Enable temperature sampling.	0x0	RW
		0	Temperature sampling disabled.		
		1	Temperature sampling enabled.		
2	VIN_EN		Enable V_{IN} sampling.	0x1	RW
		0	V_{IN} sampling disabled.		
		1	V_{IN} sampling enabled.		
1	VOUT_EN		Enable V_{OUT} sampling.	0x0	RW
		0	V_{OUT} sampling disabled.		
		1	V_{OUT} sampling enabled.		
0	IRANGE		V_{IN} sense range.	0x1	RW
		0	Sets the gain on the current sense channel to give a full scale at ($V_{SENSE+} - V_{SENSE-}$) = 15 mV.		
		1	Sets the gain on the current sense channel to give a full scale at ($V_{SENSE+} - V_{SENSE-}$) = 30 mV.		

ALERT 1 CONFIGURATION REGISTER

Address: 0xD5, Reset: 0x0000, Name: ALERT1_CONFIG

This commands allows different combinations of faults and warnings to be configured on the GPO1/$\overline{\text{ALERT1}}$/CONV output pin. The GPO1/$\overline{\text{ALERT1}}$/CONV pin can operate in different modes as configured by the DEVICE_CONFIG command.

Table 45. Bit Descriptions for ALERT1_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	FET_HEALTH_FAULT_EN1		FET health fault alert mode enable (not available in source mode).	0x0	RW
14	IOUT_OC_FAULT_EN1		I_{OUT} overcurrent fault alert mode enable (not available in source mode).	0x0	RW
13	VIN_OV_FAULT_EN1		V_{IN} overvoltage fault alert mode enable (not available in source mode).	0x0	RW
12	VIN_UV_FAULT_EN1		V_{IN} undervoltage fault alert mode enable (not available in source mode).	0x0	RW
11	CML_ERROR_EN1		Communications error alert mode enable (not available in source mode).	0x0	RW
10	IOUT_OC_WARN_EN1		I_{OUT} overcurrent warning alert and source mode enable.	0x0	RW
9	HYSTERETIC_EN1		I_{OUT} hysteretic warning alert and source mode enable.	0x0	RW
8	VIN_OV_WARN_EN1		V_{IN} overvoltage warning alert and source mode enable.	0x0	RW
7	VIN_UV_WARN_EN1		V_{IN} Undervoltage warning alert and source mode enable.	0x0	RW
6	VOUT_OV_WARN_EN1		V_{OUT} overvoltage warning alert and source mode enable.	0x0	RW
5	VOUT_UV_WARN_EN1		V_{OUT} undervoltage warning alert and source mode enable.	0x0	RW
4	HS_INLIM_EN1		Hot swap in limit alert and source mode enable.	0x0	RW
3	PIN_OP_WARN_EN1		P_{IN} overpower warning alert and source mode enable.	0x0	RW
2	OT_FAULT_EN1		Overtemperature fault alert and source mode enable.	0x0	RW
1	OT_WARN_EN1		Overtemperature warning alert and source mode enable.	0x0	RW
0	INEG_EN1		Negative current detected alert and source mode enable.	0x0	RW

ALERT 2 CONFIGURATION REGISTER

Address: 0xD6, Reset: 0x0000, Name: ALERT2_CONFIG

This commands allows different combinations of faults and warnings to be configured on the GPO2/$\overline{\text{ALERT2}}$ output pin. The pin can operate in different modes as configured by the DEVICE_CONFIG command.

Table 46. Bit Descriptions for ALERT2_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	FET_HEALTH_FAULT_EN2		FET health fault alert mode enable (not available in source mode).	0x0	RW
14	IOUT_OC_FAULT_EN2		I_{OUT} overcurrent fault alert mode enable (not available in source mode).	0x0	RW
13	VIN_OV_FAULT_EN2		V_{IN} overvoltage fault alert mode enable (not available in source mode).	0x0	RW
12	VIN_UV_FAULT_EN2		V_{IN} undervoltage fault alert mode enable (not available in source mode).	0x0	RW
11	CML_ERROR_EN2		Communications error alert mode enable (not available in source mode).	0x0	RW
10	IOUT_OC_WARN_EN2		I_{OUT} overcurrent warning alert and source mode enable.	0x0	RW
9	HYSTERETIC_EN2		I_{OUT} hysteretic warning alert and source mode enable.	0x0	RW
8	VIN_OV_WARN_EN2		V_{IN} overvoltage warning alert and source mode enable.	0x0	RW
7	VIN_UV_WARN_EN2		V_{IN} undervoltage warning alert and source mode enable.	0x0	RW
6	VOUT_OV_WARN_EN2		V_{OUT} overvoltage warning alert and source mode enable.	0x0	RW
5	VOUT_UV_WARN_EN2		V_{OUT} undervoltage warning alert and source mode enable.	0x0	RW
4	HS_INLIM_EN2		Hot swap in limit alert and source mode enable.	0x0	RW
3	PIN_OP_WARN_EN2		P_{IN} overpower warning alert and source mode enable.	0x0	RW
2	OT_FAULT_EN2		Overtemperature fault alert and source mode enable.	0x0	RW
1	OT_WARN_EN2		Overtemperature warning alert and source mode enable.	0x0	RW
0	INEG_EN2		Negative current detected alert and source mode enable.	0x0	RW

PEAK TEMPERATURE REGISTER

Address: 0xD7, Reset: 0x0000, Name: PEAK_TEMPERATURE

This command reports the peak measured temperature. Writing 0x0000 to this command resets the peak value.

Table 47. Bit Descriptions for PEAK_TEMPERATURE

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_TEMPERATURE		Peak temperature measurement, expressed in direct format.	0x000	R

DEVICE CONFIGURATION REGISTER

Address: 0xD8, Reset: 0x0008, Name: DEVICE_CONFIG

This command configures the hot swap overcurrent threshold and filtering, and GPO1/GPO2 output modes. Note that multifunction pins, such as GPO1/$\overline{\text{ALERT1}}$/CONV, are referred to either by the entire pin name or by a single function of the pin, for example, GPO1, when only that function is relevant.

Table 48. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	RNDSTART_DIS		Disable the random start function.	0x0	RW
		0	Hot swap random start feature enabled.		
		1	Hot swap random start feature disabled.		
[14:13]	OC_FILT_SELECT		Severe overcurrent filter select.	0x0	RW
		00	500 ns. Hot swap severe overcurrent filter time.		
		01	1 µs.		
		10	5 µs.		
		11	10 µs.		

Bits	Bit Name	Settings	Description	Reset	Access
12	FAST_GATE_DIS		Disable fast gate recovery mode.	0x0	RW
		0	Hot swap fast gate recovery after a severe over current enabled.		
		1	Disabled.		
11	FHDIS		Disable FET health capabilities.	0x0	RW
		0	Hot swap external FET health monitoring feature enabled.		
		1	Disabled.		
10	PWR_HYST_EN		When enabled the hysteresis functions apply to power rather than current.	0x0	RW
[9:8]	GPO2_MODE		GPO2 configuration mode.	0x0	RW
		00	Alert mode. The GPO2 output is driven by the SMBus alert signal generated by the ALERT2_CONFIG.		
		01	General-purpose digital pin mode. In this mode, GPO2_INVERT controls the polarity of the output. If set, this bit disables the output and allows the pin to be used in input mode only.		
		10	Reserved.		
		11	Source mode. The output pin is driven with the value of the warning or fault bit selected by ALERT2_CONFIG.		
7	GPO2_INVERT		GPO invert mode.	0x0	RW
		0	In SMBus alert mode the output is not inverted, and active low. In general-purpose mode, the output is set low.		
		1	In SMBus alert mode the output is inverted, and active high. In general-purpose mode, the output is set high. Use general-purpose mode and set GPO2_INVERT high to configure this pin as a general-purpose digital input.		
[6:5]	GPO1_MODE		GPO1 configuration mode.	0x0	RW
		00	Alert mode. The GPO1 output is driven by the SMBus alert signal generated by ALERT1_CONFIG.		
		01	General-purpose digital pin mode. In this mode, GPO1_INVERT controls the polarity of the output. If set, this bit disables the output and allows the pin to be used in input mode only.		
		10	Convert mode. The GPO1/$\overline{\text{ALERT1}}$/CONV pin is configured as the convert (CONV) input pin.		
		11	Source mode. The output pin is driven with the value of the warning or fault bit selected by ALERT1_CONFIG.		
4	GPO1_INVERT		GPO1 invert mode.	0x0	RW
		0	In SMBus alert mode, the output is not inverted, and active low. In general-purpose mode, the output is set low.		
		1	In SMBus alert mode, the output is inverted, and active high. In general-purpose mode, the output is set high. Use general-purpose mode and set GPO1_INVERT high to configure this pin up as a general-purpose digital input.		
[3:2]	OC_TRIP_SELECT		Severe overcurrent threshold select.	0x2	RW
		00	400% hot swap severe overcurrent trip threshold as a % of current regulation level.		
		01	300%.		
		10	200% (default).		
		11	150%.		
1	OC_RETRY_DIS			0x0	RW
		0	Allows the hot swap system to attempt to keep the output on after a severe over current event.		
		1	Hot swap turns off after a severe over current event.		
0	PWRGD_SENSE		Always reads as 0.	0x0	RW
		0	Active high. When the V_{OUT} voltage is good (sensed via the PWGIN pin), the open-drain output is high impedance, which allows an external resistor to pull the pin up.		
		1	Active low. When the V_{OUT} voltage is good (sensed via the PWGIN pin), the open-drain output is enabled and drives the PWRGD pin low.		

POWER CYCLE REGISTER

Address: 0xD9, Reset: 0x, Name: POWER_CYCLE

This command is provided to allow a processor to request the hot swap to turn off and turn back on again a few seconds later. This is useful in the event that the hot swap output is powering the processor.

This command does not require any data.

PEAK POWER REGISTER

Address: 0xDA, Reset: 0x0000, Name: PEAK_PIN

This command reports the peak input power, P_{IN}. Writing 0x0000 with this command resets the peak value.

Table 49. Bit Descriptions for PEAK_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PEAK_PIN		Peak input power calculation, PIN, expressed in direct format.	0x0000	R

READ POWER (EXTENDED) REGISTER

Address: 0xDB, Reset: 0x000000, Name: READ_PIN_EXT

This command reads the extended precision version of the calculated input power, P_{IN}, from the device.

Table 50. Bit Descriptions for READ_PIN_EXT

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	READ_PIN_EXT		Extended precision version of peak input power calculation, P_{IN}, expressed in direct format.	0x000000	R

READ ENERGY (EXTENDED) REGISTER

Address: 0xDC, Reset: 0x0000000000000000, Name: READ_EIN_EXT

This command reads the extended precision Energy Metering registers in a single operation to ensure time consistent data.

Table 51. Bit Descriptions for READ_EIN_EXT

Bits	Bit Name	Settings	Description	Reset	Access
[63:40]	SAMPLE_COUNT		This is the total number of P_{IN} samples acquired and accumulated in the energy count accumulator. This is an unsigned 24-bit binary value. Byte 7 is the high byte, Byte 6 is the middle byte, and Byte 5 is the low byte.	0x000000	R
[39:24]	ROLLOVER_EXT		Number of times that the energy count has rolled over, from 0x7FFFFF to 0x000000. This is an unsigned 16-bit binary value. Byte 4 is the high byte, and Byte 3 is the low byte.	0x0000	R
[23:0]	ENERGY_EXT		Extended precision energy accumulator value in direct format. Byte 2 is the high byte, and Byte 0 is the low byte.	0x000000	R

HYSTERESIS LOW LEVEL REGISTER

Address: 0xF2, Reset: 0x0000, Name: HYSTERESIS_LOW

This command sets the lower threshold used to generate the hysteretic output signal that can be made available on a GPO pin.

Table 52. Bit Descriptions for HYSTERESIS_LOW

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	HYSTERESIS_LOW		Value setting the lower hysteresis threshold, expressed in direct format.	0x000	RW

HYSTERESIS HIGH LEVEL REGISTER

Address: 0xF3, Reset: 0xFFFF, Name: HYSTERESIS_HIGH

This command sets the higher threshold used to generate the hysteretic output signal that can be made available on a GPO pin.

Table 53. Bit Descriptions for HYSTERESIS_HIGH

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	HYSTERESIS_HIGH		Value setting the higher hysteresis threshold, expressed in direct format.	0xFFFF	RW

HYSTERESIS STATUS REGISTER

Address: 0xF4, Reset: 0x00, Name: STATUS_HYSTERESIS

This status register reports if the hysteretic comparison is above or below the user defined thresholds, and the IOUT_OC_WARN status bit as well.

Table 54. Bit Descriptions for STATUS_HYSTERESIS

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Always reads as 0000.	0x0	RESERVED
3	IOUT_OC_WARN		I_{OUT} overcurrent warning.	0x0	R
		0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
		1	An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
2	HYST_STATE		Hysteretic comparison output.	0x0	R
		0	Comparison output low.		
		1	Comparison output high.		
1	HYST_GT_HIGH		Hysteretic upper threshold comparison.	0x0	R
		0	Compared value is below upper threshold.		
		1	Compared value is above upper threshold.		
0	HYST_LT_LOW		Hysteretic lower threshold comparison.	0x0	R
		0	Compared value is above lower threshold.		
		1	Compared value is below lower threshold.		

GPIO PIN STATUS REGISTER

Address: 0xF5, Reset: 0x00, Name: STATUS_GPIO

STATUS_GPIO is the readback register for the status of the GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins.

Table 55. Bit Descriptions for STATUS_GPIO

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Always reads as 0.	0x0	RESERVED
6	GPIO2_HIGH		The GPO2/$\overline{\text{ALERT2}}$ pin has been high at some time since the last time this register was read.	0x0	R
5	GPIO2_LOW		The GPO2/$\overline{\text{ALERT2}}$ pin has been low at some time since the last time this register was read.	0x0	R
4	GPIO2_STATE		Live state of the GPIO2 pin.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
3	RESERVED		Always reads as 0.	0x0	RESERVED
2	GPIO1_HIGH		The GPO1/$\overline{\text{ALERT1}}$/CONV pin has been high at some time since the last time this register was read.	0x0	R
1	GPIO1_LOW		The GPO1/$\overline{\text{ALERT1}}$/CONV pin has been low at some time since the last time this register was read.	0x0	R
0	GPIO1_STATE		Live state of the GPO1/$\overline{\text{ALERT1}}$/CONV pin.	0x0	R

START-UP CURRENT LIMIT REGISTER

Address: 0xF6, Reset: 0x000F, Name: STRT_UP_IOUT_LIM

This command sets the current limit initially used while the hot swap is turning on the FET.

Table 56. Bit Descriptions for STRT_UP_IOUT_LIM

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED		Always reads as 0x00.	0x00	RESERVED
[7:4]	RESERVED		Always reads as 0000.	0x0	RESERVED
[3:0]	STRT_UP_IOUT_LIM		Current limit used during startup, expressed in direct format.	0xF	RW
		0000	Current limit equal to (ISTART × 1/16) (hot swap start up current limit level).		
		0001	Current limit equal to (ISTART × 2/16).		
		…	…		
		1110	Current limit equal to (ISTART × 15/16).		
		1111	Current limit equal to ISTART.		

OUTLINE DIMENSIONS

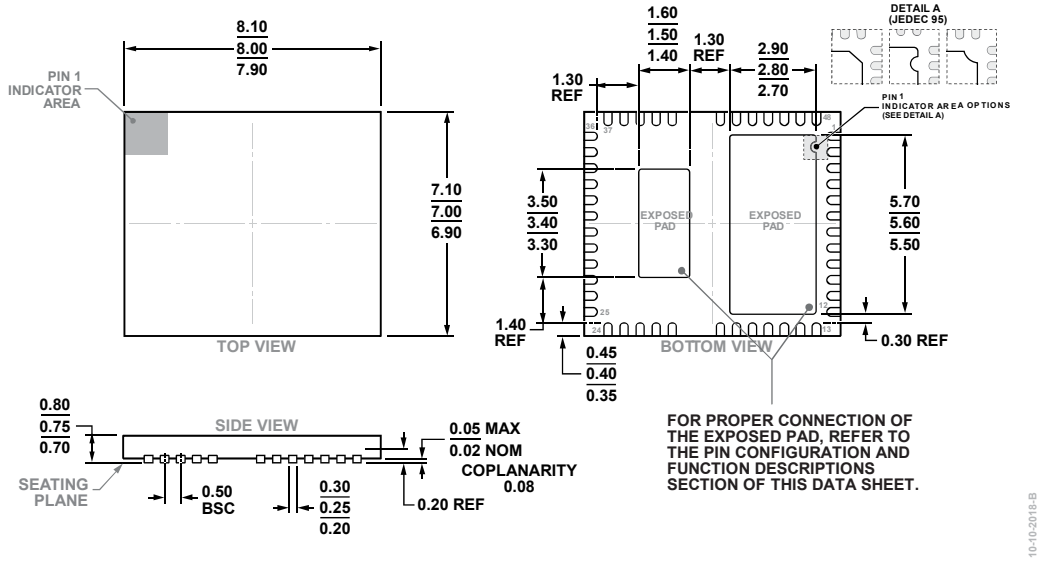


Figure 52. 48-Lead Lead Frame Chip Scale Package [LFCSP]
8 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-18)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM1272-1ACPZ	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP], Tray	CP-48-18
ADM1272-1ACPZ-RL	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP], 13" Reel	CP-48-18
EVAL-ADM1272EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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