Super Sequencer with Interchip Bus and Nonvolatile Fault Recording

Data Sheet

ADM1260

FEATURES

- Complete supervisory and sequencing solution for up to 10 supplies per device
- Interchip bus (ICB) simplifies multidevice connections and sequencing system operation
  - Supports up to 4 devices
- 16 event deep black box nonvolatile fault recording
- 10 supply fault detectors enable supervision of supplies
  - <0.5% accuracy at all voltages at 25°C
  - <1.0% accuracy across all voltages and temperatures
- 5 selectable input attenuators allow supervision of supplies
  - 14.4 V on VH and 6.0 V on VP1 to VP4 (VPx)
- 5 dual function inputs: VX1 to VX5 (VXx)
  - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
  - General-purpose logic input
- 10 programmable driver outputs: PDO1 to PDO10 (PDOx)
  - Open-collector with an external pull-up resistor
  - Push/pull output, driven to VDDCAP or VPx
  - Open-collector with weak pull-up to VDDCAP or VPx
  - Internally charge pumped high drive for use with external N-FET (PDO1 to PDO6 only)
- Sequencing engine (SE) implements state machine control of the PDOx outputs
  - State changes conditional on input events
  - Enables complex control of boards
  - Power-up and power-down sequence control
  - Fault event handling
  - Interrupt generation on warnings
  - Watchdog function can be integrated in the SE
  - Program software control of sequencing through the SMBus
- Complete voltage margining solution for 6 voltage rails
- 6 output voltage 8-bit DACs (0.300 V to 1.552 V) allow voltage adjustment via dc-to-dc converter trim/feedback node
- 12-bit ADC for readback of all supervised voltages
- Reference input (REFIN) with two input options
  - Driven directly from the 2.048 V (±0.25%) REFOUT pin
  - External reference for improved ADC performance
- Powered by the highest voltage on either VPx or VH
  - Voltage on VPx or VH must be greater than the undervoltage lockout (UVLO) threshold
- Electronically erasable programmable read-only memory (EEPROM)
- Industry-standard, 2-wire bus interface (SMBus)
- PDOx pins guaranteed low with VH and VPx = 1.2 V
- Available in a 40-lead, 6 mm × 6 mm LFCSP package

FUNCTIONAL BLOCK DIAGRAM

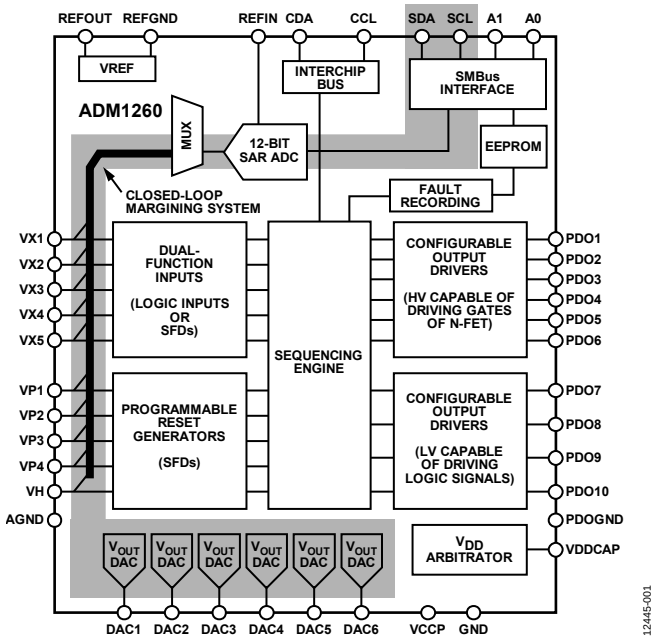


Figure 1.

APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- Digital signal processor (DSP)/field programmable gate array (FPGA) supply sequencing
- In-circuit testing of margined supplies

Rev. 0 Document Feedback

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REVISION HISTORY

4/16—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM1260 Super Sequencer® is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple supply systems.

A high speed interchip bus (ICB) allows multiple devices to be easily linked together. It is possible to create a system capable of sequencing up to 40 supplies and monitoring up to 37 supplies. Using the ADI Power Studio™ software, the operation of the ICB is transparent to the user, making multiple devices appear to operate as a single virtual sequencer.

In addition to these functions, the ADM1260 integrates a 12-bit analog-to-digital converter (ADC) and six 8-bit voltage output digital-to-analog converters (DACs). Use the ADC and the DACs to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or the reference of a dc-to-dc converter using the DAC outputs.

Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify board functionality at −5% of nominal supplies), or it can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

The device also provides up to 10 programmable inputs for monitoring undervoltage faults, overvoltage faults, or out of window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of these programmable outputs can also provide an output of up to 12 V for driving the gate of an N-FET that can be placed in the path of a supply.

The logical core of the device is a sequencing engine (SE). This state machine-based construction provides up to 61 different states. This design enables very flexible sequencing of the outputs, based on the condition of the inputs.

A block of nonvolatile EEPROM is available that can be used to store user defined information and can also be used to hold a number of fault records that are written by the sequencing engine, as defined by the user when a particular fault or sequence occurs.

The device is controlled via configuration data that can be programmed into an EEPROM. The entire configuration can be programmed using an intuitive graphical user interface (GUI)-based software package provided by Analog Devices, Inc., the ADI Power Studio software.

DETAILED FUNCTIONAL BLOCK DIAGRAM

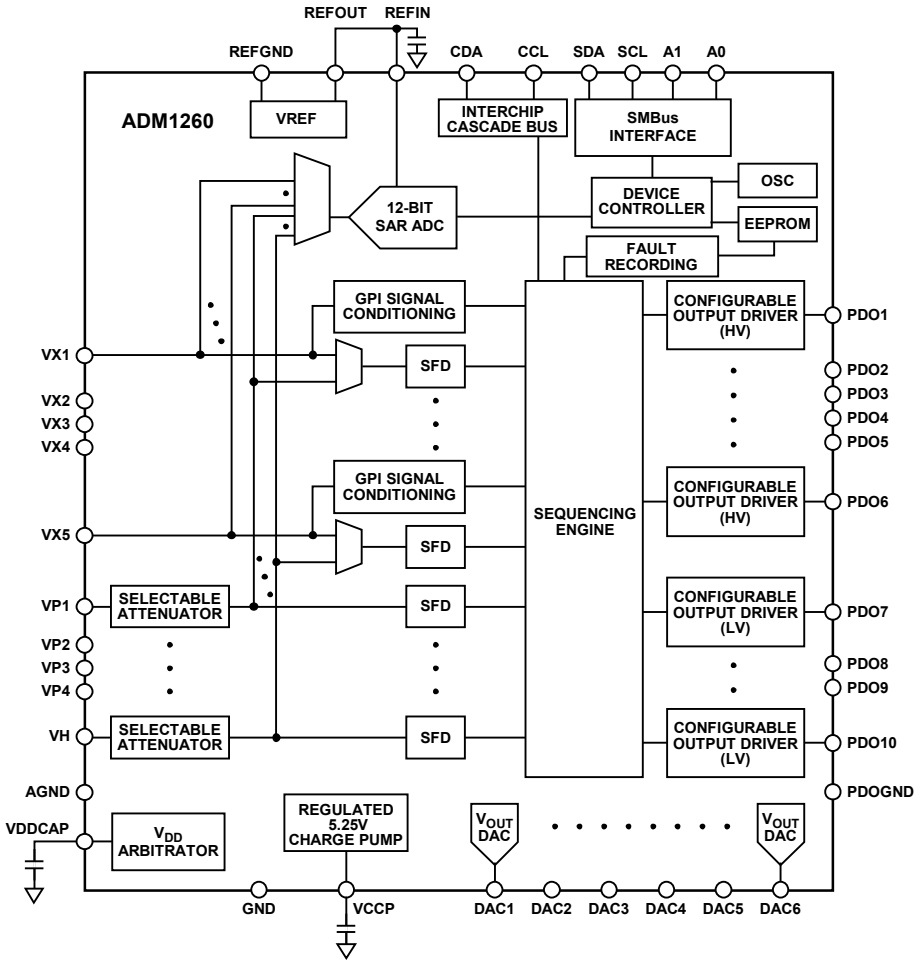


Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

VH = 3.0 V to 14.4 V,[1] VPx = 3.0 V to 6.0 V,[1] T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY ARBITRATION					
VH, VPx	3.0			V	Minimum supply required on one of VPx or VH pins
VPx			6.0	V	Maximum VDDCAP = 5.1 V, typical
VH			14.4	V	VDDCAP = 4.75 V
VDDCAP	2.7	4.75	5.4	V	Regulated low dropout (LDO) output
C_{VDDCAP}	10			µF	Minimum recommended decoupling capacitance
POWER SUPPLY					
Supply Current, I_{VH}, I_{VPx}		4.5	6.5	mA	VDDCAP = 4.75 V, PDO1 to PDO10 off, DACs off, ADC off
Additional Currents					
All PDOx FET Drivers On		1		mA	VDDCAP = 4.75 V, PDO1 to PDO6 loaded with 1 µA each, PDO7 to PDO10 off
Current Available from VDDCAP			2	mA	Maximum additional load that can be drawn from all PDO pull-ups to VDDCAP
DAC Supply Currents		2.2		mA	Six DACs on with 100 µA maximum load on each
ADC Supply Current		1		mA	Running round robin loop
EEPROM Erase Current		10		mA	1 ms duration only, VDDCAP = 3 V
SUPPLY FAULT DETECTORS					
VH					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Midrange and high range
Detection Ranges					
High Range	6.0		14.4	V	
Midrange	2.5		6.0	V	
VPx					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Low range and midrange
Detection Ranges					
Midrange	2.5		6.0	V	
Low Range	1.25		3.00	V	
Ultralow Range	0.573		1.375	V	No input attenuation error
VXx					
Input Impedance	1			MΩ	
Detection Range					
Ultralow Range	0.573		1.375	V	No input attenuation error
Absolute Accuracy			±1	%	VREF error + DAC nonlinearity + comparator offset error + input attenuation error (±0.5% at 25°C)
Threshold Resolution		8		Bits	
Digital Glitch Filter		0		µs	Minimum programmable filter length
		100		µs	Maximum programmable filter length

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG-TO-DIGITAL CONVERTER					
Signal Range	0		V_{REFIN}	V	The ADC can convert signals presented to the VH, VPx, and VXx pins; the VPx and VH input signals are attenuated depending on the selected range; a signal at the pin corresponding to the selected range is from 0.573 V to 1.375 V at the ADC input
Input Reference Voltage on REFIN Pin, V_{REFIN}		2.048		V	
Resolution		12		Bits	
Integral Nonlinearity (INL)			±2.5	LSB	Endpoint corrected, V_{REFIN} = 2.048 V
Gain Error			±0.05	%	V_{REFIN} = 2.048 V
Conversion Time		0.44		ms	One conversion on one channel
		84		ms	All 12 channels selected, 16× averaging enabled
Offset Error			±2	LSB	V_{REFIN} = 2.048 V
Input Noise		0.25		LSB rms	Direct input (no attenuator)
BUFFERED VOLTAGE OUTPUT DACs					
Resolution		8		Bits	
Code 0x7F Output Voltage					Six DACs are individually selectable for centering on one of four output voltage ranges
Range 1	0.592	0.6	0.603	V	
Range 2	0.796	0.8	0.803	V	
Range 3	0.996	1	1.003	V	
Range 4	1.246	1.25	1.253	V	
Output Voltage		601.25		mV	Reflects the DAC output voltage range, independent of center point
LSB Step Size		2.36		mV	
INL			±0.75	LSB	Endpoint corrected
DNL			±0.4	LSB	
Gain Error			1	%	
Maximum Load Current					
Source		100		µA	
Sink		100		µA	
Maximum Load Capacitance			50	pF	
Settling Time to 50 pF Load			2	µs	
Load Regulation		2.5		mV	Per mA
Power Supply Rejection Ratio (PSRR)		60		dB	DC
		40		dB	100 mV step in 20 ns with 50 pF load
REFERENCE OUTPUT					
Reference Output Voltage	2.043	2.048	2.053	V	No load
Load Regulation		−0.25		mV	Sourcing current, $I_{DACxMAX}$ = −100 µA
		0.25		mV	Sinking current, $I_{DACxMAX}$ = 100 µA
Minimum Load Capacitance	1			µF	Capacitor required for decoupling, stability
PSRR		60		dB	DC
PROGRAMMABLE DRIVER OUTPUTS					
High Voltage Charge Pump Mode (PDO1 to PDO6)					
Output Impedance		500		kΩ	
Output Voltage When PDOx is High (V_{OH})	11	12.5	14	V	Current drawn when PDOx is high (I_{OH}) = 0 µA
	10.5	12	13.5	V	I_{OH} = 1 µA
	8	10	13.5	V	I_{OH} = 7 µA[2]
Average Output Current (I_{OUTAVG})		20		µA	2 V < V_{OH} < 7 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Standard (Digital Output) Mode (PDO1 to PDO10)					
V_{OH}	2.4			V	Pull-up resistor to VDDCAP or VPx (V_{PU}) = 2.7 V, I_{OH} = 0.5 mA
			4.5	V	V_{PU} to VPx = 6.0 V, I_{OH} = 0 mA
	V_{PU} − 0.3			V	V_{PU} ≤ 2.7 V, I_{OH} = 0.5 mA
Output Voltage When PDOx is Low (V_{OL})	0		0.50	V	I_{OL} = 20 mA
Output Sink Current When PDOx is Low (I_{OL}[2])			20	mA	Maximum sink current per PDOx pin
Total Sink Current of PDOx Pins (I_{SINK}[2])			60	mA	Maximum total sink for all PDOx pins
$R_{PULL-UP}$	16	20	29	kΩ	Internal pull-up resistor
Maximum Current Drawn from VPx When PDOx is Internally Pulled Up to VPx (I_{SOURCE})[2]			2	mA	Current load on any VPx pull-up resistors, that is, the total source current available through any number of the PDOx pull-up switches configured onto any one VPx pin
Three-State Output Leakage Current			10	µA	V_{PDO} = 14.4 V
Oscillator Frequency	90	100	110	kHz	All on-chip time delays are derived from this clock
DIGITAL INPUTS (VXx, A0, A1)					
Input Voltage					
High, V_{IH}	2.0			V	Maximum V_{IN} = 5.5 V
Low, V_{IL}			0.8	V	Maximum V_{IN} = 5.5 V
Input Current					
High, I_{IH}	−1			µA	V_{IN} = 5.5 V
Low, I_{IL}			1	µA	V_{IN} = 0 V
Input Capacitance		5		pF	
Programmable Pull-Down Current, $I_{PULL-DOWN}$		20		µA	VDDCAP = 4.75 V, T_A = 25°C, if known logic state is required
SERIAL BUS, ICB DIGITAL INPUTS/ OUTPUT (SDA, SCL, CDA, CCL)					
Input Voltage					
High, V_{IH}	2.0			V	
Low, V_{IL}			0.8	V	
Input Low Current, I_{IL}			1	µA	V_{IN} = 0 V
Output Low Voltage, V_{OL}[2]			0.4	V	I_{OUT} = −3.0 mA
CDA, CCL Input Glitch Filter, t_{SP}		50		ns	
CDA, CCL Output Low Current, I_{OL}			5	mA	V_{OL} = 0.4 V
SDA, SCL SERIAL BUS TIMING[3]					See Figure 40
Clock Frequency, f_{SCLK}			400	kHz	
Bus Free Time, t_{BUF}	1.3			µs	
Start Setup Time, $t_{SU;STA}$	0.6			µs	
Stop Setup Time, $t_{SU;STO}$	0.6			µs	
Start Hold Time, $t_{HD;STA}$	0.6			µs	
SCL Low Time, t_{LOW}	1.3			µs	
SCL High Time, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_R			300	ns	
SCL, SDA Fall Time, t_F			300	ns	
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	250			ns	
CDA, CCL SERIAL BUS[3]					
Clock Frequency, f_{SCLK}			400	kHz	
Bus Capacitance			240	pF	I_{OL} = 5mA
Pin Capacitance			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SEQUENCING ENGINE TIMING					
State Change Time		45		µs	
Black Box (Exit)		350		µs	With delay or timeout configured as 0 µs in the state

[1] At least one of the VH and VPx pins must be ≥ 3.0 V to maintain the device supply on VDDCAP.
[2] Specification is not production tested but is supported by characterization data at initial product release.
[3] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VH	16 V
VPx	7 V
VXx	−0.3 V to +6.5 V
A0, A1	−0.3 V to +7 V
REFIN, REFOUT	5 V
VDDCAP, VCCP	6.5 V
DACx	6.5 V
PDOx	16 V
SDA, SCL, CDA, CCL	7 V
GND, AGND, PDOGND, REFGND	−0.3 V to +0.3 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature ($T_{J\,MAX}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering Vapor Phase, 60 sec	215°C
ESD Rating, All Pins	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead LFCSP	26.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

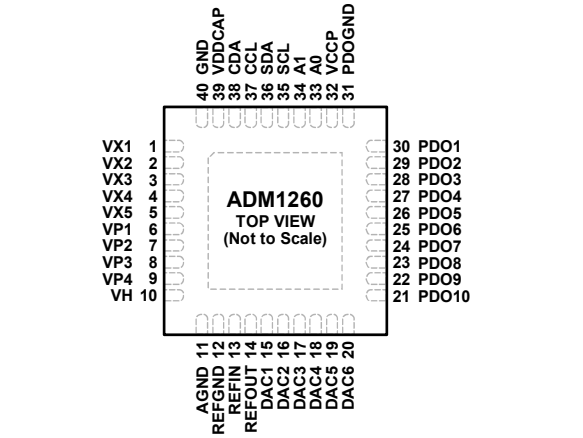


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 5	VX1 to VX5 (VXx)	High Impedance Inputs to Supply the Fault Detectors. Fault thresholds can be set from 0.573 V to1.375 V. Alternatively, use these pins as general-purpose logic inputs.
6 to 9	VP1 to VP4 (VPx)	Low Voltage Inputs to Supply the Fault Detectors. Three input ranges can be set by altering the input attenuation on a potential divider connected to these pins, the output of which connects to a supply fault detector. These pins allow thresholds from 2.5 V to 6.0 V, from 1.25 V to 3.00 V, and from 0.573 V to 1.375 V.
10	VH	High Voltage Input to Supply the Fault Detectors. Two input ranges can be set by altering the input attenuation on a potential divider connected to this pin, the output of which connects to a supply fault detector. This pin allows thresholds from 6.0 V to 14.4 V and from 2.5 V to 6.0 V.
11	AGND[1]	Ground Return for Input Attenuators.
12	REFGND[1]	Ground Return for On-Chip Reference Circuits.
13	REFIN	Reference Input for the ADC. This pin is nominally 2.048 V and must be driven by a reference voltage. Use the on-board reference by connecting the REFOUT pin to the REFIN pin.
14	REFOUT	Reference Output, 2.048 V. This pin is typically connected to REFIN. Note that the recommended 10 µF capacitor must be connected between this pin and REFGND.
15 to 20	DAC1 to DAC6	Voltage Output DACs. These pins default to high impedance at power-up.
21 to 30	PDO10 to PDO1	Programmable Driver Outputs.
31	PDOGND[1]	Ground Return for Driver Outputs.
32	VCCP	Central Charge Pump Voltage of 5.25 V (Positive/Negative). A reservoir capacitor must be connected between this pin and GND. A 10 µF capacitor is recommended for this purpose.
33	A0	Logic Input 0. This pin sets the seventh bit of the SMBus interface address.
34	A1	Logic Input 1. This pin sets the sixth bit of the SMBus interface address.
35	SCL	SMBus Clock. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
36	SDA	SMBus Data. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
37	CCL	ICB Clock. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
38	CDA	ICB Data. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
39	VDDCAP	Device Supply Voltage. This pin is linearly regulated from the highest of the VPx and VH pins to a typical of 4.75 V. Note that the minimum 10 µF capacitor must be connected between this pin and GND.
40	GND[1]	Supply Ground.
	EPAD	Exposed Pad. This pad is a no connect (NC). If possible, solder this pad to the board for improved mechanical stability. The exposed pad may be connected to ground, though this connection is not required.

[1] In a typical application, all ground pins are connected together.

TYPICAL PERFORMANCE CHARACTERISTICS

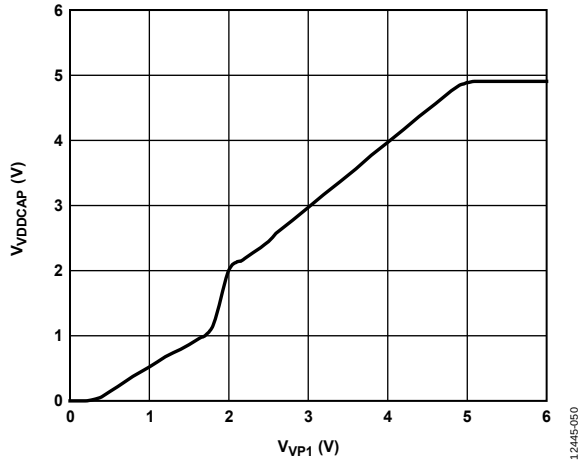


Figure 4. V_{VDDCAP} vs. V_{VP1}

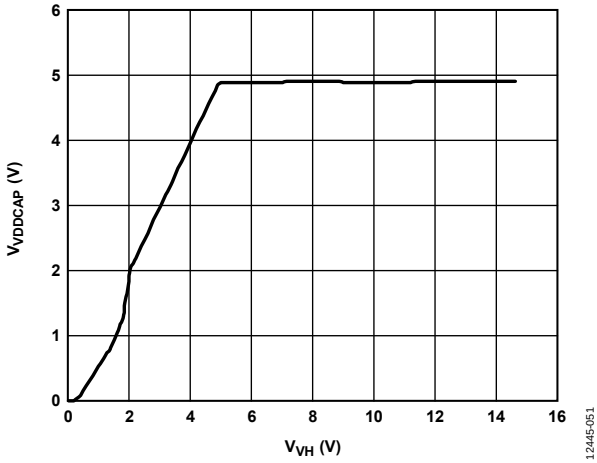


Figure 5. V_{VDDCAP} vs. V_{VH}

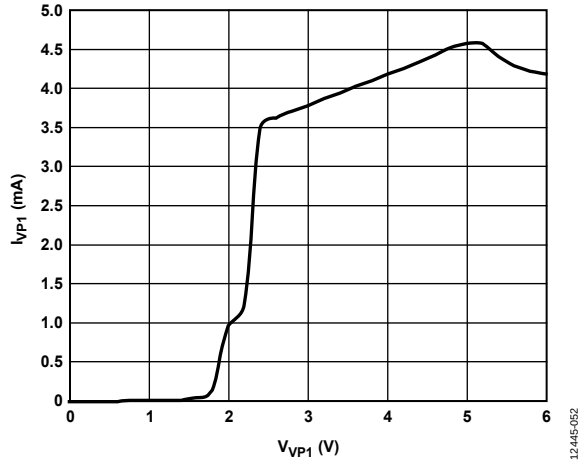


Figure 6. I_{VP1} vs. V_{VP1} (VP1 as the Supply)

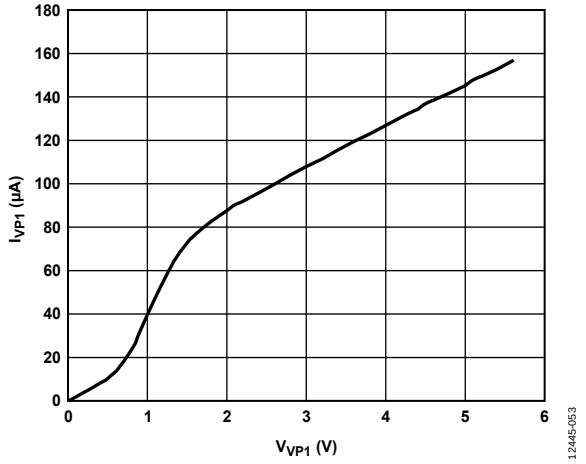


Figure 7. I_{VP1} vs. V_{VP1} (VP1 Not the Supply)

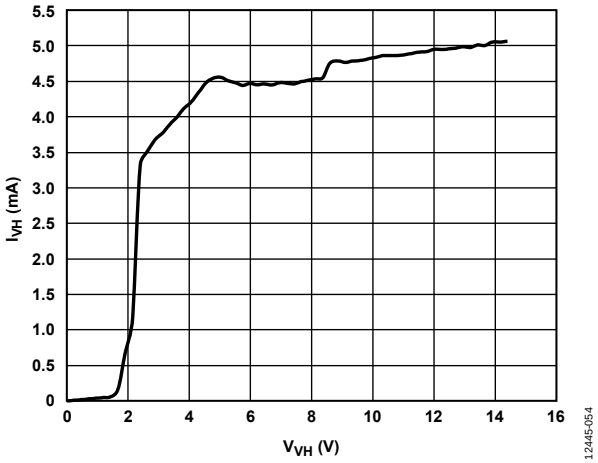


Figure 8. I_{VH} vs. V_{VH} (VH as the Supply)

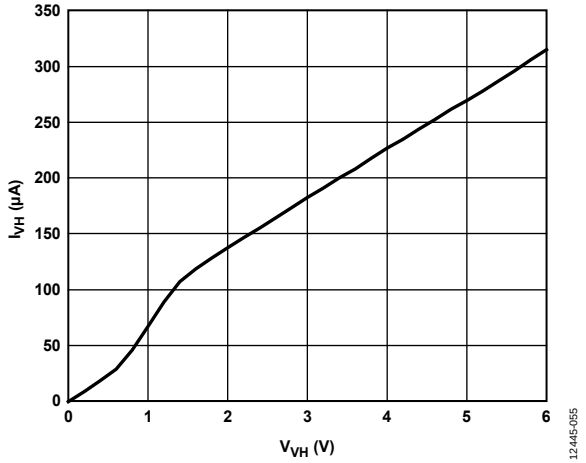


Figure 9. I_{VH} vs. V_{VH} (VH Not the Supply)

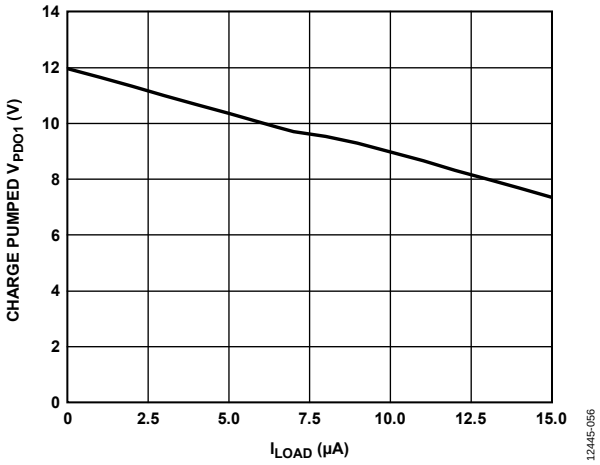


Figure 10. Charge Pumped V_{PDO1} (FET Drive Mode) vs. I_{LOAD}

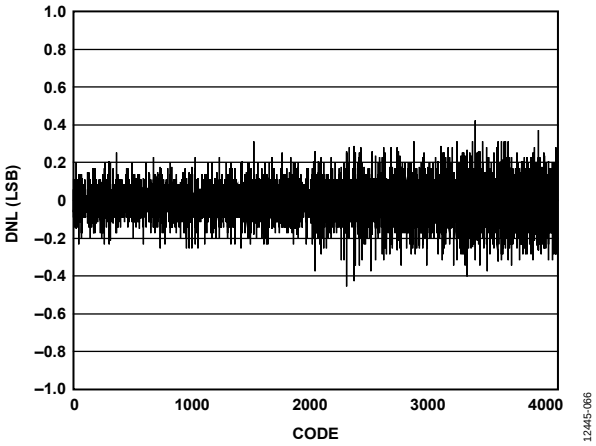


Figure 13. DNL for the ADC

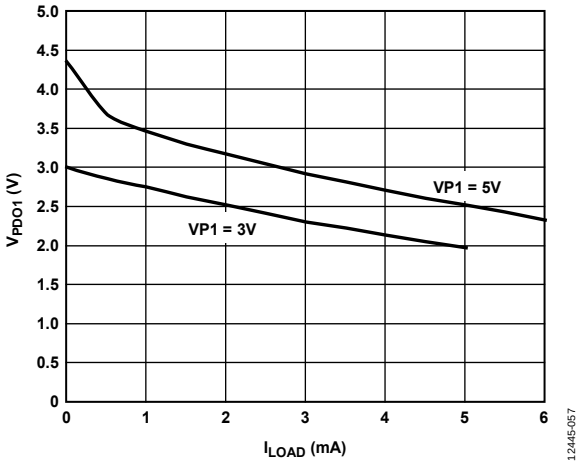


Figure 11. V_{PDO1} (Strong Pull-Up to VPx) vs. I_{LOAD}

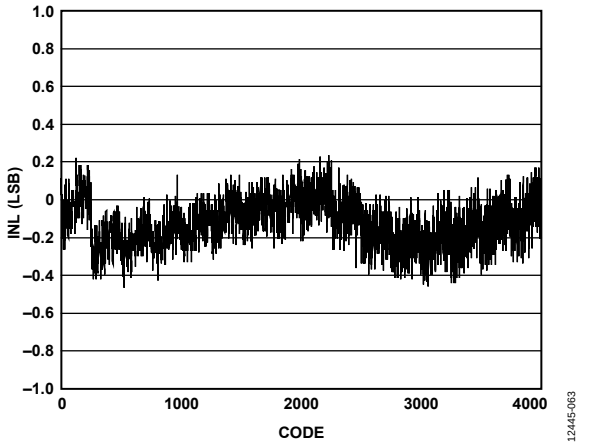


Figure 14. INL for the ADC

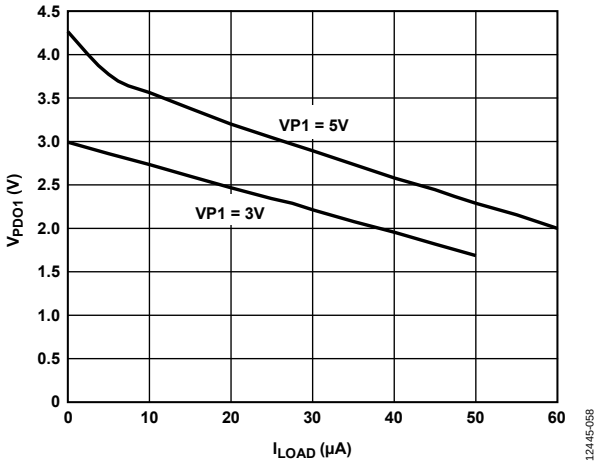


Figure 12. V_{PDO1} (Weak Pull-Up to VPx) vs. I_{LOAD}

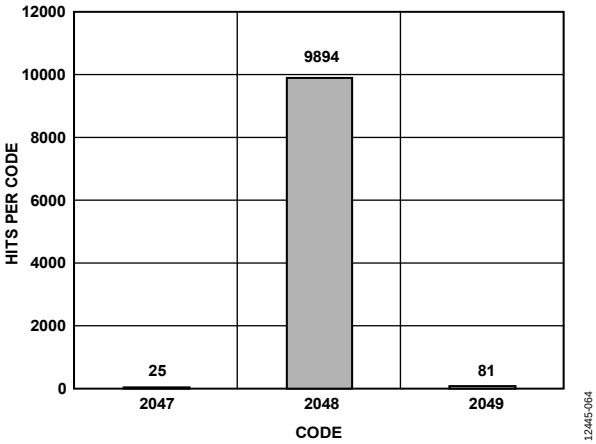


Figure 15. ADC Noise, Midcode Input, 10,000 Reads

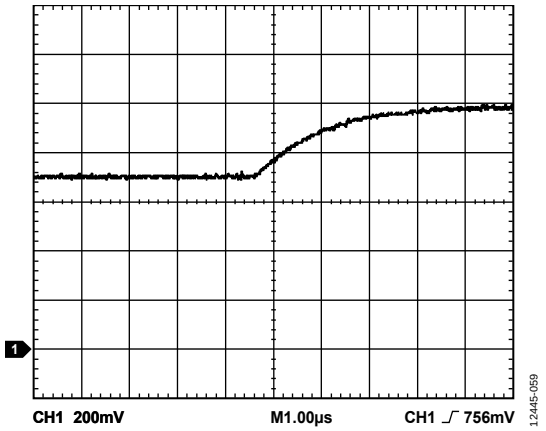


Figure 16. Transient Response of the DAC Code Change into a Typical Load (See Figure 20 for the Corresponding Probe Point Diagram)

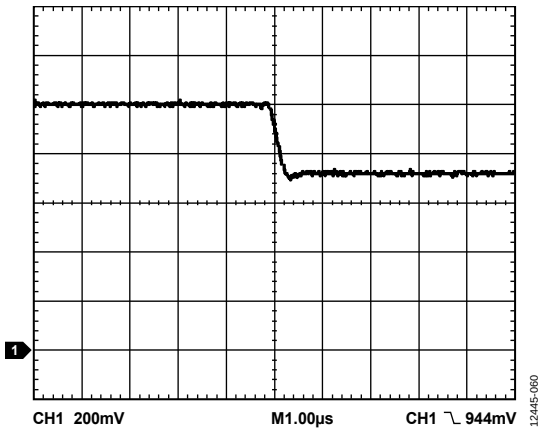


Figure 17. Transient Response of a DAC to Turn On from a High-Z State (See Figure 21 for the Corresponding Probe Point Diagram)

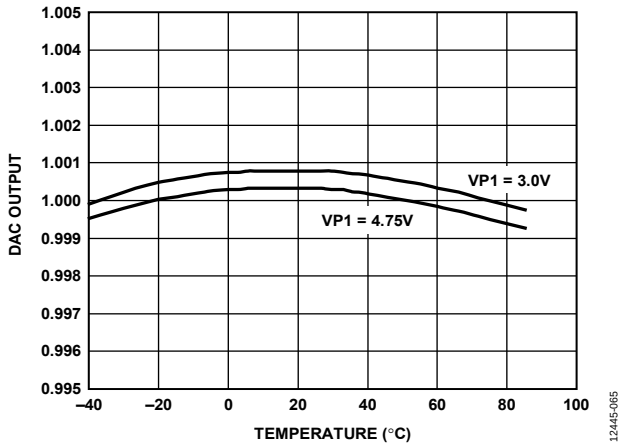


Figure 18. DAC Output vs. Temperature

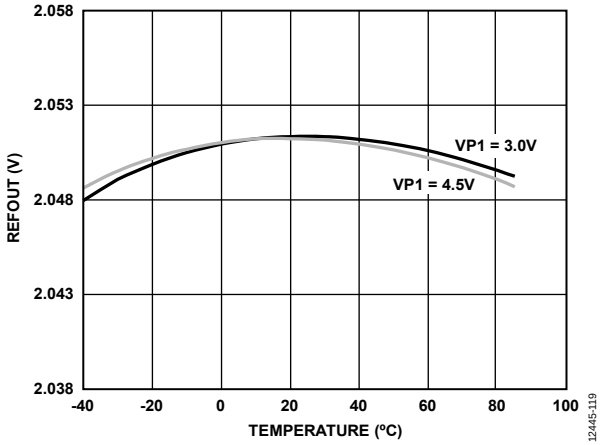


Figure 19. REFOUT vs. Temperature

TEST CIRCUITS

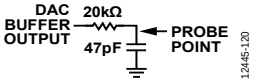


Figure 20. Probe Point for Transient Response of the DAC Code Change into a Typical Load (See Figure 16 for the Corresponding Graph)

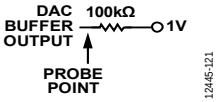


Figure 21. Probe Point for Transient Response of a DAC to Turn On from a High-Z State (See Figure 17 for the Corresponding Graph)

POWERING THE ADM1260

The ADM1260 is powered from the highest voltage input on either the positive only supply inputs (VPx) or the high voltage supply input (VH). This technique offers improved redundancy because the device is not dependent on any particular voltage rail to keep it operational. The same pins are used for supply fault detection (see the Supply Supervision section). A V_{DD} arbitrator on the device chooses which supply to use. The arbitrator can be considered an OR'ing of five low dropout regulators (LDOs) together. A supply comparator chooses the highest input to provide the on-chip supply. There is minimal switching loss with this architecture (~0.2 V), resulting in the ability to power the ADM1260 from a supply as low as 3.0 V. Note that the supply on the VXx pins cannot be used to power the device.

An external capacitor to GND is required to decouple the on-chip supply from noise. Connect this capacitor to the VDDCAP pin, as shown in Figure 22. The capacitor has another use during a brownout (a momentary loss of power). Under these conditions, when the input supply (VPx or VH) dips transiently below V_{DD}, the synchronous rectifier switch immediately turns off so that it does not pull V_{DD} down. The V_{DD} capacitor can then act as a reservoir to keep the device active until the next highest supply takes over the powering of the device. A 10 µF capacitor is recommended for this reservoir/decoupling function.

The value of the VDDCAP capacitor may be increased if it is necessary to guarantee that a complete fault record is written into the EEPROM if all supplies fail. The value of the recommended capacitor is discussed in the Black Box Writes with No External Supply section.

The VH input pin accommodates supplies of up to 14.4 V, which allows the ADM1260 to be powered using a 12 V backplane supply. In cases where this 12 V supply is hot swapped, it is recommended that the ADM1260 not be connected directly to the supply. Take suitable precautions, such as the use of a hot swap controller or RC filter network, to protect the device from transients that can cause damage during hot swap events.

When two or more supplies are within 100 mV of each other, the supply that first takes control of V_{DD} maintains control. For example, if VP1 is connected to a 3.3 V supply, V_{DD} powers up to approximately 3.1 V through VP1. If VP2 is then connected to another 3.3 V supply, VP1 still powers the device, unless VP2 goes 100 mV higher than VP1.

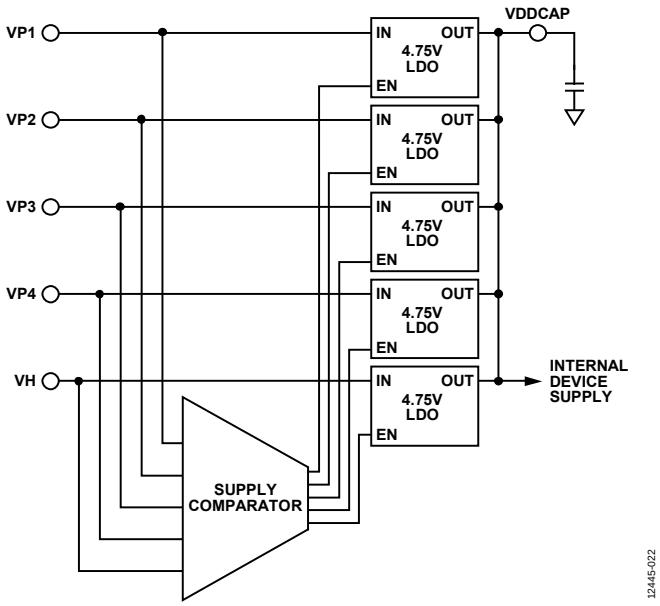


Figure 22. V_{DD} Arbitrator Operation

In a system where multiple ADM1260 devices are on the same ICB, these devices must power up using the same supply rail. This simultaneous power-up is due to the requirement that all the devices on the same ICB be synchronized before they start sequencing.

SLEW RATE CONSIDERATIONS

When the ambient operating temperature is less than approximately −20°C, and in the event of a power loss where all the supply inputs fail for less than a few hundreds of milliseconds (for example, due to a system supply brownout), it is recommended that the supply voltage recover with a ramp rate of at least 1.5 V/ms or less than 0.5 V/ms.

INPUTS

SUPPLY SUPERVISION

The ADM1260 has 10 programmable inputs. Five of these inputs are dedicated supply fault detectors (SFDs). These dedicated inputs are VH and VPx (VP1 to VP4) by default. The other five inputs are VXx (VX1 to VX5) and have dual functionality. These dual function inputs can be used either as SFDs, with functionality similar to that of VH and VPx, or as CMOS-/TTL-compatible logic inputs to the device. Therefore, the ADM1260 can have up to 10 analog inputs, a minimum of five analog inputs and five digital inputs, or a combination thereof. If an input is used as an analog input, it cannot be used as a digital input. Therefore, a configuration requiring 10 analog inputs has no available digital inputs. Table 6 shows the details of each input.

PROGRAMMING THE SUPPLY FAULT DETECTORS

The ADM1260 can have up to 10 SFDs on its 10 input channels. These highly programmable reset generators enable the supervision of up to 10 supply voltages. The supplies can be as low as 0.573 V and as high as 14.4 V. The inputs can be configured to detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out of window fault (the input voltage is outside a preprogrammed range). The thresholds can be programmed to an 8-bit resolution in registers provided in the ADM1260. This 8-bit resolution translates to a voltage resolution that is dependent on the range selected.

The resolution is given by

$$Step\ Size = Threshold\ Range/255$$

Therefore, if the high range is selected on VH, calculate the step size as

$$(14.4\ V - 6.0\ V)/255 = 32.9\ mV$$

Table 5 lists the upper and lower limits of each available range, the bottom of each range (V_B), and the range itself (V_R).

Table 5. Voltage Range Limits

Voltage Range (V)	V_B (V)	V_R (V)
0.573 to 1.375	0.573	0.802
1.25 to 3.00	1.25	1.75
2.5 to 6.0	2.5	3.5
6.0 to 14.4	6.0	8.4

The threshold value required is given by

$$V_T = (V_R \times N)/255 + V_B$$

where:
V_T is the desired threshold voltage (undervoltage or overvoltage).
V_R is the voltage range.
N is the decimal value of the 8-bit code.
V_B is the bottom of the range.

Reversing the equation, the code for a desired threshold is given by

$$N = 255 \times (V_T - V_B)/V_R$$

For example, if the user wants to set a 5 V overvoltage threshold on VP1, the code to be programmed in the PS1OVTH register is given by

$$N = 255 \times (5 - 2.5)/3.5$$

Therefore, N = 182 (1011 0110 or 0xB6).

INPUT COMPARATOR HYSTERESIS

The undervoltage and overvoltage comparators shown in Figure 23 are always monitoring VPx. To avoid chatter (multiple transitions when the input is very close to the set threshold level), these comparators have digitally programmable hysteresis. The hysteresis can be programmed up to the values shown in Table 6.

The hysteresis is added after a supply voltage goes out of tolerance. Therefore, the user can program the amount above the undervoltage threshold to which the input must rise before an undervoltage fault is deasserted. Similarly, the user can program the amount below the overvoltage threshold to which an input must fall before an overvoltage fault is deasserted.

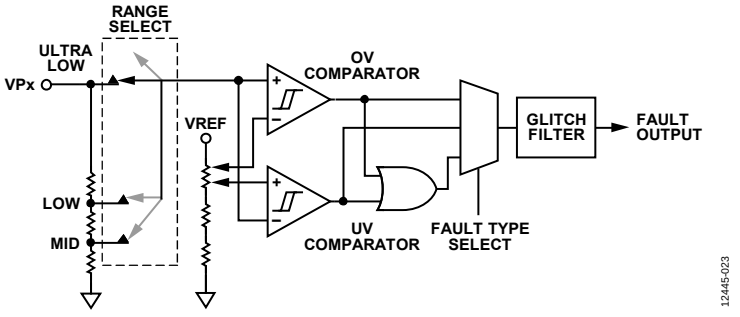


Figure 23. Supply Fault Detector Block

Table 6. Input Functions, Thresholds, and Ranges

Input	Function	Voltage Range (V)	Maximum Hysteresis	Voltage Resolution (mV)	Glitch Filter (µs)
VH	High voltage analog input	2.5 to 6.0	425 mV	13.7	0 to 100
		6.0 to 14.4	1.02 V	32.9	0 to 100
VPx	Positive analog input	0.573 to 1.375	97.5 mV	3.14	0 to 100
		1.25 to 3.00	212 mV	6.8	0 to 100
		2.5 to 6.0	425 mV	13.7	0 to 100
VXx	High-Z analog input	0.573 to 1.375	97.5 mV	3.14	0 to 100
	Digital input	0 to 5.0	Not applicable	Not applicable	0 to 100

The hysteresis value is given by

$$V_{HYST} = V_R \times N_{THRESH}/255$$

where:
V_{HYST} is the desired hysteresis voltage.
V_R is the voltage range.
N_{THRESH} is the decimal value of the 5-bit hysteresis code.

Note that N_{THRESH} has a maximum value of 31. The maximum hysteresis for the ranges is listed in Table 6.

INPUT GLITCH FILTERING

The final stage of the SFDs is a glitch filter. This block provides time domain filtering on the output of the SFD comparators, which allows the user to remove any spurious transitions, such as supply bounce, at turn on. The glitch filter function is in addition to the digitally programmable hysteresis of the SFD comparators. The glitch filter timeout is programmable up to 100 µs.

For example, when the glitch filter timeout is 100 µs, any pulse appearing on the input of the glitch filter block that is less than 100 µs in duration is prevented from appearing on the output of the glitch filter block. Any input pulse that is longer than 100 µs appears on the output of the glitch filter block. The output is delayed by 100 µs with respect to the input. The filtering process is shown in Figure 24.

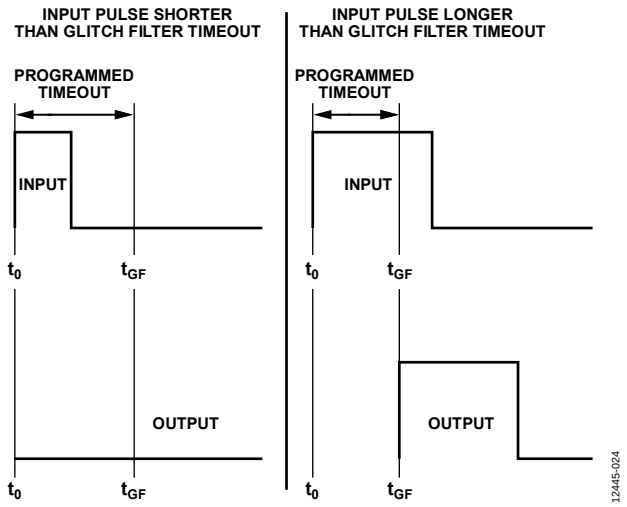


Figure 24. Input Glitch Filter Function

SUPPLY SUPERVISION WITH THE VXx INPUTS

The VXx inputs have two functions: they can be used as either supply fault detectors or digital logic inputs. When selected as analog (SFD) inputs, the VXx pins have functionality that is very similar to the VH and VPx pins. The primary difference is that the VXx pins have only one input range, 0.573 V to 1.375 V. Therefore, the VXx inputs can directly supervise only the very low supplies. However, the input impedance of the VXx pins is high, allowing an external resistor divider network to be connected to the pin. Thus, potentially any supply can be divided down into the input range of the VXx pin and supervised. This enables the ADM1260 to monitor other supplies, such as −5 V, +24 V, and +48 V.

An additional supply supervision function is available when the VXx pins are selected as digital inputs. In this case, the analog function is available as a second detector on each of the dedicated analog inputs, VPx and VH. The analog function of VX1 is mapped to VP1, VX2 is mapped to VP2, and so on. VX5 is mapped to VH. In this case, these SFDs can be viewed as secondary or warning SFDs.

The secondary SFDs are fixed to the same input range as the primary SFDs. They indicate warning levels rather than failure levels. The primary and secondary SFDs allows faults and warnings to be generated on a single supply using only one pin. For example, if VP1 is set to output a fault when a 3.3 V supply drops to 3.0 V, VX1 can be set to output a warning at 3.1 V. Warning outputs are available for readback from the status registers. These outputs are also OR'ed together and fed into the SE, allowing warnings to generate interrupts on the PDOs. Therefore, in this example, if the supply drops to 3.1 V, a warning is generated, and remedial action can be taken before the supply drops out of tolerance.

VXx PINS AS DIGITAL INPUTS

As described in the Supply Supervision with the VXx Inputs section, the VXx input pins on the ADM1260 have dual functionality. The second function is as a digital logic input to the device. Therefore, the ADM1260 can be configured for up to five digital inputs. These inputs are TTL-/CMOS-compatible inputs. Standard logic signals can be applied to the pins: reset from reset generators, power-good (PWRGD) signals, fault flags, and manual resets. These signals are available as inputs to the SE and, therefore, can be used to control the status of the PDOs. The inputs can be configured to detect either a change in level or an edge.

When configured for level detection, the output of the digital block is a buffered version of the input. When configured for edge detection, a pulse of programmable width is output from the digital block once the logic transition is detected. The width is programmable from 0 µs to 100 µs. The digital blocks feature the same glitch filter function that is available on the SFDs. This function enables the user to ignore spurious transitions on the inputs. For example, the filter can be used to debounce a manual reset switch.

When configured as digital inputs, each VXx pin has a weak (10 µA) pull-down current source available for placing the input into a known condition, even if left floating. The current source, if selected, weakly pulls the input to GND.

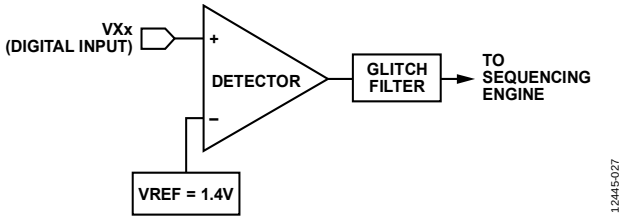


Figure 25. VXx Digital Input Function

OUTPUTS

SUPPLY SEQUENCING THROUGH CONFIGURABLE OUTPUT DRIVERS

Supply sequencing is achieved with the ADM1260 using the programmable driver outputs (PDOs) on the device as control signals for supplies. The output drivers can be used as logic enables or as FET drivers.

The sequence in which the PDOs are asserted (and, therefore, the supplies are turned on) is controlled by the sequencing engine (SE). The SE determines what action is taken with the PDOs, based on the condition of the ADM1260 inputs. Therefore, the PDOs can be set up to assert when the SFDs are in tolerance, the correct input signals are received on the VXx digital pins, and no warnings are received from any of the inputs of the device. The PDOs can be used for a variety of functions. The primary function is to provide enable signals for LDOs or dc-to-dc converters that generate supplies locally on a board. The PDOs can also provide a power-good signal when all the SFDs are in tolerance, or a reset output if one of the SFDs goes out of specification (this output from the PDO can be used as a status signal for a DSP, FPGA, or other microcontroller).

The PDOs can be programmed to pull up to a number of different options. The outputs can be programmed as follows:

- Open drain (allowing the user to connect an external pull-up resistor).
- Open drain with a weak pull-up to V_{DD}.
- Open drain with a strong pull-up to V_{DD}.
- Open drain with a weak pull-up to VPx.
- Open drain with a strong pull-up to VPx.
- Strong pull-down to GND.
- Internally charge pumped high drive (12 V, PDO1 to PDO6 only).

The last option (available only on PDO1 to PDO6) allows the user to directly drive a voltage high enough to fully enhance an external N-FET, which is used to isolate, for example, a card side voltage from a backplane supply (a PDO can sustain greater than 10.5 V into a 1 µA load). The pull-down switches can also be used to drive status LEDs directly.

The data driving each of the PDOs comes from one of three sources. Enable the specific source in the PDOxCFG configuration register.

The data sources are as follows:

- Output from the SE.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This configuration enables software control of the PDOs. Therefore, a microcontroller can be used to initiate a software power-up/power-down sequence.
- On-chip clock. A 100 kHz clock is generated on the device. This clock can be made available on any of the PDOs. It can be used, for example, to clock an external device, such as an LED.

DEFAULT OUTPUT CONFIGURATION

All of the internal registers in an unprogrammed ADM1260 device from the factory are set to 0. Because of this factory setting, the PDOx pins are pulled to GND by a weak (20 kΩ), on-chip pull-down resistor.

As the input supply to the ADM1260 ramps up on VPx or VH, all the PDOx pins behave as follows:

- Input supply = 0 V to 1.2 V. The PDOs are high impedance.
- Input supply = 1.2 V to 2.7 V. The PDOs are pulled to GND by a weak (20 kΩ), on-chip pull-down resistor.
- Supply > 2.7 V. The factory programmed devices continue to pull all PDOs to GND by a weak (20 kΩ), on-chip, pull-down resistor. The programmed devices download current EEPROM configuration data, and the programmed setup is latched. The PDO then goes to the state demanded by the configuration, which provides a known condition for the PDOs during power-up.

The internal pull-down resistor can be overdriven with an external pull-up resistor of suitable value tied from the PDOx pin to the required pull-up voltage. The 20 kΩ resistor must be accounted for in calculating a suitable value. For example, if PDOx must be pulled up to 3.3 V, and 5 V is available as an external supply, the pull-up resistor value (R_{UP}) is given by

$$3.3\ V = 5\ V \times 20\ k\Omega/(R_{UP} + 20\ k\Omega)$$

Therefore,

$$R_{UP} = (100\ k\Omega - 66\ k\Omega)/3.3\ V = 10\ k\Omega$$

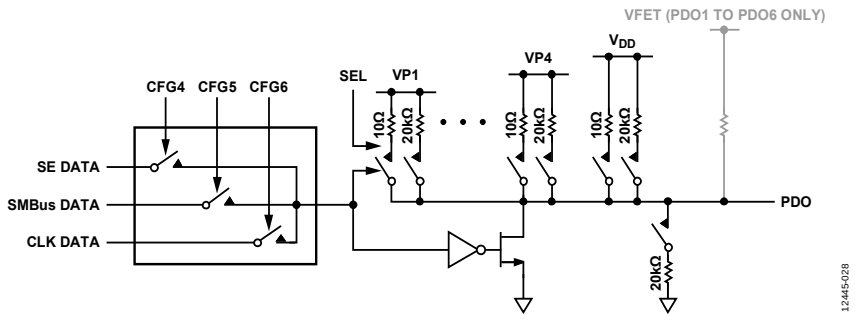


Figure 26. Programmable Driver Output

SEQUENCING ENGINE

OVERVIEW

The ADM1260 SE provides the user with powerful and flexible control of sequencing. The SE implements state machine control of the PDO outputs, with state changes conditional on input events. SE programs can enable complex control of boards such as power-up and power-down sequence control, fault event handling, and interrupt generation on warnings. A watchdog function that verifies the continued operation of a processor clock can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing.

The SE state machine comprises 61 free state cells in each ADM1260. Each state has the following attributes:

- Monitors signals indicating the status of the 10 input pins, VP1 to VP4, VH, and VX1 to VX5.
- Can respond to and generate messages on the ICB to provide transparent, multidevice sequencing and monitoring
- Can be entered from any other state.
- Three exit routes move the state machine onto a next state: sequence detection, fault monitoring, and timeout.
- Delay timers for the sequence and timeout blocks can be programmed independently and changed with each state change. The range of timeouts is from 100 ms to 400 ms.
- Output condition of the 10 PDO pins is defined and fixed within a state.
- The transition from one state to the next is made in approximately 45 µs (except when exiting out of Blackbox write state), which is the time taken to send one byte of message over the ICB and to download a state definition from the EEPROM to the SE.
- Can trigger a write of the black box fault and status registers into the black box section of the EEPROM.

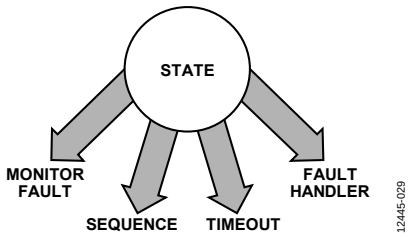


Figure 27. State Cell

The ADM1260 offers up to 61 state definitions. The signals monitored to indicate the status of the input pins are the outputs of the SFDs. In a multidevice system the number of user programmable states varies depending on the number of states used for ping-pong between devices.

WARNINGS

The SE also monitors warnings. These warnings can be generated when the ADC readings violate their limit register value or when the secondary voltage monitors on VPx or VH are triggered. The warnings are OR'ed together and are available as a single warning input to each of the three blocks that enable exiting a state.

SMBUS JUMP (UNCONDITIONAL JUMP)

The SE can be forced to advance to the next state unconditionally, which enables the user to force the SE to advance. Examples of the use of this feature include moving to a margining state or debugging a sequence. The SMBus jump or go to command can be seen by the user as another input to sequence and timeout blocks to provide an exit from each state.

Table 7. Sample Sequence State Entries

State	Sequence	Timeout	Monitor
IDLE1	If VX1 is low, go to State IDLE2.		
IDLE2	If VP1 is good, go to State EN3V3.		
EN3V3	If VP2 is good, go to State EN2V5.	If VP2 is not good after 10 ms, go to State DIS3V3.	If VP1 is not good, go to State IDLE1.
DIS3V3	If VX1 is high, go to State IDLE1.		
EN2V5	If VP3 is good, go to State PWRGD.	If VP3 is not good after 20 ms, go to State DIS2V5.	If VP1 or VP2 is not good, go to State FSEL2.
DIS2V5	If VX1 is high, go to State IDLE1.		
FSEL1	If VP3 is not good, go to State DIS2V5.		If VP1 or VP2 is not good, go to State FSEL2.
FSEL2	If VP2 is not good, go to State DIS3V3.		If VP1 is not good, go to State IDLE1.
PWRGD	If VX1 is high, go to State DIS2V5.		If VP1, VP2, or VP3 is not good, go to State FSEL1.

INTERCHIP BUS

In addition to local device conditions, a number of different ICB messages can affect the operation of the SE. These messages are used by the ADM1260 to coordinate the sequencing activities, and to inform other devices of faults within the system.

There are four basic types of ICB messages.

- Sequence action
- Timeout fault
- Monitor fault
- Black box trigger

The sequence action message has two forms. In a device to device form (the first form), this message is used to hand over sequencing responsibility from one device to the another. The transfer of sequencing control is done using a ping-pong handshake to ensure a robust handover of control. In the second form, the message is broadcast to all devices and instructs them to execute the sequence condition of the active SE state. All devices connected by the ICB advance their state machines together in lock step to maintain a coherent overall system state.

The sequence condition can be set to generate a sequence action message that is sent to a specific device, or is broadcast to all devices.

The sequence condition in the SE state must be set to wait for a ping (from a specific device or from a broadcast) for the device to receive and act upon it.

The timeout and monitor fault messages are always broadcast messages. They are used by one device to inform all other devices connected to the ICB that a timeout or monitor fault has occurred, and to follow the exit state defined in the active SE state.

The timeout and monitor messages are always active on the ADM1260. The timeout and monitor conditions do not need to be programmed as part of the SE definition to respond to the messages being received on the ICB.

The black box trigger is a broadcast message automatically sent by an ADM1260 when a sequence condition causes the device to enter a state where the black box trigger is enabled.

In normal operation, the ADM1260 evaluation software, ADI Power Studio, generates a virtual sequence for all the devices that share the same ICB. The software automatically inserts the necessary ICB messages and generates the sequence engine of each device connected to the ICB. In practice, the end user does not need to insert the ICB message handling into the SE.

The ICB must be pulled up for the SE to progress; otherwise, the devices remain in a reserved state.

The SE follows the fault handler path in case of an ICB bus fault or ping-pong fault if one of the devices in the sequence is non-operational.

ICB Message Address

Each device on the ICB is assigned a 4-bit address, which is automatically configured by the GUI. This address is used for device to device sequence action messages. The ADM1260 supports up to four devices on the ICB.

SE APPLICATION EXAMPLE

The application in this section demonstrates the operation of the SE. Figure 29 shows how the simple building block of a single SE state can be used to build a power-up sequence for a three-supply system. Table 8 lists the PDOx outputs for each state in the same SE implementation. In this system, a good 5 V supply on the VP1 pin and the VX1 pin held low are the triggers required to start a power-up sequence. Next, the sequence turns on the 3.3 V supply, then the 2.5 V supply (assuming successful turn on of the 3.3 V supply). When all three supplies turn on correctly, the power-good state is entered, where the SE remains until a fault occurs on one of the three supplies or until it is instructed to go through a power-down sequence by VX1 going high. Faults are dealt with throughout the power-up sequence on a case by case basis. The following three sections in this data sheet (the Sequence Detector section, the Monitoring Fault Detector section, and the Timeout Detector section) describe the individual blocks and use the sample application shown in Figure 29 to demonstrate the actions of the SE.

Table 8. PDO Outputs for Each State

	Sequence State[1]								
PDOx Output	**IDLE1**	**IDLE2**	**EN3V3**	**EN2V5**	**DIS3V3**	**DIS2V5**	**PWRGD**	**FSEL1**	**FSEL2**
PDO1 = 3V3ON[2]	0	0	1	1	0	1	1	1	1
PDO2 = 2V5ON[3]	0	0	0	1	1	0	1	1	1
PDO3 = FAULT[4]	0	0	0	0	1	1	0	1	1

[1] The various sequence states are described in Table 7.
[2] 3V3ON means that a particular PDOx pin enables the signal of the 3.3 V LDO.
[3] 2V5ON means that a particular PDOx pin enables the signal of the 2.5 V LDO.
[4] PDO3 is used to send a fault signal to the microcontroller or FPGA.

Sequence Detector

The sequence detector block detects when a step in a sequence is complete. The sequence detector looks for one of the SE inputs to change state, and is most often used as the gate for successful progress through a power-up or power-down sequence. A timer block included in this detector inserts delays into a power-up or power-down sequence, if required. Timer delays can be set from 0 µs to 400 ms. Figure 28 shows a block diagram of the sequence detector.

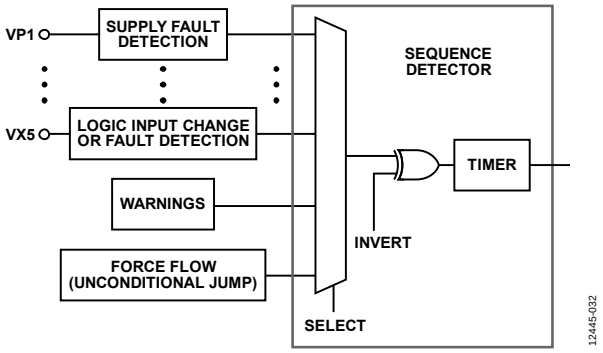


Figure 28. Sequence Detector Block Diagram

If a timer delay is specified, the input to the sequence detector must remain in the defined state for the duration of the timer delay. If the input changes state during the delay, the timer is reset.

The sequence detector can also help to identify monitoring faults. In the sample application shown in Figure 29, the FSEL1 and FSEL2 states first identify which of the VP1, VP2, or VP3 pins faulted; then, the states take the appropriate action.

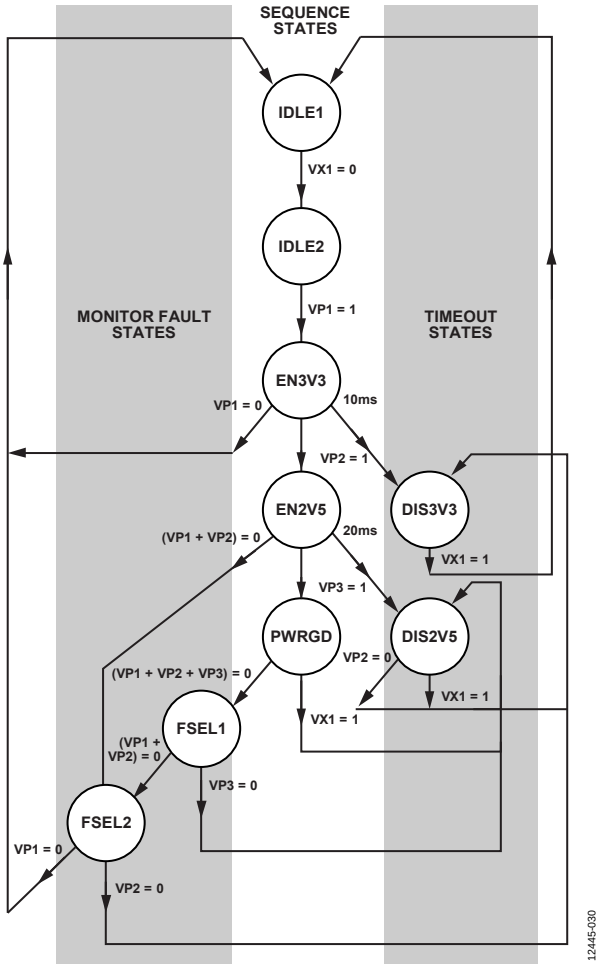


Figure 29. Sample Application Flow Diagram

Monitoring Fault Detector

The monitoring fault detector block detects a failure on an input. The logical function implementing this is a wide OR gate that can detect when an input deviates from its expected condition. The clearest demonstration of the use of this block is in the PWRGD state, where the monitor block indicates that a failure on one or more of the VPx, VXx, or VH inputs occurred.

No programmable delay is available in this block because the triggering of a fault condition is likely caused by a supply falling out of tolerance. In this situation, the device must react as quickly as possible. Some latency occurs when moving out of this state because it takes a finite amount of time (~45 µs) for the state configuration to download from the EEPROM into the SE. Figure 30 is a block diagram of the monitoring fault detector.

If multiple ADM1260 devices are connected through the interchip bus and a monitor fault is detected on any of the devices, the device where the fault occurred transmits a broadcast message on the interchip bus. Because this is a broadcast message, all the devices see the monitor event message and transition their own local SE by following the monitor exit state programmed in their active local state.

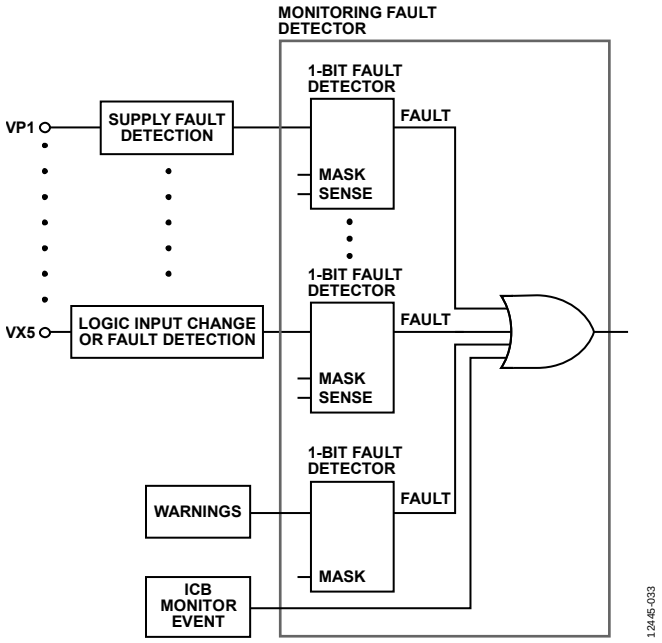


Figure 30. Monitoring Fault Detector Block Diagram

Timeout Detector

The timeout detector allows the user to trap a failure to ensure proper progress through a power-up or power-down sequence.

In the sample application shown in Figure 29, the timeout next state transition is from the EN3V3 and EN2V5 states. For the EN3V3 state, the 3V3ON signal is asserted on the PDO1 output pin upon entry to this state to turn on a 3.3 V supply.

This 3.3 V supply rail is connected to the VP2 pin, and the sequence detector looks for the VP2 pin to go above its undervoltage threshold, which is set in the SFD attached to that pin.

The power-up sequence progresses when it is detected that the VP2 pin went above the undervoltage threshold. If, however, the supply fails (perhaps due to a short circuit overloading this supply), the timeout block traps the problem. In this example, if the 3.3 V supply fails within 10 ms, the SE moves to the DIS3V3 state and turns off this supply by bringing PDO1 low. It also indicates that a fault has occurred by taking PDO3 high. Timeout delays of 100 µs to 400 ms are programmable.

If multiple ADM1260 devices are connected through the interchip bus and a timeout is detected in any of the devices, the device transmits a broadcast timeout message on the interchip bus. Because this is a broadcast message, all the devices see the timeout event message and transition their own local state machine by following the timeout exit state programmed in their active local state.

FAULT AND STATUS REPORTING

The ADM1260 has a number of input status registers. These registers include more detailed information, such as whether an undervoltage or overvoltage fault is present on a particular input. The status registers also include information on the ADC limit faults. The contents of the fault register can be read out over the SMBus.

There are two sets of these registers with different behaviors. The first set of status registers is not latched in any way and, therefore, can change at any time in response to changes on the inputs. These registers provide information on the undervoltage (UV) and overvoltage (OV) state of the inputs, the digital state of the general-purpose input (GPI) VXx input pins, and also the ADC warning limit status.

The second set of registers update each time the sequence engine changes state and are latched until the next state change. The second set of registers provides the same information as the first set, but in a more compact form. The reason for this compact form is that these registers are used by the black box feature when writing status information for the previous state into EEPROM.

NONVOLATILE BLACK BOX FAULT RECORDING

A section of EEPROM, Address 0xF980 to Address 0xF9FF, can be used to store up to 16 fault records instead of user data.

The user can designate any sequencing engine state as a black box write trigger state. Each time the sequence engine enters that state, a fault record is written into EEPROM. The fault record provides a snapshot of the entire ADM1260 state at the point in time when the last state exited, just prior to entering the designated black box write state. A fault record contains the following information:

- A flag bit set to 0 after the fault record is written.
- The state number of the previous state prior to the fault record write state.
- Whether a sequence/timeout/monitor condition caused the previous state to exit.
- Whether the transition was caused by the reception of an ICB message.
- The UVSTATx and OVSTATx input comparator status.
- The VXx GPISTAT status.
- The LIMSTATx status.
- A checksum byte.

Each fault record contains eight bytes, with each byte taking typically approximately 250 µs to write to EEPROM, for a total write time of approximately 2 ms. After the black box begins to write a fault record into EEPROM, the ADM1260 ensures that the write is complete before attempting to write any additional fault records. This means that if consecutive sequencing engine states are designated as black box write states, a time delay must be used in the first state to ensure that the fault record is written before moving to the next state.

When the ADM1260 powers on initially, it performs a search to find the first fault record that is not written to. The device does this by checking the flag bit in each fault record until it finds a record where the flag bit is 1. The first fault record is stored at Address 0xF980 and at multiples of eight bytes after that, with the last record stored at Address 0xF9F8.

The fault recorder is only able to write in the EEPROM. It is unable to erase the EEPROM prior to writing the fault record. Therefore, to ensure correct operation, it is important that the fault record EEPROM be erased prior to use. After all EEPROM locations for the fault records are used, no more fault records can be written. This limitation ensures that the first fault in any cascading fault is stored and not overwritten and lost.

To avoid the fault recorder filling up and fault records being lost, an application can periodically poll the ADM1260 to determine if there are fault records to be read. Alternatively, one of the PDOx outputs can be used to generate an interrupt for a processor in the fault record write state to signal the need to read one or more fault records.

After reading fault records during normal operation, the following two things must be done before the fault recorder can reuse the EEPROM locations:

- The EEPROM section must be erased.
- The fault recorder must be reset so that it performs its search again for the first unused location of EEPROM that is available to store a fault record.

In a multiple device system, when one of the ADM1260 devices moves to a black box state due to a sequence, monitor, or timeout condition, it generates an ICB message on the bus with the black box bit asserted. This assertion causes a black box write on all the devices on the ICB. This write enables the ability to capture the status of all the devices when a fault occurs. The devices have the same number of black box records that are on the same ICB. The devices that perform the black box write due to the ICB message is stated in the black box record.

BLACK BOX WRITES WITH NO EXTERNAL SUPPLY

In cases where all the input supplies fail, for example, if the card is removed from a powered backplane, the state machine can be programmed to trigger a write into the black box EEPROM. The decoupling capacitors on the rail that power the ADM1260 and the other loads on the board form an energy reservoir. Depending on the other loads on the board and their behavior as the supply rails drop, there may be sufficient energy in the decoupling capacitors to allow the ADM1260 to write a complete fault record (8 bytes of data). CCL and CDA must be pulled up, at least for the duration required for the SE to transition to the black box trigger state.

Typically, it takes 2 ms to write to the eight bytes of a fault record. If the ADM1260 is powered using a 12 V supply on the VH pin, a UV threshold at 6 V can be set and used as the state machine trigger to start writing a fault record to EEPROM. The higher the threshold, the earlier the black box write begins, and the more energy is available in the decoupling capacitors to ensure that the write completes successfully.

Provided that the VH supply, or another supply connected to a VPx pin, remains above 3.0 V during the time to write, the entire fault record is always written to EEPROM. In many cases, there are sufficient decoupling capacitors on a board to power the ADM1260 as it writes into EEPROM.

In cases where the decoupling capacitors are not able to supply sufficient energy for a complete fault record to be written after the board is removed, the value of the capacitor on VDDCAP may be increased. In a worst case scenario, assuming that no energy is supplied to the ADM1260 by external decoupling capacitors, and that the VDDCAP capacitor has 4.75 V across it at the start of the black box write to EEPROM, a VDDCAP value of 68 µF is sufficient to guarantee that a single, complete black box record can be written to EEPROM.

VOLTAGE READBACK

The ADM1260 has an on-board, 12-bit accurate ADC for voltage readback over the SMBus. The ADC has a 10-channel analog mux on the front end. The 10 channels are the SFD inputs (VH, VPx, and VXx). Any or all of these inputs can be selected to be read, in turn, by the ADC. The circuit controlling this operation is called the round robin circuit. This circuit can be selected to run through its loop of conversions once or continuously. Averaging is also provided for each channel. In this case, the round robin circuit runs through its loop of conversions 16 times before returning a result for each channel. At the end of this cycle, the results are written to the output registers.

The ADC samples single-sided inputs with respect to the AGND pin. A 0 V input outputs Code 0, and an input equal to the voltage on REFIN outputs full code (4095 decimal).

The inputs to the ADC come directly from the VXx pins and from the back of the input attenuators on the VPx and VH pins, as shown in Figure 31 and Figure 32, respectively.

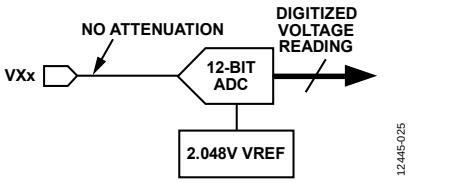


Figure 31. ADC Reading on VXx Pins

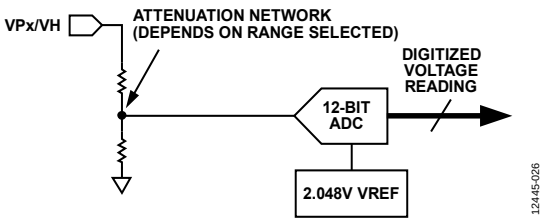


Figure 32. ADC Reading on VPx/VH Pins

Derive the voltage at the input pin using the following equation:

$$V = \frac{ADC\ \ Code}{4095} \times Attenuation\ Factor \times V_{REFIN}$$

where V_{REFIN} = 2.048 V when the internal reference is used (that is, the REFIN pin is connected to the REFOUT pin).

The ADC input voltage ranges for the SFD input ranges are listed in Table 9.

Table 9. ADC Input Voltage Ranges

SFD Input Range (V)	Attenuation Factor	ADC Input Voltage Range (V)
0.573 to 1.375	1	0 to 2.048
1.25 to 3.00	2.181	0 to 4.46
2.5 to 6.0	4.363	0 to 6.0[1]
6.0 to 14.4	10.472	0 to 14.4[1]

[1] The upper limit of this range is the absolute maximum allowed voltage on the VPx and VH pins.

The typical method for supplying the reference to the ADC on the REFIN pin is to connect the REFOUT pin to the REFIN pin. REFOUT provides a 2.048 V reference; therfore, the supervising range covers less than half of the normal ADC range. However, it is possible to provide the ADC with a more accurate external reference for improved readback accuracy.

Supplies can also be connected to the input pins purely for ADC readback, even though these pins may go above the expected supervisory range limits (but not above the absolute maximum ratings on these pins). For example, a 1.5 V supply connected to the VX1 pin can be correctly read out as an ADC code of approximately ¾ of full scale, but it always sits above any supervisory limits that can be set on that pin. The maximum setting for the REFIN pin is 2.048 V.

SUPPLY SUPERVISION WITH THE ADC

In addition to the readback capability, another level of supervision is provided by the on-chip, 12-bit ADC. The ADM1260 has limit registers that allow the user to program a maximum or minimum allowable threshold. Exceeding the threshold generates a warning that can either be read back from the status registers or input into the SE to determine what sequencing action the ADM1260 must take. Only one register is provided for each input channel. Therefore, either an undervoltage threshold or overvoltage threshold (but not both) can be set for a given channel. The round robin circuit can be enabled via an SMBus write, or it can be programmed to turn on in any state in the SE program. For example, the round robin circuit can be set to start after a power-up sequence is complete and after all supplies are known to be within expected tolerance limits.

Note that latency is built into this supervision and is dictated by the conversion time of the ADC. With all 12 channels selected, the total time for the round robin operation (with averaging off) is approximately 6 ms (500 µs per channel selected). Supervision using the ADC, therefore, does not provide the same real-time response as the SFDs.

SUPPLY MARGINING

OVERVIEW

It is often necessary for the system designer to adjust supplies, either to optimize their level or to force them away from nominal values to characterize the system performance under these conditions. This is a function typically performed during an in-circuit test (ICT), such as when a manufacturer wants to guarantee that a product under test functions correctly at nominal supplies minus 10%.

OPEN-LOOP SUPPLY MARGINING

The simplest method of margining a supply is to implement an open-loop technique (see Figure 33). A typically used method is to switch extra resistors into the feedback node of a power module, such as a dc-to-dc converter or LDO. The extra resistor alters the voltage at the feedback or trim node and forces the output voltage to margin up or down by a certain amount.

The ADM1260 performs open-loop margining for up to six supplies. The six on-board voltage DACs (DAC1 to DAC6) drive into the feedback pins of the power modules to be margined. The simplest circuit to implement this function is an attenuation resistor that connects the DACx pin to the feedback node of a dc-to-dc converter. When the DACx output voltage is set equal to the feedback voltage, no current flows into the attenuation resistor, and the dc-to-dc converter output voltage does not change. Taking DACx above the feedback voltage forces current into the feedback node, and the output of the dc-to-dc converter is forced to fall to compensate for this forced current. The dc-to-dc converter output can be forced high by setting the DACx output voltage lower than the feedback node voltage. The series resistor can be split in two, and the node between them can be decoupled with a capacitor to ground. This decoupling capacitor helps decouple any noise picked up from the board. Decoupling to a ground local to the dc-to-dc converter is recommended.

Update the values on the relevant DAC output to command the ADM1260 to margin a supply up or down over the SMBus.

CLOSED-LOOP SUPPLY MARGINING

Implementing a closed-loop system (see Figure 34) is a more accurate and comprehensive method of margining when compared to open-loop supply margining. In a closed-loop system, the voltage on the rail to be margined can be read back to accurately margin the rail to the target voltage. The ADM1260 incorporates all the circuits required to do this, with the 12-bit successive approximation ADC used to read back the level of the supervised voltages, and the six voltage output DACs, implemented as described in the Open-Loop Supply Margining section, used to adjust supply levels. These circuits can be used along with other intelligence, such as a microcontroller, to implement a closed-loop margining system that allows any dc-to-dc converter or LDO supply to be set to any voltage, accurate to within ±0.5% of the target value.

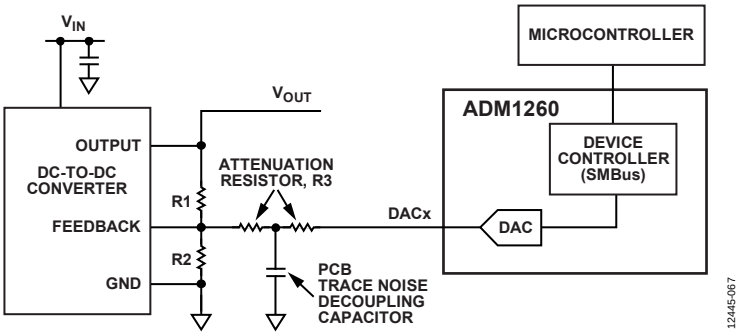


Figure 33. Open-Loop Margining System Using the ADM1260

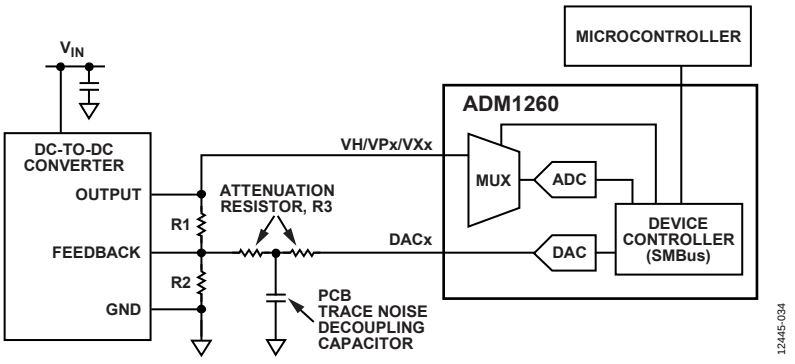


Figure 34. Closed-Loop Margining System Using the ADM1260

Use the following procedure to implement closed-loop margining:

1. Disable the six DACx outputs.
2. Set the DAC output voltage equal to the voltage on the feedback node.
3. Enable the DAC.
4. Read the voltage at the dc-to-dc converter output that is connected to one of the VPx, VH, or VXx pins.
5. If necessary, modify the DACx output code up or down to adjust the dc-to-dc converter output voltage. Otherwise, do not take any action because the target voltage is achieved.
6. Set the DAC output voltage to a value that alters the supply output by the required amount (for example, by ±5%).
7. Repeat Step 4 through Step 6 until the measured supply reaches the target voltage.

Step 1 to Step 3 ensure that when the DACx output buffer is turned on, it has little effect on the dc-to-dc converter output. The DAC output buffer is designed to power up without glitching by first powering up the buffer to follow the pin voltage. The buffer does not drive out onto the pin at this time. After the output buffer is properly enabled, the buffer input is switched over to the DAC, and the output stage of the buffer turns on. Output glitching is negligible.

WRITING TO THE DACs

Four DAC ranges are available on the ADM1260. These ranges can be placed with midcode (Code 0x7F) at 0.6 V, 0.8 V, 1.0 V, and 1.25 V. These voltages are placed to correspond to the most common feedback voltages. Centering the DAC outputs in this way provides the best use of the DAC resolution. For most supplies, it is possible to place the DAC midcode at the point where the dc-to-dc converter output is not modified, thereby giving half of the DAC range to margin up and the other half to margin down.

The DAC output voltage is set by the code written to the DACx register. The voltage is linear with the unsigned binary number in this register. Code 0x7F is placed at the midcode voltage, as described previously. The output voltage is given by

$$DAC\ Output = (DACx - 0x7F)/255 \times 0.6015 + V_{OFF}$$

where V_{OFF} is one of the four offset voltages.

There are 256 DAC settings available. The midcode value is located at DAC Code 0x7F as close as possible to the middle of the 256 code range. The full output swing of the DACs is +302 mV (+128 codes) and −300 mV (−127 codes) around the selected midcode voltage. The voltage range for each midcode voltage is shown in Table 10.

Table 10. Ranges for Midcode Voltages

Midcode Voltage (V)	Minimum Voltage Output (V)	Maximum Voltage Output (V)
0.6	0.300	0.902
0.8	0.500	1.102
1.0	0.700	1.302
1.25	0.950	1.552

CHOOSING THE SIZE OF THE ATTENUATION RESISTOR

The size of the attenuation resistor, R3, determines how much the DAC voltage swing affects the output voltage of the dc-to-dc converter being margined (see Figure 34).

Because the voltage at the feedback pin remains constant, the current flowing from the feedback node to GND through R2 is a constant. In addition, the feedback node itself is high impedance. This means that the current flowing through R1 is the same as the current flowing through R3.

Therefore, a direct relationship exists between the extra voltage drop across R1 during margining and the voltage drop across R3.

This relationship is given by the following equation:

$$\Delta V_{OUT} = \frac{R1}{R3}\ (V_{FB} - V_{DACOUT})$$

where:
ΔV_{OUT} is the change in V_{OUT}.
V_{FB} is the voltage at the feedback node of the dc-to-dc converter.
V_{DACOUT} is the voltage output of the margining DAC.

This equation demonstrates that if the user wants the output voltage to change by ±300 mV, then R1 = R3. If the user wants the output voltage to change by ±600 mV, then R1 = 2 × R3, and so on.

It is best to use the full DAC output range to margin a supply. Choosing the attenuation resistor in this way provides the most resolution from the DAC, meaning that with one DAC code change, the smallest effect on the dc-to-dc converter output voltage is induced. If the resistor is sized up to use a code such as 27 decimal to 227 decimal to move the dc-to-dc converter output by ±5%, it takes 100 codes to move 5% (each code moves the output by 0.05%). This is beyond the readback accuracy of the ADC, but it does not prevent the user from building a circuit to use the most resolution.

DAC LIMITING AND OTHER SAFETY FEATURES

Limit registers on the device (DPLIMx and DNLIMx) offer the user some protection from firmware bugs that can cause catastrophic board problems by forcing supplies beyond their allowable output ranges. Essentially, the DAC code written into the DACx register is clipped such that the code used to set the DAC voltage is given by

```
DAC Code
= DACx,       DACx ≥ DNLIMx and DACx ≤ DPLIMx
= DNLIMx,     DACx < DNLIMx
= DPLIMx,     DACx > DPLIMx
```

In addition, the DAC output buffer is three-stated if DNLIMx > DPLIMx. By programming the limit registers this way, the user can make it very difficult for the DAC output buffers to turn on during normal system operation. The limit registers are among the registers downloaded from EEPROM at startup.

APPLICATIONS INFORMATION

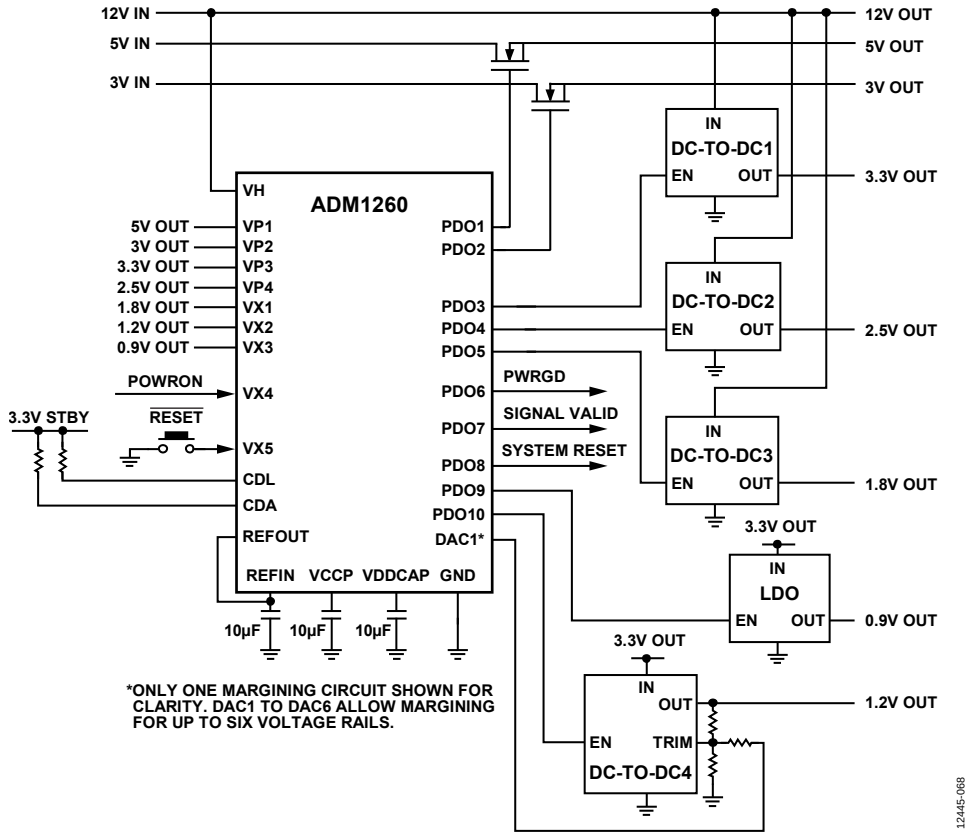


Figure 35. Single Device Applications Diagram

MULTIPLE DEVICES LINKED BY ICB AND POWER ISLAND MANAGEMENT

Figure 36 shows a sequencing system with two ADM1260 devices, linked by the ICB, controlling a number of dc-to-dc supplies. In some sequencing systems, there may be a need to manage groups of supplies due to modules being plugged in and out, or a desire to reduce energy usage by turning off portions of the board to save power. Achieve these power management requirements by treating each group as a power island.

These supplies are split into two power islands: one island is for the main board, and the other island is for a plug in module. Note that the dc-to-dc supplies in each power island can be split between the ADM1260 as required; these supplied do not have to be divided up in the blocks. The supplies are shown this way in Figure 36 for clarity.

At power-up, the main board supplies are sequenced on by the ADM1260 devices, and the sequence engine enters the user defined main board power-good state. In this state, the sequence engine is programmed to look at the state of the VX5 digital input pin, which provides a module detect signal. When this signal is high, it is detected by Device 1 and initiates the power-up sequence for the module power island.

The module detect signal is on Device 1, and all the module supplies are on Device 2. When Device 1 sees that the module detect signal is high, it signals an event to Device 2 using the ICB. Then, Device 2 sequences the supplies for the module on.

Similarly, when the module detect signal goes low, Device 1 signals Device 2, and the module power-down sequence is executed.

The design of the sequence engine allows two power islands to be easily controlled in this manner. It is also possible to manage three or perhaps four power islands, depending on the complexity of the sequencing required.

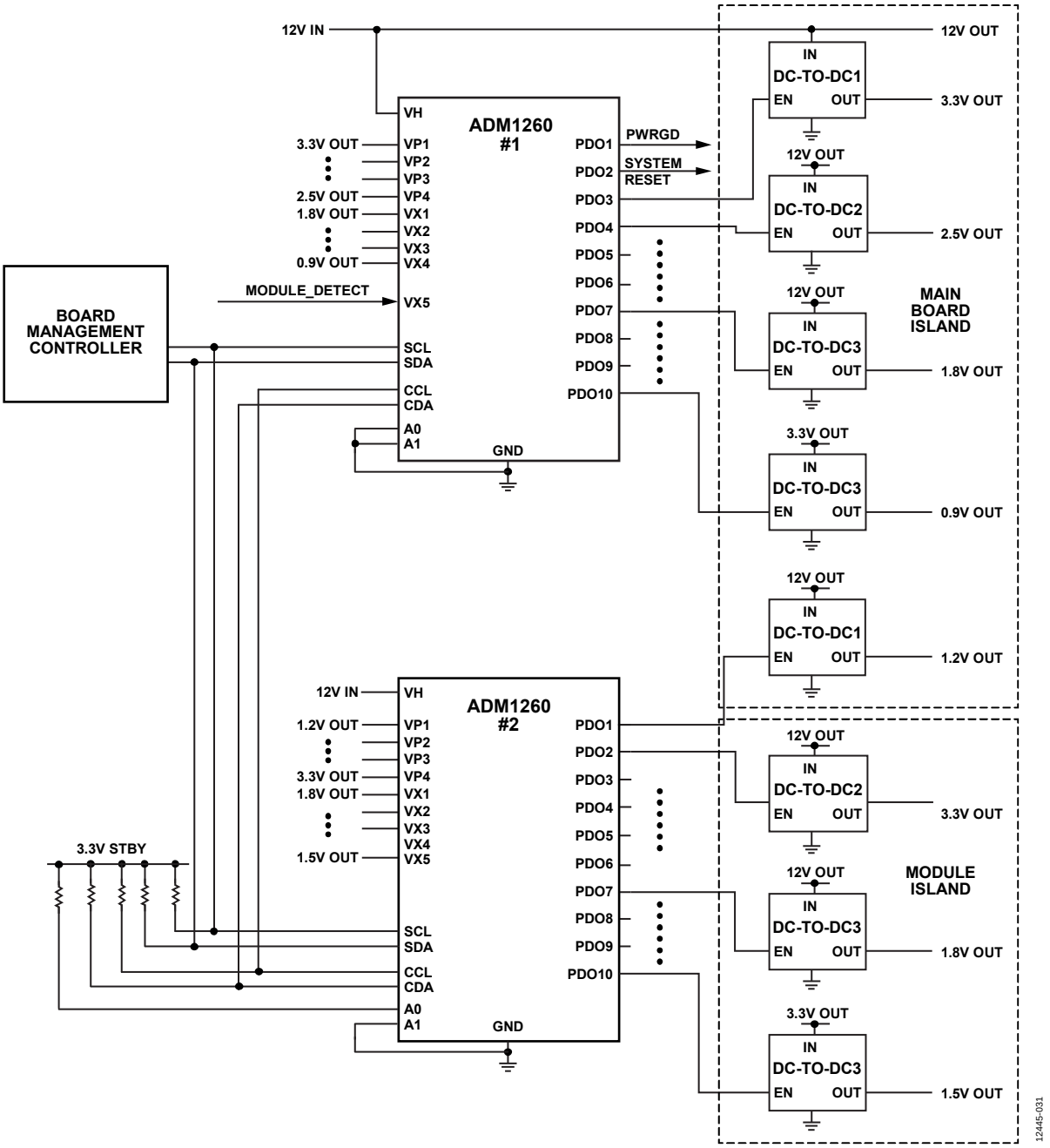


Figure 36. Multiple Devices Linked by the ICB Managing a Power Island

COMMUNICATING WITH THE ADM1260

CONFIGURATION DOWNLOAD AT POWER-UP

The configuration of the ADM1260 (undervoltage/overvoltage thresholds, glitch filter timeouts, and PDOx configurations) is dictated by the contents of the RAM. The RAM comprises digital latches that are local to each function on the device. The latches are double buffered and have two identical latches, Latch A and Latch B. Therefore, when an update to a function occurs, the contents of Latch A are updated first, and then the contents of Latch B are updated with identical data. The advantages of this architecture are explained in detail in the Updating the Configuration section.

The two latches are volatile memory and lose their contents at power-down. Therefore, the configuration in the RAM must be restored at power-up by downloading the contents of the EEPROM (nonvolatile memory) to the local latches. This download occurs in steps, as follows:

1. With no power applied to the device, the PDOx pins are all high impedance.
2. When 1.2 V appears on any of the inputs connected to the VDD arbitrator (VH or VPx), the PDOx pins are all weakly pulled to GND with a 20 kΩ resistor.
3. When the supply rises above the UVLO threshold of the device (2.5 V), the EEPROM starts to download to the RAM.
4. The EEPROM downloads its contents to all Latch As.
5. When the contents of the EEPROM are completely downloaded to the Latch As, the device controller signals all Latch As to download to all Latch Bs simultaneously, completing the configuration download.
6. At 0.5 ms after the configuration download completes, the first state definition is downloaded from the EEPROM into the SE.

Any attempt to communicate with the device prior to the completion of the download causes the ADM1260 to issue a no acknowledge .

UPDATING THE CONFIGURATION

After power-up, with all the configuration settings loaded from the EEPROM into the RAM registers, the user may need to alter the configuration of functions on the ADM1260, such as changing the undervoltage or overvoltage limit of an SFD, changing the fault output of an SFD, or adjusting the rise time delay of one of the PDOx pins.

The ADM1260 provides several options that allow the user to update the configuration over the SMBus interface. The following three options are controlled in the UPDCFG register.

Option 1

Update the configuration in real time. Write to the RAM across the SMBus to update the configuration immediately.

Option 2

Update the Latch As without updating the Latch Bs. With this method, the configuration of the ADM1260 remains unchanged and continues to operate in the original setup until the instruction is given to update the Latch Bs.

Option 3

Change the EEPROM register contents without changing the RAM contents, and then download the revised EEPROM contents to the RAM registers. With this method, the configuration of the ADM1260 remains unchanged and continues to operate in the original setup until the instruction is given to update the RAM.

The instruction to download from the EEPROM in Option 3 is also a useful way to restore the original EEPROM contents if revisions to the configuration are unsatisfactory. For example, to alter an overvoltage threshold, update the RAM register as described in the Option 1 section. However, if the user is not satisfied with the change and wants to revert to the original programmed value, the device controller can issue a command to download the EEPROM contents to the RAM again, as described in the Option 3 section, restoring the ADM1260 to its original configuration.

The topology of the ADM1260 makes this type of operation possible. The local, volatile registers (RAM) are all double buffered latches. Setting Bit 0 of the UPDCFG register to 1 leaves the double buffered latches open at all times. If Bit 0 is set to 0 when a RAM write occurs across the SMBus, only the first side of the double buffered latch is written to. The user must then write a 1 to Bit 1 of the UPDCFG register. This write generates a pulse to update all the second latches simultaneously. EEPROM writes occur in a similar way.

The final bit in this register can enable or disable EEPROM page erasure. If this bit is set high, the contents of an EEPROM page can all be set to 1. If this bit is set low, the contents of a page cannot be erased, even if the command code for page erasure is programmed across the SMBus. The bit map for the UPDCFG register is shown in Figure 51. A flow diagram for download at power-up and subsequent configuration updates is shown in Figure 37.

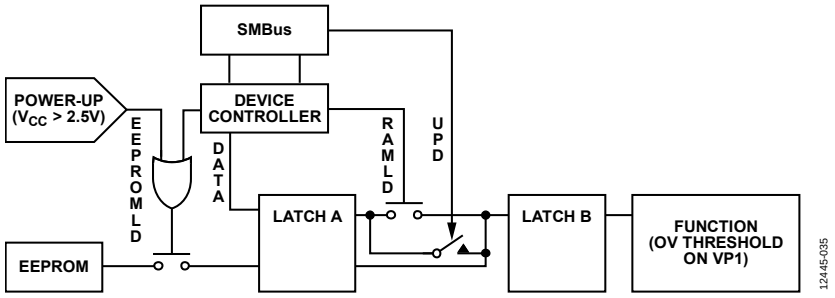


Figure 37. Configuration Update Flow Diagram

UPDATING THE SEQUENCING ENGINE

SE functions are not updated in the same way as regular configuration latches. The SE has its own dedicated, 512-byte, nonvolatile EEPROM for storing state definitions, providing 61 individual states each with a 64-bit word (one state is reserved). At power-up, the first state is loaded from the SE EEPROM into the engine itself. When the conditions of this state are met, the next state is loaded from the EEPROM into the engine, and so on. The loading of each new state takes approximately 45 µs.

To alter a state, the required changes must be made directly to the EEPROM. RAM for each state does not exist. The relevant alterations must be made to the 64-bit word, which is then uploaded directly to the EEPROM.

INTERNAL REGISTERS

The ADM1260 contains a large number of data registers. The principal registers are the address pointer register and the configuration registers.

Address Pointer Register

The address pointer register contains the address that selects one of the other internal registers. When writing to the ADM1260, the first byte of data is always a register address that is written to the address pointer register.

Configuration Registers

The configuration registers provide control and configuration for various operating parameters of the ADM1260.

EEPROM

The ADM1260 has two 512-byte cells of nonvolatile EEPROM from Address 0xF800 to Address 0xFBFF. The EEPROM is used for permanent storage of data that is not lost when the ADM1260 is powered down. One EEPROM cell, Address 0xF800 to Address 0xF9FF, contains the configuration data, user information, and, if enabled, any fault records of the device. The other EEPROM cell section, Address 0xFA00 to Address 0xFBFF, contains the state definitions for the SE. Although referred to as read-only memory, the EEPROM can be written to and read from using the serial bus in exactly the same way as the other registers.

The major differences between the EEPROM and other registers are as follows:

- An EEPROM location must be blank before it can be written to. If it contains data, the data must first be erased.
- Writing to the EEPROM is slower than writing to the RAM.
- Restrict writing to the EEPROM because it has a limited write/cycle life of typically 10,000 write operations due to typical EEPROM wear out mechanisms.

The first EEPROM is split into 16, 32-byte pages (Page 0 to Page 15). Page 0 to Page 4, from Address 0xF800 to Address 0xF89F, hold the configuration data for the applications on the ADM1260, such as the SFDs and PDOx pins. These EEPROM addresses are the same as the RAM register addresses, prefixed by F8. Page 5 to Page 7, from Address 0xF8A0 to Address 0xF8FF, are reserved.

Page 8 and Page 9 store information required by the GUI. Page 10 and Page 11 are available for the user to store any information required by the customer in an application. Users can store information on Page 12 to Page 15, or these pages can store the fault records written by the sequencing engine if users decide to enable writing of the fault records for different states.

Download data from the EEPROM to the RAM in one of the following ways:

- At power-up, when Page 0 to Page 4 are downloaded.
- By setting Bit 0 of the UDOWNLD register (Register 0xD8), which performs a user download of Page 0 to Page 4.

When the SE is enabled, it is not possible to access the section of EEPROM from Address 0xFA00 to Address 0xFBFF. The SE must be halted before it is possible to read or write to this range. Attempting to read or write to this range if the sequence engine is not halted generates a no acknowledge.

Read/write access to the configuration and the user EEPROM ranges from Address 0xF800 to Address 0xF89F and Address 0xF900 to Address 0xF9FF depends on whether the black box fault recorder is enabled. If the fault recorder is enabled and one or more states are set as fault record trigger states, it is not possible to access any EEPROM location in this range without first halting the black box. Attempts to read or write this EEPROM range while the fault recorder is operating are acknowledged by the device but do not return any useful data or modify the EEPROM in any way.

If none of the states are set as fault record trigger states, the black box is considered disabled, and read/write access is allowed without having to first halt the black box fault recorder.

SERIAL BUS INTERFACE

The ADM1260 is controlled via the serial system management bus (SMBus) and is connected to this bus as a slave device under

the control of a master device. It takes approximately 1 ms after power-up for the ADM1260 to download from the EEPROM. Therefore, access to the ADM1260 is restricted until the download is complete.

Identifying the ADM1260 on the SMBus

The ADM1260 has a 7-bit serial bus slave address. The device is powered up with a default serial bus address. The five MSBs of the address are set to 01100, and the two LSBs are determined by the logical states of the A1 and A0 pins. This means it is possible to have four ADM1260 devices connected to a single SMBus.

All the devices on the same SMBus must also be connected to the same ICB because all devices connected to the ICB are intended to operate together.

Table 11. Serial Bus Slave Addresses

A1 Pin	A0 Pin	Address	7-Bit Address
0	0	0x34	011 0100
0	1	0x35	011 0101
1	0	0x36	011 0110
1	1	0x37	011 0111

The device also has several identification registers (read only) that can be read across the SMBus. Table 12 lists these registers with their values and functions.

Table 12. Identification Register Values and Functions

Name	Address	Value	Function
MANID	0xF4	0x41	Manufacturer ID for Analog Devices
REVID	0xF5	0x2y	Super Sequencer family, 2 signifies the ADM1260 and y signifies the silicon revision

General SMBus Timing

Figure 38, Figure 39, and Figure 40 are timing diagrams for general read and write operations using the SMBus. The SMBus specification defines specific conditions for different types of read and write operations, which are discussed in the Write Operations section and the Read Operations section.

The general SMBus protocol operates in the following three steps:

1. The master initiates data transfer by establishing a start condition, defined as a high to low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit slave address (MSB first) plus an R/$\overline{W}$ bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write, 1 = read). The peripheral with an address corresponding to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and by holding it low during the high period of this clock pulse.
   All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low to high transition when the clock is high may be interpreted as a stop signal. If the operation is a write operation, the first data byte after the slave address is a command byte. This command byte tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written. Because data can flow in only one direction as defined by the R/$\overline{W}$ bit, sending a command to a slave device during a read operation is not possible. Before a read operation, it may be necessary to perform a write operation to tell the slave what type of read operation to expect and/or the address from which data is to be read.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse and then high during the 10th clock pulse to assert a stop condition.

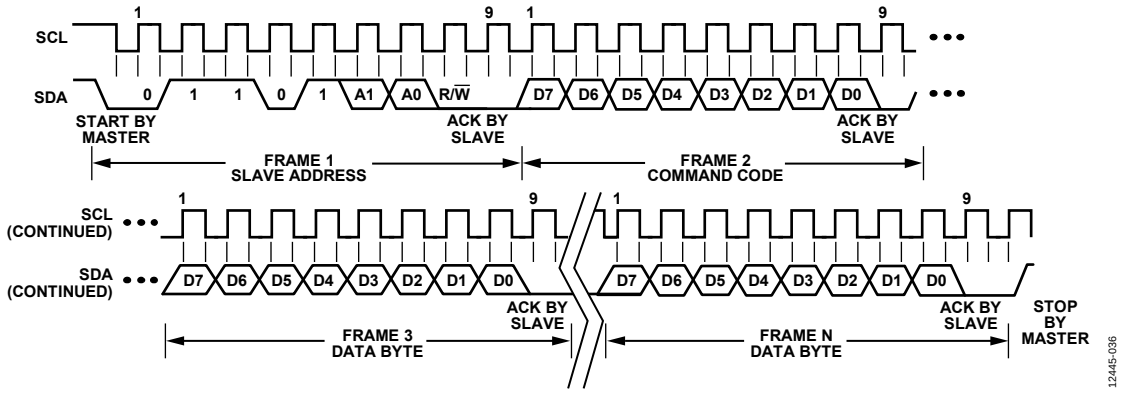


Figure 38. General SMBus Write Timing Diagram

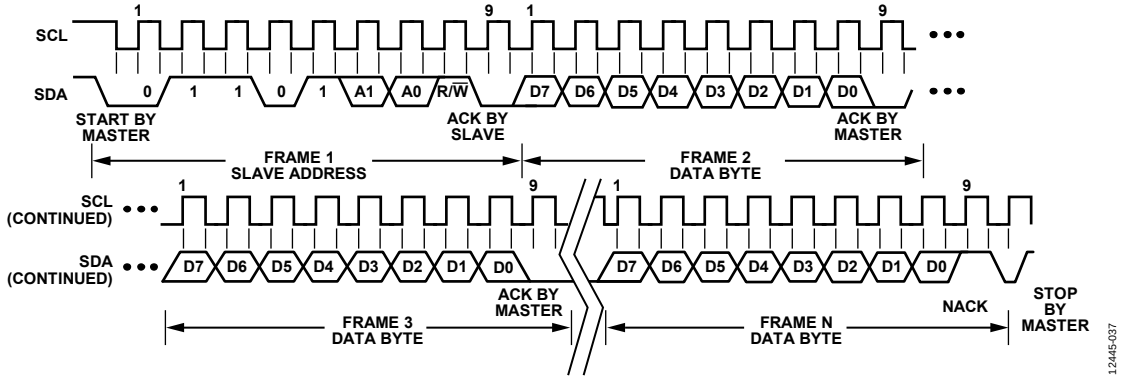


Figure 39. General SMBus Read Timing Diagram

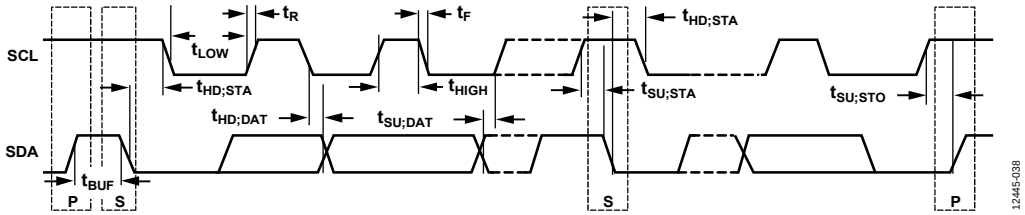


Figure 40. Serial Bus Timing Diagram

SMBus PROTOCOLS FOR RAM AND EEPROM

The ADM1260 contains volatile registers (RAM) and nonvolatile registers (EEPROM). User RAM occupies Address 0x00 to Address 0xDF, and the EEPROM occupies Address 0xF800 to Address 0xFBFF.

Data can be written to and read from both the RAM and the EEPROM as single data bytes. Data can be written only to unprogrammed EEPROM locations. To write new data to a programmed location, the location contents must first be erased. EEPROM erasure cannot be done at the byte level. The EEPROM is arranged as 32 pages of 32 bytes each, and an entire page must be erased.

Page erasure is enabled by setting Bit 2 in the UPDCFG register (Address 0x90) to 1. If this bit is not set, page erasure cannot occur, even if the command byte (0xFE) is programmed across the SMBus.

WRITE OPERATIONS

The SMBus specification defines several protocols for different types of read and write operations. The following abbreviations are used in Figure 41 to Figure 49:

- S = start
- P = stop
- R = read
- W = write
- A = acknowledge
- $\overline{A}$ = no acknowledge

The ADM1260 uses the SMBus write protocols discussed in the following sections.

Send Byte

In a send byte operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code.
5. The slave asserts an acknowledge on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADM1260, the send byte protocol is used for the following two purposes:

- To write a register address to the RAM for a subsequent single-byte read from the same address, or for a block read or block write starting at that address, as shown in Figure 41.

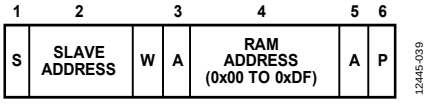


Figure 41. Setting a RAM Address for a Subsequent Read

- To erase a page of EEPROM memory. EEPROM memory can be written to only if it is unprogrammed. Before writing to one or more EEPROM memory locations that are already programmed, the page(s) containing those locations must first be erased. EEPROM memory is erased by writing a command byte.

The master sends a command code telling the slave device to erase the page. The ADM1260 command code for a page erasure is 0xFE (1111 1110). Note that for a page erasure to occur, the page address must be given in the previous write word transaction (see the Write Byte/Word section). In addition, Bit 2 in the UPDCFG register (Address 0x90) must be set to 1.

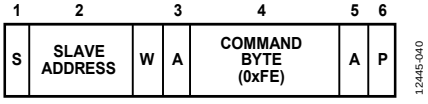


Figure 42. EEPROM Page Erasure

As soon as the ADM1260 receives the command byte, page erasure begins. The master device can send a stop command as soon as it sends the command byte. Page erasure takes approximately 20 ms. If the ADM1260 is accessed before erasure is complete, it responds with a no acknowledge .

Write Byte/Word

In a write byte/word operation, the master device sends a command byte and one or two data bytes to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte.
7. The slave asserts an acknowledge on SDA.
8. The master sends a data byte or asserts a stop condition.
9. The slave asserts an acknowledge on SDA.
10. The master asserts a stop condition on SDA to end the transaction.

In the ADM1260, the write byte/word protocol is used for the following three purposes:

- To write a single byte of data to the RAM. In this case, the command byte is RAM Address 0x00 to RAM Address 0xDF, and the only data byte is the actual data, as shown in Figure 43.

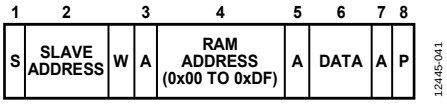


Figure 43. Single Byte Write to the RAM

- To set up a 2-byte EEPROM address for a subsequent read, write, block read, block write, or page erase. In this case, the command byte is the high byte of EEPROM Address 0xF8 to EEPROM Address 0xFB. The only data byte is the low byte of the EEPROM address, as shown in Figure 44.

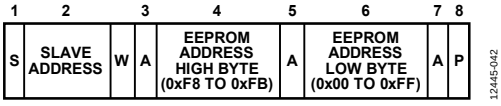


Figure 44. Setting an EEPROM Address

Because a page consists of 32 bytes, only the three MSBs of the address low byte are important for page erasure. The lower five bits of the EEPROM address low byte specify the addresses within a page and are ignored during an erase operation.

- To write a single byte of data to the EEPROM. In this case, the command byte is the high byte of EEPROM Address 0xF8 to EEPROM Address 0xFB. The first data byte is the low byte of the EEPROM address, and the second data byte is the actual data, as shown in Figure 45.

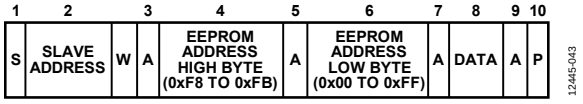


Figure 45. Single Byte Write to the EEPROM

Block Write

In a block write operation, the master device writes a block of data to a slave device. The start address for a block write must be set previously. In the ADM1260, a send byte operation sets a RAM address, and a write byte/word operation sets an EEPROM address, as follows:

8. The master device asserts a start condition on SDA.
9. The master sends the 7-bit slave address followed by the write bit (low).
10. The addressed slave device asserts an acknowledge on SDA.
11. The master sends a command code that tells the slave device to expect a block write. The ADM1260 command code for a block write is 0xFC (1111 1100).
12. The slave asserts an acknowledge on SDA.
13. The master sends a data byte that tells the slave device how many data bytes are being sent. The SMBus specification allows a maximum of 32 data bytes in a block write.
14. The slave asserts an acknowledge on SDA.
15. The master sends N data bytes.
16. The slave asserts an acknowledge on SDA after each data byte.
17. The master asserts a stop condition on SDA to end the transaction.

Unlike some EEPROM devices that limit block writes to within a page boundary, there is no limitation on the start address when performing a block write to EEPROM, except when

- There must be at least N locations from the start address to the highest EEPROM address (0xFBFF) to avoid writing to invalid addresses.
- An address crosses a page boundary. In this case, both pages must be erased before programming.

Note that the ADM1260 features a clock extend function for writes to the EEPROM. Programming an EEPROM byte takes approximately 250 µs, which limits the SMBus clock for repeated or block write operations. The ADM1260 pulls SCL low and extends the clock pulse when it cannot accept any more data.

READ OPERATIONS

The ADM1260 uses the SMBus read protocols discussed in the following sections.

Receive Byte

In a receive byte operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts a no acknowledge on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADM1260, the receive byte protocol is used to read a single byte of data from a RAM or EEPROM location whose address has previously been set by a send byte or write byte/word operation, as shown in Figure 46.

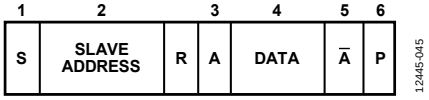


Figure 46. Single Byte Read from the EEPROM or RAM

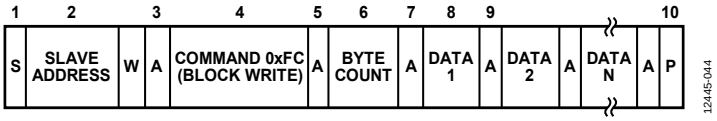


Figure 47. Block Write to the EEPROM or RAM

Block Read

In a block read operation, the master device reads a block of data from a slave device. The start address for a block read must be set previously. In the ADM1260, this is achieved by a send byte operation to set a RAM address, or a write byte/word operation to set an EEPROM address. The block read operation itself consists of a send byte operation that sends a block read command to the slave, immediately followed by a repeated start and a read operation that reads out multiple data bytes, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code that tells the slave device to expect a block read. The ADM1260 command code for a block read is 0xFD (1111 1101).
5. The slave asserts an acknowledge on SDA.
6. The master asserts a repeat start condition on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts an acknowledge on SDA.
9. The ADM1260 sends a byte count data byte that tells the master how many data bytes to expect. The ADM1260 always returns 32 data bytes (0x20), which is the maximum allowed by the SMBus Version 1.1 specification.
10. The master asserts an acknowledge on SDA.
11. The master receives 32 data bytes.
12. The master asserts an acknowledge on SDA after each data byte and a no acknowledge is generated after the last byte to signal the end of the read.
13. The master asserts a stop condition on SDA to end the transaction.

Error Correction

The ADM1260 provides the option of issuing a packet error correction (PEC) byte after a write to the RAM, a write to the EEPROM, a block write to the RAM/EEPROM, or a block read from the RAM/EEPROM. This option enables the user to verify that the data received by or sent from the ADM1260 is correct. The PEC byte is an optional byte sent after the last data byte is written to or read from the ADM1260. The protocol is the same as a block read for Step 1 to Step 12 and then proceeds as follows:

1. The ADM1260 issues a PEC byte to the master. The master checks the PEC byte and issues another block read, if the PEC byte is incorrect.
2. A no acknowledge is generated after the PEC byte to signal the end of the read.
3. The master asserts a stop condition on SDA to end the transaction.

Note that the PEC byte is calculated using CRC-8. The frame check sequence (FCS) conforms to CRC-8 by the polynomial

$$C(x) = x^8 + x^2 + x^1 + 1$$

See the SMBus Version 1.1 specification for details. An example of a block read with the optional PEC byte is shown in Figure 49.

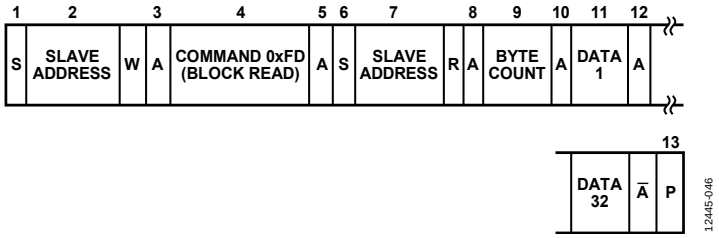


Figure 48. Block Read from the EEPROM or RAM

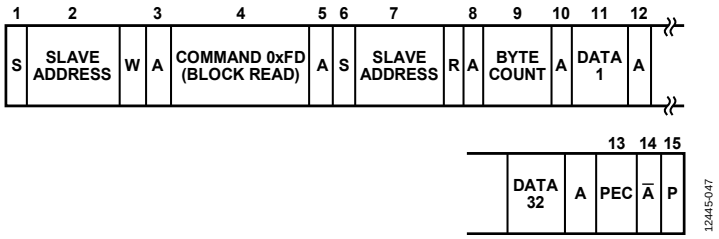


Figure 49. Block Read from the EEPROM or RAM with PEC

INTERCHIP BUS

OVERVIEW

The interchip bus (ICB) is the fundamental way to solve scalability from a hardware point of view. The ICB makes the linking of multiple ADM1260 devices trivial to support sequencing, monitoring, and managing a large number of supply rails. The ICB uses only two dedicated pins (CCL, CDA) and supports up to four ADM1260 devices on the same bus.

The ICB coordinates sequencing operations and transitions between the SEs in a system with multiple ADM1260 devices. For example, multiple devices are monitoring different input supplies. If a fault condition is detected in one of the rails in a particular device, that condition can be communicated to all the other devices. The receipt of a message on the ICB informs the other devices of the type of transition, and instructs those devices to synchronize the transition of their SEs and, therefore, their PDOx status change based on the sequence condition. The ICB can be thought of as linking the SEs of multiple devices so that all the devices can work as a single entity.

The ADI Power Studio software configures a sequencing system built with multiple ADM1260 devices. The software provides an abstraction to the end user for managing the complexity of dealing with multiple devices by representing the devices as a single virtual sequencer. The software maps the user configuration of the virtual sequencer to each of the sequencer devices, using the ICB to implement the virtual sequence defined by the user in the ADI Power Studio. The software generates any pings and pongs necessary, and the user does not need to manage them manually.

The user can manage from the ADI Power Studio one virtual sequencer with N × 10 rails instead of having to manage the sequencing between N physical sequencer devices, with 10 supplies each. The user can turn on the N × 10 supply rails in any order in the virtual sequencer. However, it is highly recommended to sequence all the rails in one physical device before moving to the next device to avoid using up states for a ping-pong action. The software acknowledges the ICB and the physical devices that monitor and control the rails. The software uses this knowledge to coordinate and hand over sequencing responsibilities between the devices while remaining transparent to the user.

MESSAGE FORMATS

Each ICB message consists of 8 bits of data on the CDA line followed by an acknowledge bit, and the message is transmitted using a 400 kHz (typical) clock on the CCL line.

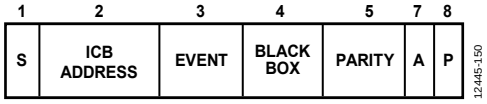


Figure 50. ICB Message Format

Message priority is defined by the destination and event type; broadcasts have higher priority than unicasts. Among the broadcast messages, monitor events have the highest priority, followed by timeout, and then sequence broadcast.

Every state transition generates one (1 byte) ICB message. Typically, it takes 25 µs to transmit one message over the ICB. State transition happens only after the message is successfully transmitted.

ICB ADDRESSING AND EVENT

There are two types of ICB addressing: broadcast addressing and unicast addressing. Broadcast address is set to 0x0 and is used when a message is being sent to all devices. Unicast addressing is used when a message is being sent to only one device. Each ADM1260 on the ICB is given a unique ICB address, and the address is independent of the I²C address. Because a maximum number of four ADM1260 devices can be cascaded, the valid range of an ICB address is 0x1 to 0x4.

There are two bits for defining the event type in a message, and there are four defined events that can be sent on the ICB: monitor exit, timeout exit, broadcast sequence exit, and local sequence exit.

A monitor broadcast message is transmitted when an active monitor condition occurs. When the message is received, it causes a device to jump to the state defined by the monitor exit state in the active physical state. There is no need for an active monitor; the exit state is still followed in the case of a monitor broadcast message.

A timeout broadcast message is transmitted when an active timeout condition occurs. When received, it causes a device jump to the state defined by timeout exit state in the active physical state. A timeout condition does not need to be defined or enabled.

A sequence jump message can be one of two types: sequence broadcast or local sequence unicast.

A sequence broadcast message is transmitted when an active sequence condition occurs and the sequence broadcast enable bit is set in the active physical state. When the sequence broadcast message is received by the other devices on the bus, it jumps to the physical state that is defined locally in those devices.

A local sequence unicast message is transmitted when a supply monitoring or SMBus jump sequence condition triggers a sequence exit condition. This message is sent by the device to its own unicast address and is only for informational purposes.

ICB FAULT HANDLING

The system jumps to a bus fault state in the case of a parity bit error, or if either CDA or CCL is held low for more than 128 µs. The local state machine jumps to the bus fault state defined by the ICBCFG2 register.

If a device loses power, it pulls down the CDA line as the VDDCAP pin enters UVLO. However, if the other devices on the bus are operating normally, they recognize the CDA pull-down as a bus fault and jump to bus fault state.

ICB PULL-UP RESISTOR

Pull up the ICB line before or at the same time as the ADM1260 powers up. The pull-up must stay as long as the ADM1260 is powered and operating. Keep the lines glitch free to avoid false ICB fault triggering. It is recommended to use a 1.1 kΩ pull-up resistor for voltages up to 5 V.

CONFIGURATION REGISTERS

UPDATING THE MEMORY, ENABLING BLOCK ERASURE, AND DOWNLOADING EEPROM

The ADM1260 contains both volatile and nonvolatile memory, which must be set up correctly if any alterations to the configuration are to be updated properly in the device. The volatile memory of the device is constructed with double buffered latches.

The register and bit details in Figure 51 show the configurations required to perform the following actions:

- Update the volatile memory in real time.
- Update the volatile memory offline, then update the memory all at once.
- Enable block erasure.
- Download EEPROM contents to the RAM.

There are also a number of configuration bits that update the sequencing engine. These bits are detailed in Table 13.

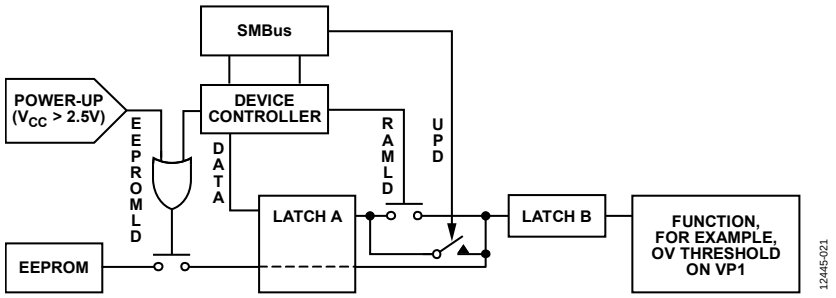


Figure 51. Configuration Update Flow Diagram

Table 13. Configuration Bits to Update the Sequencing Engine

Register Address	Register Name	Bits	Bit Names	R/W	Description
0x90	UPDCFG	[7:3]	Not applicable	Not applicable	These bits cannot be used.
		2	EEBLKERS	R/W	This bit enables the configuration EEPROM block erasure.
		1	CFGUPD	W	This bit updates the configuration registers from holding other registers; this bit self clears.
		0	CONTUPD	R/W	This bit enable the continuous update of the configuration registers.
0xD8	UDOWNLD	[7:1]	Not applicable	Not applicable	These bits cannot be used.
		0	EEDWNLD	W	This bit downloads configuration data from EEPROM (which also happens automatically at power-up); this bit self clears on completion.
0xF4	MANID	[7:0]	MANID	R	These bits are the manufacturer ID; they return 0x41 and can be used to verify communication with the device.

INPUTS

The ADM1260 has 10 inputs. Five of these inputs are dedicated supply fault detectors, highly programmable reset generators with inputs that can detect overvoltage, undervoltage, or out of window faults. With these five inputs, voltages from 0.573 V to 14.4 V can be supervised. The undervoltage and overvoltage thresholds can all be programmed to an 8-bit resolution. The comparators that detect faults on the inputs have digitally programmable hysteresis to provide immunity to supply bounce. Each of these inputs also has a glitch filter with a timeout programmable up to 100 µs.

The other five inputs on the ADM1260 have dual functionality. They can be used as analog inputs, as with the first five channels, as previously described, or as general-purpose logic inputs. As analog inputs, these channels function exactly the same as those described earlier in this section. The major difference is that these inputs do not have internal potentiometer resistors and present a true high impedance to the input pin. Their input range is thus limited to 0.573 V to 1.375 V, but the high impedance means that an external resistor divider network can be used to divide down any out of range supply to a value within range. Therefore, −5 V, −12 V, +24 V, and +48 V can all be supervised by these channels with the appropriate external resistor divider network.

As digital inputs, these pins can be used to detect enable signals (such as PWRGD and POWRON) and are TTL- and CMOS-compatible. When used in this mode, the analog circuitry of these pins can be mapped to their sister input pins (one of the first five inputs previously described). Thus, VX1 can be used as a second detector on VP1, VX2 can be used with VP2, and so on. VX5 is mapped to VH. With a second detector available, the user can program warnings as well as fault functions.

Table 14 details all of the registers used to configure the inputs to perform the functions described in this section.

Table 14. Registers Used to Configure the Inputs

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description			
VP1	0x00	PS1OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage (OV) threshold on PS1 SFD.			
	0x01	PS1OVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS1OVTH when OV is true.			
	0x02	PS1UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on PS1 SFD.			
	0x03	PS1UVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from PS1UVTH when undervoltage (UV) is true.			
	0x04	SFDV1CFG	[7:5]	Not applicable		These bits cannot be used.			
			[4:2]	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			[1:0]	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Selection**	
						0	0	Overvoltage	
						0	1	Undervoltage or overvoltage	
						1	0	Undervoltage	
						1	1	Off	
	0x05	SFDV1SEL	[7:2]	Not applicable		These bits cannot be used			
			[1:0]	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Selection**	
						0	0	Midrange (2.5 V to 6.0 V)	
						0	1	Low range (1.25 V to 3.00 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	
VP2	0x08	PS2OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on PS2 SFD.			
	0x09	PS2OVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS2OVTH when OV is true.			
	0x0A	PS2UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on PS2 SFD.			

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description			
	0x0B	PS2UVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from PS2UVTH when UV is true.			
	0x0C	SFDV2CFG	[7:5]	Not applicable		These bits cannot be used.			
			[4:2]	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			[1:0]	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Selection**	
						0	0	Overvoltage	
						0	1	Undervoltage or overvoltage	
						1	0	Undervoltage	
						1	1	Off	
	0x0D	SFDV2SEL	[7:2]	Not applicable		These bits cannot be used.			
			[1:0]	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Selection**	
						0	0	Midrange (2.5 V to 6.0 V)	
						0	1	Low range (1.25 V to 3.00 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	
VP3	0x10	PS3OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on PS3 SFD.			
	0x11	PS3OVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS3OVTH when OV is true.			
	0x12	PS3UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undevoltage threshold on PS3 SFD.			
	0x13	PS3UVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from PS3UVTH when UV is true.			
	0x14	SFDV3CFG	[7:5]	Not applicable		These bits cannot be used.			
			[4:2]	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			[1:0]	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Selection**	
						0	0	Overvoltage	
						0	1	Undervoltage or overvoltage	
						1	0	Undervoltage	
						1	1	Off	
	0x15	SFDV3SEL	[7:2]	Not applicable		These bits cannot be used.			
			[1:0]	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Select**	
						0	0	Midrange (2.5 V to 6.0 V)	
						0	1	Low range (1.25 V to 3.00 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description			
VP4	0x18	PS4OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on PS4 SFD.			
	0x19	PS4OVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS4OVTH when OV is true.			
	0x1A	PS4UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on PS4 SFD.			
	0x1B	PS4UVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from PS4UVTH when UV is true.			
	0x1C	SFDV4CFG	[7:5]	Not applicable		These bits cannot be used.			
			[4:2]	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			[1:0]	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Selection**	
						0	0	Overvoltage	
						0	1	Undervoltage or overvoltage	
						1	0	Undervoltage	
						1	1	Off	
	0x1D	SFDV4SEL	[7:2]	Not applicable		These bits cannot be used.			
			[1:0]	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Selection**	
						0	0	Midrange (2.5 V to 6.0 V)	
						0	1	Low range (1.25 V to 3.00 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	
VH	0x20	PSVHOVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on PSVH SFD.			
	0x21	PSVHOVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PSVHOVTH when OV is true.			
	0x22	PSVHUVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the UV threshold on PSVH SFD.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from PSVHUVTH when UV is true.			
	0x24	SFDVHCFG	[7:5]	Not applicable		These bits cannot be used.			
			[4:2]	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			[1:0]	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Selection**	
						0	0	Overvoltage	
						0	1	Undervoltage or overvoltage	
						1	0	Undervoltage	
						1	1	Off	
	0x25	SFDVHSEL	[7:1]	Not applicable		These bits cannot be used.			
			0	SEL0	R/W	**SEL0**	**Range Selection**		
						0	Low range (2.5 V to 6.0 V)		
						1	High range (6.0 V to 14.4 V)		

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VX1	0x28	X1OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on the VX1 SFD.
	0x29	X1OVHYST	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X1OVTH when OV is true.
	0x2A	X1UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on X1 SFD.
	0x2B	X1UVHYST	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from X1UVTH when UV is true.
	0x2C	SFDX1CFG	[7:5]	Not applicable		These bits cannot be used.
			[4:2]	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100
			[1:0]	RS1 to RS0	R/W	**RS1** / **RS0** / **Fault Type Selection** 0 / 0 / Overvoltage 0 / 1 / Undervoltage or overvoltage 1 / 0 / Undervoltage 1 / 1 / Off
	0x2D	SFDVX1SEL	[7:2]	Not applicable		These bits cannot be used.
			[1:0]	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Function Selection** 0 / 0 / SFD (fault) only 0 / 1 / GPI (fault) only 1 / 0 / GPI (fault) + SFD (warning) 1 / 1 / No function (input can still be used as ADC input)
	0x2E	GPIX1CFG	7	Not applicable		This bit cannot be used.
			6	INVIN	R/W	If this bit is high, the input is inverted.
			5	INTYP	R/W	This bit determines whether a level or an edge is detected on the pin. **INTYP Setting** / **Level or Edge Detection** 0 / Detects level 1 / Detects edge
			[4:3]	PULS1 to PULS0	R/W	These bits determine the length of the pulse output after an edge is detected on the input. **PULS1 Setting** / **PULS0 Setting** / **Pulse Length (µs)** 0 / 0 / 10 0 / 1 / 100 1 / 0 / 1000 1 / 1 / 10,000
			[2:0]	GF2 to GF0	R/W	Glitch filter. These bits determine the length of time for which a pulse is ignored. **GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VX2	0x30	X2OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on the VX2 SFD.
	0x31	X2OVHYST	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X2OVTH when OV is true.
	0x32	X2UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on the VX2 SFD.
	0x33	X2UVHYST	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from X2UVTH when UV is true.
	0x34	SFDX2CFG	[7:5]	Not applicable		These bits cannot be used.
			[4:2]	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100
			[1:0]	RS1 to RS0	R/W	**RS1** / **RS0** / **Fault Type Selection** 0 / 0 / Overvoltage 0 / 1 / Undervoltage or overvoltage 1 / 0 / Undervoltage 1 / 1 / Off
	0x35	SFDVX2SEL	[7:2]	Not applicable		These bits cannot be used.
			[1:0]	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Function Selection** 0 / 0 / SFD (fault) only 0 / 1 / GPI (fault) only 1 / 0 / GPI (fault) + SFD (warning) 1 / 1 / No function (input can still be used as ADC input)
	0x36	GPIX2CFG	7	Not applicable		This bit cannot be used.
			6	INVIN	R/W	If this bit is high, the input is inverted.
			5	INTYP	R/W	This bit determines whether a level or an edge is detected on the pin. **INTYP Setting** / **Level or Edge Detection** 0 / Detects level 1 / Detects edge
			[4:3]	PULS1 to PULS0	R/W	These bits determine the length of the pulse output after an edge is detected on the input. **PULS1 Setting** / **PULS0 Setting** / **Pulse Length (µs)** 0 / 0 / 10 0 / 1 / 100 1 / 0 / 1000 1 / 1 / 10,000
			[2:0]	GF2 to GF0	R/W	Glitch filter. These bits determine the length of time for which a pulse is ignored. **GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VX3	0x38	X3OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on the VX3 SFD.
	0x39	X3OVHYST	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X3OVTH when OV is true.
	0x3A	X3UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on the VX3 SFD.
	0x3B	X3UVHYST 7	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from X3UVTH when UV is true.
	0x3C	SFDX3CFG	[7:5]	Not applicable		These bits cannot be used.
			[4:2]	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100
			[1:0]	RS1 to RS0	R/W	**RS1** / **RS0** / **Fault Type Selection** 0 / 0 / Overvoltage 0 / 1 / Undervoltage or overvoltage 1 / 0 / Undervoltage 1 / 1 / Off
	0x3D	SFDVX3SEL	[7:2]	Not applicable		These bits cannot be used.
			[1:0]	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Function Selection** 0 / 0 / SFD (fault) only 0 / 1 / GPI (fault) only 1 / 0 / GPI (fault) + SFD (warning)
	0x3E	GPIX3CFG	7	Not applicable		This bit cannot be used.
			6	INVIN	R/W	If this bit is high, the input is inverted.
			5	INTYP	R/W	This bit determines whether a level or an edge is detected on the pin. **INTYP Setting** / **Level or Edge Detection** 0 / Detects level 1 / Detects edge
			[4:3]	PULS1 to PULS0	R/W	These bits determine the length of the pulse output after an edge is detected on the input. **PULS1** / **PULS0** / **Pulse Length (µs)** 0 / 0 / 10 0 / 1 / 100 1 / 0 / 1000 1 / 1 / 10,000
			[2:0]	GF2 to GF0	R/W	Glitch filter. These bits determine the length of time for which a pulse is ignored. **GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VX4	0x40	X4OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on the VX4 SFD.
	0x41	X4OVHYST	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X4OVTH when OV is true.
	0x42	X4UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on the VX4 SFD.
	0x43	X4UVHYST	[7:5]	Not applicable		These bits cannot be used.
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from X4UVTH when UV is true.
	0x44	SFDX4CFG	[7:5]	Not applicable		These bits cannot be used.
			[4:2]	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100
			[1:0]	RS1 to RS0	R/W	**RS1** / **RS0** / **Fault Type Selection** 0 / 0 / Overvoltage 0 / 1 / Undervoltage or overvoltage 1 / 0 / Undervoltage 1 / 1 / Off
	0x45	SFDVX4SEL	[7:2]	Not applicable		These bits cannot be used.
			[1:0]	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Function Selection** 0 / 0 / SFD (fault) only 0 / 1 / GPI (fault) only 1 / 0 / GPI (fault) + SFD (warning) 1 / 1 / No function (input can still be used as ADC input)
	0x46	GPIX4CFG	7	Not applicable		This bit cannot be used.
			6	INVIN	R/W	If this bit is high, the input is inverted.
			5	INTYP	R/W	This bit determines whether a level or an edge is detected on the pin. **INTYP Setting** / **Level or Edge Detection** 0 / Detects level 1 / Detects edge
			[4:3]	PULS1 to PULS0	R/W	These bits determine the length of the pulse output after an edge is detected on the input. **PULS1** / **PULS0** / **Pulse Length (µs)** 0 / 0 / 0 0 / 1 / 100 1 / 0 / 1000 1 / 1 / 10,000
			[2:0]	GF2 to GF0	R/W	Glitch filter. These bits determine the length of time for which a pulse is ignored. **GF2** / **GF1** / **GF0** / **Delay (µs)** 0 / 0 / 0 / 0 0 / 0 / 1 / 5 0 / 1 / 0 / 10 0 / 1 / 1 / 20 1 / 0 / 0 / 30 1 / 0 / 1 / 50 1 / 1 / 0 / 75 1 / 1 / 1 / 100

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description			
VX5	0x48	X5OVTH	[7:0]	OV7 to OV0	R/W	8-bit digital value for the overvoltage threshold on the VX5 SFD.			
	0x49	5OVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X5OVTH when OV is true.			
	0x4A	X5UVTH	[7:0]	UV7 to UV0	R/W	8-bit digital value for the undervoltage threshold on the VX5 SFD.			
	0x4B	X5UVHYST	[7:5]	Not applicable		These bits cannot be used.			
			[4:0]	HY4 to HY0	R/W	5-bit hysteresis to be added from X5UVTH when UV is true.			
	0x4C	SFDX5CFG	[7:5]	Not applicable		These bits cannot be used.			
			[4:2]	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			[1:0]	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Selection**	
						0	0	Overvoltage	
						0	1	Undervoltage or overvoltage	
						1	0	Undervoltage	
						1	1	Off	
	0x4D	SFDVX5SEL	[7:2]	Not applicable		These bits cannot be used.			
			[1:0]	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Function Selection**	
						0	0	SFD (fault) only	
						0	1	GPI (fault) only	
						1	0	GPI (fault) + SFD (warning)	
						1	1	No function (input can still be used as ADC input)	
	0x4E	GPIX5CFG	7	Not applicable		These bits cannot be used.			
			6	INVIN	R/W	If this bit is high, the input is inverted.			
			5	INTYP	R/W	This bit determines whether a level or an edge is detected on the pin.			
						INTYP Setting	**Level or Edge Detection**		
						0	Detects level		
						1	Detects edge		
			[4:3]	PULS1 to PULS0	R/W	These bits determine the length of the pulse output after an edge is detected on the input.			
						PULS1	**PULS0**	**Pulse Length (µs)**	
						0	0	0	
						0	1	100	
						1	0	1000	
						1	1	10,000	
			[2:0]	GF2 to GF0	R/W	Glitch filter. These bits determine the length of time for which a pulse is ignored.			
						GF2	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100

OUTPUTS

The ADM1260 has 10 programmable driver outputs. Supply sequencing is achieved with the devices by using the PDOx pins as control signals for supplies. The output drivers can be used either as logic enables or FET drivers.

The PDOx pins can be used for a number of functions; the primary function is to provide enable signals for LDOs or dc-to-dc converters, which generate supplies locally on a board. The PDOx pins can also be used to provide a power-good signal when all of the SFDs are in tolerance or to provide a reset output if one of the SFDs goes out of specification (this can be used as a status signal for a DSP, FPGA, or other microcontroller).

The PDOx pins can be programmed to pull up to a number of different options. The outputs can be programmed as follows:

- Open drain, allowing the user to connect an external pull-up resistor.
- Open drain with a weak pull-up to VDDCAP.
- Push-pull to VDDCAP.
- Open drain with a weak pull-up to VPx.
- Push-pull to VPx.
- As a strong pull-down to GND.
- Internally charge pumped high drive (12 V, PDO1 to PDO6).

The last option (available only on PDO1 to PDO6) allows the user to directly drive a voltage high enough to fully enhance an external N-FET, which is used to isolate, for example, a card side voltage from a backplane supply (when a PDOx pin sustains greater than 10.5 V into a 1 µA load). The pull-down switches can be used to drive status LEDs.

The data driving each of the PDOx pins can come from one of three sources. The source can be enabled for a particular output, that is, PDO1, in the PDOCFG configuration register. The data sources are as follows:

- An output from the SE.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This enables software control of the PDOs. Thus, a microcontroller can be used to initiate a software power-up/power-down sequence.
- An on-chip clock. A 100 kHz clock is generated on the device. This clock can be made available on any of the PDOx pins and can be used to clock an external device, such as an LED.

Table 15 details all of the registers used to configure the outputs to perform the functions described in this section.

Table 15. Registers Used to Configure the Outputs[1]

Output	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
PDO1	0x07	PDO1CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

PDO2	0x0F	PDO2CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

Output	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
PDO3	0x17	PDO3CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

PDO4	0x1F	PDO4CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP

Output	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
PDO5	0x27	PDO5CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP

PDO6	0x2F	PDO6CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	None

Output	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
PDO7	0x37	PDO7CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Do not use
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

PDO8	0x3F	PDO8CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

			[3:0]	CFG3 to CFG0	R/W	These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOs Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Do not use
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

Output	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
PDO9	0x47	PDO9CFG	7	Not applicable		This bit cannot be used.
			[6:4]	CFG6 to CFG4	R/W	These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

[3:0] CFG3 to CFG0 R/W — These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Do not use
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

PDO10 0x4F PDO10CFG 7 Not applicable — This bit cannot be used.

[6:4] CFG6 to CFG4 R/W — These bits control the logic source driving the PDOx pin, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDOx Status
0	0	0	Disabled, with a weak pull-down resistor
0	0	1	Enabled; follows the logic driven by the SE
0	1	0	Enables SMBus data, driven low
0	1	1	Enables SMBus data, driven high
1	X	X	Enables the 100 kHz clock out onto the pin

[3:0] CFG3 to CFG0 R/W — These bits determine the format of the pull-up resistor on the PDOx pin.

CFG3	CFG2	CFG1	CFG0	PDOx Pull-Up Resistor
0	0	0	X	None
0	0	1	X	Do not use
0	1	0	0	Weak, open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak, open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak, open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak, open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak, open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

[1] X means don't care.

SEQUENCING ENGINE

The ADM1260 incorporate a sequencing engine (SE) that provides the user with powerful and flexible control of sequencing. The SE implements state machine control of the PDOx outputs, with state changes conditional on input events. SE programs can enable complex control of boards, such as power-up and power-down sequence control, fault event handling, and interrupt generation on warnings. A watchdog function to verify the continued operation of a processor clock can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing. Considering the function of the SE from an applications viewpoint, it is best to think of the SE as providing a state for a state machine.

The ADM1260 offers up to 61 such state definitions. Each state is defined by a 64-bit word.

Table 17 shows the details of the 64 bits that define a state.

Table 20 details how to communicate with the SE in the ADM1260.

Table 21 provides details of additional sequence engine control registers present the ADM1260 that allow the sequence engine to be restarted.

Table 16. Starting Address for Each State in the SE

State	Start Address (Hexadecimal)
Reserved state	0xFA00
State 1 (configured as bus fault state by the GUI)	0xFA08
State 2	0xFA10
State 3	0xFA18
State 4	0xFA20
State 5	0xFA28
State 6	0xFA30
State 7	0xFA38
State 8	0xFA40
State 9	0xFA48
State 10	0xFA50
State 11	0xFA58
State 12	0xFA60
State 13	0xFA68
State 14	0xFA70
State 15	0xFA78
State 16	0xFA80
State 17	0xFA88
State 18	0xFA90
State 19	0xFA98
State 20	0xFAA0
State 21	0xFAA8
State 22	0xFAB0
State 23	0xFAB8
State 24	0xFAC0
State 25	0xFAC8
State 26	0xFAD0
State 27	0xFAD8
State 28	0xFAE0
State 29	0xFAE8
State 30	0xFAF0
State 31	0xFAF8
State 32	0xFB00
State 33	0xFB08
State 34	0xFB10
State 35	0xFB18
State 36	0xFB20
State 37	0xFB28
State 38	0xFB30
State 39	0xFB38

State	Start Address (Hexadecimal)
State 40	0xFB40
State 41	0xFB48
State 42	0xFB50
State 43	0xFB58
State 44	0xFB60
State 45	0xFB68
State 46	0xFB70
State 47	0xFB78
State 48	0xFB80
State 49	0xFB88
State 50	0xFB90
State 51	0xFB98
State 52	0xFBA0
State 53	0xFBA8
State 54	0xFBB0
State 55	0xFBB8
State 56	0xFBC0
State 57	0xFBC8
State 58	0xFBD0
State 59	0xFBD8
State 60	0xFBE0
State 61	0xFBE8
State 62	0xFBF0
State 63 (configured as sequence fault state by the GUI)	0xFBF8

Table 17. Bit Map for the Definition of Each State in the SE

Bit No.	Operation/If Set to 0	If Set to 1	Description
0	Set PDO1 low	Set PDO1 high	PDO1 output data.
1	Set PDO2 low	Set PDO2 high	PDO2 output data
2	Set PDO3 low	Set PDO3 high	PDO3 output data.
3	Set PDO4 low	Set PDO4 high	PDO4 output data.
4	Set PDO5 low	Set PDO5 high	PDO5 output data.
5	Set PDO6 low	Set PDO6 high	PDO6 output data.
6	Set PDO7 low	Set PDO7 high	PDO7 output data.
7	Set PDO8 low	Set PDO8 high	PDO8 output data.
8	Set PDO9 low	Set PDO9 high	PDO9 output data.
9	Set PDO10 low	Set PDO10 high	PDO10 output data.
10	Monitor fault if VP1 = 0	Monitor fault if VP1 = 1	Monitoring of faults on VP1 must be unmasked for this function to execute (next bit).
11	Mask VP1 monitoring	Unmask VP1 monitoring	Bit 11 = 1; turns on monitoring on the VP1 channel.
12	Monitor fault if VP2 = 0	Monitor fault if VP2 = 1	Monitoring of faults on VP2 must be unmasked for this function to execute (next bit).
13	Mask VP2 monitoring	Unmask VP2 monitoring	Bit 13 = 1; turns on monitoring on the VP2 channel.
14	Monitor Fault if VP3 = 0	Monitor fault if VP3 = 1	Monitoring of faults on VP3 must be unmasked for this function to execute (next bit).
15	Mask VP3 monitoring	Unmask VP3 monitoring	Bit 15 = 1; turns on monitoring on the VP3 channel.
16	Monitor fault if VP4 = 0	Monitor fault if VP4 = 1	Monitoring of faults on VP4 must be unmasked for this function to execute (next bit).
17	Mask VP4 monitoring	Unmask VP4 monitoring	Bit 17 = 1; turns on monitoring on the VP4 channel.
18	Monitor fault if VH = 0	Monitor fault if VH = 1	Monitoring of faults on VH must be unmasked for this function to execute (next bit).
19	Mask VH monitoring	Unmask VH monitoring	Bit 19 = 1; turns on monitoring on the VH channel.

Bit No.	Operation/If Set to 0	If Set to 1	Description
20	Monitor fault if VX1 = 0	Monitor fault if VX1 = 1	Monitoring of faults on VX1 must be unmasked for this function to execute (next bit).
21	Mask VX1 monitoring	Unmask VX1 monitoring	Bit 21 = 1; turns on monitoring on the VX1 channel.
22	Monitor fault if VX2 = 0	Monitor fault if VX2 = 1	Monitoring of faults on VX2 must be unmasked for this function to execute (next bit).
23	Mask VX2 monitoring	Unmask VX2 monitoring	Bit 23 = 1; turns on monitoring on the VX2 channel.
24	Monitor fault if VX3 = 0	Monitor fault if VX3 = 1	Monitoring of faults on VX3 must be unmasked for this function to execute (next bit).
25	Mask VX3 monitoring	Unmask VX3 monitoring	Bit 25 = 1; turns on monitoring on the VX3 channel.
26	Monitor fault if VX4 = 0	Monitor fault if VX4 = 1	Monitoring of faults on VX4 must be unmasked for this function to execute (next bit).
27	Mask VX4 monitoring	Unmask VX4 monitoring	Bit 27 = 1; turns on monitoring on the VX4 channel.
28	Monitor fault if VX5 = 0	Monitor fault if VX5 = 1	Monitoring of faults on VX5 must be unmasked for this function to execute (next bit).
29	Mask VX5 monitoring	Unmask VX5 monitoring	Bit 29 = 1; turns on monitoring on the VX5 channel.
30	Mask warning monitoring	Unmask warning monitoring	Can only generate a monitor fault on warning = 1. Is unmasked.
[31:34]	TIMEOUT0 to TIMEOUT3	Not applicable	Timeout length (see Table 18).
[35:38]	SEQCOND0 to SEQCOND3	Not applicable	Sequence condition (see Table 18).
39	Sequence on selected input = high	Sequence on selected input = low	SEQSENSE.
[40:43]	SEQDELAY0 to SEQDELAY3	Not applicable	Sequence delay (see Table 18). This is also used as the ICB message address to send a ping when SEQCOND is set to send a ping. When SEQCOND is set to wait for a ping, this is used as the ICB message address to send the pong message back after a ping.
[44:49]	MONADDR0 to MONADDR5	Not applicable	MONADDRx is the state number to jump to if a monitor function fault occurs.
[50:55]	TIMADDR0 to TIMADDR5	Not applicable	TIMADDRx is the state number to jump to if a timeout fault occurs.
[56:61]	SEQADDR0 to SEQADDR5	Not applicable	SEQADDRx is the state number to jump to if a sequence fault occurs.
62	Round robin disable	Round robin enable	This is OR'ed with the enable (Address 0x82, Bit 1).
63	Do not send a broadcast sequence message	Send a broadcast sequence message	When this bit is set to 1 and the SE exits due to a local sequence condition, a broadcast sequence message is sent.

Table 18. Timeouts and Delays for Functions in the SE

TIMEOUT[3:0], SEQDELAY[3:0]	Delay (ms)	Ping-Pong ICB Message Address
0	0 for SEQCONDx; disables the TIMEOUTx condition	0
1	0.1	1
2	0.2	2
3	0.4	3
4	0.7	4
5	1	5
6	2	6
7	4	7
8	7	8
9	10	9
10	20	10
11	40	11
12	70	12
13	100	13
14	200	14
15	400	15

Table 19. SEQCOND[3:0] and Sequence On Signal From Within the SE

SEQCOND[3:0]	Sequence on Signal Source
0	Never sequence; always set SEQSENSE(Bit 39) = 0 to ensure no sequence (see Table 17).
1	VP1.
2	VP2.
3	VP3.
4	VP4.
5	VH.
6	VX1.
7	VX2.
8	VX3.
9	VX4.
10	VX5.
11	Warning.
12	SMBus jump. Wait for the SMBus command before jumping to the next state. Set SEQSENSE = 0 to ensure proper operation.
13	Reserved.
14	Send ping to the ICB message address defined by SEQDELAY.
15	Wait for ping and respond to the ICB message address defined by SEQDELAY.

Table 20. Communicating with the SE

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0x93	SECTRL	[7:3]	Not applicable		Reserved.
		2	SMBUS_JUMP	W	This bit allows software control of the SE state changes. This bit forces an unconditional jump to the next state and can be set as the condition for an end of step change. This setting enables the user to clear external interrupts by moving forward a state. This bit self clears to 0 after the state change occurs.
		1	SWSTEP	R/W	This bit steps the SE forward to the next state. Use this bit in conjunction with the halt bit to step through a sequence. This bit can be used as a tool for debugging sequences.
		0	Halt	R/W	This bit halts the SE, meaning that state changes do not occur. This bit must be set to allow read, erase, or write access to the SE EEPROM.
0xE9	SEADDR	[7:6]	Not applicable		Reserved.
		[5:0]	ADDR	R	This bit is the SE current state and is used in conjunction with the halt bit (Register 0x93, Bit 0).

Table 21. Additional SE Control Registers

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0xDA	UNLOCKSE	[7:0]	UNLOCK_KEY	W	Writing 0x27 and then 0x10 to this register in consecutive writes unlocks the SEDOWNLD register so that it can be written to. To reset the lock, write 0x00 to the unlock key. Writing to SEDOWNLD does not reset the lock.
0xDB	SEDOWNLD	[7:1]	Not applicable		Reserved.
		0	Restart	W	Writing a 1 to this bit causes the SE to restart immediately from the reserved state if the SE is running, that is, if the halt bit in the SECTRL register = 0. If the SE is halted, that is, if the halt bit in the SECTRL register = 1, the restart occurs when the halt bit in the SECTRL register is written to 0. This bit self clears.

CONFIGURING SEQUENCE ENGINE STATES TO WRITE INTO THE BLACK BOX EEPROM

The ADM1260 can use a section of EEPROM to store fault records when the SE enters a user defined trigger state. These states are defined in EEPROM and downloaded to registers along with the other configuration data when the ADM1260 is being initialized. The register locations of the black box write triggers are shown in Table 22. These locations are loaded from the same locations in the 0xF8xx EEPROM block. The BBWRTRGx registers are read/write and, therefore, can be modified by software if required after the download.

When one or more of the bits in the BBWRTRx registers are set to 1, the black box is enabled, and fault records are written into EEPROM when the sequence engine enters a state that has its corresponding BBWRTRGx bit set to 1.

When the black box is enabled, all access to the configuration, user, and black box EEPROM sections is inhibited unless a 1 is written to the halt bit in the BBCTRL register (Register 0x9C, Bit 0) to stop the black box.

When an ADM1260 powers up, the black box automatically searches the black box section of EEPROM to find the first unused location for the next fault record to be written. After this section of EEPROM is erased, the black box may be instructed to perform this search again so that it uses the correct location for the next fault record write. The reset bit in the BBSEARCH register (Register 0xD9, Bit 0) initiates this action.

Table 22. Bit Map for Definition of the Black Box Write Triggers for Each SE State[1]

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0x94	BBWRTRG1	7	STATE7	R/W	State 7 write trigger.
		6	STATE6	R/W	State 6 write trigger.
		5	STATE5	R/W	State 5 write trigger.
		4	STATE4	R/W	State 4 write trigger.
		3	STATE3	R/W	State 3 write trigger.
		2	STATE2	R/W	State 2 write trigger.
		1	STATE1	R/W	State 1 black box trigger; must always be set to 0.
		0	Reserved	R/W	Reserved state black box trigger; must always be set to 0.
0x95	BBWRTRG2	7	STATE15	R/W	State 15 write trigger.
		6	STATE14	R/W	State 14 write trigger.
		5	STATE13	R/W	State 13 write trigger.
		4	STATE12	R/W	State 12 write trigger.
		3	STATE11	R/W	State 11 write trigger.
		2	STATE10	R/W	State 10 write trigger.
		1	STATE9	R/W	State 9 write trigger.
		0	STATE8	R/W	State 8 write trigger.
0x96	BBWRTRG3	7	STATE23	R/W	State 23 write trigger.
		6	STATE22	R/W	State 22 write trigger.
		5	STATE21	R/W	State 21 write trigger.
		4	STATE20	R/W	State 20 write trigger.
		3	STATE19	R/W	State 19 write trigger.
		2	STATE18	R/W	State 18 write trigger.
		1	STATE17	R/W	State 17 write trigger.
		0	STATE16	R/W	State 16 write trigger.
0x97	BBWRTRG4	7	STATE31	R/W	State 31 write trigger.
		6	STATE30	R/W	State 30 write trigger.
		5	STATE29	R/W	State 29 write trigger.
		4	STATE28	R/W	State 28 write trigger.
		3	STATE27	R/W	State 27 write trigger.
		2	STATE26	R/W	State 26 write trigger.
		1	STATE25	R/W	State 25 write trigger.
		0	STATE24	R/W	State 24 write trigger.

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0x98	BBWRTRG5	7	STATE39	R/W	State 39 write trigger.
		6	STATE38	R/W	State 38 write trigger.
		5	STATE37	R/W	State 37 write trigger.
		4	STATE36	R/W	State 36 write trigger.
		3	STATE35	R/W	State 35 write trigger.
		2	STATE34	R/W	State 34 write trigger.
		1	STATE33	R/W	State 33 write trigger.
		0	STATE32	R/W	State 32 write trigger.
0x99	BBWRTRG6	7	STATE47	R/W	State 47 write trigger.
		6	STATE46	R/W	State 46 write trigger.
		5	STATE45	R/W	State 45 write trigger.
		4	STATE44	R/W	State 44 write trigger.
		3	STATE43	R/W	State 43 write trigger.
		2	STATE42	R/W	State 42 write trigger.
		1	STATE41	R/W	State 41 write trigger.
		0	STATE40	R/W	State 40 write trigger.
0x9A	BBWRTRG7	7	STATE55	R/W	State 55 write trigger.
		6	STATE54	R/W	State 54 write trigger.
		5	STATE53	R/W	State 53 write trigger.
		4	STATE52	R/W	State 52 write trigger.
		3	STATE51	R/W	State 51 write trigger.
		2	STATE50	R/W	State 50 write trigger.
		1	STATE49	R/W	State 49 write trigger.
		0	STATE48	R/W	State 48 write trigger.
0x9B	BBWRTRG8	7	STATE63	R/W	State 63 black box trigger; must always be set to 0.
		6	STATE62	R/W	State 62 write trigger.
		5	STATE61	R/W	State 61 write trigger.
		4	STATE60	R/W	State 60 write trigger.
		3	STATE59	R/W	State 59 write trigger.
		2	STATE58	R/W	State 58 write trigger.
		1	STATE57	R/W	State 57 write trigger.
		0	STATE56	R/W	State 56 write trigger.

[1] When the trigger bit for a given state is set to 1, a fault record is written into the next free location in the black box section of EEPROM when the SE enters that state. When the trigger bit is set to 0, no fault record is written.

Table 23. ADM1260 Black Box Control Registers

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0x9C	BBCTRL	[7:1]	Not applicable		These bits cannot be used.
		0	Halt	R/W	The black box function is enabled when one or more of the BBWRTRGx register bits are set to 1. When the black box is enabled, it is no longer possible to read or write to the configuration, user, and black box sections of EEPROM. Writing this bit to 1 disables the black box and enables read and write access to the configuration, user, and black box sections of EEPROM. This bit cannot be set while a fault record is being written into the EEPROM; therefore, this bit must always be read after a write to ensure that the bit is set correctly.
0xD9	BBSEARCH	[7:1]	Not applicable		These bits cannot be used.
		0	Reset	R	When written to 1, the black box searches from Address 0xF980 to find the first unused fault record. After erasing the section of EEPROM holding the black box fault records, and for the black box to start writing records from the first location, write a 1 to this bit.

ADC

The ADM1260 features an on-chip, 12-bit ADC. The ADC has a 12-channel analog mux on the front end. Any or all of these inputs can be selected to be read by the ADC; therefore, the ADC can be set up to continuously read the selected channels. The circuit controlling this operation is called the round robin. The user selects the channels to operate on, and the ADC performs a conversion on each in turn. Averaging can be turned on, setting the round robin to take 16 conversions on each channel; otherwise, a single conversion is made on each channel. At the end of this cycle, the results are written to the output registers and, at the same time, compared with preset thresholds provided on the ADM1260, which can be programmed to a maximum or minimum allowable threshold. Only one register is provided for each input channel; therefore, a UV or OV threshold, but not both, can be set for a given channel. Exceeding the threshold generates a warning that can be read back from the status registers or input into the SE via an OR gate. The round robin can be enabled via an SMBus write or can be programmed to turn on at a particular point in the SE program; for instance, it can be set to start once a power-up sequence is complete and all supplies are known to be within expected fault limits.

Table 24 through Table 28 show the details of the registers required to set up the ADC and its inputs.

ADC Readback Configuration Registers

Table 24. Limit Registers[1]

Input	Reg.	Reg. Name	Bits	Bit Name	R/W	Description
VP1	0x70	ADCVP1LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VP1 input
VP2	0x71	ADCVP2LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VP2 input
VP3	0x72	ADCVP3LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VP3 input
VP4	0x73	ADCVP4LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VP4 input
VH	0x74	ADCVHLIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VH input
VX1	0x75	ADCVX1LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VX1 input
VX2	0x76	ADCVX2LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VX2 input
VX3	0x77	ADCVX3LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VX3 input
VX4	0x78	ADCVX4LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VX4 input
VX5	0x79	ADCVX5LIM	[7:0]	LIM7 to LIM0	R/W	Limit register for ADC conversion on the VX5 input

[1] An ADC reading above or below these limits generates a warning.

Table 25. Sense Registers[1, 2]

Reg.	Reg. Name	Bits	Bit Name	R/W	Description	Input
0x7D	LSENSE1	7	SENS7	R/W	Limit sense for VX3. 0 = ADC > ADCVX3LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX3LIM gives a warning, that is, undervoltage.	VX3
		6	SENS6	R/W	Limit sense for VX2. 0 = ADC > ADCVX2LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX2LIM gives a warning, that is, undervoltage.	VX2
		5	SENS5	R/W	Limit sense for VX1. 0 = ADC > ADCVX1LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX1LIM gives a warning, that is, undervoltage.	VX1
		4	SENS4	R/W	Limit sense for VH. 0 = ADC > ADCVHLIM gives a warning, that is, overvoltage; 1 = ADC < ADCVHLIM gives a warning, that is, undervoltage.	VH
		3	SENS3	R/W	Limit sense for VP4. 0 = ADC > ADCVP4LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVP4LIM gives a warning, that is, undervoltage.	VP4
		2	SENS2	R/W	Limit sense for VP3 0 = ADC > ADCVP3LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVP3LIM gives a warning, that is, undervoltage.	VP3
		1	SENS1	R/W	Limit sense for VP2. 0 = ADC > ADCVP2LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVP2LIM gives a warning, that is, undervoltage.	VP2
		0	SENS0	R/W	Limit sense for VP1. 0 = ADC > ADCVP1LIM gives a warning, that is, overvoltage; 1= ADC < ADCVP1LIM gives a warning, that is, undervoltage.	VP1
0x7E	LSENSE2	7	SENS7		This bit cannot be used.	N/A
		6	SENS6		This bit cannot be used.	N/A
		5	SENS5		This bit cannot be used.	N/A
		4	SENS4		This bit cannot be used.	N/A
		3	SENS3		This bit cannot be used.	N/A
		2	SENS2		This bit cannot be used.	N/A

Reg.	Reg. Name	Bits	Bit Name	R/W	Description	Input
		1	SENS1	R/W	Limit sense for VX5. 0 = ADC > ADCVX5LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX5LIM gives a warning, that is, undervoltage.	VX5
		0	SENS0	R/W	Limit sense for VX4. 0 = ADC > ADCVX4LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX4LIM gives a warning, that is, undervoltage.	VX4

[1] These registers determine when a warning is generated.
[2] N/A means not applicable.

Table 26. Round Robin (RR) Select Registers[1, 2]

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VX3	0x80	RRSEL1	7	VX3CHAN	R/W	0 = VX3 is included in RR. 1 = VX3 is excluded from RR.
VX2			6	VX2CHAN	R/W	0 = VX2 is included in RR. 1 = VX2 is excluded from RR.
VX1			5	VX1CHAN	R/W	0 = VX1 is included in RR. 1 = VX1 is excluded from RR.
VH			4	VHCHAN	R/W	0 = VH is included in RR. 1 = VH is excluded from RR.
VP4			3	VP4CHAN	R/W	0 = VP4 is included in RR. 1 = VP4 is excluded from RR.
VP3			2	VP3CHAN	R/W	0 = VP3 is included in RR. 1 = VP3 is excluded from RR.
VP2			1	VP2CHAN	R/W	0 = VP2 is included in RR. 1 = VP2 is excluded from RR.
VP1			0	VP1CHAN	R/W	0 = VP1 is included in RR. 1 = VP1 is excluded from RR.
N/A	0x81	RRSEL2	7	Not applicable		This bit cannot be used.
N/A			6	Not applicable		This bit cannot be used.
N/A			5	Not applicable		This bit cannot be used.
N/A			4	Not applicable		This bit cannot be used.
N/A			3	Not applicable		This bit cannot be used.
N/A			2	Not applicable		This bit cannot be used.
VX5			1	VX5CHAN	R/W	0 = VX5 is included in RR. 1= VX5 is excluded from RR.
VX4			0	VX4CHAN	R/W	0 = VX4 is included in RR. 1= VX4 is excluded from RR.

[1] These registers determine which inputs are actually read by the ADC as it cycles.
[2] N/A means not applicable.

Table 27. Round Robin Control Register[1]

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0x82	RRCTRL	[7:5]			These bits cannot be used.
		4	CLEARLIM	R/W	Write this bit high to clear limit warnings. Then, this bit self clears.
		3	STOPWRITE	R/W	This bit inhibits the RR from writing the results to the output registers.
		2	AVERAGE	R/W	This bit turns on 16× averaging.
		1	ENABLE	R/W	This bit turns on the RR for continuous operation.
		0	GO	R/W	This bit starts the RR.

[1] This register activates an ADC read and determines whether averaging is used and whether there is a continuous read present.

Table 28. ADC Value Registers

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VP1	0xA0	ADCHVP1	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VP1 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VP1 when Register 0x82, Bit 2 (average) = 1.
	0xA1	ADCLVP1	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VP1 input.

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VP2	0xA2	ADCHVP2	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VP2 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VP2 when Register 0x82, Bit 2 (average) = 1.
	0xA3	ADCLVP2	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VP2 input.
VP3	0xA4	ADCHVP3	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VP3 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VP3 when Register 0x82, Bit 2 (average) = 1.
	0xA5	ADCLVP3	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VP3 input.
VP4	0xA6	ADCHVP4	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VP4 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VP4 when Register 0x82, Bit 2 (average) = 1.
	0xA7	ADCLVP4	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VP4 input.
VH	0xA8	ADCHVH	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VH when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VH when Register 0x82, Bit 2 (average) = 1.
	0xA9	ADCLVH	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VH input.
VX1	0xAA	ADCHVX1	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VX1 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VX1 when Register 0x82, Bit 2 (average) = 1.
	0xAB	ADCLVX1	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VX1 input.
VX2	0xAC	ADCHVX2	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VX2 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VX2 when Register 0x82, Bit 2 (average) = 1.
	0xAD	ADCLVX2	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VX2 input.
VX3	0xAE	ADCHVX3	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VX3 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VX3 when Register 0x82, Bit 2 (average) = 1.
	0xAF	ADCLVX3	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VX3 input.

Input	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
VX4	0xB0	ADCHVX4	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VX4 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VX4 when Register 0x82, Bit 2 (average) = 1.
	0xB1	ADCLVX4	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VX4 input.
VX5	0xB2	ADCHVX5	[7:4]	Not applicable		These bits are not used if Register 0x82, Bit 2 (average) = 0.
			[3:0]	OUT3 to OUT0	R/W	These bits are the 4 MSBs of the 12-bit result of the ADC conversions on VX5 when Register 0x82, Bit 2 (average) = 0.
			[7:0]	OUT7 to OUT0	R/W	These bits are the 8 MSBs of the 16-bit result of the ADC conversions on VX5 when Register 0x82, Bit 2 (average) = 1.
	0xB3	ADCLVX5	[7:0]	OUT7 to OUT0	R/W	These bits are the 8 LSBs of 12-bit or 16-bit result of the ADC conversions on the VX5 input.

DACS

The ADM1260 features six voltage output DACs. These DACs are primarily used to adjust the output voltage of a dc-to-dc converter by altering the current at its feedback node. These DACs, therefore, provide an open-loop margining system. The ADC on the ADM1260, along with an external microcontroller, can be used to close this loop.

When the DACx output buffer is turned on, it has very little effect on the dc-to-dc output. The DAC output buffer is designed to power up without glitching. The output buffer accomplishes this by first powering up the buffer to follow the pin voltage; the voltage on the feedback pin of the LDO does not drive out onto the pin at this time. After the output buffer is properly enabled, the buffer input is switched over to the DAC, and the output stage of the buffer is turned on. Output glitching is negligible.

Four DAC ranges are available and placed with midcode (Code 0x7F) at 0.6 V, 0.8 V, 1.0 V, and 1.25 V to correspond to the most common feedback voltages. Centering the DAC outputs in this way provides the best use of the DAC resolution; that is, for most supplies it is possible to place the DAC midcode at the point where the dc-to-dc output is not modified, thus giving each of the DACs one half of the full range to margin up and down. The DAC output voltage is set by the code written to the DACx register. The voltage is linear with the unsigned binary number in this register. Code 0x7F is placed at the midcode voltage.

The output voltage is given by the following equation:

$$DAC\ Output = (DACx - 0x7F)/255 \times 0.6015 + V_{OFF}$$

where V_{OFF} is one of the four offset voltages described earlier in this section.

Limit registers on the device (DPLIMx and DNLIMx) offer the user some protection from firmware bugs that can cause catastrophic board problems by forcing supplies beyond their allowable output ranges. The DAC code written into the DACx register is clipped so that the code used to set the DAC voltage is actually given by

$$DACCode$$
$$= DACx,\ DNLIMx \le DACx \le DPLIMx$$
$$= DNLIMx,\ DACx < DPLIMx$$
$$= DPLIMx,\ DACx > DPLIMx$$

The DAC output buffer is three-stated if DNLIMx > DPLIMx. The user can make it difficult for the DAC output buffers to be turned on at all in normal system operation by programming the limit registers in this way (these are among the registers downloaded from EEPROM at startup).

Table 29 shows the detail of the registers required to set up the DACs.

Table 29. DAC Configuration Registers

Output	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description		
DAC1	0x50	DACCTRL1	[7:3]	Not applicable		These bits cannot be used.		
			2	ENDAC	R/W	This bit enables DAC1.		
			[1:0]	OFFSEL1 to OFFSEL0	R/W	These bits select the center voltage (midcode) output of DAC1.		
						OFFSEL1	**OFFSEL0**	**(Midcode) Output Voltage (V)**
						0	0	1.25
						0	1	1.0
						1	0	0.8
						1	1	0.6
	0x58	DAC1	[7:0]	DAC7 to DAC0	R/W	These bits are the 8-bit DAC code (0x7F is midcode).		
	0x60	DPLIM1	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC positive limit code. If DAC1 is set to a higher code, the DAC code limits to the contents of this register.		
	0x68	DNLIM1	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC negative limit code. If DAC1 is set to a lower code, the DAC code limits to the contents of this register. Note that if DNLIM1 is set to be greater than DPLIM1, the DAC output is always disabled (this is a safety feature).		
DAC2	0x51	DACCTRL2	[7:3]	Not applicable		These bits cannot be used.		
			2	ENDAC	R/W	This bit enables DAC2.		
			[1:0]	OFFSEL1 to OFFSEL0	R/W	These bits select the center voltage (midcode) output of DAC2.		
						OFFSEL1	**OFFSEL0**	**(Midcode) Output Voltage (V)**
						0	0	1.25
						0	1	1.0
						1	0	0.8
						1	1	0.6
	0x59	DAC2	[7:0]	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).		
	0x61	DPLIM2	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC positive limit code. If DAC2 is set to a higher code, the DAC code limits to the contents of this register.		
	0x69	DNLIM2	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC negative limit code. If DAC2 is set to a lower code, the DAC code limits to the contents of this register. Note that if DNLIM2 is set to be greater than DPLIM2, the DAC output is always disabled (this is a safety feature).		
DAC3	0x52	DACCTRL3	[7:3]	Not applicable		These bits cannot be used.		
			2	ENDAC	R/W	This bit enables DAC3.		
			[1:0]	OFFSEL1 to OFFSEL0	R/W	These bits select the center voltage (midcode) output of DAC3.		
						OFFSEL1	**OFFSEL0**	**(Midcode) Output Voltage (V)**
						0	0	1.25
						0	1	1.0
						1	0	0.8
						1	1	0.6
	0x5A	DAC3	[7:0]	DAC7 to DAC0	R/W	These bits are the 8-bit DAC code (0x7F is midcode).		
	0x62	DPLIM3	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC positive limit code. If DAC3 is set to a code higher than this, the DAC code limits to the contents of this register.		
	0x6A	DNLIM3	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC negative limit code. If DAC3 is set to a code lower than this, the DAC code limits to the contents of this register. Note that if DNLIM3 is set to be greater than DPLIM3, the DAC output is always disabled (this is a safety feature).		

Output	Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description		
DAC4	0x53	DACCTRL4	[7:3]	Not applicable		These bits cannot be used.		
			2	ENDAC	R/W	This bit enables DAC4.		
			[1:0]	OFFSEL1 to OFFSEL0	R/W	These bits select the center voltage (midcode) output of DAC4.		
						OFFSEL1	**OFFSEL0**	**(Midcode) Output Voltage (V)**
						0	0	1.25
						0	1	1.0
						1	0	0.8
						1	1	0.6
	0x5B	DAC4	[7:0]	DAC7 to DAC0	R/W	These bits are the 8-bit DAC code (0x7F is midcode).		
	0x63	DPLIM4	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC positive limit code. If DAC4 is set to a higher code, the DAC code limits to the contents of this register.		
	0x6B	DNLIM4	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC negative limit code. If DAC4 is set to a lower code, the DAC code limits to the contents of this register. Note that if DNLIM4 is set to be greater than DPLIM4, the DAC output is always disabled (this is a safety feature).		
DAC5	0x54	DACCTRL5	[7:3]	Not applicable		These bits cannot be used.		
			2	ENDAC	R/W	This bit enables DAC5.		
			[1:0]	OFFSEL1 to OFFSEL0	R/W	These bits select the center voltage (midcode) output of DAC5.		
						OFFSEL1	**OFFSEL0**	**(Midcode) Output Voltage (V)**
						0	0	1.25
						0	1	1.0
						1	0	0.8
						1	1	0.6
	0x5C	DAC5	[7:0]	DAC7 to DAC0	R/W	These bits are the 8-bit DAC code (0x7F Is midcode).		
	0x64	DPLIM5	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC positive limit code. If DAC5 is set to a higher code, the DAC code limits to the contents of this register.		
	0x6C	DNLIM5	[7:0]	LIM7 to LIM0	R/W	These bits are the 8-bit DAC negative limit code. If DAC5 is set to a lower code, the DAC code limits to the contents of this register. Note that if DNLIM5 is set to be greater than DPLIM5, the DAC output is always disabled (this is a safety feature).		
DAC6	0x55	DACCTRL6	[7:3]	Not applicable		These bits cannot be used.		
			2	ENDAC	R/W	This bit enables DAC6.		
			[1:0]	OFFSEL1 to OFFSEL0	R/W	These bits select the center voltage (midcode) output of DAC6.		
						OFFSEL1	**OFFSEL0**	**(Midcode) Output Voltage (V)**
						0	0	1.25
						0	1	1.0
						1	0	0.8
						1	1	0.6
	0x5D	DAC6	7:0	DAC7 to DAC0	R/W	These bits are the 8-bit DAC code (0x7F is midcode).		
	0x65	DPLIM6	7:0	LIM7 to LIM0	R/W	These bits are the 8-bit DAC positive limit code. If DAC6 is set to a higher code, the DAC code limits to the contents of this register.		
	0x6D	DNLIM6	7:0	LIM7 to LIM0	R/W	These bits are the 8-bit DAC negative limit code. If DAC6 is set to a lower code, the DAC code limits to the contents of this register. Note that if DNLIM6 is set to be greater than DPLIM6, the DAC output is always disabled (this is a safety feature).		

WARNINGS, FAULTS, AND STATUS

Warnings

The ADM1260 features a low level of fault detection that can be used in conjunction with the fault detection provided on the inputs. These low level fault reports are provided by the ADC limit registers and by the secondary SFDs on the VP1 to VP4 and VH inputs. The secondary SFDs are available on these pins when VX1 to VX5 are used as digital inputs.

Warning is provided as a single input to the SE. It consists of a wide OR of the ADC limit registers and the secondary SFD outputs. Selecting warning as an input to the SE is shown in the Sequencing Engine section.

Status Reporting

The ADM1260 features a number of status registers that can be read at any time to determine the status of the inputs. The contents of these registers can change at any time; that is, the data is not latched in these registers. Table 30 shows the details of status registers.

Table 30. Status Registers

Register Address	Register Name	Bits	Bit Name	R/W	Description
0xE2	OVSTAT1	7	OV_VX3	R	Overvoltage threshold exceeded on VX3 (SFD) or VP3 (warning).
		6	OV_VX2	R	Overvoltage threshold exceeded on VX2 (SFD) or VP2 (warning).
		5	OV_VX1	R	Overvoltage threshold exceeded on VX1 (SFD) or VP1 (warning).
		4	OV_VH	R	Overvoltage threshold exceeded on the VH SFD.
		3	OV_VP4	R	Overvoltage threshold exceeded on the VP4 SFD.
		2	OV_VP3	R	Overvoltage threshold exceeded on the VP3 SFD.
		1	OV_VP2	R	Overvoltage threshold exceeded on the VP2 SFD.
		0	OV_VP1	R	Overvoltage threshold exceeded on the VP1 SFD.
0xE3	OVSTAT2	[7:2]	Not applicable		These bits cannot be used.
		1	OV_VX5	R	Overvoltage threshold exceeded on VX5 (SFD) or VH (warning).
		0	OV_VX4	R	Overvoltage threshold exceeded on VX4 (SFD) or VP4 (warning).
0xE4	UVSTAT1	7	UV_VX3	R	Undervoltage threshold exceeded on VX3 (SFD) or VP3 (warning).
		6	UV_VX2	R	Undervoltage threshold exceeded on VX2 (SFD) or VP2 (warning).
		5	UV_VX1	R	Undervoltage threshold exceeded on VX1 (SFD) or VP1 (warning).
		4	UV_VH	R	Undervoltage threshold exceeded on the VH SFD.
		3	UV_VP4	R	Undervoltage threshold exceeded on the VP4 SFD.
		2	UV_VP3	R	Undervoltage threshold exceeded on the VP3 SFD.
		1	UV_VP2	R	Undervoltage threshold exceeded on the VP2 SFD.
		0	UV_VP1	R	Undervoltage threshold exceeded on the VP1 SFD.
0xE5	UVSTAT2	[7:2]	Not applicable		These bits cannot be used.
		1	UV_VX5	R	Undervoltage threshold exceeded on VX5 (SFD) or VH (warning).
		0	UV_VX4	R	Undervoltage threshold exceeded on VX4 (SFD) or VP4 (warning).
0xE6	LIMSTAT1	7	VX3 CH	R	VX3 limit status; used with LSENSE 1.
		6	VX2 CH	R	VX2 limit status; used with LSENSE 1.
		5	VX1 CH	R	VX1 limit status; used with LSENSE 1.
		4	VH CH	R	VH limit status; used with LSENSE 1.
		3	VP4 CH	R	VP4 limit status; used with LSENSE 1.
		2	VP3 CH	R	VP3 limit status; used with LSENSE 1.
		1	VP2 CH	R	VP2 limit status; used with LSENSE 1.
		0	VP1 CH	R	VP1 limit status; used with LSENSE 1.
0xE7	LIMSTAT2	[7:2]	Not applicable	R	These bits cannot be used.
		1	VX5 CH	R	VX5 CH limit status; used with LSENSE 2.
		0	VX4 CH	R	VX4 CH limit status; used with LSENSE 2.
0xE8	GPISTAT	[7:5]	Not applicable		These bits cannot be used.
		4	VX5_STAT	R	VX5 GPI input status (after signal conditioning).
		3	VX4_STAT	R	VX4 GPI input status (after signal conditioning).
		2	VX3_STAT	R	VX3 GPI input status (after signal conditioning).
		1	VX2_STAT	R	VX2 GPI input status (after signal conditioning).
		0	VX1_STAT	R	VX1 GPI input status (after signal conditioning).

BLACK BOX STATUS REGISTERS AND FAULT RECORDS

Each time the ADM1260 SE changes state, the contents of the UVSTATx, OVSTATx, LIMSTATx, and GPISTATx registers, along with some other pieces of information relating to the SE state and the cause of the last state transition, are latched into seven black box status registers.

These registers provide a snapshot of the state of the inputs being monitored by the ADM1260, what the last state was, and what caused the last state change.

After the SE changes state, if the new state it enters has its corresponding STATEx bit set (see the BBWRTRGx registers), the seven black box status registers are written sequentially into the next available location in the black box EEPROM section.

After the seven bytes are written, an eighth checksum byte is written to provide a method to check data integrity. This check is important if only a partial record is written because all the supplies powering the device failed.

The checksum byte is a simple addition of the values written into the seven other EEPROM location for a given fault record.

The order of the bytes in a fault record stored in EEPROM is as follows:

1. PREVSTEXT
2. PREVSEQST
3. BBSTAT1
4. BBSTAT2
5. BBSTAT3
6. BBSTAT4
7. BBSTAT5
8. CHECKSUM

The bytes are stored from lowest to the highest EEPROM address; therefore, for the first fault record location in the black box EEPROM, PREVSTEXT is stored at 0xF980 and CHECKSUM at 0xF987.

Table 31. Black Box Fault and Status Registers[1]

Register Address	Register Name	Bits	Bit Name	R/W	Description
0xEA	PREVSTEXT	7	BBUSED	N/A	This bit always reads as 0. When this bit is written to the first byte of a fault record in EEPROM, it marks all eight bytes in use. When the black box is searching for the next free location to use, this bit is examined. If this bit is 0, then even if the previous fault record is only partially written to EEPROM, the eight bytes of the fault record are ignored.
		6	ICBMSG	R	This bit indicates that the previous state transition was triggered by a message received on the ICB.
		5	SMBJUMP	R	This bit indicates that the previous state transition was due to an SMB jump being received.
		4	LIMWARN	R	This bit indicates that the previous state transition was due to one or more ADC warning limits being exceeded.
		3	SFDCMP	R	This bit indicates that the previous state transition was due to one or more supply fault detector limits being exceeded.
		2	Timeout	R	This bit indicates that the previous state transition was due to the timeout condition becoming true.
		1	Monitor	R	This bit indicates that the previous state transition was due to the monitor condition becoming true.
		0	Sequence	R	This bit indicates that the previous state transition was due to the sequence condition becoming true.
0xEB	PREVSEQST	[5:0]	PREVADDR	R	State number of the state that was active immediately prior to the current state.
0xEC	BBSTAT1	7	UV_VX3	R	Undervoltage threshold exceeded on VX3 (SFD) or VP3 (warning).
		6	UV_VX2	R	Undervoltage threshold exceeded on VX2 (SFD) or VP2 (warning).
		5	UV_VX1	R	Undervoltage threshold exceeded on VX1 (SFD) or VP1 (warning).
		4	UV_VH	R	Undervoltage threshold exceeded on the VH SFD.
		3	UV_VP4	R	Undervoltage threshold exceeded on the VP4 SFD.
		2	UV_VP3	R	Undervoltage threshold exceeded on the VP3 SFD.
		1	UV_VP2	R	Undervoltage threshold exceeded on the VP2 SFD.
		0	UV_VP1	R	Undervoltage threshold exceeded on the VP1 SFD.

Register Address	Register Name	Bits	Bit Name	R/W	Description
0xED	BBSTAT2	7	OV_VX1	R	Overvoltage threshold exceeded on VX1 (SFD) or VP1 (warning).
		6	OV_VH	R	Overvoltage threshold exceeded on the VH SFD.
		5	OV_VP4	R	Overvoltage threshold exceeded on the VP4 SFD.
		4	OV_VP3	R	Overvoltage threshold exceeded on the VP3 SFD.
		3	OV_VP2	R	Overvoltage threshold exceeded on the VP2 SFD.
		2	OV_VP1	R	Overvoltage threshold exceeded on the VP1 SFD.
		1	UV_VX5	R	Undervoltage threshold exceeded on VX5 (SFD) or VH (warning).
		0	UV_VX4	R	Undervoltage threshold exceeded on VX4 (SFD) or VP4 (warning).
0xEE	BBSTAT3	7	VX4_STAT	R	VX4 GPI input status (after signal conditioning).
		6	VX3_STAT	R	VX3 GPI input status (after signal conditioning).
		5	VX2_STAT	R	VX2 GPI input status (after signal conditioning).
		4	VX1_STAT	R	VX1 GPI input status (after signal conditioning).
		3	OV_VX5	R	Overvoltage threshold exceeded on VX5 (SFD) or VH (warning).
		2	OV_VX4	R	Overvoltage threshold exceeded on VX4 (SFD) or VP4 (warning).
		1	OV_VX3	R	Overvoltage threshold exceeded on VX3 (SFD) or VP3 (warning).
		0	OV_VX2	R	Overvoltage threshold exceeded on VX2 (SFD) or VP2 (warning).
0xEF	BBSTAT4	7	VX2 CH	R	VX2 limit status; used with LSENSE 1.
		6	VX1 CH	R	VX1 limit status; used with LSENSE 1.
		5	VH CH	R	VH limit status; used with LSENSE 1.
		4	VP4 CH	R	VP4 limit status; used with LSENSE 1.
		3	VP3 CH	R	VP3 limit status; used with LSENSE 1.
		2	VP2 CH	R	VP2 limit status; used with LSENSE 1.
		1	VP1 CH	R	VP1 limit status; used with LSENSE 1.
		0	VX5_STAT	R	VX5 GPI input status (after signal conditioning).
0xF0	BBSTAT5	[7:3]	Reserved		These bits cannot be used.
		2	VX5 CH	R	VX5 CH limit status; used with LSENSE 2.
		1	VX4 CH	R	VX4 CH limit status; used with LSENSE 2.
		0	VX3 CH	R	VX3 limit status; used with LSENSE 1.
0xF1	BBADDR	[7:0]	ADDR	R	These bits are the low byte of the address location in the 0xF980 to 0xF9FF range that the next fault record is written to. When no fault records are written, the value is 0x80, and increments by 8 each time a fault record is written. The value is 0x F8 when there is only one fault record not written. When all locations are written to and the black box EEPROM is full, the value is 0x00.

[1] N/A means not applicable.

USE OF THE REVID REGISTER

The ADM1066, ADM1166, and ADM1260 have the same I²C addresses range, and both return the value of 0x41 when the MANID register is read. REVID is a read only register that determines whether a device at a given address is an ADM1066, an ADM1166, or an ADM1260 (see Table 32).

INTERCHIP BUS CONFIGURATION

The ADM1260 uses a dedicated interchip bus (ICB) to coordinate sequencing activities between multiple devices.

Each device on the ICB is assigned a unique address to identify it to other devices.

The ICBADDR bits are independent of the I²C address assigned by the A0 and A1 address pins.

Table 32. Decoding the REVID Register

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0xF5	REVID	[7:4]	Family	R	When the value of these bits is 0x2, the device is an ADM1260.
		[3:0]	HWVER	R	The value on these bits is the hardware revision number.

Table 33. Fault and Status Registers

Reg. Addr.	Register Name	Bits	Bit Name	R/W	Description
0x56	ICBCFG1	[7:4]	Reserved		These bits cannot be used.
		[3:0]	ICBADDR	R/W	These bits are the address used to identify the device on the ICB and is different from the SMBus address. The ADM1260 has an address range of 1 to 4. A value of 0 is not a valid device address because that is used by broadcast messages.
0x57	ICBCFG2	[7:6]	Reserved		These bits cannot be used.
		[5:0]	BUSFAULT	R/W	These bits set the state to jump in case of a bus fault on the ICB. These bits are set by the GUI.
0x5E	ICBCFG3	[7:6]	Reserved		These bits cannot be used.
		[5:0]	SEQFAULT	R/W	These bits set the state to jump in case of a sequence fault. These bits are set by the GUI.

REGISTER MAP QUICK REFERENCE

Table 34 provides a quick reference for the registers described in this data sheet.

Table 34. Register Map Quick Reference[1]

Base (Hex)	Function	0	1	2	3	4	5	6	7
00	VP1	PS1OVTH	PS1OVHYST	PS1UVTH	PS1UVHYST	SFDV1CFG	SFDV1SEL	N/A	PDO1CFG
08	VP2	PS2OVTH	PS2OVHYST	PS2UVTH	PS2UVHYST	SFDV2CFG	SFDV2SEL	N/A	PDO2CFG
10	VP3	PS3OVTH	PS3OVHYST	PS3UVTH	PS3UVHYST	SFDV3CFG	SFDV3SEL	N/A	PDO3CFG
18	VP4	PS4OVTH	PS4OVHYST	PS4UVTH	PS4UVHYST	SFDV4CFG	SFDV4SEL	N/A	PDO4CFG
20	VH	PSVHOVTH	PSVHOVHYST	PSVHUVTH	PSVHUVHYST	PSVHDVHCFG	SFDVHSEL	N/A	PDO5CFG
28	VX1	X1OVTH	X1OVHYST	X1UVTH	X1UVHYST	SFDX1CFG	SFDVX1SEL	XGPI1CFG	PDO6CFG
30	VX2	X2OVTH	X2OVHYST	X2UVTH	X2UVHYST	SFDX2CFG	SFDVX2SEL	XGPI2CFG	PDO7CFG
38	VX3	X3OVTH	X3OVHYST	X3UVTH	X3UVHYST	SFDX3CFG	SFDVX3SEL	XGPI3CFG	PDO8CFG
40	VX4	X4OVTH	X4OVHYST	X4UVTH	X4UVHYST	SFDX4CFG	SFDVX4SEL	XGPI4CFG	PDO9CFG
48	VX5	X5OVTH	X5OVHYST	X5UVTH	X5UVHYST	SFDX5CFG	SFDVX5SEL	XGPI5CFG	PDO10CFG
50	DAC control	DACCTRL1	DACCTRL2	DACCTRL3	DACCTRL4	DACCTRL5	DACCTRL6	ICBCFG1	ICBCFG2
58	DAC code	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6	ICBCFG3	N/A
60	DAC upper limit	DPLIM1	DPLIM2	DPLIM3	DPLIM4	DPLIM5	DPLIM6	N/A	N/A
68	DAC lower limit	DNLIM1	DNLIM2	DNLIM3	DNLIM4	DNLIM5	DNLIM6	N/A	N/A
70	ADCLIM	ADCVP1LIM	ADCVP2LIM	ADCVP3LIM	ADCVP4LIM	ADCVHLIM	ADCVX1LIM	ADCVX2LIM	ADCVX3LIM
78	ADCLIM	ADCVX4LIM	ADCVX5LIM	N/A	N/A	N/A	LSENSE1	LSENSE2	N/A
80	ADC setup	RRSEL1	RRSEL2	RRCTRL	N/A	N/A	N/A	N/A	N/A
88	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
90	Miscellaneous	UPDCFG	PDEN1	PDEN2	SECTRL	BBWRTRG1	BBWRTRG2	BBWRTRG3	BBWRTRG4
98	Miscellaneous	BBWRTRG5	BBWRTRG6	BBWRTRG7	BBWRTRG8	BBCTRL	N/A	N/A	N/A
A0	ADC readback	ADCHVP1	ADCLVP1	ADCHVP2	ADCLVP2	ADCHVP3	ADCLVP3	ADCHVP4	ADCLVP4
A8	ADC readback	ADCHVH	ADCLVH	ADCHVX1	ADCLVX1	ADCHVX2	ADCLVX2	ADCHVX3	ADCLVX3
B0	ADC readback	ADCHVX4	ADCLVX4	ADCHVX5	ADCLVX5	N/A	N/A	N/A	N/A
B8	ADC readback	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
C0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
C8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
D0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
D8	Miscellaneous	UDOWNLD	BBSEARCH	UNLOCKSE	SEDOWNLD	N/A	N/A	N/A	N/A
E0	Fault (read only)	N/A	N/A	OVSTAT1	OVSTAT2	UVSTAT1	UVSTAT2	LIMSTAT1	LIMSTAT2
E8	Fault (read only)	GPISTAT	SEADDR	PREVSTEXT	PREVSEQST	BBSTAT1	BBSTAT2	BBSTAT4	BBSTAT4
F0	Miscellaneous	BBSTAT5	BBADDR	N/A	N/A	MANID	REVID	N/A	N/A
F8	Commands	EEALOW	EEAHIGH	EEBLOW	EEBHIGH	BLKWR	BLKRD	BLKER	N/A

[1] N/A means not applicable and indicates that a register location does not exist.

OUTLINE DIMENSIONS

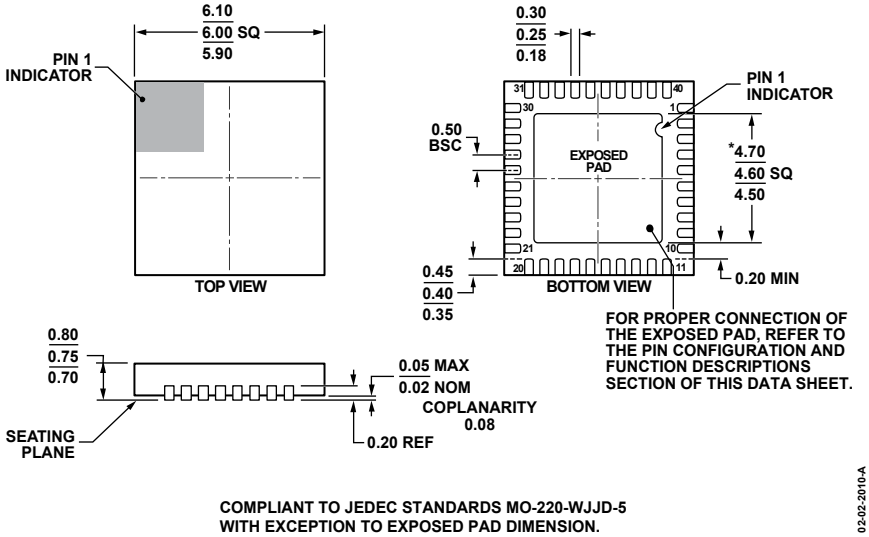


Figure 52. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM1260ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
ADM1260ACPZ-RL7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
EVAL-ADM1260EBZ		Evaluation Kit	

[1] Z = RoHS Compliant Part.

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