# Ultralow Power, Adaptive Linear Power, Dual-Port ADSL/ADSL2+ Line Driver

Data Sheet **ADLD8403**

## FEATURES

- 2 differential DSL channels comprising current feedback, high output current amplifiers with integrated feedback resistors plus biasing network
- Ideal for use as ADSL/ADSL2+ dual-channel central office (CO) line drivers
- Low power consumption using Class H technology
  - Single 12.5 V supply operation
    - 20.4 dBm line power, 1:1 transformer
  - Less than 600 mW per channel total power dissipation while driving 20.4 dBm (includes 110 mW line power)
  - Less than 275 mW per channel total power dissipation while driving 14.5 dBm (including line power)
- High output voltage and current drive
  - 43.4 V differential output voltage swing
- Low distortion
  - −65 dBc typical multitone power ratio (MTPR) at 20.4 dBm, 26 kHz to 2.2 MHz
- Low cost protection components enable ITU-T-K20 and GR-1089 compliance

## APPLICATIONS

- ADSL/ADSL2+ CO line drivers

## INTERNAL SCHEMATIC

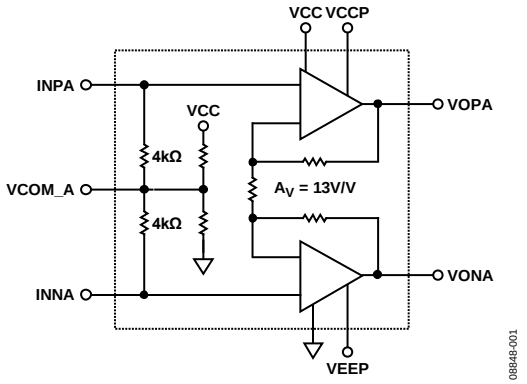



*Figure 1. Channel A Internal Schematic*

## GENERAL DESCRIPTION

The ADLD8403 comprises two differential, high output current, low power consumption operational amplifiers. It is particularly well suited for the CO driver interface in digital subscriber line systems, such as ADSL and ADSL2+. The driver can deliver 20.4 dBm to a line while compensating for losses due to hybrid insertion and back termination resistors. The ADLD8403 uses the Analog Devices, Inc., second generation Adaptive Linear Power™ (Class H) architecture to achieve unprecedented power efficiency using a single power supply. Additional functionality allows the shutdown of pumps for enhanced power savings for line powers of less than 14.5 dBm. This functionality yields the smallest printed circuit board (PCB) footprint and lowest total cost of ownership.

The low power consumption, high output current, high output voltage swing, and robust thermal packaging enable the ADLD8403 to be the CO line driver in ADSL and other xDSL systems.

The ADLD8403 is available in a 4 mm × 4 mm, 20-lead LFCSP.

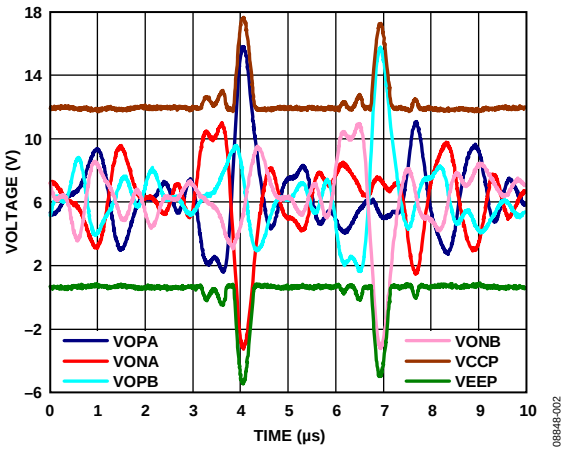



*Figure 2. Outputs and Pumps Time Domain Response, Typical ADSL/ADSL2+ Application Circuit, $V_{CC}$ = 12.5 V, $P_{OUT}$ = 20.4 dBm, Crest Factor = 5.45*


**Rev. D** Document Feedback


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## REVISION HISTORY

**3/2017—Rev. C to Rev. D**

Changed LFCSP_WQ to LFCSP ..... Throughout
Change to Table 3 ..... 4
Updated Outline Dimensions ..... 10
Changes to Ordering Guide ..... 10

**9/2014—Revision C: Initial Version**

# SPECIFICATIONS

$V_{CC}$ = 12.5 V, $R_L$ = 100 Ω, $G_{DIFF}$ = 13 (fixed), PD_A = 0, PD_B = 0, T = 25°C, typical DSL application circuit, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | | 8 | | MHz | $V_{OUT}$ = 0.1 V p-p, differential |
| −3 dB Large Signal Bandwidth | | 8 | | MHz | $V_{OUT}$ = 2 V p-p, differential |
| Differential Gain | 12.8 | 13 | 13.2 | V/V | |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Multitone Power Ratio (MTPR) | | −65 | | dBc | 26 kHz to 2.2 MHz, $Z_{LINE}$ = 100 Ω, differential load |
| Differential Output Noise | | 120 | | nV/√Hz | f = 10 kHz |
| INPUT CHARACTERISTICS | | | | | |
| Referred to Output (RTO) Offset Voltage | | <100 | | mV | Single-ended |
| | | 15 | 200 | mV | Differential |
| Input Resistance | | 8 | | kΩ | Differential |
| Input Capacitance | | 1 | | pF | Differential |
| OUTPUT CHARACTERISTICS | | | | | |
| Differential Output Voltage Swing | | 43.4 | | V | $\Delta V_{OUT}$, $R_L$ = 100 Ω |
| POWER SUPPLY | | | | | |
| Operating Range, Single Supply | 11.75 | 12.5 | | V | |
| Total Quiescent Current | | | | | Full chip |
| PD_A = 0, PD_B = 0, PD_PMP = 0 | | 35.6 | 38 | mA | Pumps are on, both channels active |
| PD_A = 0, PD_B = 0, PD_PMP = 1 | | 22.0 | 25 | mA | Pumps are off, both channels active |
| PD_A = 0, PD_B = 1, PD_PMP = 0 | | 21.0 | 23.5 | mA | Pumps are on, one channel active |
| PD_A = 0, PD_B = 1, PD_PMP = 1 | | 10.6 | 13 | mA | Pumps are off, one channel active |
| PD_A = 1, PD_B = 1 | | 2.5 | 3.5 | mA | Pumps are off, both channels inactive |
| Common-Mode Voltage | | 20 | | mV | With respect to midsupply |
| Threshold | | | | | |
| PD_A = 0, PD_B = 0 | | | 0.8 | V | |
| PD_A = 1, PD_B = 1 | 2.4 | | | V | |
| Input Current | | | | | |
| PD_A = 0, PD_B = 0 | | 35 | 60 | µA | 0 ≡ 0.8 V |
| PD_A = 1, PD_B = 1 | | 5 | 10 | µA | 1 ≡ 2.4 V |

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 13.2 V |
| Power Dissipation | See Figure 3 |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified in still air with the exposed pad soldered to a 4-layer JEDEC test board. $\theta_{JC}$ is specified at the exposed pad.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 20-Lead LFCSP (CP-20-8) | 36.1 | 5.7 | °C/W |

## MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADLD8403 is limited by its junction temperature on the die.

The maximum safe junction temperature of plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is 150°C. Exceeding this limit may temporarily cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding this limit for an extended period can result in device failure.

Figure 3 shows the maximum power dissipation in the package vs. the ambient temperature for the 20-lead LFCSP on a JEDEC standard 4-layer board. $\theta_{JA}$ values are approximations.

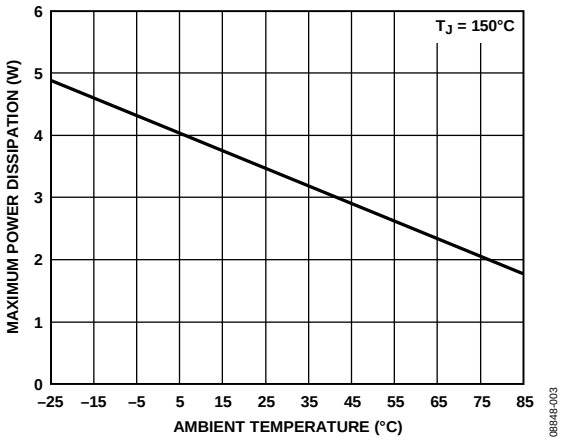



*Figure 3. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board*

The power dissipated in the package ($P_D$) is easily computed by taking the total power consumed while driving a signal and subtracting the power dissipated in the load. The total power consumed is simply the product of the voltage between the supply pins (VCC, VEEP, and VCCP) times the supply current ($I_S$). Use rms voltages and currents.

Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, more copper in direct contact with the package leads from PCB traces, through holes, ground, and power planes reduces $\theta_{JA}$.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

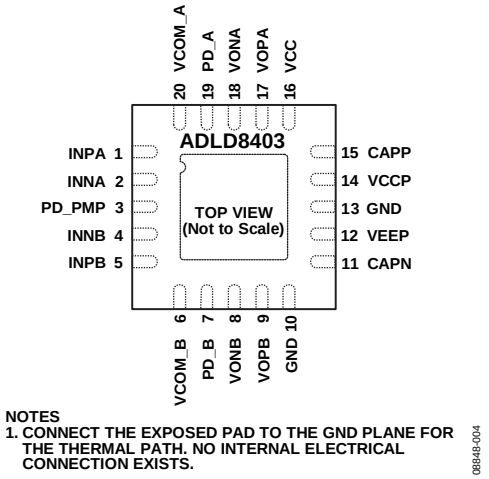



*Figure 4. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | INPA | Port A Input P |
| 2 | INNA | Port A Input N |
| 3 | PD_PMP | Control for Port A and Port B Pumps |
| 4 | INNB | Port B Input N |
| 5 | INPB | Port B Input P |
| 6 | VCOM_B | Port B $V_{COM}$ |
| 7 | PD_B | Port B Shutdown |
| 8 | VONB | Port B Output N |
| 9 | VOPB | Port B Output P |
| 10 | GND | Ground |
| 11 | CAPN | Pump Capacitor Negative |
| 12 | VEEP | Dynamic Negative Supply |
| 13 | GND | Ground |
| 14 | VCCP | Dynamic Positive Supply |
| 15 | CAPP | Pump Capacitor Positive |
| 16 | VCC | Positive Power Supply |
| 17 | VOPA | Port A Output P |
| 18 | VONA | Port A Output N |
| 19 | PD_A | Port A Shutdown |
| 20 | VCOM_A | Port A $V_{COM}$ |
| | EPAD | Exposed Pad. Connect the exposed pad to the GND plane for the thermal path. No internal electrical connection exists. |

# TYPICAL PERFORMANCE CHARACTERISTICS

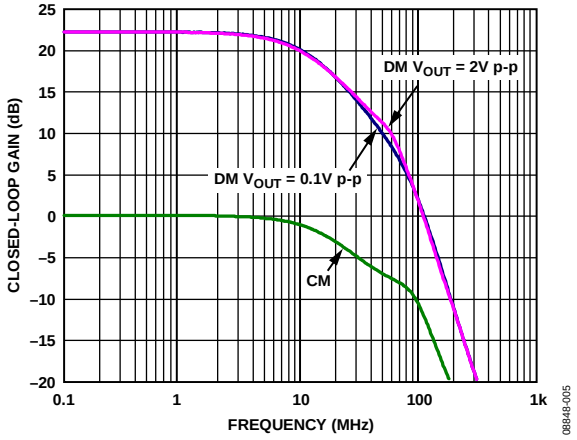



Figure 5. Closed-Loop Gain vs. Frequency, $R_L$ = 100 Ω

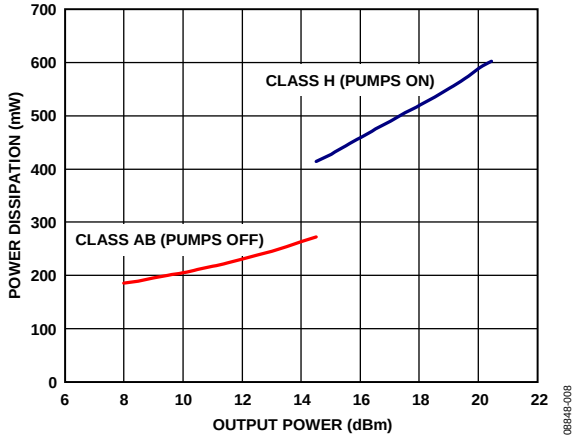



Figure 8. Power Dissipation per Channel vs. Output Power; Includes Line Power

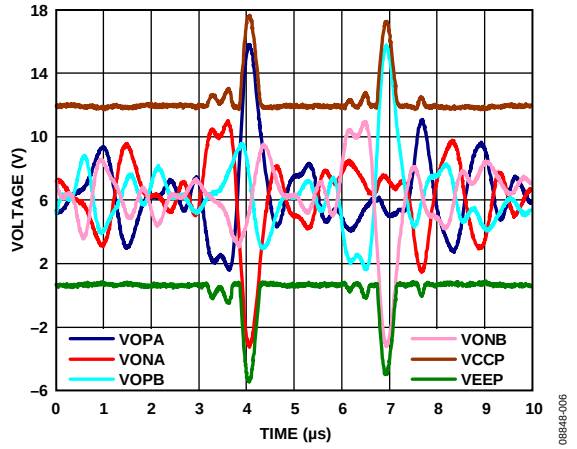



Figure 6. Outputs and Pumps Time Domain Response, Typical ADSL/ADSL2+ Application Circuit, $V_{CC}$ = 12.5 V, $P_{OUT}$ = 20.4 dBm, Crest Factor = 5.45

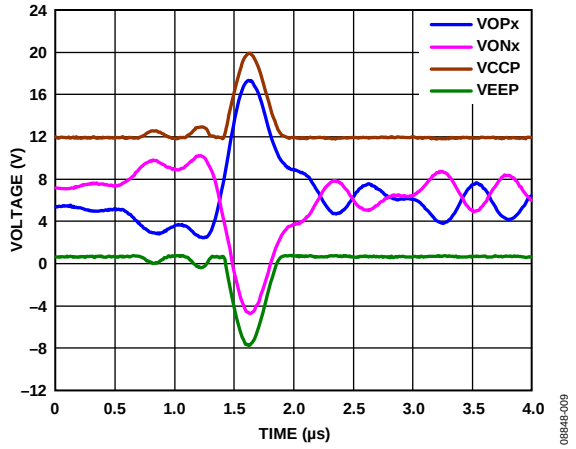



Figure 9. Outputs and Pumps Time Domain Response, Typical ADSL/ADSL2+ Application Circuit, $V_{CC}$ = 12.5 V, $P_{OUT}$ = 19.8 dBm, Crest Factor = 6.9

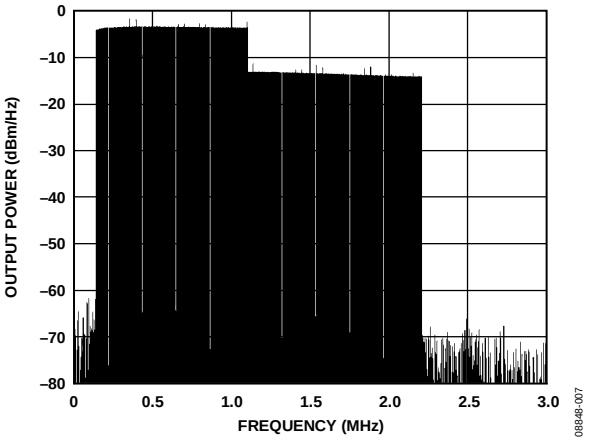



Figure 7. Multitone Power Ratio (MTPR), Typical ADSL/ADSL2+ Application Circuit, $V_{CC}$ = 12.5 V, $P_{OUT}$ = 20.4 dBm, Crest Factor = 5.45

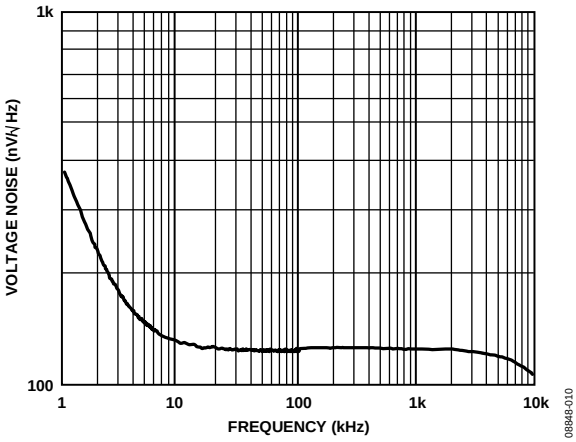



Figure 10. Differential Output Voltage Noise vs. Frequency

# THEORY OF OPERATION

A Class H DSL line driver achieves power savings by using internally developed, signal tracking, power supplies. These tracking power supplies are derived from a single $V_{CC}$ power supply of 12.5 V nominal. The power savings occur due to minimum headroom provided by the tracking, or pumped, supplies to ensure nonsaturation of the output buffer amplifier. For Class H drivers, the average total power that the amplifier consumes is lower than that of conventional Class AB amplifier architectures using a fixed supply.

The ADLD8403 is the second implementation of a patented amplifier architecture developed by Analog Devices. This new architecture, known as Adaptive Linear Power (ALP), is optimized to process signals with occasional peaks that are much greater than the rms level, such as the discrete multitone (DMT) signals used in xDSL applications. Figure 11 shows the ADLD8403 block diagram. Included are two Class AB current feedback (CFB) amplifiers, along with the ALP unit and standard bias block. The architecture combines Class AB amplifiers with the ALP to provide a system that generates internal supplies (VCCP and VEEP) that move linearly with the input signal. This movement is achieved by sampling the input signal via the input pins, INPA and INNA, and applying the appropriate gain to create the variable supplies at the VCCP and VEEP pins.

The ADLD8403 contains two complete channels of ADSL2+ compliant drivers. Each channel has a power mode signal, or PD pin (PD_A and PD_B), that enables the output buffer. Additionally, in applications where less than 14.5 dBm of line power is required, a third PD_PMP signal is used to disable the signal tracking, power supplies. This feature reduces power consumption by approximately 125 mW for these reduced line powers. Because both channels share the pumped supplies in the ADLD8403, the PD_PMP pin is used only when both channels require less than 14.5 dBm of line power.

The ADLD8403 is intended for use in digital subscriber line access multiplexor (DSLAM) applications. The ADLD8403 a simple process and allows for ease of upgrading existing DSLAM systems.

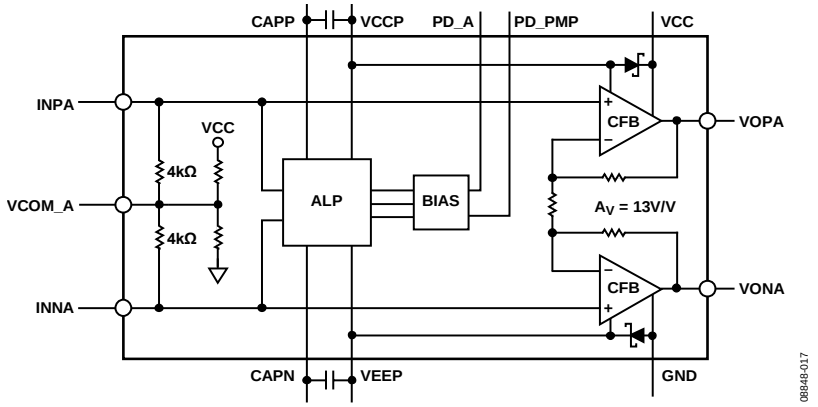



*Figure 11. Block Diagram*

# APPLICATIONS INFORMATION

## SUPPLIES, GROUNDING, AND LAYOUT

The ADLD8403 is powered from a single 12.5 V power supply. For optimum performance, use a well-regulated low ripple power supply. As with all high speed amplifiers, pay close attention to supply decoupling, grounding, and overall board layout. Provide low frequency supply decoupling by using a 10 µF tantalum capacitor between VCC and ground. In addition, decouple VCC to ground using a high quality 0.1 µF ceramic chip capacitor placed as close as possible to the driver. Use an internal low impedance ground plane to provide a common ground point for all driver and decoupling capacitor ground requirements. Whenever possible, use separate ground planes for analog and digital circuitry.

Do not decouple the pumped supply pins, VCCP and VEEP, because doing so adversely affects the operation of the internal charge pumps.

Keep input and output traces as short as possible and as far apart from each other as practical to minimize crosstalk. Keep all differential signal traces as symmetrical as possible.

## POWER MANAGEMENT

A digitally programmable logic pin switches each port of the ADLD8403 between active bias and shutdown states. The PD_A pin controls Port A, and the PD_B pin controls Port B. These pins can be controlled directly with either 3.3 V or 5 V CMOS logic using the GND pins as a reference. If left unconnected, the PD_A and PD_B pins float high, placing the amplifier in the power-down state. Additionally, for lower output power applications in which the differential DMT peaks are below 10 V (assuming a supply voltage of 12.5 V), the PD_PMP pin can be used to turn off the internal charge pumps for additional power savings. If left unconnected, the PD_PMP pin floats high, placing the charge pump in the inactive state. In the event that PD_A and PD_B are both held high, the charge pump is disabled, regardless of the logic level on PD_PMP. See the Specifications section for the quiescent current for each of the available bias states.

## DYNAMIC SUPPLIES

The ADLD8403 uses the stored charge of capacitors to provide the supply boost necessary to pass the peaks of the xDSL signal. The capacitors are placed between CAPP and VCCP, as well as between CAPN and VEEP, as shown in Figure 11. The charge pump capacitors must be 0.47 µF with a minimum dc voltage rating of 16 V. Using a dielectric X7R capacitor is recommended.

Charging time is critical for proper chip operation because, depending on the application, peak currents can be large (up to 250 mA). The system is optimized for signals with occasional peaks that are much greater than the rms level, such as the DMT waveform used in xDSL applications. It may not be applicable for a system processing a periodic sinusoidal waveform with an amplitude that exceeds the dc supply (VCC) into a heavy load (<500 Ω).

## TYPICAL ADSL/ADSL2+ APPLICATION

In a typical ADSL/ADSL2+ application, a differential line driver takes the signal from the analog front end (AFE) and drives it onto the twisted pair telephone line. Referring to the typical circuit representation in Figure 12, the differential input appears at $V_{IN+}$ and $V_{IN-}$ from the AFE, and the differential output is transformer-coupled to the telephone line at the tip and ring. The common-mode operating point, generally midway between the supplies, is set internally and is available at both VCOM_A and VCOM_B.

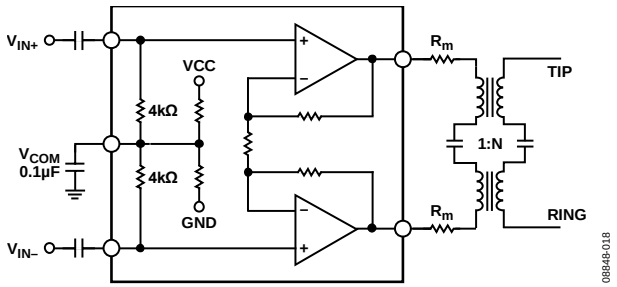



*Figure 12. Typical ADSL/ADSL2+ Application Circuit*

## MULTITONE POWER RATIO (MTPR)

The DMT signal used in ADSL/ADSL2+ systems carries data in discrete tones or bins, which appear in the frequency domain in evenly spaced 4.3125 kHz intervals. In applications using this type of waveform, the MTPR is commonly used to measure ac linearity. In general, designers are concerned with two types of MTPR: in-band and out-of-band. In-band MTPR is the measured difference from the peak of one tone that is loaded with data to the peak of an adjacent empty tone. Out-of-band MTPR is the spurious emissions that occur in bands just below and above the transmit band. For ADSL2+ applications, the out-of-band MTPR is the receive band between 25.875 kHz and 138 kHz and the region above 2.208 MHz. Figure 13 shows the out-of-band MTPR for the ADLD8403.

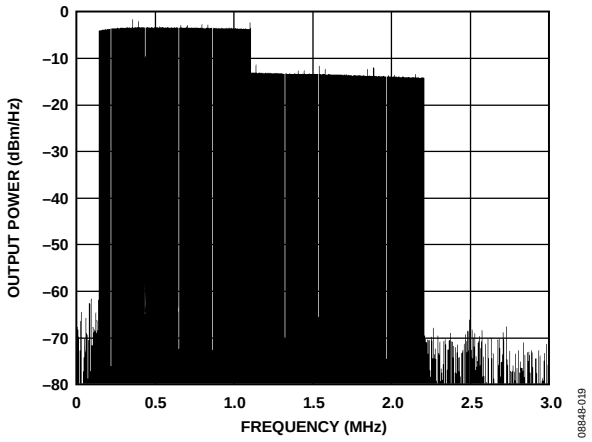



*Figure 13. Out-of-Band MTPR*

## LIGHTNING AND AC POWER FAULT

As an ADSL/ADSL2+ line driver, the ADLD8403 is transformer coupled to the twisted pair telephone line. In this environment, the ADLD8403 is subject to large line transients resulting from events such as lightning strikes or downed power lines. Additional circuitry is required to protect the ADLD8403 from damage due to these events.

# OUTLINE DIMENSIONS

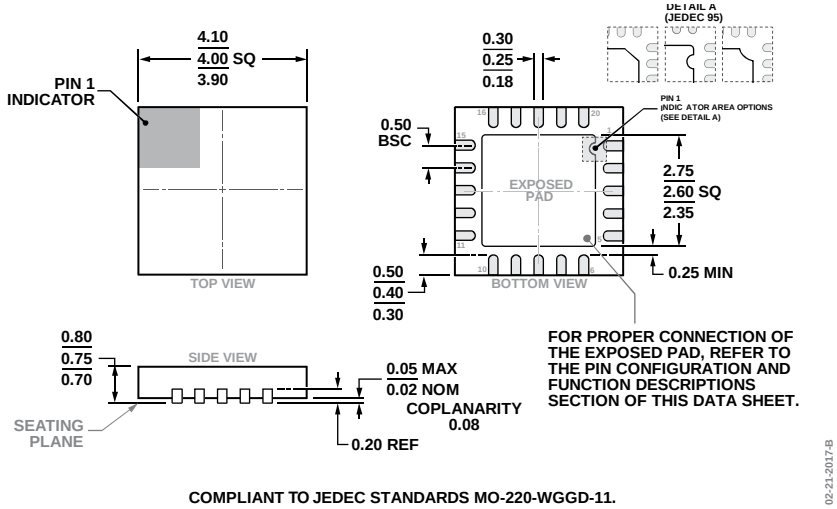



*Figure 14. 20-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CP-20-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADLD8403ACPZ-R2 | −40°C to +85°C | 20-Lead Lead Frame Chip Scale Package [LFCSP] | CP-20-8 |
| ADLD8403ACPZ-R7 | −40°C to +85°C | 20-Lead Lead Frame Chip Scale Package [LFCSP] | CP-20-8 |
| ADLD8403ACPZ-RL | −40°C to +85°C | 20-Lead Lead Frame Chip Scale Package [LFCSP] | CP-20-8 |

[1] Z = RoHS Compliant Part.

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