DC to 6 GHz, ≤45 dB Envelope Threshold Detector/Trigger

Data Sheet

ADL5910

FEATURES

- Envelope threshold detection and latching
- Broad input frequency range: dc to 6 GHz
- ±1.0 dB input range: ≤45 dB
- ±1.0 dB input level: −30 dBm to +15 dBm at 100 MHz
- Programmable threshold and latch reset function
- Propagation delay: 12 ns typical from RFIN to Q/$\overline{Q}$ latch
- All functions temperature and supply stable
- Operates at 3.3 V from −40°C to +105°C
- Quiescent current: 3.5 mA typical
- Power-down current: 100 µA typical
- 16-lead, 3 mm × 3 mm LFCSP package

APPLICATIONS

- Wireless power amplifier input and output protection
- Wireless receiver input protection
- RF pulse detection and triggering

FUNCTIONAL BLOCK DIAGRAM

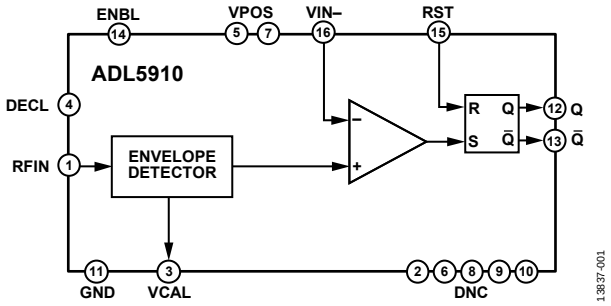


Figure 1.

GENERAL DESCRIPTION

The ADL5910[1] is a radio frequency (RF) detector that operates from dc to 6 GHz. It provides a programmable envelope threshold detection function.

The envelope threshold detection function compares the voltage from an internal envelope detector with a user defined input voltage. When the voltage from the envelope detector exceeds the user defined threshold voltage, an internal comparator captures and latches the event to a set or reset (SR) flip flop. The response time from the RF input signal exceeding the user programmed threshold to the output latching is 12 ns. The latched event is held on the flip flop until a reset pulse is applied.

The RF input of the ADL5910 is dc-coupled, allowing operation down to arbitrarily low ac frequencies. It operates on a 3.3 V supply and consumes 3.5 mA. Power-down mode reduces this current to 100 µA when a logic low is applied to the ENBL pin.

The ADL5910 is supplied in a 3 mm × 3 mm, 16-lead LFCSP for operation over the wide temperature range of −40°C to +105°C.

[1] Protected by U.S. Patent 9,379,675.

Rev. 0
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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Technical Support
www.analog.com

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REVISION HISTORY

4/2017—Revision 0: Initial Version

SPECIFICATIONS

VPOS = 3.3 V, continuous wave (CW) input, T_A = 25°C, and rms capacitance (C_{RMS}) = 10 nF, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		DC		6	GHz
f = 10 MHz					
±1.0 dB Input Range			45		dB
±1.0 dB Input Level					
Maximum	Three-point calibration at −25 dBm, −10 dBm, and +10 dBm		15		dBm
Minimum			−30		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		743		mV
	For threshold detection at 0 dBm		240		mV
	For threshold detection at −10 dBm		80		mV
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, RF input power on the RFIN pin (P_{IN}) ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.3/0[1]		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.5/0[1]		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.3/0[1]		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.5/0[1]		dB
f = 30 MHz					
±1.0 dB Input Range			45		dB
±1.0 dB Input Level					
Maximum	Three-point calibration at −25 dBm, −10 dBm, and +10 dBm		15		dBm
Minimum			−30		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		723		V
	For threshold detection at 0 dBm		238		mV
	For threshold detection at −10 dBm		80		mV
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		0/0.2[1]		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.4/−0.2[1]		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.4/0[1]		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		0/0.2[1]		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.4/−0.2[1]		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.4/0[1]		dB
f = 100 MHz					
±1.0 dB Input Range			45		dB
±1.0 dB Input Level					
Maximum	Three-point calibration at −25 dBm, −10 dBm, and +10 dBm		15		dBm
Minimum			−30		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		742		mV
	For threshold detection at 0 dBm		239		mV
	For threshold detection at −10 dBm		81		mV
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		±0.1		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.4/−0.2[1]		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.5/0[1]		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		±0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.4/−0.2[1]		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.5/0[1]		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f = 900 MHz					
±1.0 dB Input Range			45		dB
±1.0 dB Input Level					
Maximum	Three-point calibration at −20 dBm, 0 dBm, and +10 dBm		17		dBm
Minimum			−28		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		752		mV
	For threshold detection at 0 dBm		241		mV
	For threshold detection at −10 dBm		81		mV
Threshold Variation vs. Temperature	$-40°C < T_A < +85°C$, $P_{IN} \approx 10$ dBm		±0.1		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx 0$ dBm		−0.2/+0.1[1]		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx -10$ dBm		0.1/0.3[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 10$ dBm		±0.1		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 0$ dBm		−0.2/+0.1[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx -10$ dBm		0.1/0.3[1]		dB
f = 1900 MHz					
±1.0 dB Input Range			45		dB
±1.0 dB Input Level					
Maximum	Three-point calibration at −20 dBm, 0 dBm, and +10 dBm		17		dBm
Minimum			−28		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		774		mV
	For threshold detection at 0 dBm		241		mV
	For threshold detection at −10 dBm		78		mV
Threshold Variation vs. Temperature	$-40°C < T_A < +85°C$, $P_{IN} \approx 10$ dBm		−0.2/+0.1[1]		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx 0$ dBm		−0.1/0[1]		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx -10$ dBm		±0.2		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 10$ dBm		−0.2/+0.1[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 0$ dBm		−0.1/0[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx -10$ dBm		±0.2		dB
f = 2600 MHz					
±1.0 dB Input Range			43.5		dB
±1.0 dB Input Level					
Maximum	Three-point calibration at −20 dBm, 0 dBm, and +10 dBm		16		dBm
Minimum			−27.5		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		775		mV
	For threshold detection at 0 dBm		236		mV
	For threshold detection at −10 dBm		76		mV
Threshold Variation vs. Temperature	$-40°C < T_A < +85°C$, $P_{IN} \approx 10$ dBm		−0.3/+0.1[1]		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx 0$ dBm		−0.2/0[1]		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx -10$ dBm		−0.4/−0.1[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 10$ dBm		−0.3/+0.1[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 0$ dBm		−0.2/0[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx -10$ dBm		−0.4/−0.1[1]		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f = 3500 MHz					
±1.0 dB Input Range			42		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −18 dBm, 0 dBm, and +10 dBm		17		dBm
Minimum			−25		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		608		mV
	For threshold detection at 0 dBm		177		mV
	For threshold detection at −10 dBm		55		mV
Threshold Variation vs. Temperature	$-40°C < T_A < +85°C$, $P_{IN} \approx 10$ dBm		±0.2		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx 0$ dBm		±0.1		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx -10$ dBm		−0.5/−0.1[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 10$ dBm		±0.2		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 0$ dBm		±0.1		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx -10$ dBm		−0.5/−0.1[1]		dB
f = 5800 MHz					
±1.0 dB Input Range			37		dB
±1.0 dB Input Level					
Maximum	Three-point calibration at −10 dBm, 0 dBm, and +10 dBm		19		dBm
Minimum			−18		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		334		mV
	For threshold detection at 0 dBm		92		mV
	For threshold detection at −10 dBm		29		mV
Threshold Variation vs. Temperature	$-40°C < T_A < +85°C$, $P_{IN} \approx 10$ dBm		±0.2		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx 0$ dBm		±0.4		dB
	$-40°C < T_A < +85°C$, $P_{IN} \approx -10$ dBm		−0.6/+0.4[1]		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 10$ dBm		±0.2		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx 0$ dBm		±0.4		dB
	$-40°C < T_A < +105°C$, $P_{IN} \approx -10$ dBm		−0.6/+0.4[1]		dB
THRESHOLD DETECT OUTPUT	Q, $\overline{Q}$, and RST pins, 900 MHz input frequency				
Propagation Delay	From RFIN to Q/$\overline{Q}$ latch				
	RFIN pin = off to 10 dBm, V_{IN-} = 400 mV (5 dB overdrive)		12		ns
	RFIN pin = off to −5 dBm, V_{IN-} = 75 mV (5 dB overdrive)		12		ns
Output Voltage	Q, $\overline{Q}$				
Low	I_{OL} = 1 mA			300	mV
High	I_{OH} = 1 mA	3.0			V
RESET INTERFACE	RST pin				
RST Input Voltage					
Low				0.6	V
High		2			V
RST Input Bias Current			20		nA
Reset Time	RST at 50% to Q low and $\overline{Q}$ high		15		ns
COMPARATOR INTERFACE	VIN− pin				
VIN− Input Range			0 to 1.5		V
VIN− Input Bias Current			−20		µA
VIN− for Comparator Disable		V_{POS}			V
VCAL INTERFACE	VCAL pin				
VCAL Output Voltage	RFIN pin = off		750		mV
	RFIN pin = −10 dBm, 900 MHz		825		mV
	RFIN pin = 10 dBm, 900 MHz		1.5		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN INTERFACE	ENBL pin				
Voltage Level					
To Enable		2		V_{POS}	V
To Disable		0		0.6	V
Input Bias Current	V_{ENBL} = 2.2 V		<20		nA
POWER SUPPLY INTERFACE	VPOS pin				
Supply Voltage		3.15	3.3	3.45	V
Quiescent Current	T_A = 25°C, no signal at RFIN		3.5		mA
	T_A = 105°C, no signal at RFIN		4		mA
Power-Down Current	ENBL = low		100		µA

[1] The slash indicates a range. For example, −0.3/0 means −0.3 to 0.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
Input Average RF Power[1]	25 dBm
Equivalent Voltage, Sine Wave Input	5.62 V peak
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Drive this parameter from a 50 Ω source. It is input ac-coupled with an external 82.5 Ω shunt resistor, and VPOS = 3.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-16-22	80.05	4.4	°C/W

[1] Thermal impedance simulated value is based on no airflow with the exposed pad soldered to a 4-layer JEDEC board.
[2] Thermal impedance from junction to exposed pad on underside of package.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

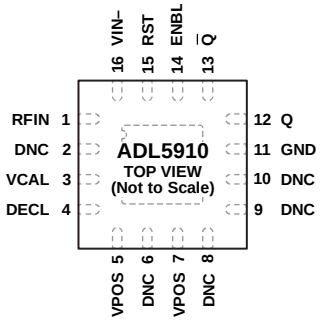


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. The RFIN pin is dc-coupled and is not internally matched. A broadband 50 Ω match is achieved using an external 82.5 Ω shunt resistor with a 0.47 µF ac coupling capacitor placed between the shunt resistor and the RF input. Smaller ac coupling capacitor values can be used if low frequency operation is not required.
2, 6, 8, 9, 10	DNC	Do Not Connect. Do not connect to these pins.
3	VCAL	Threshold Calibration. The voltage on this pin determines the correct threshold voltage that must be applied to Pin 16 (VIN–) to set a particular RF power threshold. This process has two steps: first, measure the output voltage on VCAL with no RF signal applied to RFIN (this voltage is typically 750 mV). Next, apply the RF input power to RFIN, which causes the circuit to trip and again measure the voltage on the VCAL pin. The difference between these two voltages is equal to the threshold voltage that must be applied to VIN– during operation.
4	DECL	Internal Decoupling. Bypass this pin to ground using a 4.02 Ω resistor connected in series with a 100 nF capacitor.
5, 7	VPOS	Power Supply. The supply voltage range = 3.3 V ±10%. Place power supply decoupling capacitors on Pin 5. There is no requirement for power supply decoupling capacitors on Pin 7.
11	GND	Device Ground. Connect the GND pin to system ground using a low impedance path.
12, 13	Q, $\overline{Q}$	Differential Digital Outputs of Threshold Detection Flip Flop. Q latches high when the output of the internal envelope detector exceeds the threshold voltage on the internal comparator VIN– input.
14	ENBL	Device Enable. Connect the ENBL pin to logic high to enable the device.
15	RST	Flip Flop Reset. Taking RST high clears the latched flip flop output, setting the Q and $\overline{Q}$ outputs to low and high, respectively.
16	VIN–	Inverting Input to the Threshold Detection Comparator. The voltage on this pin is compared to the output voltage of the internal envelope detector, which is driven by the RF input level. If the output voltage of the envelope detector exceeds the voltage on VIN–, the flip flop latches the Q output to high and the $\overline{Q}$ output to low.
	EPAD	Exposed Pad. Connect the exposed pad to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VPOS = 3.3 V, input levels referred to 50 Ω source. Input RF signal is a sine wave (CW), unless otherwise noted.

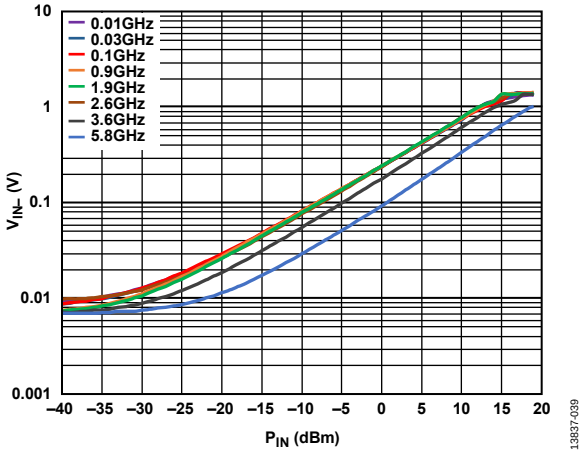


Figure 3. V_{IN-} vs. P_{IN} at Various Frequencies

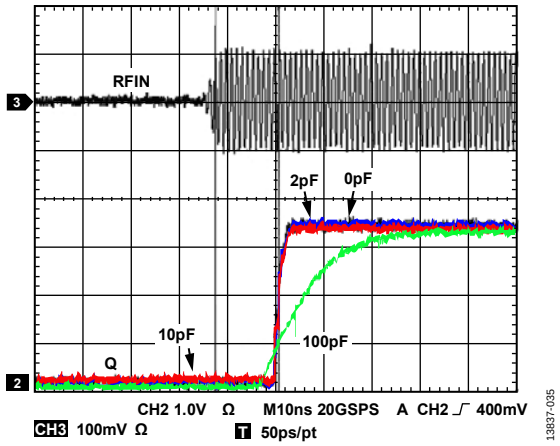


Figure 6. Q Output Response vs. Load Capacitance, P_{IN} = Off to −10 dBm, Overdrive Threshold Voltage Set to Trigger at −11 dBm (Overdrive Level = 1 dB, VIN− = 65 mV)

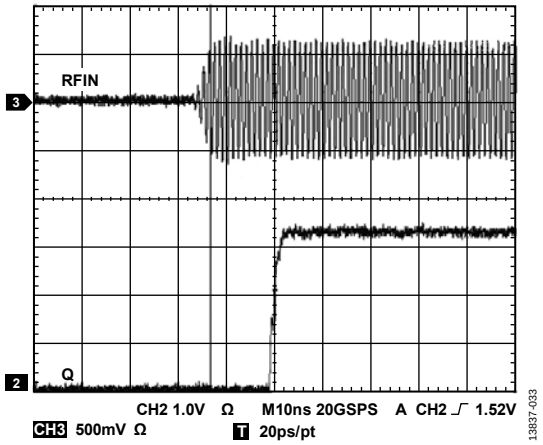


Figure 4. Q Output Response, P_{IN} = Off to 6 dBm, VIN− (400 mV) Set to Trigger at 5 dBm (Overdrive Level = 1 dB)

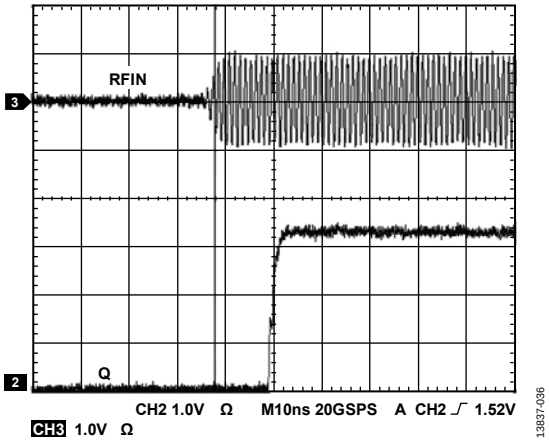


Figure 7. Q Output Response, P_{IN} = Off to 10 dBm, VIN− (400 mV) Set to Trigger at 5 dBm (Overdrive Level = 5 dB)

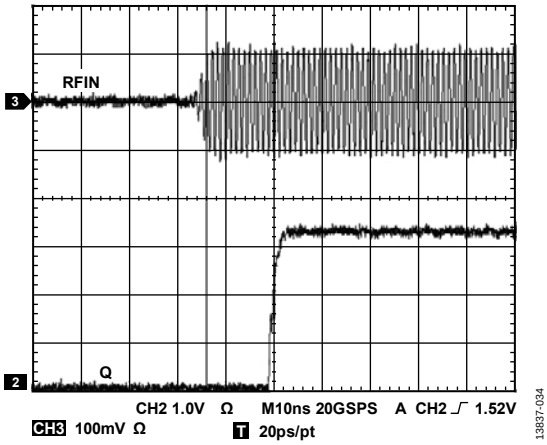


Figure 5. Q Output Response, P_{IN} = Off to −9 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 1 dB, VIN− = 75 mV)

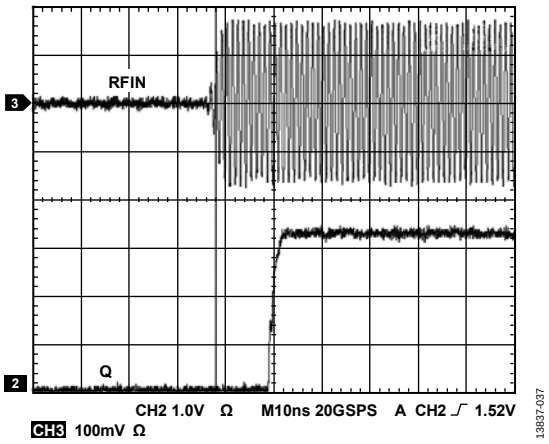


Figure 8. Q Output Response, P_{IN} = Off to −5 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 5 dB, VIN− = 75 mV)

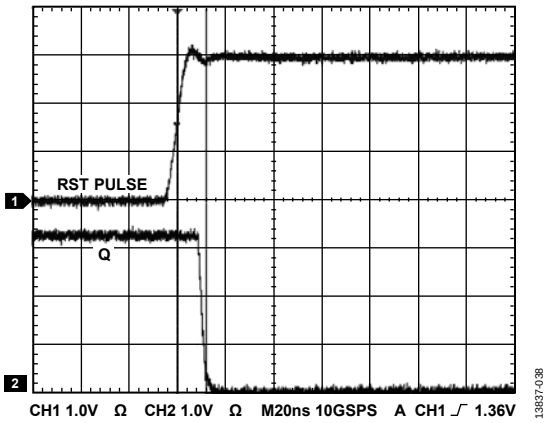


Figure 9. Response of Q Output to RST

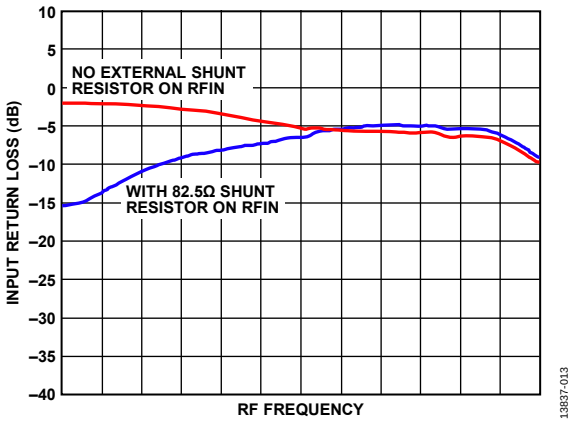


Figure 11. Input Return Loss vs. RF Frequency (With and Without External 82.5 Ω Shunt Resistor on RFIN) from 10 MHz to 6 GHz

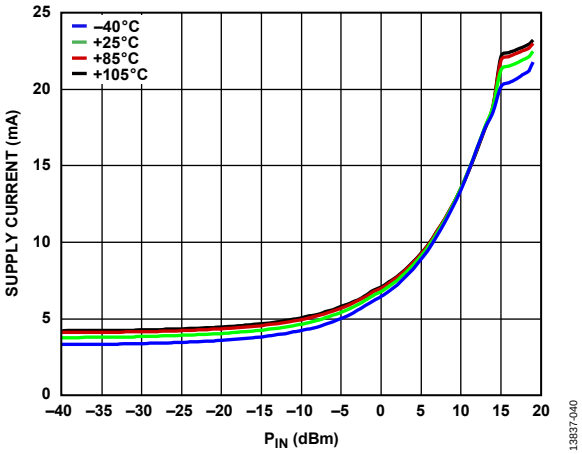


Figure 10. Supply Current vs. P_{IN} for Various Temperatures

THEORY OF OPERATION

The ADL5910 is a threshold detector with a 45 dB of detection range at 1.9 GHz and a useable range up to 6 GHz. It features no error ripple over its range, low temperature drift, and very low power consumption.

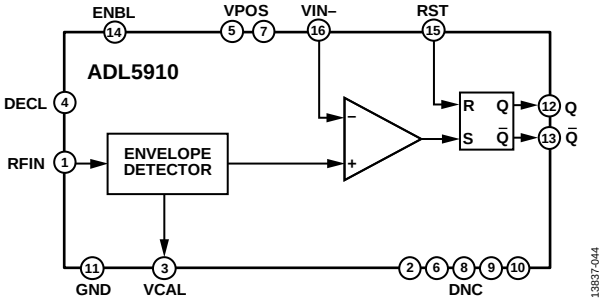


Figure 12. Functional Block Diagram

The output of the envelope detector drives the noninverting input of a threshold detecting comparator. The inverting input of this comparator is typically driven by a fixed external dc voltage. When the output of the envelope detector exceeds the voltage on the inverting input of the comparator, the comparator goes high. This excursion is then captured and held by an SR flip flop. The state of this flip flop is then held until the level sensitive RST pin is taken high.

$$VIN- = Slope \times (V_{RFIN} - Intercept) \quad (1)$$

$$VIN- = Slope \times \left(\sqrt{\frac{R \times \log^{-1}\left(\frac{P_{IN}}{10}\right)}{10^3}} - Intercept \right) \quad (2)$$

BASIC CONNECTIONS

The ADL5910 requires a single supply of 3.3 V. The supply is connected to the VPOS supply pins. Decouple these pins using two capacitors with values equal or similar to those shown in Figure 13. Place these capacitors as close to Pin 5 as possible. Connect Pin 11 (GND) and the exposed pad to a ground plane with low electrical and thermal impedance.

A single-ended input at the RFIN pin drives the ADL5910. Because the input is dc-coupled, an external ac coupling capacitor must be used. A 470 nF capacitor is recommended for applications that require frequency coverage from 6 GHz down to tens of kilohertz. For applications that do not need such low frequency coverage, a larger value of capacitance can be used.

In addition to the ac-coupling capacitor, an external 82.5 Ω shunt resistor is required to provide a wideband input match. Figure 11 shows a comparison of the input return loss, with and without the external shunt resistor.

The DECL pin provides a bypass capacitor connection for an on-chip regulator. The DECL pin is connected to ground with a 4.02 Ω resistor and a 0.1 µF capacitor.

The ENBL pin configures the device enable interface. Connecting the ENBL pin to a logic high signal (2 V to V_{POS}) enables the device, and connecting the pin to a logic low signal (0 V to 0.6 V) disables the device. The exposed pad is internally connected to GND and must be soldered to a low impedance ground plane.

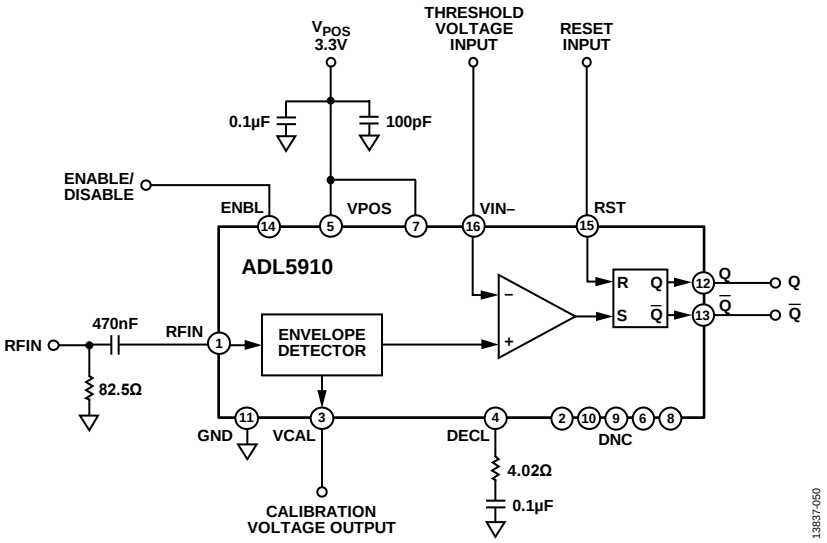


Figure 13. Basic Connections

A threshold voltage is applied to the VIN− input that corresponds to the RF power level at which the circuit trips. When the level on RFIN drives the envelope detector to an output voltage that exceeds the programmed threshold, the comparator output goes high causing the Q output to latch high and the $\overline{Q}$ output to latch low. The levels on Q and $\overline{Q}$ can be reset by setting the RST pin high (note that the RST function is level triggered, not edge triggered). Q and $\overline{Q}$ are held at low and high states, respectively, as long as RST is high, even if the RF input level is exceeding the programmed threshold voltage. RST must be taken low for the threshold detection circuit to reactivate.

Q AND $\overline{Q}$ RESPONSE TIME

Figure 14 shows the response of the Q output when the input power exceeds the programmed threshold by approximately 1 dB. The response time from the input power exceeding the threshold to the Q output reaching 50% of its final value is approximately 12 ns.

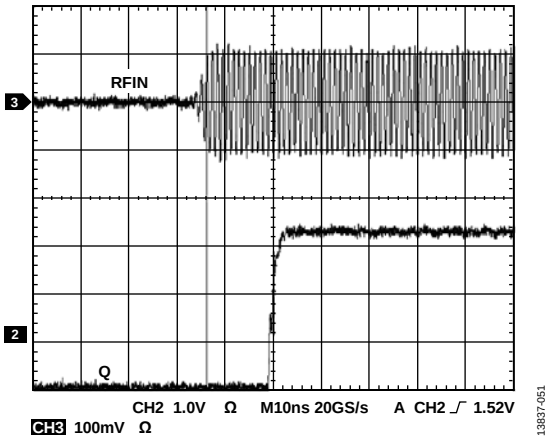


Figure 14. Q Output Response at 900 MHz, P_{IN} = Off to −9 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 1 dB)

The response time of the Q and $\overline{Q}$ outputs is somewhat dependent on the level of overdrive with higher overdrive levels, giving a slightly faster response time. Figure 15 shows the response of the Q output when the RF input level overdrives the threshold by 5 dB, which reduces the response time to approximately 12 ns. Overdrive levels beyond 5 dB tend not to reduce the response time below this level. Capacitive loading on Q also affects the response time, as shown in Figure 6.

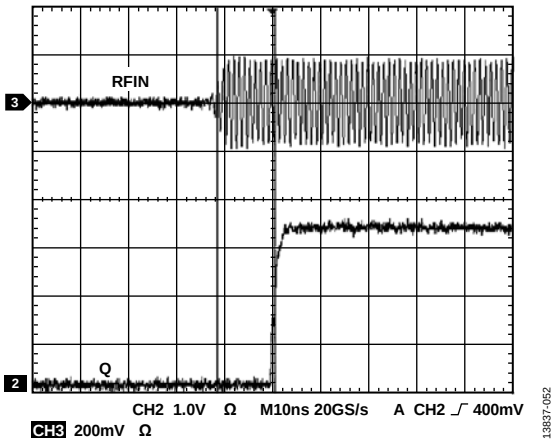


Figure 15. Q Output Response, P_{IN} = Off to −5 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 5 dB, VIN− = 75 mV)

Figure 16 shows the response of the $\overline{Q}$ output, which goes low when the input threshold is exceeded. As shown in Figure 16, the response time of $\overline{Q}$ is equal to that of the Q output.

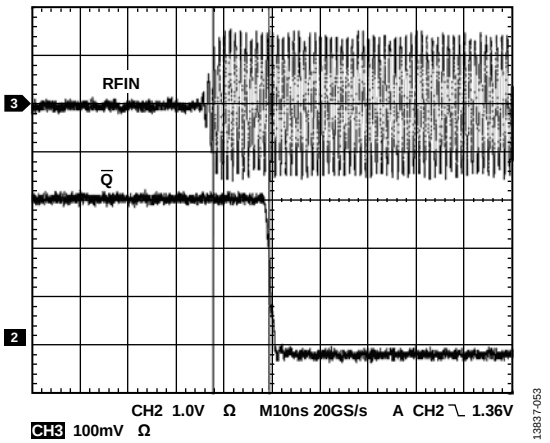


Figure 16. $\overline{Q}$ Output Response, P_{IN} = Off to −7 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 3 dB)

SETTING THE V_{IN-} THRESHOLD DETECTION VOLTAGE

Figure 17 shows the typical relationship between the voltage on the VIN− pin and the RF input power on the RFIN pin This data is also presented in Table 5.

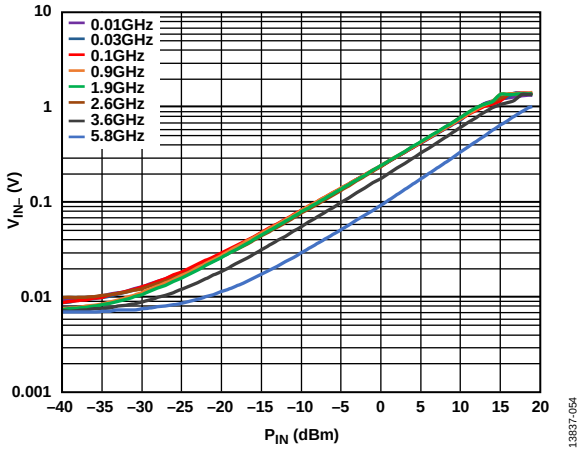


Figure 17. Relationship Between the Voltage on the VIN− Pin (V_{IN-}) and the RF Input Power on the RFIN Pin (P_{IN})

Use Figure 17 and Table 5 to set the threshold voltage on the VIN− pin. However, because the relationship between the threshold voltage on VIN− and the resulting RF threshold power varies from device to device, there is an error level of up to ±2.5 dB. For example, if the voltage on VIN− is set to cause the circuit to trip when the input power exceeds 0 dBm at 900 MHz (V_{IN-} = 241 mV from Table 5), the trip point can vary from device to device by ±2.5 dB at frequencies at or above 100 MHz and +2.5 dB to −5.5 dB for frequencies below 100 MHz. In Table 5, no recommended voltages are provided for input power levels less than −25 dBm from 10 MHz to 3.5 GHz and less than −20 dBm at 5.8 GHz because of the increased temperature drift at these input power levels. Likewise, from 10 MHz to 3.5 GHz, no recommended voltages are provided for input power levels more than 13 dBm because at this power level the response of the ADL5910 starts to become more nonlinear.

To set the threshold detect level more precisely, there are two calibration options. A single-point calibration is accomplished easily by applying the threshold trip power level and then adjusting VIN− until Q trips high. Initially, set VIN− to a high level such as 2 V, and then assert RST high and back to low to ensure that Q is low. Next, apply the RF input threshold power level to RFIN. Then, reduce the voltage on VIN− until the Q output goes high. Use this resulting voltage to set the threshold level when the equipment is in operation.

Table 5. Recommended Typical Values for Threshold Voltage (V_{IN-}) When Operating Uncalibrated

Input Threshold Power (dBm)	Threshold Voltage (mV)[1]							
	10 MHz	30 MHz	100 MHz	900 MHz	1900 MHz	2600 MHz	3500 MHz	5800 MHz
−25.0	18	18	18	17	16	17	12	N/A
−24.0	19	19	20	18	17	18	13	N/A
−23.0	21	21	22	20	19	20	14	N/A
−22.0	23	23	24	22	21	22	15	N/A
−21.0	25	25	26	25	23	24	17	N/A
−20.0	28	28	29	27	26	26	19	11
−19.0	31	31	32	31	29	29	21	12
−18.0	34	34	35	34	32	32	23	13
−17.0	37	38	39	38	36	35	25	14
−16.0	41	42	43	42	40	39	28	16
−15.0	47	47	48	47	45	44	31	17
−14.0	52	52	53	52	50	49	35	19
−13.0	58	58	59	58	56	54	39	21
−12.0	64	64	66	65	62	60	44	23
−11.0	71	72	73	72	70	68	49	26
−10.0	80	80	81	81	78	76	55	29
−9.0	88	89	90	90	87	84	61	32
−8.0	98	99	101	101	97	94	69	36
−7.0	110	111	112	112	109	105	77	40
−6.0	123	123	125	125	122	118	87	45
−5.0	137	137	139	139	136	132	98	51
−4.0	154	153	155	155	153	148	110	57
−3.0	172	172	173	173	171	167	124	64
−2.0	193	192	193	193	192	186	140	73
−1.0	214	214	216	216	215	210	158	81
0.0	240	238	239	241	241	236	177	92
+1.0	269	266	268	272	270	266	200	104
+2.0	300	298	300	304	303	298	226	119
+3.0	336	334	336	340	341	337	255	135
+4.0	376	374	377	380	383	380	289	153
+5.0	421	419	421	425	431	425	327	175
+6.0	472	466	471	477	485	481	370	199
+7.0	529	522	528	534	543	544	419	225
+8.0	592	585	591	598	611	610	474	257
+9.0	664	652	663	670	688	690	537	293
+10.0	743	723	742	752	774	775	608	334
+11.0	858	844	830	842	871	875	684	381
+12.0	939	957	927	942	976	982	774	434
+13.0	1078	1072	1005	1047	1066	1061	876	495
+14.0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	564
+15.0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	642

[1] N/A means not applicable.

Alternatively, by measuring the voltage on the VCAL output pin with and without RF power applied, an equation can be derived that establishes a precise relationship between the VIN− voltage and the associated RF input power trip point.

Within the linear operating range of the ADL5910, there is a linear relationship between VCAL − $VCAL_{OFF}$ and the input voltage on RFIN.

$$VCAL - VCAL_{OFF} = Slope \times (V_{RFIN} - Intercept) \quad (3)$$

where:
VCAL is the measured output voltage on the VCAL pin.
$VCAL_{OFF}$ is the measured output voltage on the VCAL pin with no RF input signal applied.
V_{RFIN} is the RF input power (in dBm) converted into volts rms, that is,

$$V_{RFIN} = \sqrt{\frac{R \times \log^{-1}\left(\frac{P_{IN}}{10}\right)}{10^3}} \quad (4)$$

where:
R is the characteristic impedance (usually 50 Ω).
P_{IN} is the RF input power on the RFIN pin in dBm.

Rewriting the equation results in

$$VCAL - VCAL_{OFF} = Slope \times \left(\sqrt{\frac{R \times \log^{-1}\left(\frac{P_{IN}}{10}\right)}{10^3}} - Intercept \right) \quad (5)$$

The voltage that must be applied to the VIN− pin for a particular input power is equal to (VCAL − $VCAL_{OFF}$). Therefore, Equation 5 can be rewritten as

$$VIN - - = Slope \times \left(\sqrt{\frac{R \times \log^{-1}\left(\frac{P_{IN}}{10}\right)}{10^3}} - Intercept \right) \quad (6)$$

Use a two-point or a three-point calibration to establish the slope and intercept values in Equation 6. The procedure for a two-point calibration follows:

1. With no RF input signal applied, measure the voltage on the VCAL pin ($VCAL_{OFF}$).
2. Apply an RF input power that is toward the minimum limit of the RF input range ($RFIN_{LOW}$). Calculate the associated input voltage ($V_{RFIN_{LOW}}$) and measure the voltage on the VCAL pin ($VCAL_{LOW}$).
3. Apply an RF input power that is toward the maximum limit of the RF input range ($RFIN_{HIGH}$). Calculate the associated input voltage ($V_{RFIN_{HIGH}}$) and measure the voltage on the VCAL pin ($VCAL_{HIGH}$) pin.
4. Calculate the slope by using the following equation:

   $Slope = (VCAL_{HIGH} - VCAL_{LOW})/(V_{RFIN_{HIGH}} - V_{RFIN_{LOW}})$

5. Calculate the intercept by using the following equation:

   $Intercept = V_{RFIN} - (VCAL - VCAL_{OFF})/Slope$

When the slope and intercept are known, insert them into Equation 6, where $P_{THRESHOLD}$ is the desired RF power level at which the circuit trips.

$$VIN - - = Slope \times \left(\sqrt{\frac{R \times \log^{-1}\left(\frac{P_{THRESHOLD}}{10}\right)}{10^3}} - Intercept \right)$$

APPLICATIONS INFORMATION

A COMPLETE INPUT PROTECTION CIRCUIT

Figure 18 shows a block diagram of a complete input protection circuit that protects the input to a power amplifier or the input to a receiver to frequencies of approximately 2.6 GHz. This circuit consists of a single-pole, single throw (SPST) switch (for this example, the HMC550A), an asymmetrical power splitter/coupler circuit, and the ADL5910. The main signal path is through the coupler and SPST switch. The circuit in this example protects against input levels to the receiver or the power amplifier that exceed 20 dBm.

Under normal operation, the switch is closed. The closed switch results in insertion loss, which is the sum of the switch insertion loss and the insertion loss of the splitter/coupler. In the example shown in Figure 18, the coupling factor is 20 dB, which results in an insertion loss of 1.72 dB. Different resistor values can reduce the insertion loss, which results in a lower level on the coupled signal. The insertion loss of the switch is approximately 0.7 dB, resulting in a total insertion loss of approximately 2.5 dB.

The coupled signal is applied to the RF input of the ADL5910. Because of the coupling factor of 20 dB, the ADL5910 must be configured to respond to input levels in excess of 2.5 dBm. As is shown in Table 5 and Figure 18, the threshold level on VIN− must be set to approximately 300 mV. If high triggering precision is required, perform calibration because the threshold voltage for a particular input power level varies from device to device.

When the output of the ADL5910 triggers after an overdrive event, the $\overline{Q}$ output goes low and opens the HMC550A switch. When the HMC550A switch is open, the attenuation in the signal path increases to the specified isolation of the HMC550A switch and the insertion loss of the coupler, ranging from 15 dB to 40 dB based on frequency.

In the example shown in Figure 18, the $\overline{Q}$ output also drives an interrupt input of a microprocessor or microcontroller. Program the microprocessor or microcontroller to issue short periodic reset pulses. After each reset pulse, the ADL5910 either remains reset (if the input level drops below the threshold) or reopens the switch.

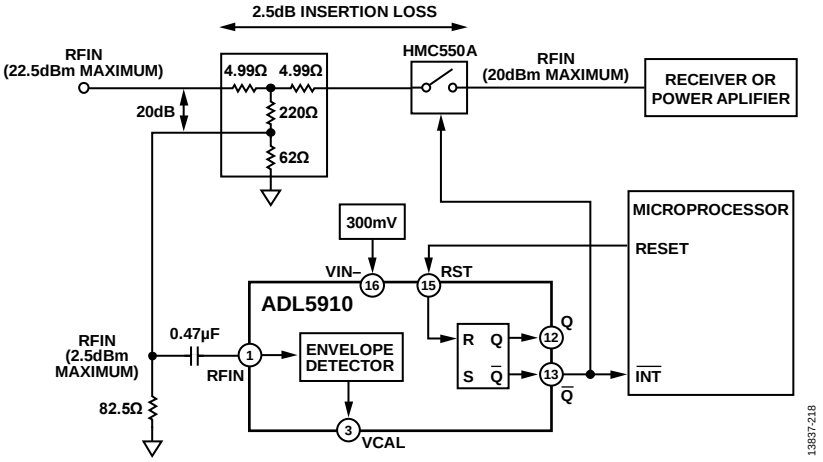


Figure 18. A Complete Input Protection Circuit (Power Supply and Decoupling Omitted for Clarity)

RESET ON ENABLE OR AT POWER-UP

The ADL5910 normally powers up with the Q and $\overline{Q}$ outputs high and low, respectively. If a logic low on the Q output is required on power-up or enable, use the circuit shown in Figure 19. This circuit consists of a capacitor from ENBL to RST and a resistor from RST to ground. When ENBL is asserted, the RST voltage goes high shortly before being pulled back to 0 V by R5.

When the ENBL pin is not used (that is, ENBL is tied to VPOS), tie the C3 capacitor directly to VPOS.

IMPROVING FREQUENCY FLATNESS

For applications where input protection is required over a wide range of input frequencies, use the application circuit shown in Figure 20 to compensate for the frequency roll-off of the ADL5910 detector.

Across its full range, the frequency response of ADL5910 varies by approximately 9 dB with most of the variation between 2 GHz and 6 GHz. As a result, higher power levels are required at higher frequencies to trip the internal comparator (assuming a constant threshold voltage on the VIN− input pin to the comparator). To compensate for this roll-off, insert a preemphasis filter in front of the RF input. The attenuation of this filter decreases with increasing frequency, resulting in an overall flatter response in the combined filter/detector circuit.

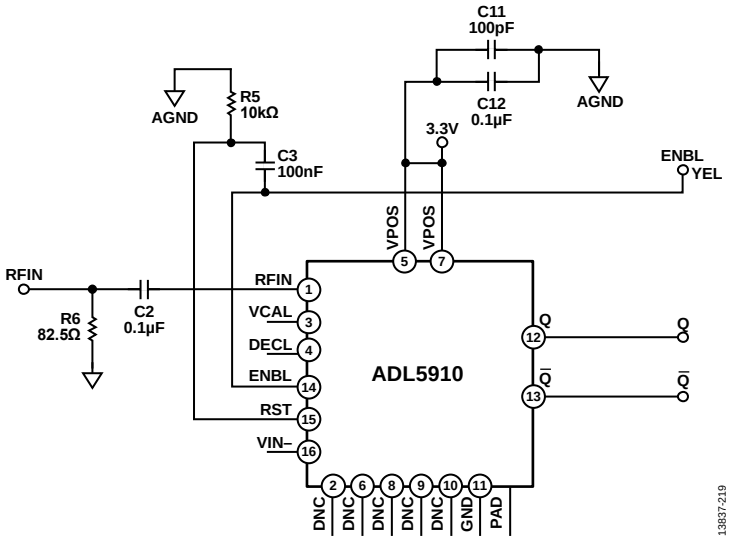


Figure 19. Reset of Q Output on Power-Up/Enable (Additional Connections Omitted for Clarity)

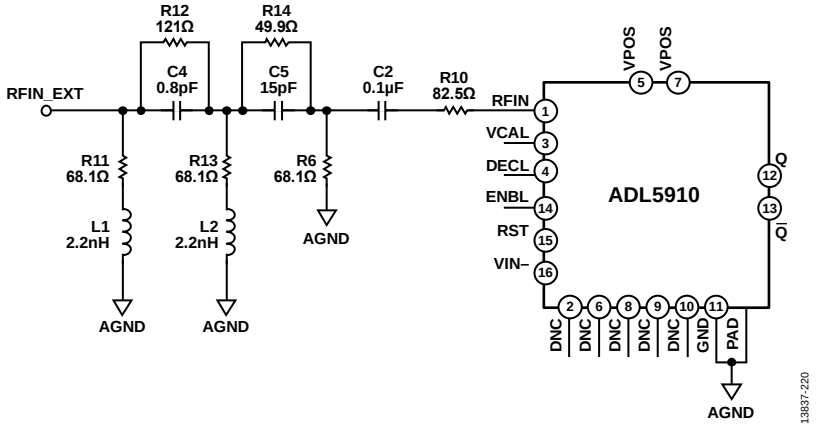


Figure 20. Recommended Schematic for Improving Flatness vs. Frequency Using a Preemphasis Circuit

Figure 21 shows the frequency response of this circuit along with the response with no compensation. In this example, the threshold voltage on VIN− was set to 30 mV.

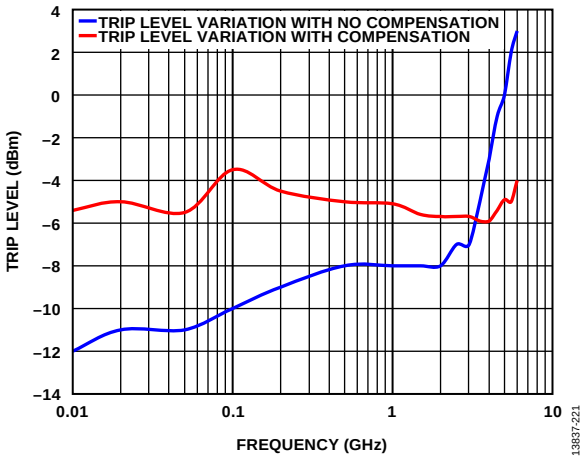


Figure 21. Variation in Threshold Trip Point with and Without Frequency Pre-Emphasis

Figure 22 shows the measured input return loss of the circuit.

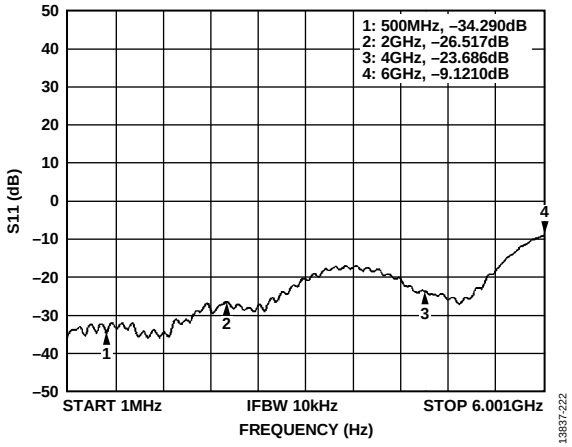


Figure 22. Input Return Loss of ADL5910 with Pre-Emphasis Circuit

EVALUATION BOARD

The ADL5910-EVALZ is a fully populated, 4-layer, FR4 evaluation board that includes an SPST and an asymmetrical power coupling circuit. In its default configuration, the circuit operates as a complete input protection circuit that can connect to the input of a receiver or a power amplifier. A single 3.3 V power supply (VPOS) and GND test loops provide power for the complete board.

The primary signal path on the evaluation board is from the RFIN_SW SMA connector to the RFOUT_SW SMA connector. In this path, there is a HMC550A SPST switch and an asymmetrical power splitter/coupler. The insertion loss of the splitter/coupler is 1.72 dB, which combines with the insertion loss of HMC550A (0.7 dB typical) to product a total signal path loss of approximately 2.5 dB.

The coupling factor of the splitter/coupler is 20 dB, that is, the signal level between R47 and R45 with respect to the signal level at the input of R46.

The coupled signal is applied at the RF input of ADL5910. The threshold level of the ADL5910 is set by an on-board mechanical potentiometer, R8 (an external voltage can also be applied to the VNEXT SMA connector or to the VIN− yellow test loop).

When the RF input level exceeds the equivalent voltage level on VIN−, the $\overline{Q}$ output of the ADL5910 opens the HMC550A, which increases the signal path attenuation to between −40 dB and −20 dB (based on the input frequency). The inline attenuation is the off isolation of the switch. An overdrive trigger also turns on a flashing LED on the evaluation board that is driven by the Q output of the ADL5910. To reset the ADL5910 outputs, press the S1 push down switch.

The evaluation board can also be configured for standalone testing of the ADL5910 by removing R16, placing a 0 Ω resistor on the R9 pad, and applying the RF input signal on the RFIN_ADL5910 SMA connector.

The evaluation board also includes a series of pads in the signal chain that are adjacent to the RF input of the ADL5910. Place capacitors and inductors on these pads to improve RF flatness (see the Applications Information section).

Detailed configuration options for the evaluation board are listed in Table 6.

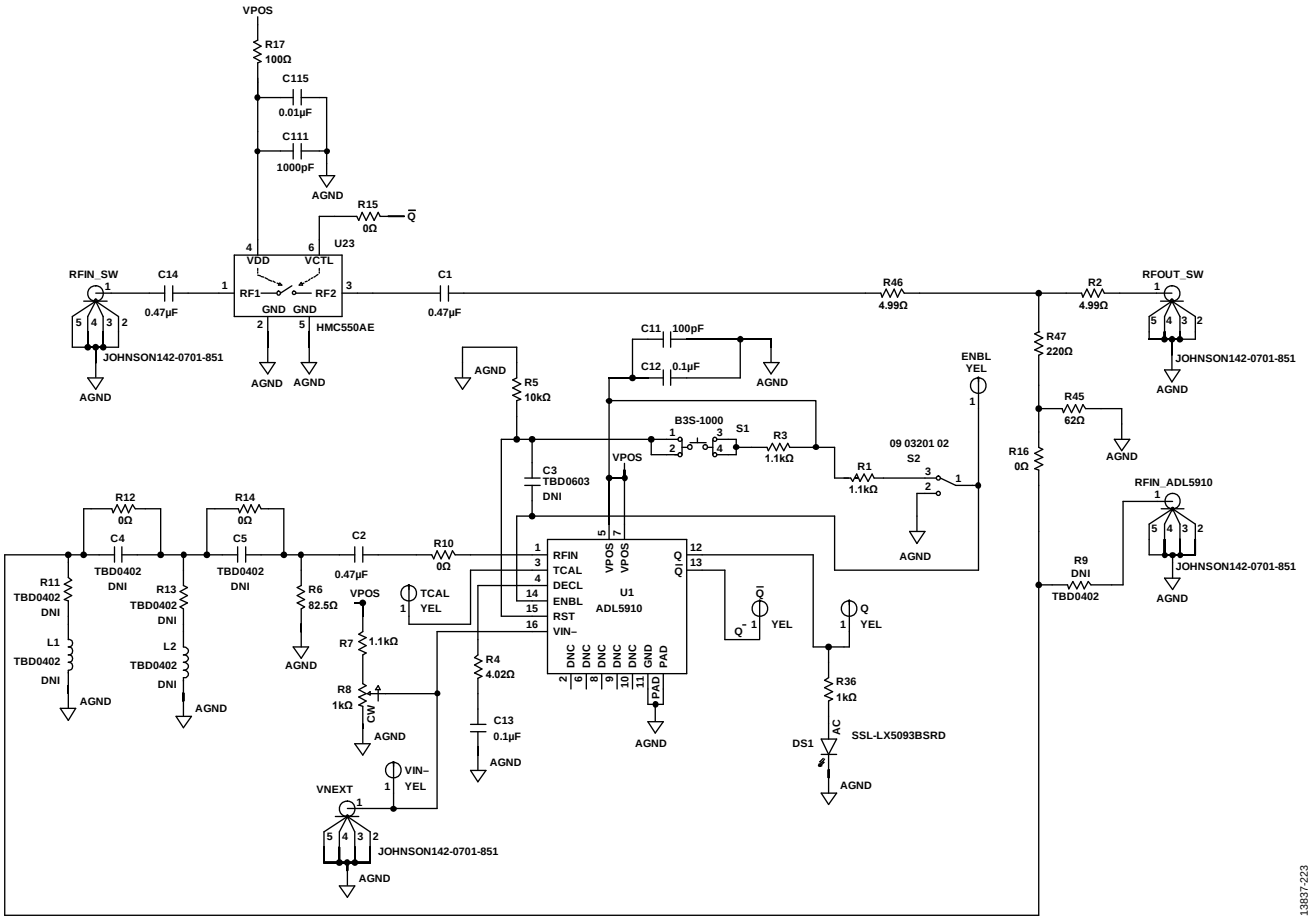


Figure 23. Evaluation Board Schematic

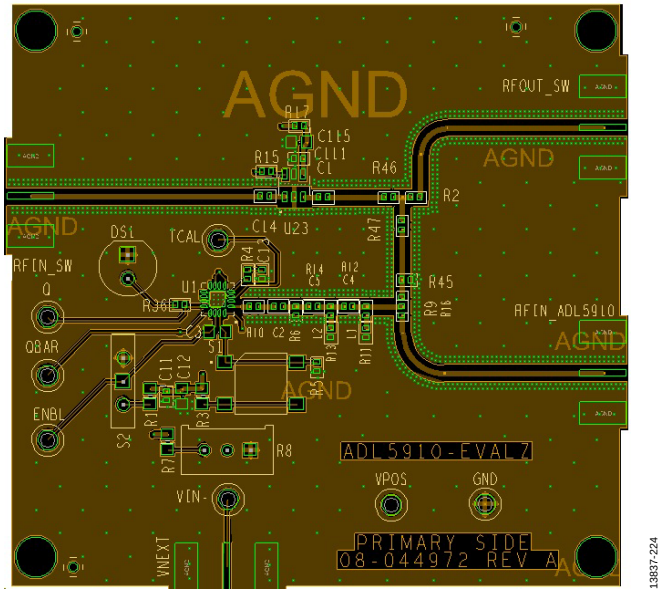


Figure 24. Evaluation Board Layout

Table 6. Evaluation Board Configuration Options

Component	Function	Notes	Default Values[1]
RFIN_SW, RFOUT_SW, R2, R45, R46, R47	RF switch path	To operate the full input protection circuit, route the input signal through the RFIN_SW and RFOUT_SW SMA connectors. The values of the R46, R2, R47, and R45 resistors determine the coupling factor (20 dB) and insertion loss of the asymmetrical splitter/coupler.	R2, R46 = 4.99 Ω (0402), R45 = 62 Ω (0402), R47 = 220 Ω (0402)
RFIN_ADL5910, R9, R16	RF input	To drive the ADL5910 directly and bypass the coupler/switch circuit, apply the RF input signal to the RFIN_ADL5910 SMA. To operate in this mode, remove R16 and place a 0 Ω resistor on R9.	R9 = open/DNI (0402), R16 = 0 Ω (0402)
R6, R10 to R14, C2, C4, C5, L1, L2	Input preemphasis and termination network	The resistance on R6 combines with the internal impedance to provide a broad 50 Ω input match. C2 provides ac coupling between R6 and the RF inpu.t (The RF input of the ADL5910 is internally dc-coupled.) A broadband 50 Ω match is achieved using 82.5 Ω on R6 and a 0.47 µF ac coupling capacitor on C2. A pre-emphasis network can be implemented by placing capacitors and inductors on the pads to the left of R6.	R6 = 82.5 Ω, R10 = 0 Ω (0402) R11, R13 = open/DNI (0402), R12, R14 = 0 Ω (0402), C2 = 0.47 µF, C4, C5 = open/DNI (0402), L1, L2 = open/DNI (0402)
TCAL, R7, R8, VNEXT, VIN–	VCAL threshold calibration	The output voltage from the threshold calibration pin (VCAL, Pin 3) is available on the yellow TCAL clip lead. Use the voltage on this pin to determine the correct threshold voltage that must be applied to Pin 16 (VIN–) to set a particular RF power threshold. This process includes two steps. First, measure the output voltage on the TCAL yellow clip lead with no RF signal applied to RFIN (this voltage is approximately 750 mV). Second, apply the RF input power to RFIN, which causes the circuit to trip, and again measure the voltage on the TCAL yellow clip lead. The difference between these two voltages is equal to the voltage that must be applied to VIN– during operation. This voltage can be applied either to the VNEXT SMA connector or to the VIN– yellow clip lead. This voltage can also be set by the R8 mechanical potentiometer on the board.	R7 = 1.1 kΩ (0603), R8 = 1 kΩ (mechanical potentiometer)

Component	Function	Notes	Default Values[1]
VPOS, GND, C11, C12	Power supply interface	Apply the 3.3 V power supply for the evaluation board to the VPOS (red) and GND (black) test loops. The nominal supply decoupling consists of a 100 pF capacitor and a 0.1 µF capacitor, with the 100 pF capacitor placed closest to the VPOS pin (Pin 5).	C12 = 0.1 µF (0402), C11 = 100 pF (0402), VPOS = 3.3 V
Q, $\overline{Q}$, R36, DS1	Threshold detect output (Q and $\overline{Q}$)	The threshold detect flip flop outputs (Q and $\overline{Q}$) are available on the Q and $\overline{Q}$ yellow test loops. The Q output drives the DS1 flashing LED.	R36 = 1 kΩ
ENBL, S2, R1	Enable interface	Apply 3.3 V to the ENBL yellow test loop or assert the S2 switch, to enable the ADL5910. The enable voltage must be equal to but not greater than the 3.3 V supply voltage. R1 provides current limiting in case a voltage is connected to the ENBL test loop when Switch S2 is in Position 3.	R1 = 1.1 kΩ (0603)
S1 push-button switch, R3, R5, C3	Threshold detect reset	The threshold detection flip flop is reset by using the RST push button switch. The RST switch is connected to the VPOS supply voltage through a 1.1 kΩ resistor (R3). A 10 kΩ pull-down resistor (R5) is connected to the RST pin, which pulls RST low in the absence of any other stimulus. The ADL5910 normally powers up with the Q and $\overline{Q}$ outputs high and low, respectively. To implement a reset on the power-up circuit, install a capacitor (C3). When ENBL is asserted, RST goes high shortly before being pulled back low by R5.	R3 = 1.1 kΩ (0603), R5 = 10 kΩ (0603), C3 = open/DNI (0603)
R4, C13	Decoupling network for the DECL pin	Resistor R4 and Capacitor C13 provide decoupling for the DECL pin of the ADL5910.	R4 = 4.02 Ω (0402), C13 = 0.1 µF (0402)

[1] DNI means do not install.

OUTLINE DIMENSIONS

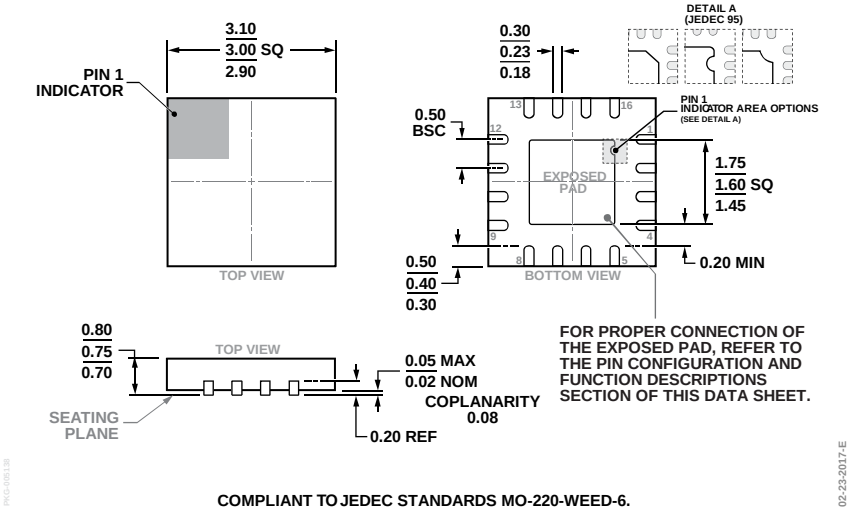


Figure 25. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5910ACPZN-R7	−40°C to +105°C	16-Lead LFCSP, 7″ Tape and Reel	CP-16-22	Q28	3000
ADL5910-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

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