700 MHz to 2700 MHz 1 W RF Driver Amplifier

Data Sheet

ADL5604

FEATURES

Operation from 700 MHz to 2700 MHz
Gain of 12.2 dB at 2630 MHz
OIP3 of 42.2 dBm at 2630 MHz
P1dB of 29.1 dBm at 2630 MHz
Noise figure of 4.6 dB at 2630 MHz
Single 5 V power supply
Low quiescent current of 318 mA
Internal active biasing
Fast power-down/up time of 50 ns
Easily externally matched
Compact 4 mm × 4 mm LFCSP
ESD rating of ±1 kV (Class 1C)

FUNCTIONAL BLOCK DIAGRAM

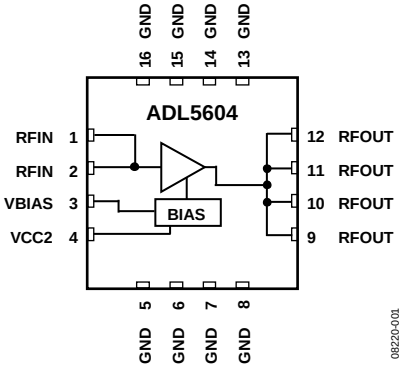


Figure 1.

GENERAL DESCRIPTION

The ADL5604 is a very broadband RF driver amplifier that operates over the wide frequency range of 700 MHz to 2700 MHz. The ADL5604 is also highly linear and has a very low power consumption, enabling the driver to be packaged in a compact 16-lead, 4 mm × 4 mm LFCSP.

For thermal management, the ADL5604 uses an exposed paddle, and the upper and lower pins of the package are all grounded, which gives the ADL5604 excellent thermal transfer characteristics.

The ADL5604 can be quickly powered down or up in 50 ns for applications requiring TX shutdown, such as TDD systems.

The ADL5604 operates on a single 5 V supply voltage and draws only 318 mA of supply current.

The driver is fabricated on a GaAs HBT process and operates from −40°C to +85°C. A fully populated evaluation board is available.

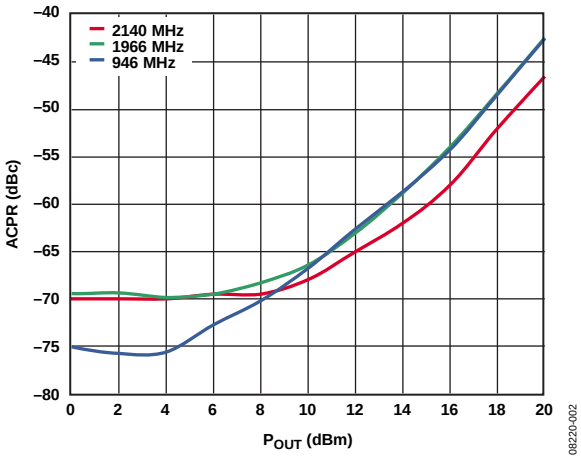


Figure 2. ACPR vs. Output Power, 3GPP 3.5 TM1-64

Rev. C **Document Feedback**
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REVISION HISTORY

8/2017—Rev. B to Rev. C

Changed CP-16-4 to CP-16-23 ... Throughout
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

9/2013—Rev. A to Rev. B

Added Figure 33; Renumbered Sequentially ... 13
Updated Outline Dimensions ... 23

2/2011—Rev. 0 to Rev. A

Changes to Figure 29, Figure 30, Figure 31 ... 13
Changed L2 Value at 880 MHz to 2.4 nH, Table 6 ... 16
Changes to Figure 41 ... 18
Changes to ACPR and EVM Section ... 19

4/2010—Revision 0: Initial Version

SPECIFICATIONS

VCC1[1] = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		700		2700	MHz
FREQUENCY = 748 MHz					
Gain[2]			15.3		dB
vs. Frequency	±20 MHz		0.38		dB
Output 1 dB Compression Point			29.1		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14 dBm per tone		42.8		dBm
Noise Figure			8.5		dB
FREQUENCY = 881 MHz					
Gain[2]			20.3		dB
vs. Frequency	±13 MHz		0.35		dB
Output 1 dB Compression Point			28.8		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14 dBm per tone		42.2		dBm
Noise Figure			4.5		dB
FREQUENCY = 942 MHz					
Gain[2]		19.8	20.5	21.3	dB
vs. Frequency	±18 MHz		±0.1		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.6		dB
vs. Supply	4.75 V to 5.25 V		±0.03		dB
Output 1 dB Compression Point			28.3		dBm
ACP	P_{OUT} =15 dBm, 3GPP 3.5 TM1-64, frequency = 946 MHz		−56		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14 dBm per tone		41.2		dBm
Noise Figure			3.8		dB
FREQUENCY = 1960 MHz					
Gain[2]		13.7	14.4	15.2	dB
vs. Frequency	±30 MHz		±0.2		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.7		dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Output 1 dB Compression Point			28.8		dBm
ACP	P_{OUT} =15 dBm, 3GPP 3.5 TM1-64, frequency = 1966 MHz		−57		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14 dBm per tone		42.1		dBm
Noise Figure			3.6		dB
FREQUENCY = 2140 MHz					
Gain[2]		13.2	14.0	14.9	dB
vs. Frequency	±30 MHz		±0.1		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.6		dB
vs. Supply	4.75 V to 5.25 V		±0.03		dB
Output 1 dB Compression Point			28.6		dBm
ACP	P_{OUT} =15 dBm, 3GPP 3.5 TM1-64		−60		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14 dBm per tone		42.1		dBm
Noise Figure			3.8		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY = 2630 MHz					
Gain[2]			12.2		dB
vs. Frequency	±60 MHz		4.8		dB
Output 1 dB Compression Point			29.1		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14 dBm per tone		42.2		dBm
Noise Figure			4.6		dB
POWER INTERFACE	Pin RFOUT				
Supply Voltage		4.75	5	5.25	V
Supply Current			318	345	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±7		mA
POWER DOWN INTERFACE					
Turn-On Time	50% of control pulse to 50% of RFOUT		50		ns
Turn-Off Time	50% of control pulse to 50% of RFOUT		50		ns

[1] VCC1 is the supply voltage to the ADL5604 through the RFOUT pins.
[2] Guaranteed maximum and minimum specified limits on this parameter are based on 6 sigma calculations.

TYPICAL SCATTERING PARAMETERS

VCC1[1] = 5 V and T_A = 25°C; the effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

Frequency (MHz)	S11		S21		S12		S22	
	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
50	−0.74	−177.7	21.45	134.7	−39.97	10.6	−2.71	−153.2
100	−0.67	−179.4	19.30	134.8	−39.81	6.4	−2.34	−163.2
150	−0.63	179.6	18.18	129.6	−39.69	4.9	−1.93	−167.2
200	−0.59	178.7	17.10	123.5	−39.55	4.0	−1.61	−170.3
250	−0.56	177.9	16.08	117.8	−39.47	3.2	−1.39	−172.9
300	−0.54	177.0	15.12	112.6	−39.53	2.8	−1.26	−175.3
350	−0.53	176.2	14.18	108.2	−39.29	3.4	−1.19	−177.3
400	−0.52	175.4	13.30	104.5	−39.05	1.6	−1.14	−179.0
450	−0.50	174.7	12.51	101.2	−39.02	−1.6	−1.11	179.5
500	−0.50	173.9	11.77	98.3	−39.24	0.3	−1.09	178.0
550	−0.49	173.1	11.09	95.6	−39.27	0.3	−1.10	176.6
600	−0.49	172.4	10.46	93.2	−38.98	0.5	−1.12	175.4
650	−0.48	171.6	9.89	90.9	−38.95	−0.7	−1.11	174.2
700	−0.49	170.8	9.35	88.7	−38.90	−0.5	−1.13	173.0
750	−0.49	170.0	8.85	86.7	−38.78	−1.0	−1.15	172.0
800	−0.49	169.3	8.39	84.7	−38.65	−1.5	−1.18	171.0
850	−0.50	168.5	7.95	82.8	−38.58	−2.3	−1.21	170.0
900	−0.50	167.8	7.55	81.0	−38.51	−2.8	−1.23	169.1
950	−0.51	167.0	7.16	79.2	−38.44	−3.4	−1.27	168.2
1000	−0.51	166.3	6.81	77.5	−38.34	−4.1	−1.28	167.3
1050	−0.52	165.6	6.47	75.8	−38.26	−4.5	−1.32	166.3
1100	−0.53	164.8	6.15	74.0	−38.20	−5.0	−1.35	165.4
1150	−0.54	164.1	5.85	72.4	−38.14	−5.6	−1.39	164.6
1200	−0.55	163.3	5.57	70.8	−38.00	−6.2	−1.43	163.7
1250	−0.56	162.6	5.29	69.2	−37.97	−7.3	−1.47	162.8
1300	−0.57	161.9	5.05	67.7	−37.87	−7.3	−1.50	162.0
1350	−0.58	161.2	4.80	66.1	−37.87	−8.1	−1.55	161.2
1400	−0.59	160.5	4.60	64.6	−37.69	−8.2	−1.57	160.4
1450	−0.59	159.7	4.40	63.0	−37.55	−9.4	−1.60	159.5
1500	−0.60	158.9	4.21	61.4	−37.45	−10.1	−1.64	158.5
1550	−0.61	158.2	4.03	59.9	−37.33	−10.7	−1.68	157.7
1600	−0.63	157.4	3.86	58.2	−37.20	−11.9	−1.74	156.8
1650	−0.64	156.7	3.70	56.7	−37.15	−12.8	−1.78	156.0
1700	−0.65	155.9	3.55	55.1	−37.09	−13.7	−1.82	155.1
1750	−0.67	155.2	3.41	53.6	−36.97	−14.3	−1.88	154.4
1800	−0.68	154.4	3.29	51.9	−36.86	−15.2	−1.92	153.3
1850	−0.69	153.6	3.17	50.3	−36.75	−16.1	−1.97	152.3
1900	−0.70	152.8	3.06	48.6	−36.65	−17.0	−2.02	151.4
1950	−0.72	152.1	2.96	47.0	−36.54	−18.1	−2.10	150.6
2000	−0.73	151.3	2.86	45.3	−36.42	−19.0	−2.17	149.5
2050	−0.75	150.5	2.77	43.7	−36.30	−20.1	−2.23	148.7
2100	−0.77	149.7	2.70	42.0	−36.19	−21.2	−2.31	147.8
2150	−0.78	148.9	2.62	40.4	−36.08	−22.2	−2.40	146.8
2200	−0.80	148.1	2.57	38.7	−35.95	−23.3	−2.45	145.8
2250	−0.82	147.3	2.52	37.0	−35.83	−24.5	−2.51	144.9
2300	−0.84	146.5	2.48	35.1	−35.70	−25.7	−2.61	143.9
2350	−0.86	145.7	2.44	33.4	−35.58	−26.9	−2.72	142.8
2400	−0.88	144.9	2.40	31.5	−35.46	−28.4	−2.81	141.7

Frequency (MHz)	S11		S21		S12		S22	
	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
2450	−0.90	144.1	2.37	29.7	−35.34	−29.8	−2.91	140.8
2500	−0.92	143.2	2.35	27.8	−35.21	−31.0	−3.03	139.7
2550	−0.94	142.4	2.33	26.0	−35.08	−32.5	−3.15	138.7
2600	−0.96	141.6	2.32	24.0	−34.96	−34.0	−3.26	137.7
2650	−0.99	140.8	2.32	22.1	−34.83	−35.5	−3.38	136.7
2700	−1.01	139.9	2.32	20.1	−34.71	−37.2	−3.52	135.6
2750	−1.04	139.1	2.33	18.0	−34.58	−38.8	−3.66	134.4
2800	−1.07	138.3	2.34	15.9	−34.45	−40.5	−3.81	133.3
2850	−1.10	137.4	2.36	13.9	−34.31	−42.2	−3.99	132.3
2900	−1.13	136.6	2.37	11.7	−34.18	−44.1	−4.16	131.1
2950	−1.16	135.7	2.39	9.5	−34.05	−45.9	−4.34	130.1
3000	−1.19	134.9	2.42	7.3	−33.94	−47.9	−4.54	129.0
3050	−1.22	134.1	2.45	5.1	−33.81	−49.9	−4.75	127.9
3100	−1.25	133.2	2.48	2.8	−33.69	−51.9	−4.96	126.9
3150	−1.29	132.4	2.52	0.4	−33.55	−54.0	−5.20	125.8
3200	−1.32	131.5	2.55	−2.0	−33.44	−56.3	−5.45	124.8
3250	−1.36	130.7	2.59	−4.4	−33.32	−58.5	−5.71	123.8
3300	−1.40	129.8	2.63	−6.9	−33.21	−60.8	−5.99	122.7
3350	−1.44	129.0	2.67	−9.4	−33.10	−63.2	−6.29	121.8
3400	−1.47	128.1	2.72	−12.0	−32.98	−65.6	−6.62	120.9
3450	−1.51	127.3	2.76	−14.7	−32.86	−68.0	−6.96	120.0
3500	−1.55	126.4	2.80	−17.3	−32.73	−70.7	−7.31	119.4
3550	−1.59	125.6	2.84	−20.0	−32.61	−73.3	−7.71	118.8
3600	−1.63	124.8	2.89	−22.7	−32.51	−76.1	−8.12	118.2
3650	−1.67	124.0	2.93	−25.5	−32.39	−79.0	−8.57	117.7
3700	−1.71	123.2	2.97	−28.4	−32.28	−82.0	−9.02	117.5
3750	−1.75	122.3	3.01	−31.2	−32.18	−85.1	−9.54	117.6
3800	−1.79	121.5	3.05	−34.1	−32.10	−88.3	−10.09	117.7
3850	−1.82	120.7	3.09	−37.1	−32.02	−91.5	−10.63	118.4
3900	−1.84	119.9	3.13	−40.0	−31.94	−94.8	−11.24	119.5
3950	−1.86	119.1	3.17	−43.0	−31.85	−98.2	−11.86	120.9
4000	−1.88	118.3	3.22	−46.1	−31.79	−101.7	−12.48	123.2

[1] VCC1 is the supply to the ADL5604 through the RFOUT pins.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VSUP	6.5 V
Input Power (50 Ω Impedance)	+25 dBm
Internal Power Dissipation (Paddle Soldered)	3.9 W
θ_{JA} (Junction to Air)	32.1°C/W
θ_{JC} (Junction to Paddle)	6°C/W
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 60 sec)	240°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

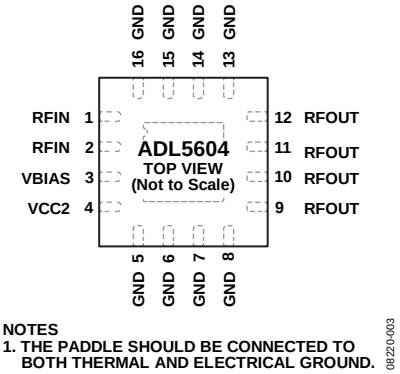


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	RFIN	RF Input. Requires a dc blocking capacitor.
5, 6, 7, 8, 13,14, 15, 16	GND	Solder to a low impedance electrical and thermal ground plane.
3	VBIAS	Dual Function Pin. Applying 5 V to this pin enables the bias circuit. Grounding this pin disables the device. When VBIAS is used alone to disable the ADL5604, the disable current is 13 mA.
4	VCC2	Under normal operation, this pin is connected to the power supply and draws approximately 5 mA of current. This pin can be grounded with the VBIAS pin to allow a disable current of <1 µA.
9, 10, 11, 12	RFOUT	RF Output and Main Supply Voltage. DC bias is provided to this pin through an inductor that is connected to the 5 V power supply. The RF path requires a dc blocking capacitor.
	EP	The exposed paddle is connected internally to ground. Solder to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

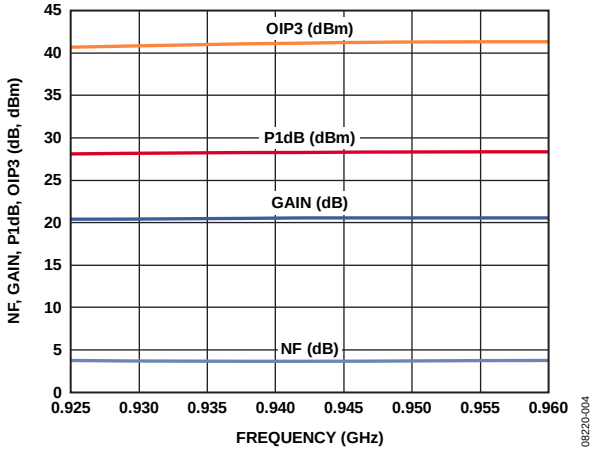


Figure 4. Gain, P1dB, OIP3 at P_{OUT} =14 dBm/Tone and Noise Figure vs. Frequency

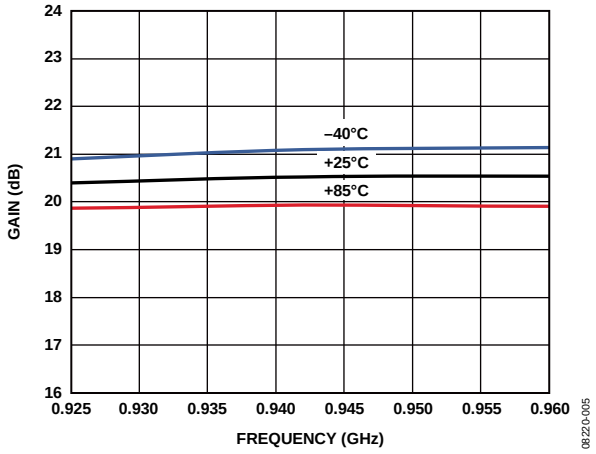


Figure 5. Gain vs. Frequency and Temperature

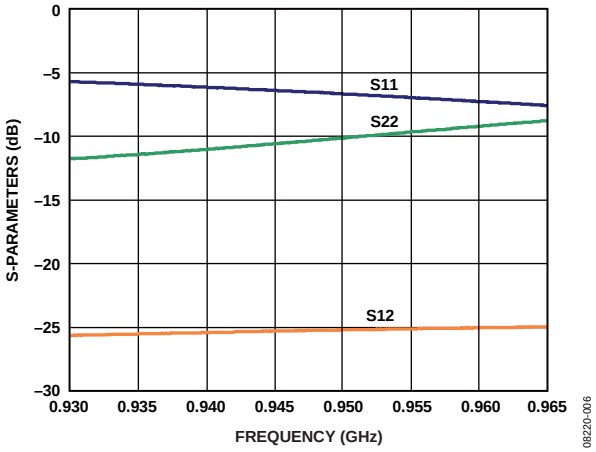


Figure 6. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

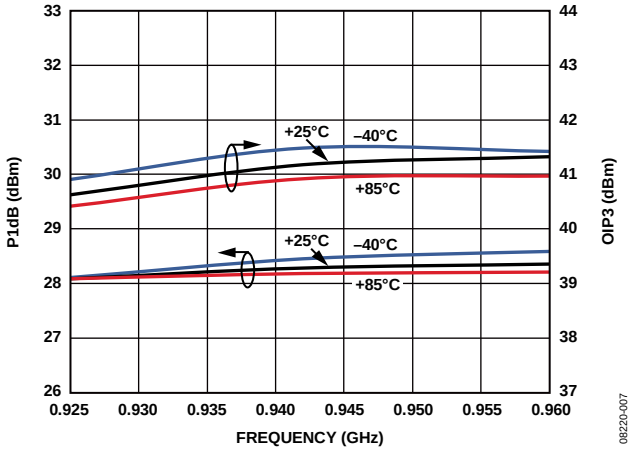


Figure 7. OIP3 at P_{OUT} =14 dBm/Tone and P1dB vs. Frequency and Temperature

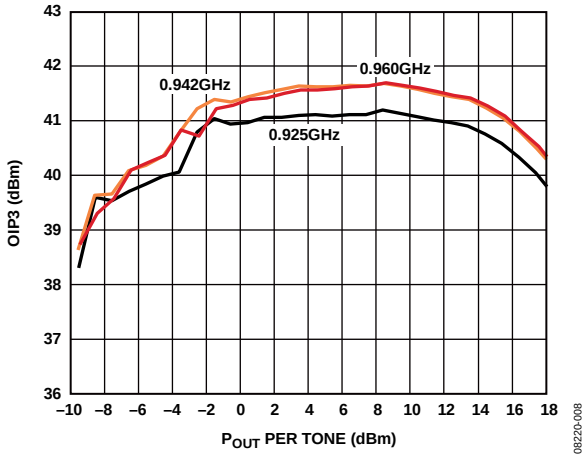


Figure 8. OIP3 vs. P_{OUT} and Frequency

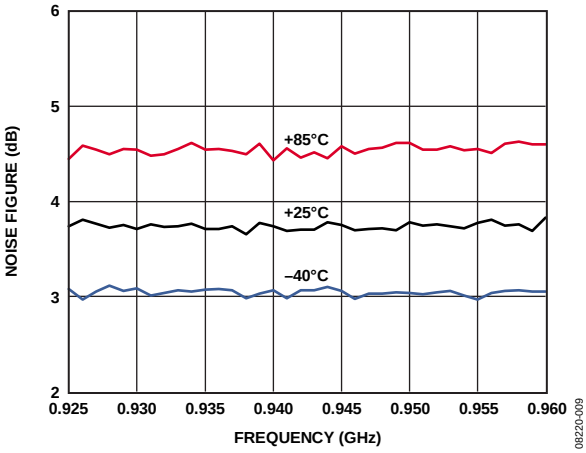


Figure 9. Noise Figure vs. Frequency and Temperature

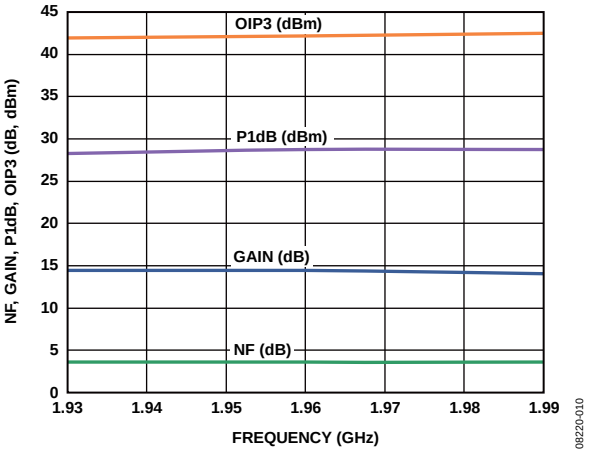


Figure 10. Gain, P1dB, OIP3 at P_{OUT} =14 dBm/Tone and Noise Figure vs. Frequency

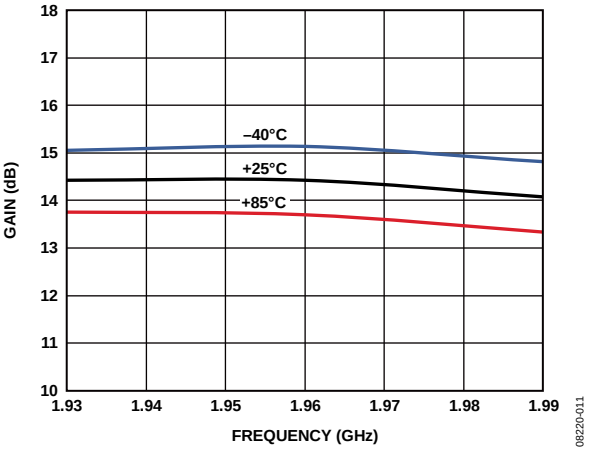


Figure 11. Gain vs. Frequency and Temperature

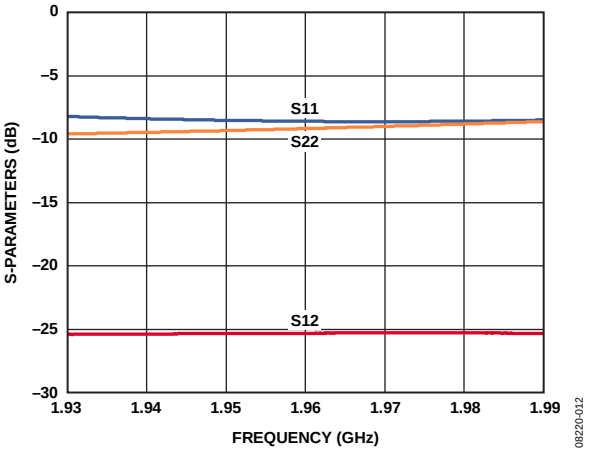


Figure 12. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

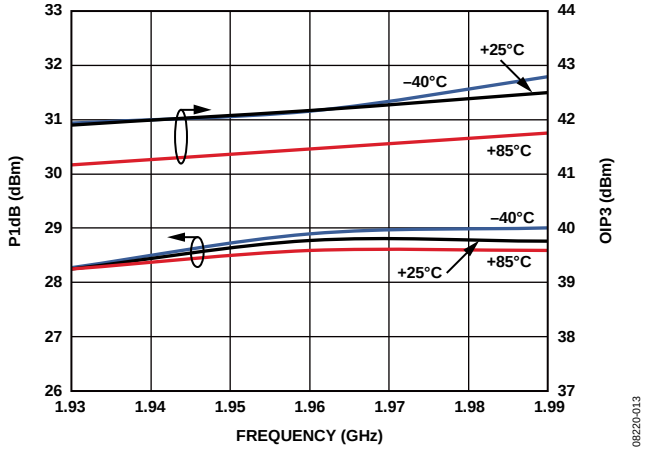


Figure 13. OIP3 at P_{OUT} =14 dBm/Tone and P1dB vs. Frequency and Temperature

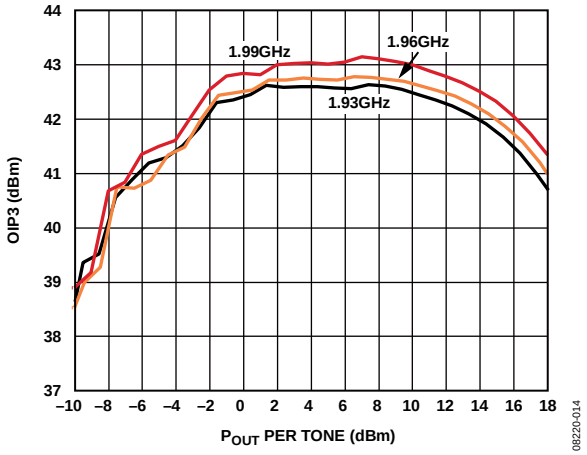


Figure 14. OIP3 vs. P_{OUT} and Frequency

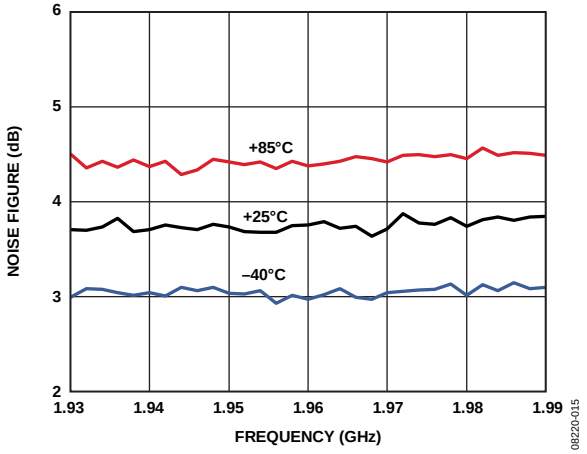


Figure 15. Noise Figure vs. Frequency and Temperature

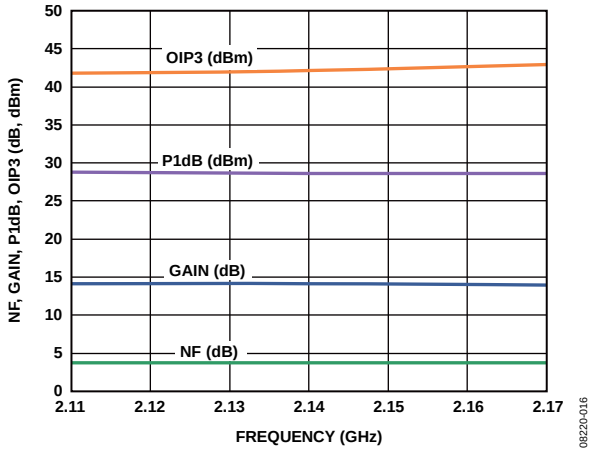


Figure 16. Gain, P1dB, OIP3 at P_{OUT} =14 dBm/Tone and Noise Figure vs. Frequency

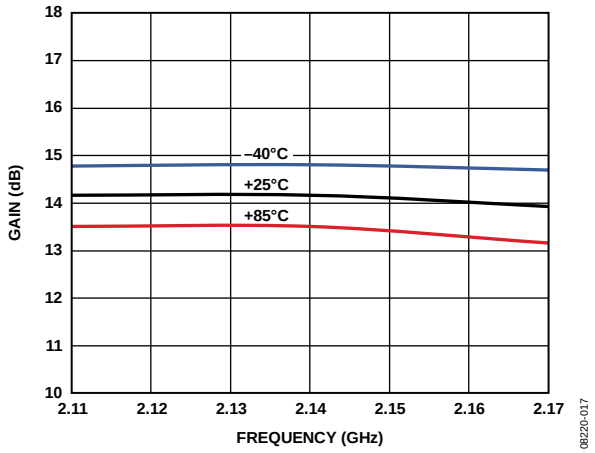


Figure 17. Gain vs. Frequency and Temperature

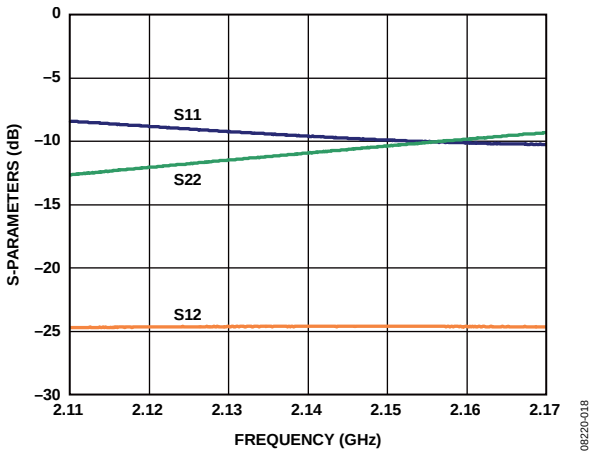


Figure 18. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

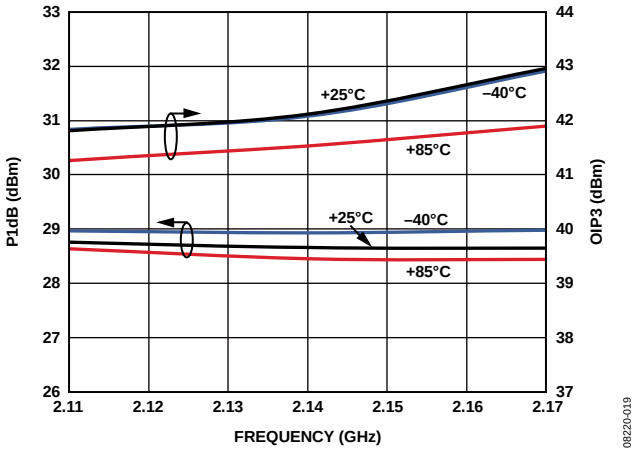


Figure 19. OIP3 at P_{OUT} =14 dBm/Tone and P1dB vs. Frequency and Temperature

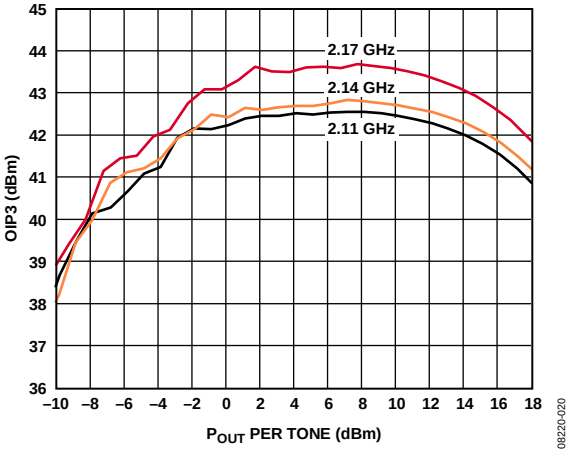


Figure 20. OIP3 vs. P_{OUT} and Frequency

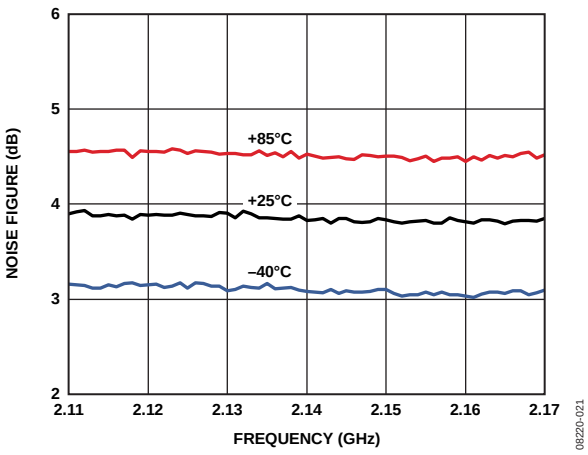


Figure 21. Noise Figure vs. Frequency and Temperature

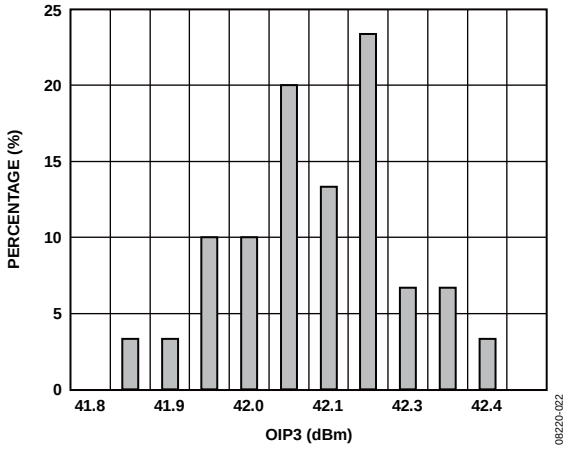


Figure 22. OIP3 Distribution at 2140 MHz

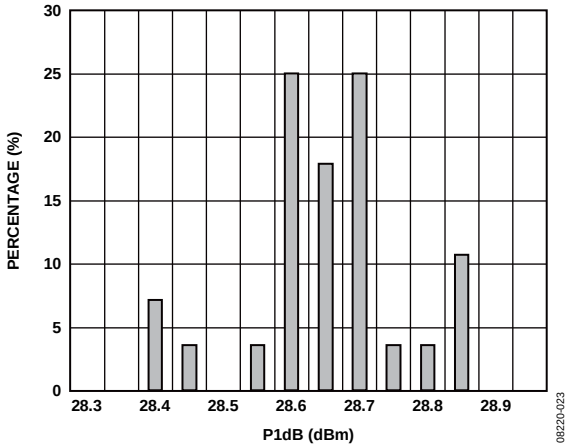


Figure 23. P1dB Distribution at 2140 MHz

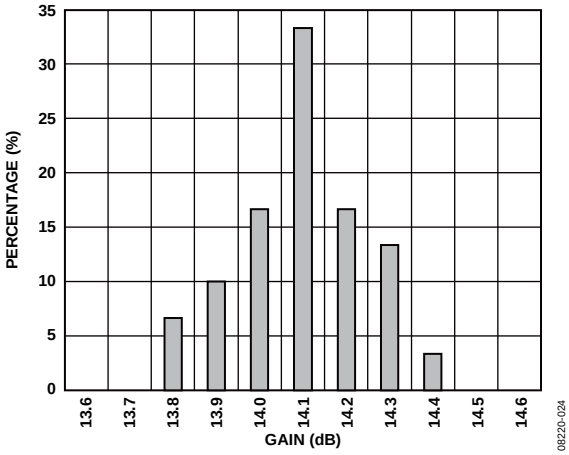


Figure 24. Gain Distribution at 2140 MHz

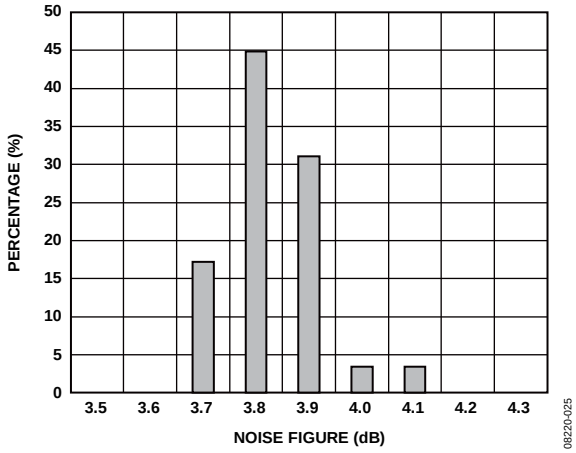


Figure 25. Noise Figure Distribution at 2140 MHz

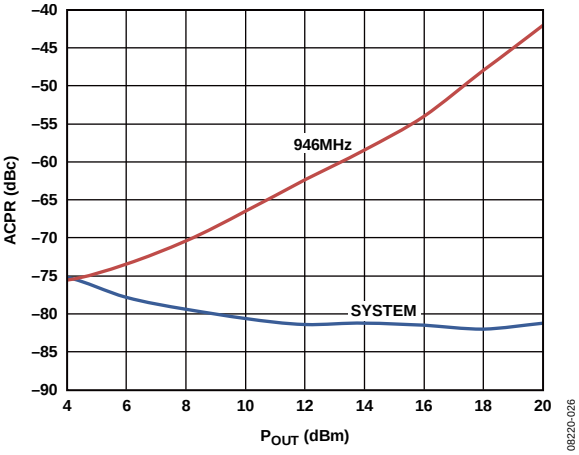


Figure 26. ACPR vs. P_{OUT}, 3GPP 3.5 TM1-64 at 946 MHz

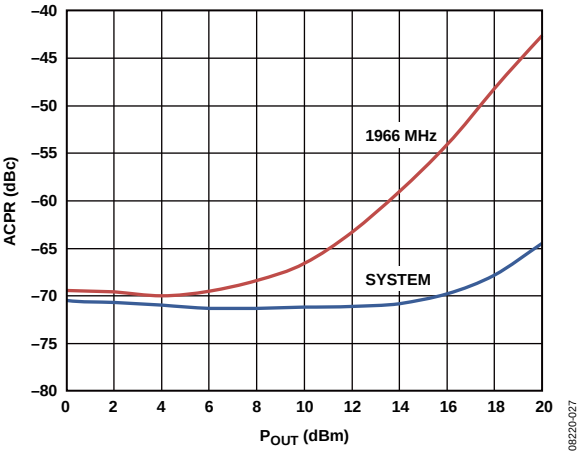


Figure 27. ACPR vs. P_{OUT}, 3GPP 3.5 TM1-64 at 1966 MHz

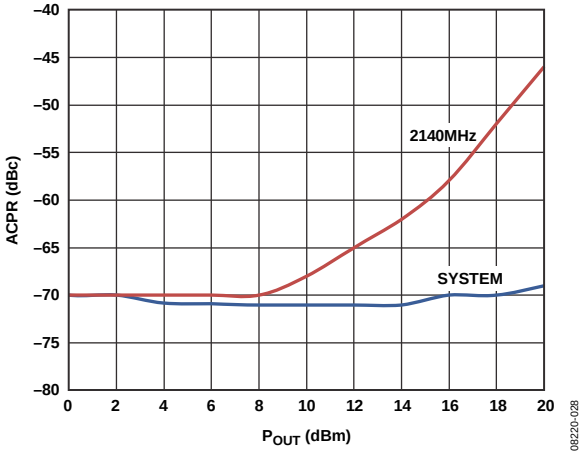


Figure 28. ACPR vs. P_{OUT}, 3GPP 3.5 TM1-64 at 2140 MHz

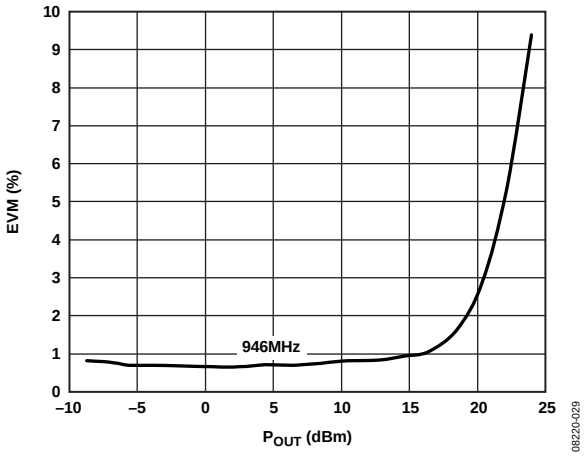


Figure 29. EVM vs. P_{OUT} at 946 MHz

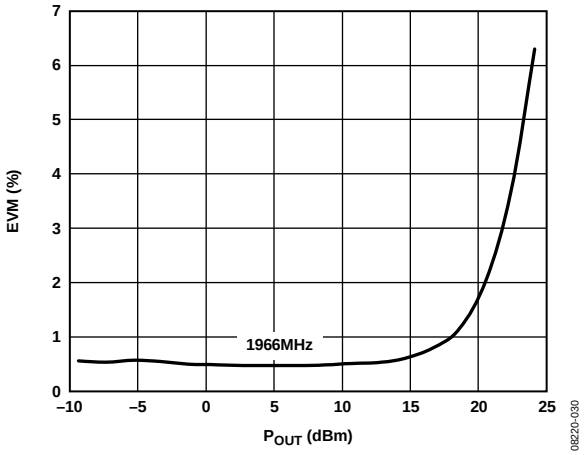


Figure 30. EVM vs. P_{OUT} at1966 MHz

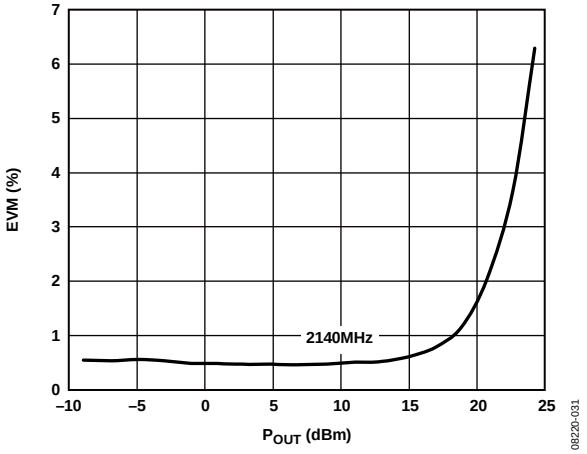


Figure 31. EVM vs. P_{OUT} at 2140 MHz

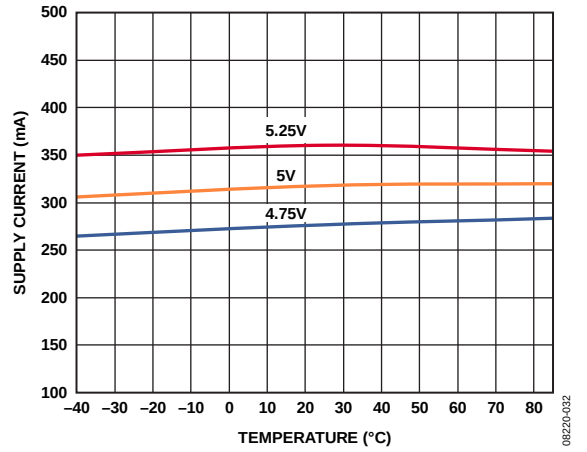


Figure 32. Supply Current vs. Supply Voltage and Temperature at 2140 MHz

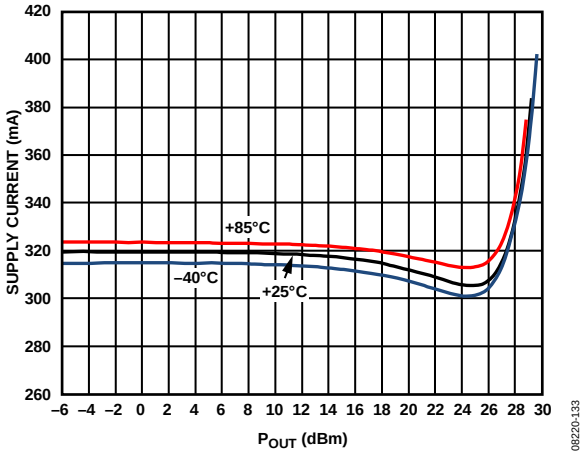


Figure 33. Supply Current vs. P_{OUT} and Temperature, V_{CC} = 5 V at 2140 MHz

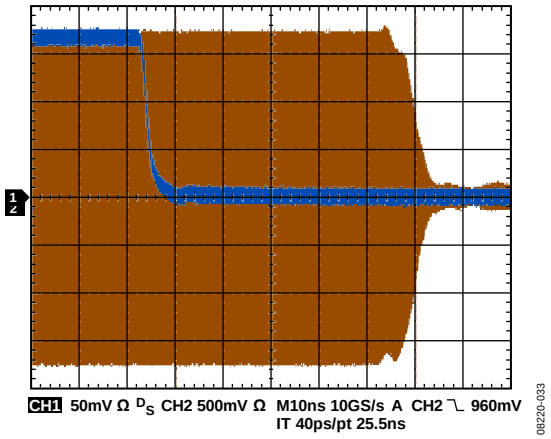


Figure 34. Turn-Off Time, 50% of Control Pulse to 50% of RF Burst

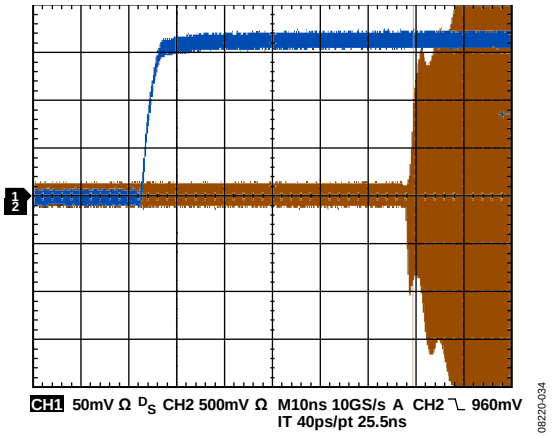


Figure 35. Turn -On Time, 50% of Control Pulse to 50% of RF Burst

APPLICATIONS INFORMATION

BASIC LAYOUT CONNECTIONS

The basic connections for operating the ADL5604 are shown in Figure 36.

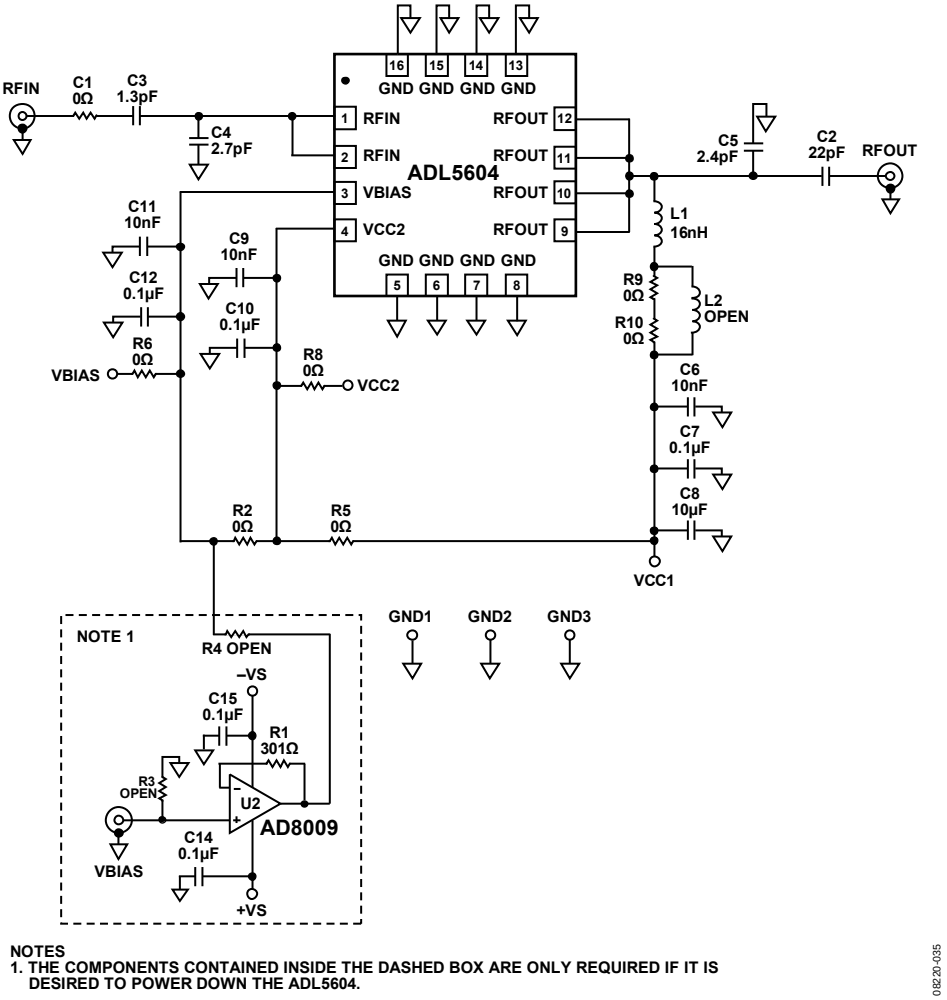


Figure 36. Basic Connections

Power Supply

The voltage supply for the ADL5604, which ranges from 4.75 V to 5.25 V, should be connected to the VCC1 pin. The dc bias to the output stage is supplied through L1 and is connected to the RFOUT pin. Three decoupling capacitors, C6, C7, and C8, are used to prevent RF signals from propagating on the dc lines. The VBIAS and VCC2 pins are connected to the main supply voltage, VCC1, through the R2 and R5 resistors. Additional decoupling capacitors, C9, C10, C11, and C12, are required on the VCC2 and VBIAS pins.

RF Input Interface

Pin 1 and Pin 2 are the RF input pins for ADL5604. The RF input is easily matched with two or three components and a microstrip line used as an inductor. If additional inductance is required, C3 can be replaced with an inductor. See the ADL5604 Match section for the component values and spacing for the different frequency bands.

RF Output Interface

Pin 9 to Pin 12 are used as the RF output pins. The C5 shunt capacitor and the inductance from the microstrip line match RF output to 50 Ω. See the ADL5604 Match section for the component values and spacing for the different frequency bands.

Power-Down Circuit

Device U2 and its associated circuitry can be used to power down the ADL5604. To connect U2, remove the R2 resistor and place a 0 Ω resistor in place of R4.

ADL5604 MATCH

The ADL5604 is easily matched with three matching components and a microstrip line used as inductance. If spacing is tight, an external inductor can take the place of the microstrip line. The output match includes a short (76 mils, including the portion that is used as the pad for the chip) non 50 Ω line to accommodate the four output pins and allow for easier low inductance output matching. The pads for Pin 9 to Pin 12 are included on this microstrip line, as well as the pad for the L1 bias inductor.

The extended length allows the bias inductor to be placed close to the chip, where the impedance is lowest, while allowing a low inductance path to a shunt capacitor to ground. This extra length allows for alternative matching but is also included in the output match at all frequencies. Table 5 and Table 6 detail the component spacing and values for the input and output matching networks for the ADL5604 for the different frequencies. Figure 37 through Figure 42 show the matching networks.

Table 5. Component Spacing

Frequency	λ1 (mils)	λ2 (mils)	λ3 (mils)	λ4 (mils)	λ5 (mils)
748 MHz	67	348	41	272	106
880 MHz	75	138	41	181	154
943 MHz	N/A	118	41	220	95
1960 MHz	35	N/A	41	232	N/A
2140 MHz	45	182	41	197	N/A
2630 MHz	55	182	41	126	N/A

Table 6. Component Values

Frequency	C1 (pF)	C2 (pF)	C3 (pF)	C4 (pF)	C5 (pF)	L1 (nH)	L2 (nH)	Lout (nH)
748 MHz	100 pF	100 pF	10.0 pF	20.0 pF	7.0 pF	16 nH	N/A	2.7 nH
880 MHz	100 pF	100 pF	N/A	9.0 pF	6.0 pF	16 nH	2.4 nH	3.6 nH
943 MHz	100 pF	100 pF	12.0 pF	N/A	6.2 pF	16 nH	N/A	3.0 nH
1960 MHz	22 pF	22 pF	0 Ω	4.3 pF	2.2 pF	16 nH	N/A	N/A
2140 MHz	0 Ω	22 pF	1.3 pF	2.7 pF	2.4 pF	16 nH	N/A	N/A
2630 MHz	22 pF	22 pF	N/A	2.2 pF	1.8 pF	16 nH	4.3 nH	N/A

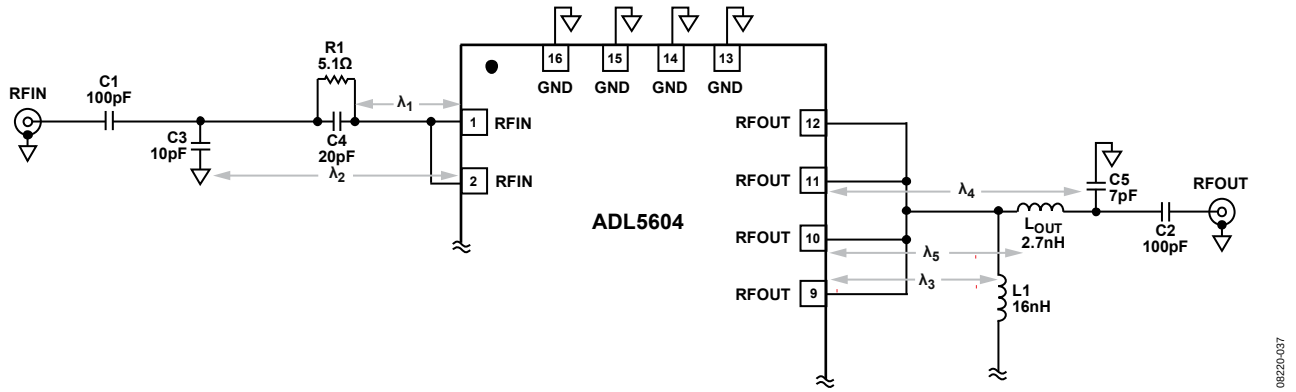


Figure 37. ADL5604 Match Parameters, 748 MHz

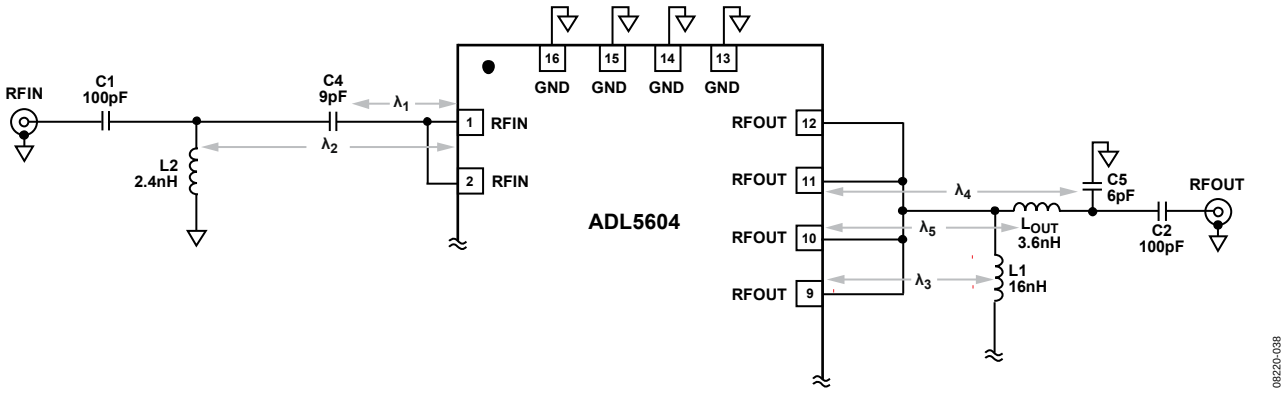


Figure 38. ADL5604 Match Parameters, 880 MHz

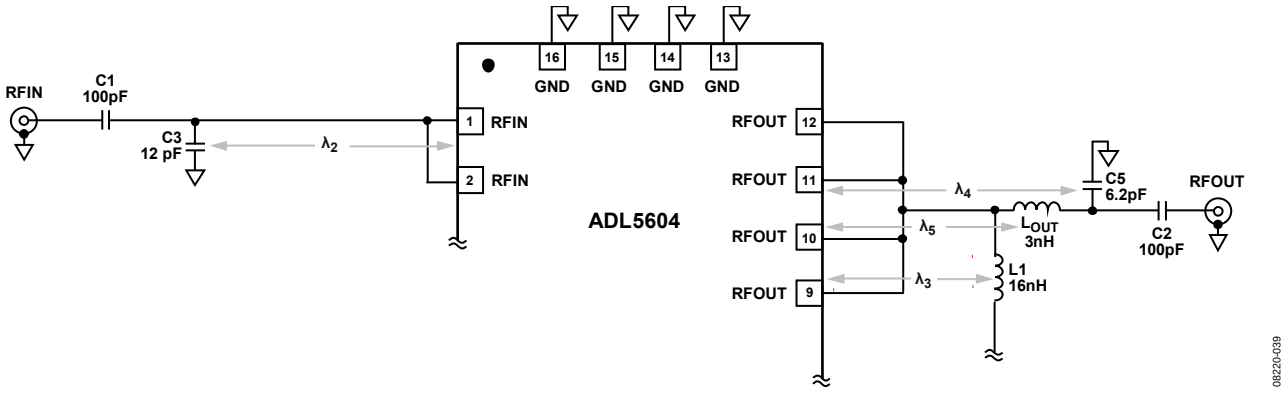


Figure 39. ADL5604 Match Parameters, 943 MHz

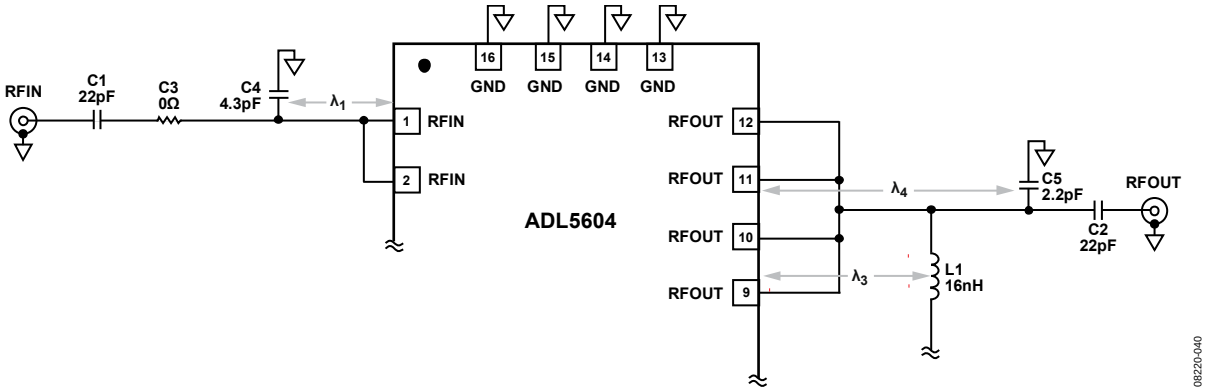


Figure 40. ADL5604 Match Parameters, 1960 MHz

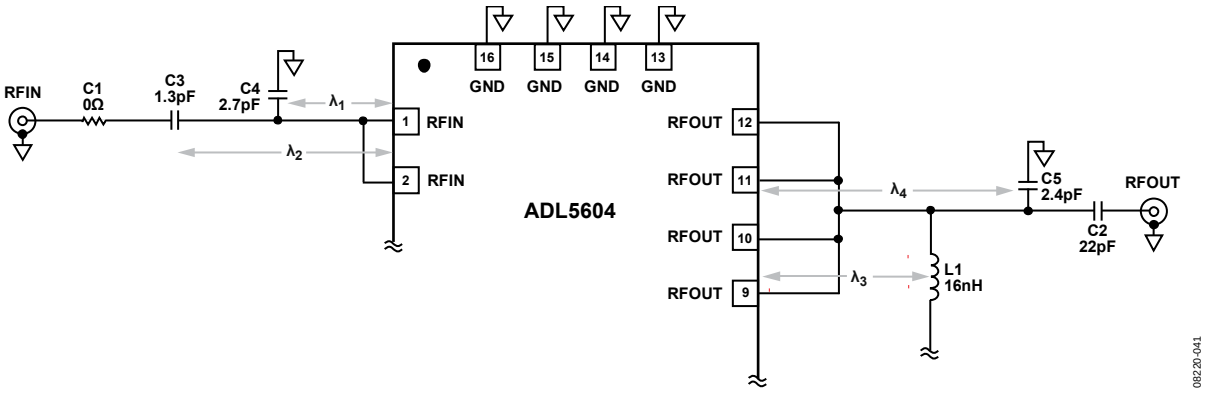


Figure 41. ADL5604 Match Parameters, 2140 MHz

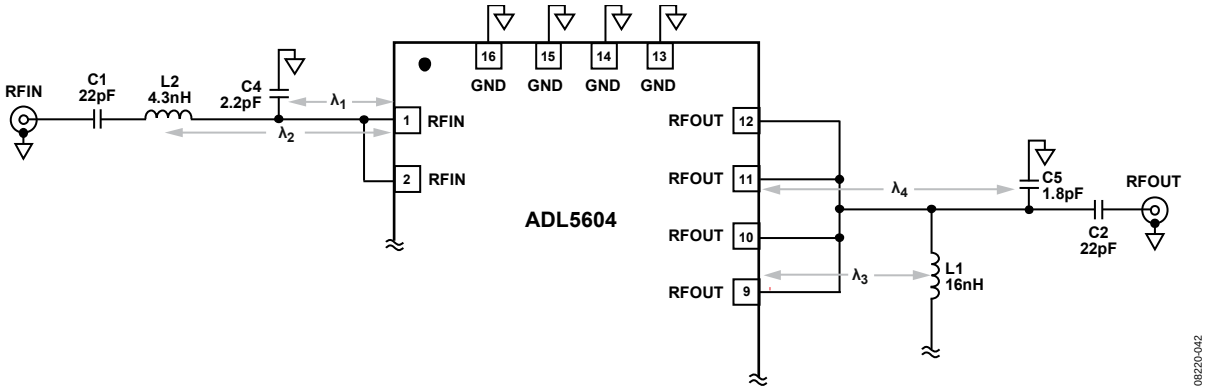


Figure 42. ADL5604 Match Parameters, 2630 MHz

ACPR AND EVM

All adjacent channel power ratio (ACPR) and error vector magnitude (EVM) measurements were made using a single W-CDMA carrier and Test Model 1-64.

The signal is generated by a very low ACPR source and is measured at the output by a high dynamic range spectrum analyzer. For ACPR measurements, the filter setting was chosen for low ACPR and for EVM measurements the low EVM setting was selected. The baseline composite EVM for the signal source used was around 0.5%. Highly linear amplifiers were used to measure ACPR and EVM at higher output power levels.

Figure 26 shows the plot of ACPR vs. P_{OUT} at 946 MHz. Shown on the same plot is the system ACPR. For power levels up to 11 dBm, an ACPR of 65 dBc or better can be achieved. Figure 27 shows the ACPR vs. P_{OUT} at 1966 MHz. Shown on the same plot is the system ACPR. For power levels up to 11 dBm, an ACPR of 65 dBc or better can be achieved.

Figure 28 shows ACPR vs. P_{OUT} at 2140 MHz. Shown on the same plot is the system ACPR. For power levels up to 12 dBm, an ACPR of 65 dBc or better can be achieved. Figure 29 shows the plot of EVM vs. P_{OUT} at 946 MHz. The EVM measured is less than 1% for power levels up to 15 dBm.

Figure 30 shows the EVM vs. P_{OUT} at 1966 MHz. The EVM measured is less than 1% for power levels up to 18 dBm. Figure 31 shows the EVM vs. P_{OUT} at 2140 MHz. The EVM measured is less than 1% for power levels up to 18 dBm.

When operated in the linear region, there is little or no contribution to EVM by the amplifier.

THERMAL CONSIDERATIONS

The ADL5604 is packaged in a thermally efficient 4 mm × 4 mm, 16-lead LFCSP. The thermal resistance from junction to air (θ_{JA}) is 32.1°C/W. The thermal resistance for the product was extracted assuming a standard 4-layer JEDEC board with nine copper filled thermal vias. The thermal resistance from junction to case (θ_{JC}) is 6°C/W where case is the exposed pad of the lead frame package.

For the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LFCSP. The above thermal resistance numbers assume a minimum of nine thermal vias arranged in a 3 × 3 array with a diameter of 8 mils and a pitch of 16 mils. Because the top and bottom leads of the package are ground, the ground pattern on the evaluation board is extended on the top and bottom to improve thermal efficiency (see the Evaluation Board section).

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 43 shows the recommended land pattern for the ADL5604. To minimize thermal impedance, the exposed paddle on the 4 mm × 4 mm LFCSP package is soldered down to a ground plane along with Pin 5 to Pin 8 and Pin 13 to Pin 16. To improve thermal dissipation, nine thermal vias are arranged in a 3 × 3 array under the exposed paddle. Areas above and below the paddle are tied with regular vias. If multiple ground layers exist, they should be tied together using vias. For more information on land pattern design and layout, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

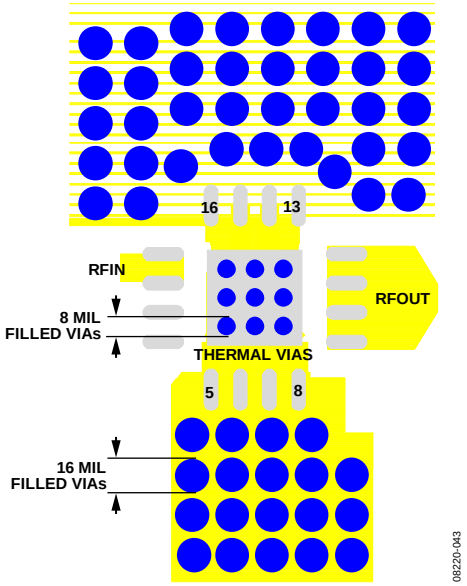


Figure 43. Recommended Land Pattern

EVALUATION BOARD

The schematic of the ADL5604 evaluation board is shown in Figure 44. This evaluation board uses 25 mils wide, 50 Ω traces and is made from IS410 material, with a 23 mils gap to ground. The evaluation board is tuned for operation at 2140 MHz. The inputs and outputs should be ac-coupled with appropriately sized capacitors; therefore, for low frequency applications, C1 and C2 may need to be increased. DC bias is provided to the output stage via an inductor connected to the RFOUT pin. A bias voltage of 5 V is recommended. The evaluation board has a short non 50 Ω line on its output to accommodate the four output pins and allow for easier low inductance output matching. The pads for Pin 9 to Pin 12 are included on this microstrip line and are included in all matches. Figure 47 shows the close-up image of the recommended output pad. The evaluation board also has hash marks close to the input and output of the ADL5604, separated by 40 mils. The hash mark closest to the input is 127 mils from the chip, and the hash mark closest to the output is 20 mils from the chip.

U2 and its associated circuitry are required only if it is desired to power down the ADL5604. On the evaluation board, it is necessary to remove R2 and install a 0 Ω resistor in the R4 position to enable this feature.

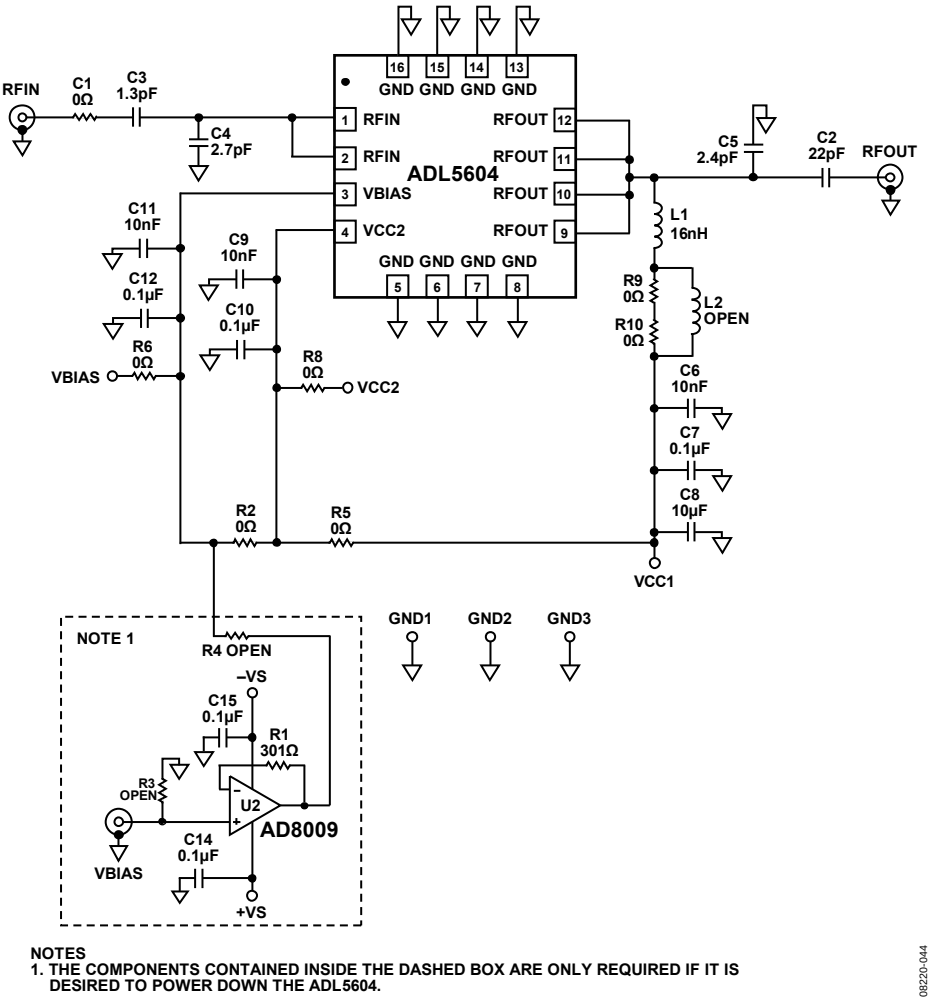


Figure 44. Evaluation Board, 2140 MHz

Table 7. Evaluation Board Configuration Options, 2140 MHz

Component	Function/Notes	Default Value
C1, C2	Input/output dc blocking capacitors at 2140 MHz. C3 provides dc blocking; therefore, a jumper is installed in place of C1.	C1 = 0 Ω, C2 = 22 pF
C3, C4	Input matching capacitors. The input match is set for 2140 MHz but is easily changed for other frequencies. C3 is set at a specific distance from C4 so that the microstrip line can act as inductance for part of the match. If space is at a premium, an inductor can take the place of the microstrip line. The ADL5604 is sensitive to the input match; therefore, the tolerance of these components and their placement must be tight.	C3 = 1.3 pF HQ, C4 = 2.7 pF HQ
C5	Output matching capacitor. The output match is set for 2140 MHz but is easily changed for other frequencies. The tolerance for this capacitor should be tight. C5 is set at a specific distance from the input; therefore, the microstrip line can act as inductance for part of the match. If space is at a premium, an inductor can take the place of the microstrip line. There is a short length of low impedance line on the output that is embedded in the match. The ADL5604 is less sensitive to the output match than the input match, but the tolerance still must be tight.	C5 = 2.4 pF
L1, L2, R9, R10	The main bias for the ADL5604 comes through L1 to its output. L1 should be high impedance for the frequency of operation, while providing low resistance for the dc current. The evaluation board uses a Coilcraft 0603HP-16NX_H inductor. It is a 16 nH inductor, which provides some of the match at 2140 MHz. As the operating frequency gets lower, the inductance must increase, but as the inductance increases, the current is more limited for a 0603 package. R9 and R10 can be removed and L2 added to allow for low frequency operation. L2 has the footprint for a Coilcraft SLC7530D-101MLB (0.4 µH).	L1 = 16 nH, L2 = open, R9 = 0 Ω, R10 = 0 Ω
C6, C7, C8, C9, C10, C11, C12, C14, C15	Power supply decoupling. The need for power supply decoupling capacitance is based on the noise and potential for noise on the power supply. The smallest capacitor should be the closest to the ADL5604. The main bias that goes through RFOUT is the most sensitive to noise because the bias is connected directly to the output.	C6, C9, C11 = 10 nF, C7, C10, C12, C14, C15 = 0.1 µF, C8 = 10 µF
R6, R8	R6 and R8 can be removed to eliminate any parasitic elements of VBIAS and VCC2 if a fast response time is required.	R6 = 0 Ω, R8 = 0 Ω
R2, R4, R5	The ADL5604 can be shut down using VBIAS alone or VBIAS and VCC2. The ADL5604 has a shutdown current of 13 mA when only VBIAS is used. The shutdown current is < 1 µA if VBIAS and VCC2 are used. However, VCC2 draws 5 mA when biased, setting the current drive capability of the shutdown controller. R2, R4, and R5 allow custom configuration of the shutdown.	R2, R5 = 0 Ω, R4 = open
U2, R1, R3	If VCC2 is used to shut down the ADL5604, 5 mA must be sourced when the part is enabled. U2, R1, and R3 are configured as a buffer to source the 5 mA.	U2 = AD8009, R1 = 3.01 Ω, R3 = open
Exposed Paddle	The paddle should be connected to both thermal and electrical ground.	

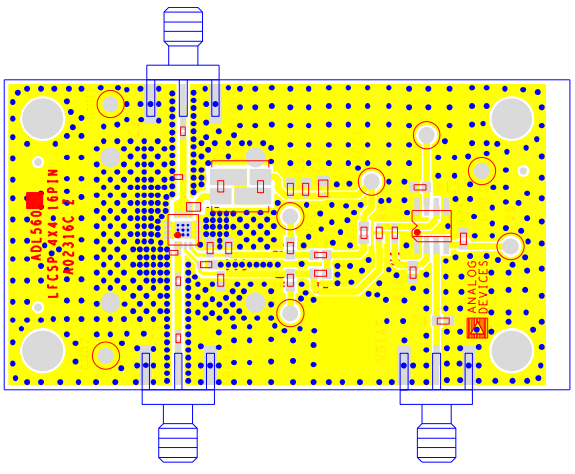


Figure 45. Evaluation Board Layout, Topside

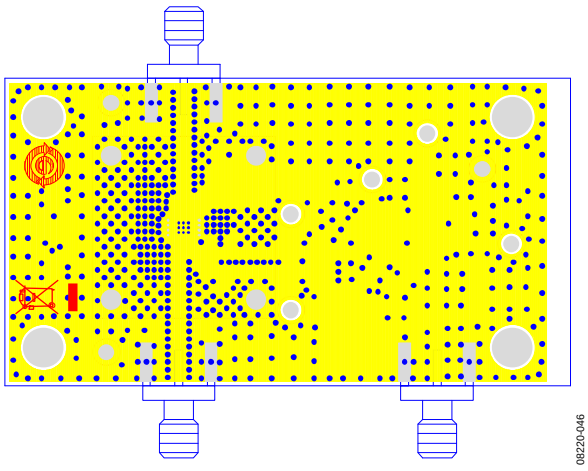


Figure 46. Evaluation Board Layout, Bottom Side

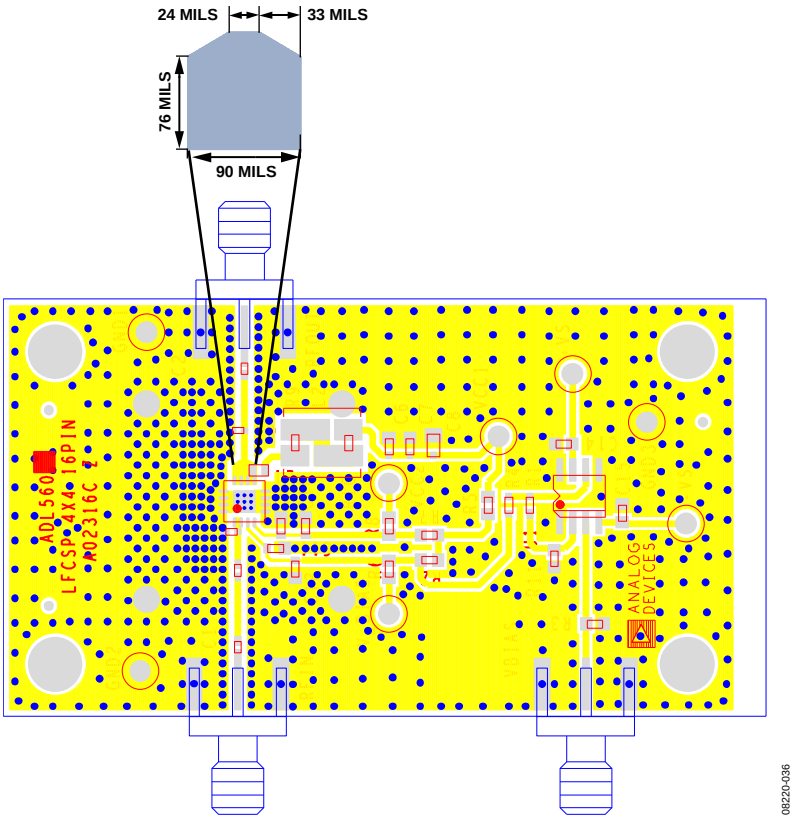


Figure 47. Evaluation Board Layout, Output Pad

OUTLINE DIMENSIONS

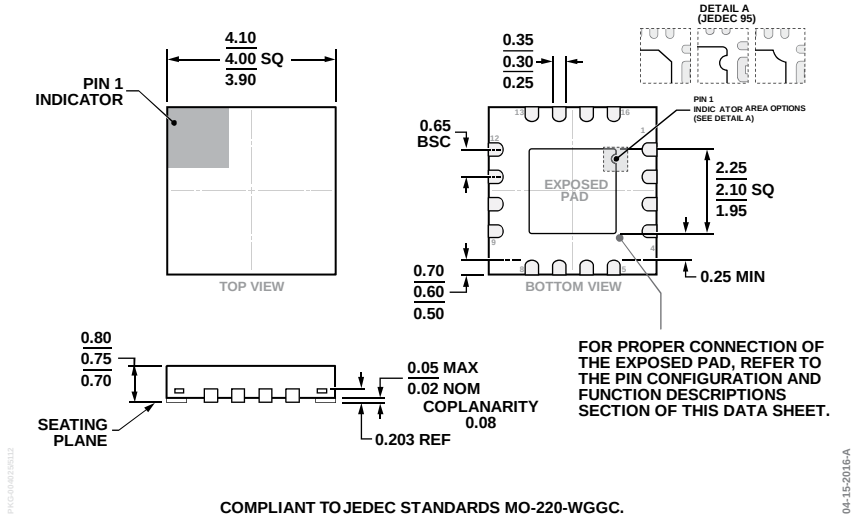


Figure 48. *16-Lead Lead Frame Chip Scale Package [LFCSP]*
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5604ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADL5604-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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