250 MHz to 2400 MHz RF Variable Gain Amplifier

ADL5592

FEATURES

Output frequency range: 250 MHz to 2400 MHz
Noise figure: 5.7 dB at 1960 MHz
OIP3 at 1960 MHz: 29 dBm at P_{IN} = 0 dBm per tone
2 digital attenuators, each with 31 dB range
1 dB attenuation step size
Single SPI port
Single supply: 4.5 V to 5.5 V
40-lead, 6 mm × 6 mm LFCSP package

APPLICATIONS

GSM/EDGE and cellular communications systems

FUNCTIONAL BLOCK DIAGRAM

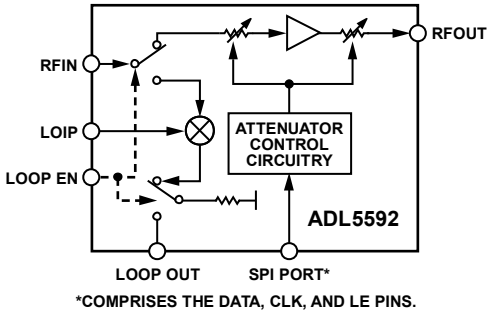


Figure 1.

GENERAL DESCRIPTION

The ADL5592 is a digitally programmable variable gain amplifier (VGA) designed for use from 250 MHz to 2400 MHz. Two digitally programmable attenuators are cascaded with a high linearity fixed-gain amplifier. The device also includes a mixer, which can be used to mix the transmitted signal into an adjacent receive band for loopback testing.

The ADL5592 can be used in conjunction with a direct-to-RF modulator, such as ADL537x and ADL539x, in cellular communications systems such as GSM/EDGE.

The ADL5592 is available in a 6 mm × 6 mm, 40-lead exposed-paddle LFCSP package. The device operates from the −40°C to +85°C temperature range.

Rev. 0
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REVISION HISTORY

6/08—Revision 0: Initial Version

SPECIFICATIONS

Measured at V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE		250		2400	MHz
DIGITAL ATTENUATORS—f_{RF} = 460 MHz to 496 MHz					
Attenuation Range		28	30.5		dB
Attenuator Step Size			1		dB
Relative Step Accuracy			−0.02	±1.0	dB
Absolute Step Accuracy			0.4	±4.0	dB
Step Size Variation vs. Frequency	Variation within transmit band		−0.02		dB
Dynamic Range Variation vs. Temperature	T_A = 0°C to 85°C		0.6		dB
VGA RF Output Power	RFIN = 4 dBm, minimum attenuation		16.3		dBm
vs. Frequency	Variation within transmit band		0.02		dB
Gain	Minimum attenuation, 270 nH choke inductor	8	12.3		dB
vs. Temperature	Variation within T_A = 0°C to 85°C		1		dB
vs. Frequency	Variation within transmit band		0.02		dB
OIP3	Two tones with Δ = 1 MHz, 0 dBm per input tone		27.7		dBm
Noise Figure	Minimum attenuation		4.3		dB
Return Loss	RFIN at minimum attenuation		−10		dB
	RFOUT at minimum attenuation		−15		dB
Modulation Spectrum	Relative to carrier in 30 kHz, P_{OUT} = 12 dBm, 8 PSK, 270 nH choke inductor				
	400 kHz carrier offset		−72		dBc
	600 kHz carrier offset		−85		dBc
	1.2 MHz carrier offset		−88		dBc
Error Vector Magnitude (EVM)	P_{OUT} = 12 dBm, 8 PSK				
	RMS		0.7		%
	Peak		2.1		%
DIGITAL ATTENUATORS—f_{RF} = 869 MHz to 960 MHz					
Attenuation Range		28	30.1		dB
Attenuator Step Size			1		dB
Relative Step Accuracy			−0.03	±1.0	dB
Absolute Step Accuracy			0.5	±4.0	dB
Step Size Variation vs. Frequency	Variation within transmit band		−0.03		dB
Dynamic Range Variation vs. Temperature	T_A = 0°C to 85°C		0.6		dB
RFOUT Power	RFIN = 4 dBm, minimum attenuation		14.8		dBm
vs. Frequency	Variation within transmit band		0.2		dB
Gain	Minimum attenuation, 270 nH choke inductor	8	10.8		dB
vs. Temperature	Variation within T_A = 0°C to 85°C		1.3		dB
vs. Frequency	Variation within transmit band		0.2		dB
OIP3	Two tones with Δ = 1 MHz, 0 dBm per input tone		28.5		dBm
Noise Figure	Minimum attenuation		4.8		dB
Return Loss	RFIN at minimum attenuation		−9.8		dB
	RFOUT at minimum attenuation		−9.8		dB
Modulation Spectrum	Relative to carrier in 30 kHz, P_{OUT} = 12 dBm, 8 PSK 270 nH choke inductor				
	400 kHz carrier offset		−72		dBc
	600 kHz carrier offset		−84		dBc
	1.2 MHz carrier offset		−88		dBc

Parameter	Conditions	Min	Typ	Max	Unit
Error Vector Magnitude (EVM)	P_{OUT} = 12 dBm, 8 PSK				
	RMS		0.9		%
	Peak		2.7		%
DIGITAL ATTENUATORS—f_{RF} = 1805 MHz to 1990 MHz					
Attenuation Range		28	30.5		dB
Attenuator Step Size			1		dB
Relative Step Accuracy			−0.02	±1.0	dB
Absolute Step Accuracy			0.24	±4.0	dB
Step Size Variation vs. Frequency	Variation within transmit band		−0.02		dB
Dynamic Range Variation vs. Temperature	T_A = 0°C to 85°C		0.7		dB
RFOUT Power	RFIN = 4 dBm, minimum attenuation		12.9		dBm
vs. Frequency	Variation within transmit band		0.2		dB
Gain	Minimum attenuation, 33 nH choke inductor	8	8.9		dB
vs. Temperature	Variation within T_A = 0°C to 85°C		1.5		dB
vs. Frequency	Variation within transmit band		0.2		dB
OIP3	Two tones with Δ = 1 MHz, 0 dBm per input tone		29		dBm
Noise Figure	Minimum attenuation		5.7		dB
Return Loss	RFIN at minimum attenuation		−16.4		dB
	RFOUT at minimum attenuation		−11.1		dB
Modulation Spectrum	Relative to carrier in 30 kHz, P_{OUT} = 12 dBm, 8 PSK 33 nH choke inductor				
	400 kHz carrier offset		−71		dBc
	600 kHz carrier offset		−86		dBc
	1.2 MHz carrier offset		−88		dBc
Error Vector Magnitude (EVM)	P_{OUT} = 12 dBm, 8 PSK				
	RMS		0.7		%
	Peak		1.9		%
LOGIC INPUTS					
Clock Speed			13		MHz
Input Logic Low	DATA, CLK, LE			0.8	V
Input Logic High		2.5			V
RF LOOP MIXER					
Input Frequency		460		1990	MHz
Output Frequency		450		1910	MHz
Input Return Loss	RFIN with loop enable active low at 1960 MHz		−13		dB
	LOIP at 80 MHz		−16		dB
Output Return Loss	LOOP OUT at 1880 MHz		−8		dB
LOIP Frequency Range		10		95	MHz
LOIP Power		−6		0	dBm
LOOP OUT Power	RFIN = 5 dBm				
	450 MHz to 486 MHz		−13.0		dBm
	824 MHz to 915 MHz		−12.1		dBm
	1710 MHz to 1910 MHz		−13.1		dBm
Output Power Flatness					
vs. Frequency	Within a received band		0.6		dB
vs. Temperature	Variation within T_A = 0°C to 85°C		1.1		dB
OIP3	Two tones with Δ = 1 MHz, 0 dBm per input tone				
	450 MHz to 486 MHz		13.8		dBm
	824 MHz to 915 MHz		13		dBm
	1710 MHz to 1910 MHz		10.1		dBm
Output Noise Density	Carrier offset > 400 kHz		−132		dBc/Hz
Loop Enable Control					V

Parameter	Conditions	Min	Typ	Max	Unit
Input Logic Low	Loopback active		0	0.8	V
Input Logic High	Loopback inactive	2.4	5		V
Switching Time	Enable/disable			500	ns
ISOLATION					
LOOP OUT to RFOUT	Loopback mode, at loop output frequency, maximum attenuation set on ATTN 1 and ATTN 2. RFIN = 4 dBm, RF loop output = −11 dBm		−68		dBm
RFIN to RFOUT	Loopback mode, at RF input frequency, maximum attenuation set on ATTN 1 and ATTN 2. RFIN = 4 dBm, RF loop output = −11 dBm		−50		dBm
RFOUT to LOOP OUT	At carrier frequency, transmit mode, minimum attenuation set on ATTN 1 and ATTN 2, P_{OUT} = 15 dBm		−50		dB
RFIN to LOOP OUT	Transmit mode, maximum attenuation set on ATTN 1 and ATTN 2, P_{INATT1} = 4 dBm		−50		dB
POWER SUPPLIES	VCC pins				
Voltage		4.5	5.0	5.5	V
Supply Current	Loopback active at T_A = 25°C		230		mA
	T_A = −40°C to +85°C		255		mA
	Loopback inactive at T_A = 25°C		189		mA
	T_A = −40°C to +85°C		208		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VCC	5.5 V
RFIN	15 dBm
LOIP	10 dBm
LOOP EN, DATA, CLK, LE	5.5 V
Internal Power Dissipation	1650 mW
θ_{JA} (Exposed Paddle Soldered Down)	47°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

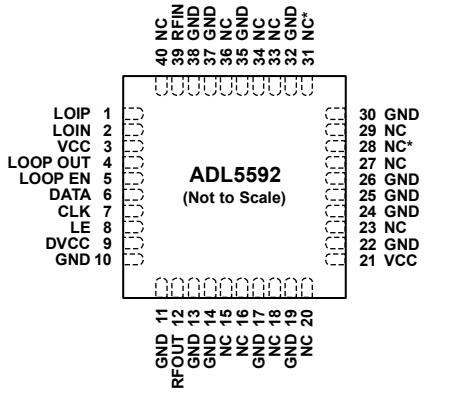


Figure 2. Pin Configuration (Top View)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	LOIP	Loopback Mixer Differential LO Input. Should be ac-coupled to the source of the mixer local oscillator signal.
2	LOIN	Loopback Mixer Differential LO Input. Should be ac-coupled to ground.
3, 21	VCC	Positive Supply. Nominally equal to 5 V. VCC and DVCC must be connected together externally and be properly bypassed.
4	LOOP OUT	Loopback Mixer RF Output. Single-ended 50 Ω output.
5	LOOP EN	Loopback Mixer Enable. Apply logic high for normal transmit mode. Apply logic mode low for loopback mode.
6	DATA	SPI Data Input. Both attenuators are programmed with a single 10-bit word.
7	CLK	SPI Clock Input. Data is clocked on the rising edge of CLK.
8	LE	SPI Latch Enable. Data is latched on the falling edge of LE.
9	DVCC	Digital Positive Supply. Nominally equal to 5 V.
12	RFOUT	RF Output. Should be ac-coupled.
39	RFIN	RF Input. Should be ac-coupled.
10, 11, 13, 14, 17, 19, 22, 24 to 26, 30, 32, 35, 37, 38	GND	Common. Connect to a low impedance ground plane.
15, 16, 18, 20, 23, 27 to 29, 31, 33, 34, 36, 40	NC	No Connection. The pad for Pin 28 and Pin 31 must remain free of traces to avoid stray capacitances.
	EP	Exposed Paddle. Connect to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5.0 V, unless otherwise noted.

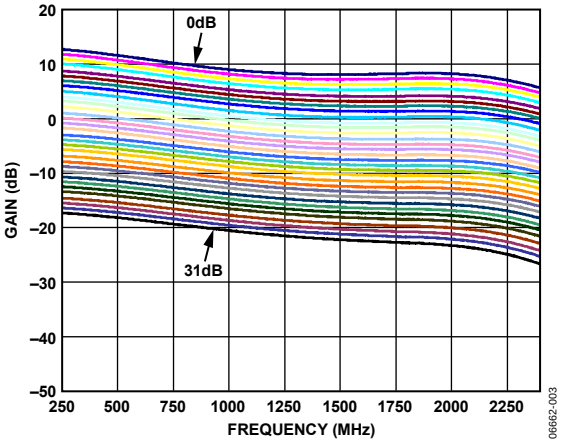


Figure 3. Gain vs. Frequency by Gain Code, All Input Attenuator (ATTN 1) Code Steps

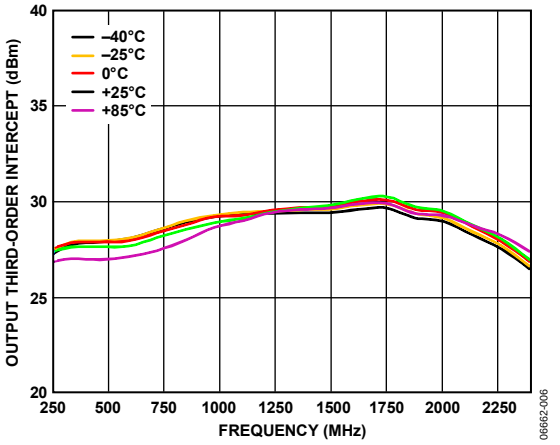


Figure 6. Output Third-Order Intercept vs. Frequency Across Temperature, Maximum Gain, 0 dBm per Input Tones with 1 MHz Spacing

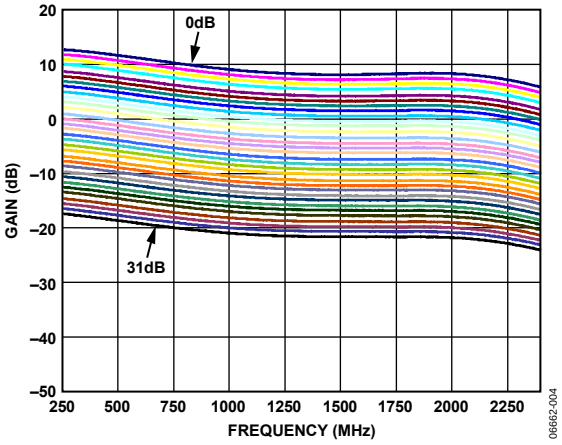


Figure 4. Gain vs. Frequency by Gain Code, All Output Attenuator (ATTN 2) Code Steps

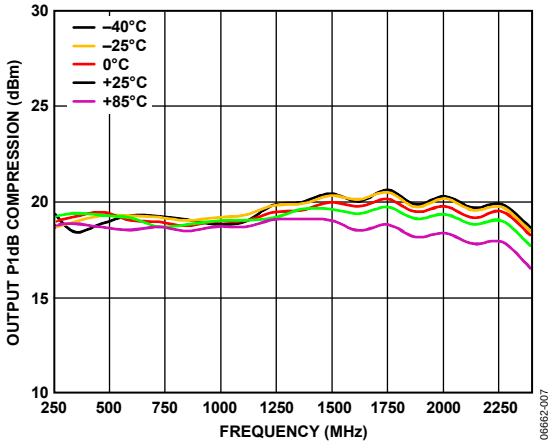


Figure 7. Output P1dB Compression vs. Frequency Across Temperature, Maximum Gain

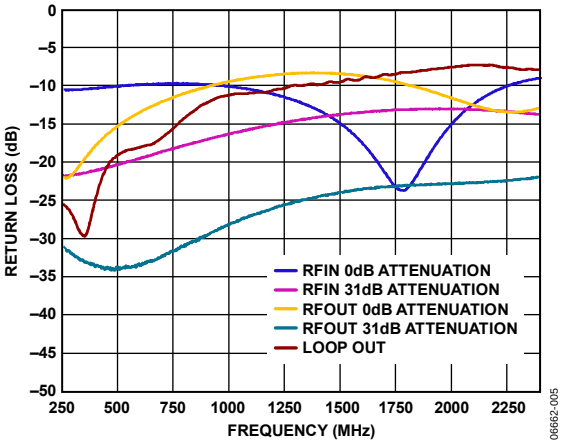


Figure 5. Return Loss vs. Frequency, RFIN, RFOUT, and LOOP OUT

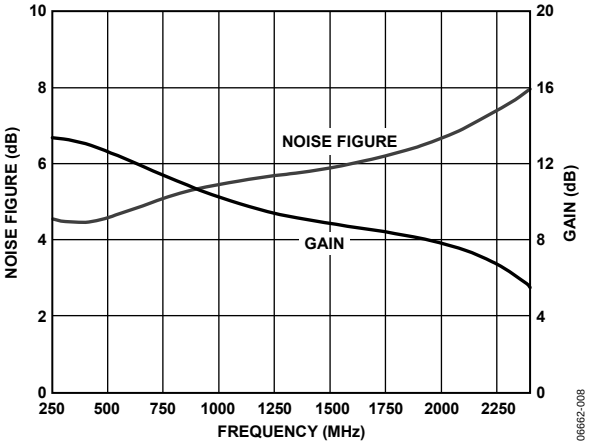


Figure 8. Noise Figure and Gain vs. Frequency, at Maximum Gain

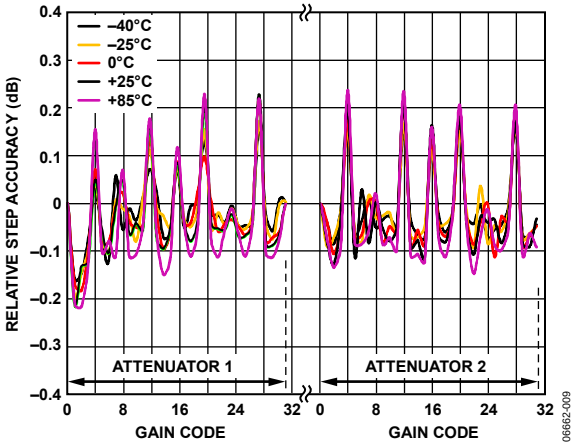


Figure 9. Gain Step Error Across Temperature, Frequency = 492 MHz (Each Attenuator Is Swept Independently from 0 to 31)

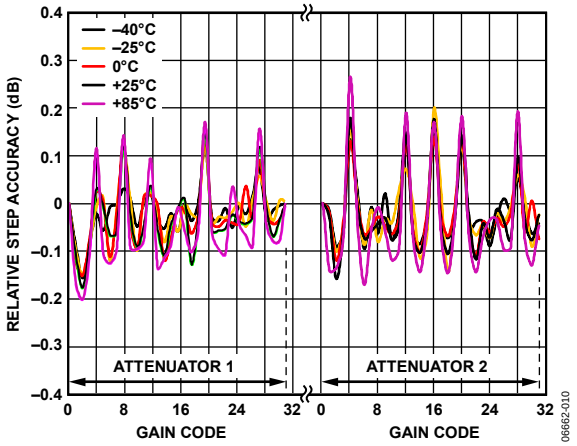


Figure 10. Gain Step Error Across Temperature, Frequency = 925 MHz (Each Attenuator Is Swept Independently from 0 to 31)

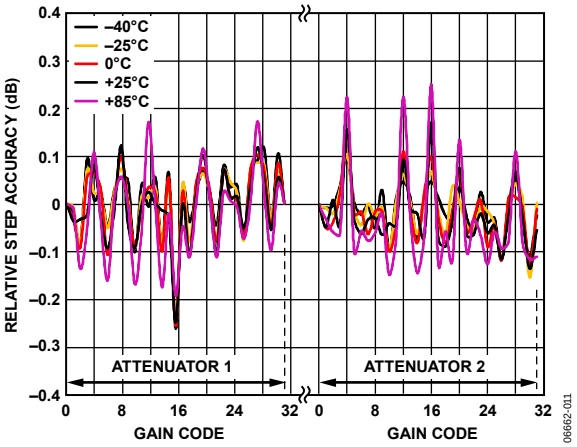


Figure 11. Gain Step Error Across Temperature, Frequency = 1960 MHz (Each Attenuator Is Swept Independently from 0 to 31)

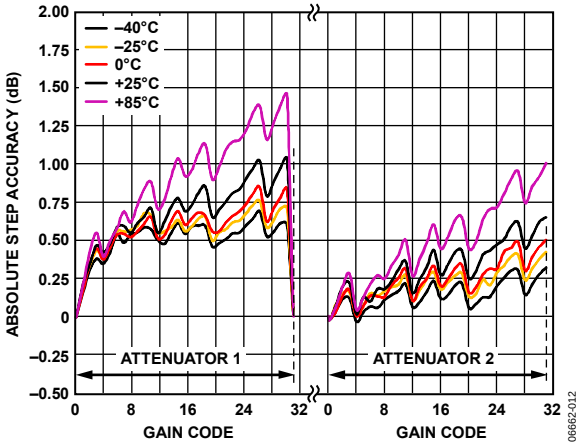


Figure 12. Absolute Gain Error Across Temperature, Frequency = 492 MHz (Each Attenuator Is Swept Independently from 0 to 31)

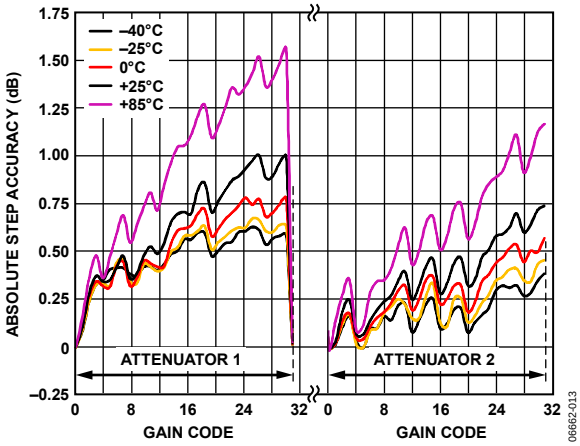


Figure 13. Absolute Gain Error Across Temperature, Frequency = 925 MHz (Each Attenuator Is Swept Independently from 0 to 31)

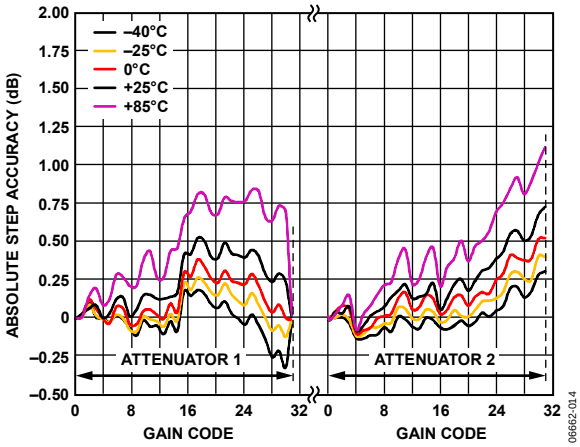


Figure 14. Absolute Gain Error Across Temperature, Frequency = 1960 MHz (Each Attenuator Is Swept Independently from 0 to 31)

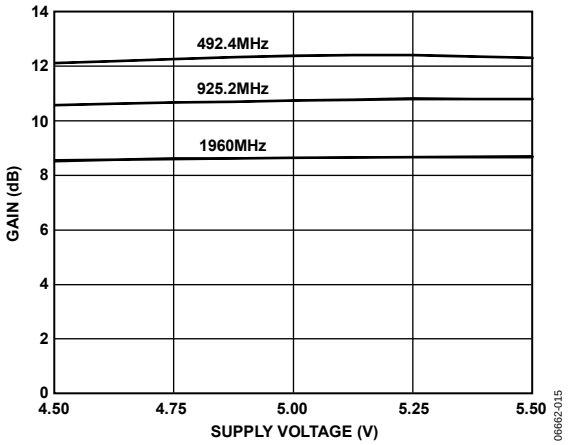


Figure 15. Gain vs. Supply Voltage at Maximum Gain

THEORY OF OPERATION

Figure 16 shows a simplified schematic of the ADL5592.

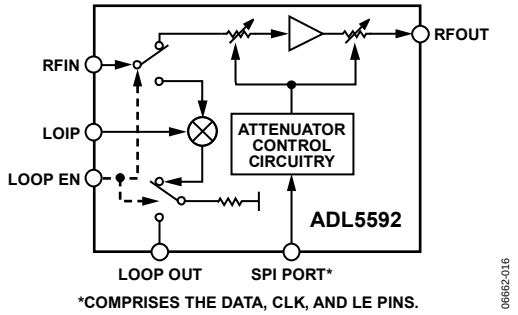


Figure 16. Simplified Schematic

INPUT SWITCH

The high performance single-pole, double throw (SPDT) GaAs pHEMT switch is connected to the RF input pin of the ADL5592 to switch the input signal between the VGA and the mixer. To diminish the impact of the switch on the performance of the VGA and the mixer, this SPDT switch exhibits low insertion loss and high isolation in the operating frequency range. The switch-state control signal is provided by a Si CMOS control circuit.

DIGITAL ATTENUATOR

The digital attenuator consists of five attenuation blocks—1 dB, 2 dB, 4 dB, 8 dB, and 16 dB—each separately controlled by a Si CMOS control circuit. Each attenuation block consists of field effect transistor (FET) switches and resistors that form either a pi- or a T- shaped attenuator. By controlling the states of the FET switches through the Si CMOS control lines, each attenuation block can be set to be in the pass state (0 dB) or the attenuation state (n dB). The various combinations of the five blocks provide the attenuation states from 0 dB to 31 dB, in 1 dB increments.

SPI INTERFACE

The ADL5592 includes a SPI-compatible, 3-wire serial interface. The Si CMOS interface internally level-shifts the SPI signals, which are used to program a 10-bit shift register and to control the loading of a 10-bit parallel latch. The outputs of the latch are fed into drivers, which convert the logic-level outputs of the latches to signals appropriate for driving the attenuators.

FIXED-GAIN AMPLIFIER

The output of the input attenuator (ATTN 1) is connected to a fixed-gain amplifier that drives the output attenuator (ATTN 2). Because the passive attenuators are linear and contribute minimal noise, the fixed-gain amplifier is the major source of nonlinear distortion and noise. This results in a constant OIP3 and noise figure throughout the different attenuation stages. The fixed-gain amplifier provides 14 dB of gain and broadband, 50 Ω, single-ended input and output impedances.

LOOPBACK MIXER

The loopback mixer is a Si CMOS Gilbert-cell mixer designed to provide 10 MHz to 100 MHz of frequency translation from the RF input to the mixer output. The mixer has 50 Ω loads at the output for a broadband, single-ended output. The input is fed from the SPDT GaAs pHEMT switch. The overall mixer gain is typically −17 dB. The mixer LO input is designed to operate from 10 MHz to greater than 100 MHz.

APPLICATIONS INFORMATION

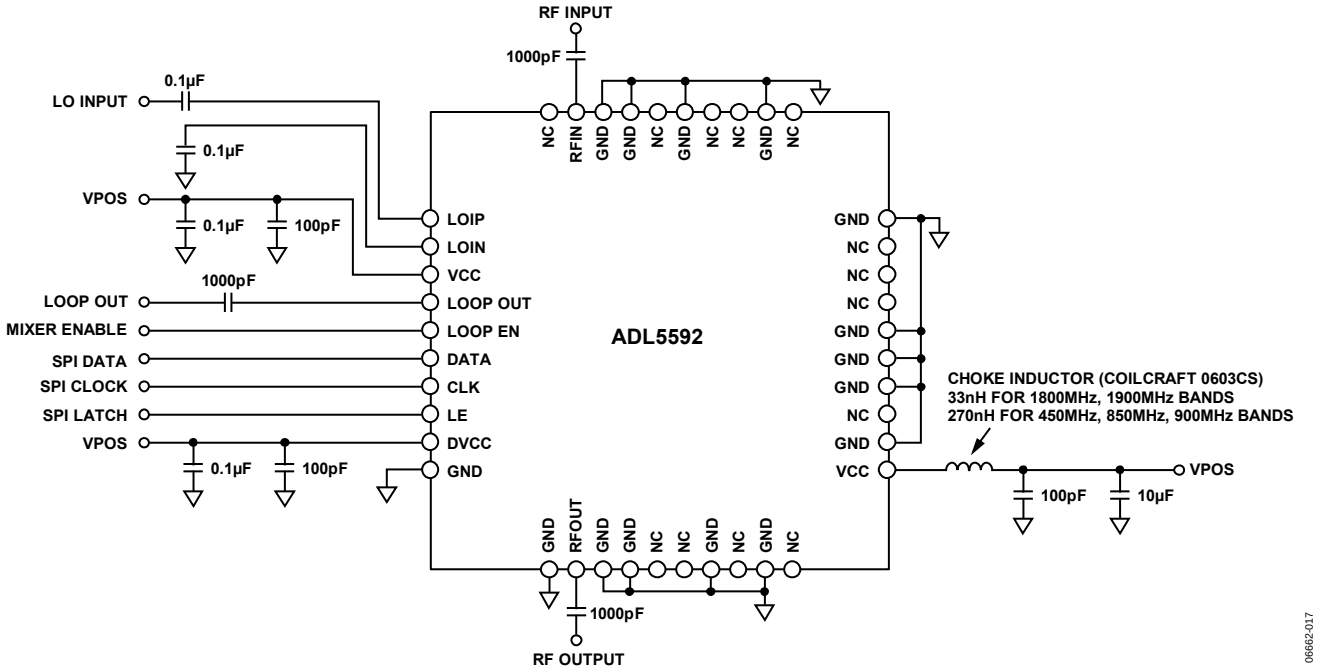


Figure 17. Basic Connections

BASIC CONNECTIONS

Figure 17 shows the basic connections for the ADL5592. A single power supply between 4.75 V and 5.25 V is applied to the VCC pins. All the VCC pins must be connected to the same potential. Each power supply pin should be decoupled using a 100 pF capacitor in addition to either a 0.1 µF or 10 µF capacitor. These capacitors should be located as close as possible to the device. One of the supply pins (Pin 21) also requires biasing of an open-collector using an RF choke (Coilcraft 0603CS). The value of the inductor is dictated by the frequency band of operation: 270 nH for the 450 MHz, 850 MHz, and 900 MHz bands and 33 nH for the 1800 MHz and 1900 MHz bands. The RFIN, RFOUT, and LOOP OUT pins have 50 Ω impedances and must be ac-coupled.

PROGRAMMING THE SPI PORT

Both attenuators are programmed with a single 10-bit word. Figure 18 shows the input and output attenuators, ATTN 1 and ATTN 2, respectively. Table 4 lists the 10-bit words corresponding to the various gain levels. The five least significant bits (LSBs) set the input attenuator, ATTN 1. The five most significant bits (MSBs) set the output attenuator, ATTN 2.

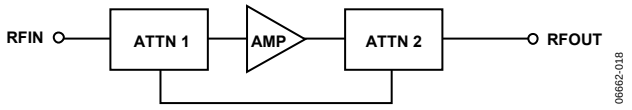


Figure 18. Block Diagram of Attenuator Chain

Figure 19 shows the timing diagram of the SPI port transmission. DATA is clocked on the rising edge of CLK. The data is latched and the attenuation is updated on the falling edge of LE (the latch enable pin). The timing requirements indicated in Figure 19 are described in Table 5.

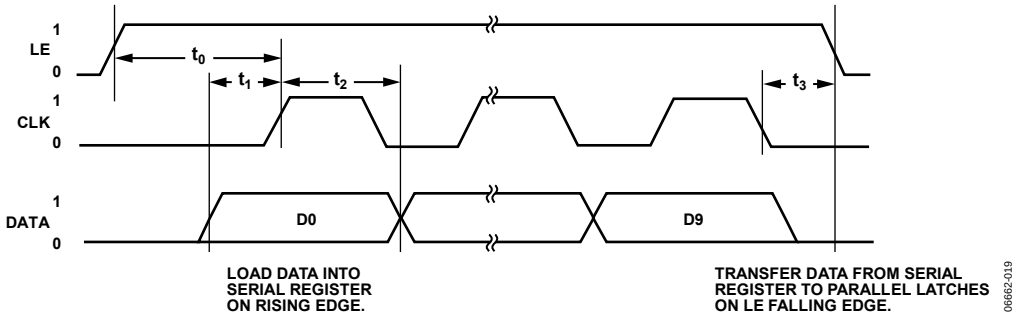


Figure 19. Timing Diagram of SPI Port Transmission

Table 4. 10-Bit Gain Words for SPI Port

ATTN 2					ATTN 1					Resulting Attenuation		
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	ATTN 1 (dB)	ATTN 2 (dB)	Total Attenuation (dB)
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	0	0	0	0	2	2
0	0	1	0	0	0	0	0	0	0	0	4	4
0	1	0	0	0	0	0	0	0	0	0	8	8
1	0	0	0	0	0	0	0	0	0	0	16	16
1	1	1	1	1	0	0	0	0	0	0	31	31
0	0	0	0	0	0	0	0	0	1	1	0	1
0	0	0	0	0	0	0	0	1	0	2	0	2
0	0	0	0	0	0	0	1	0	0	4	0	4
0	0	0	0	0	0	1	0	0	0	8	0	8
0	0	0	0	0	1	0	0	0	0	16	0	16
0	0	0	0	0	1	1	1	1	1	31	0	31
1	1	1	1	1	1	1	1	1	1	31	31	62

Table 5. Timing Requirements for the SPI Port

Mnemonic	Description	Min	Max	Unit
t_0	Latch enable setup time. Time between latch enable active (high) and first rising edge of serial clock.	15		ns
t_1	Serial data setup time. Time between valid serial data and rising clock edge. Note that this time applies to all bits in the serial data stream	15		ns
t_2	Serial data hold time. Time after rising clock edge during which the serial data line cannot change in value. Note that this time applies to all bits in the serial data stream	15		ns
t_3	Latch enable hold time. Time after final falling clock edge during which the latch enable must remain active (high).	15		ns
f_{CLK}	Clock period.		15	MHz

GSM/EDGE TRANSMIT APPLICATION

Figure 20, Figure 21, and Figure 22 show effects of different input power levels on the spectral mask and EVM. The gain code is held constant at the minimum attenuation (corresponding to Code 0 for both attenuators).

At low output power levels, both the spectral mask and EVM remain flat. At higher output power levels, however, the spectral mask expands and the EVM increases.

At an output of 12 dBm at 925.5 MHz, the peak and rms EVM are 0.56% and 1.51%, respectively. The spectral mask offsets at 400 kHz, 600 kHz, and 1.2 MHz sit at −72.2 dBc, −84.8 dBc, and −88.01 dBc, respectively.

Note that the minimum attenuation setting results in the highest spectral mask and EVM values (excluding noise floor limitations). Increasing the input attenuation of ATTN 1 causes less power to be presented to the amplifier stage. Therefore, the levels of the spectral mask and EVM decrease as the input attenuation of ATTN 1 is increased. As the output attenuation of ATTN 2 is increased, the levels of the spectral mask and EVM remain flat.

SOLDERING INFORMATION

On the underside of the chip scale package, there is an exposed compressed paddle. This paddle is internally connected to the chip's ground. Solder the paddle to the low impedance ground plane on the printed circuit board to ensure specified electrical performance and to provide thermal relief. It is also recommended that the ground planes on all layers under the paddle be stitched together with vias to reduce thermal impedance.

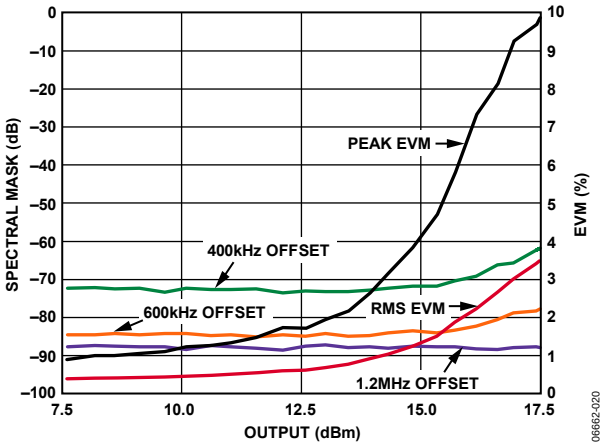


Figure 20. EVM and Spectral Mask vs. Output Power, 488.8 MHz EDGE Signal, 270 nH RF Choke, Minimum Attenuation

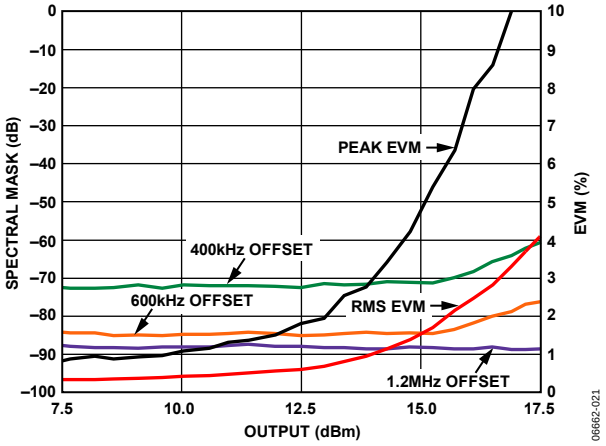


Figure 21. EVM and Spectral Mask vs. Output Power, 925.5 MHz EDGE Signal, 270 nH RF Choke, Minimum Attenuation

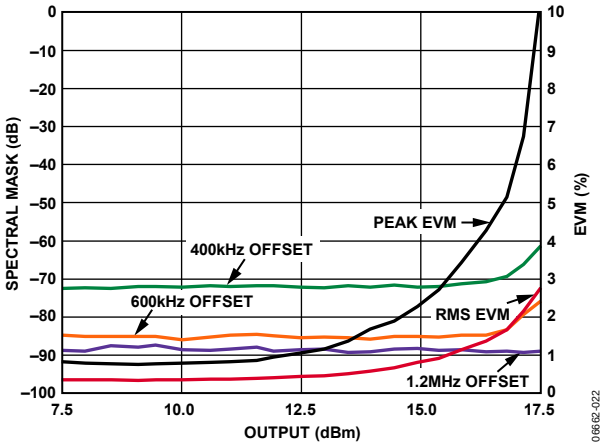


Figure 22. EVM and Spectral Mask vs. Output Power, 1960 MHz EDGE Signal, 33 nH RF Choke, Minimum Attenuation

EVALUATION BOARD

CHARACTERIZATION SETUP

The primary setup used to characterize the ADL5592 is shown in Figure 23. This setup was used to measure the frequency response, linearity, and output compression of the amplifier. A Rohde & Schwarz SMT 03 signal generator was used to drive the amplifier with a 4 dBm input. The output of the ADL5592 was connected to a Rohde & Schwarz FSIQ7 spectrum analyzer through an RF switch matrix unit. For the linearity measurement, two SMT 03 signal generators were used to generate the two-tone RF input signal. (The same SMT 03 is used for both amplifier and mixer characterization.) The gain control data was generated by a Tektronix DG2020A data generator. The DG2020A generated all three of the SPI input signals: CLK, DATA, and LE. A separate SMT 03 was used to generate the mixer local oscillator signal (LO input signal) when the loopback mixer was enabled. An Agilent Visual Engineering Environment (VEE) program controlled the test instruments through the general-purpose interface bus (GPIB) interface.

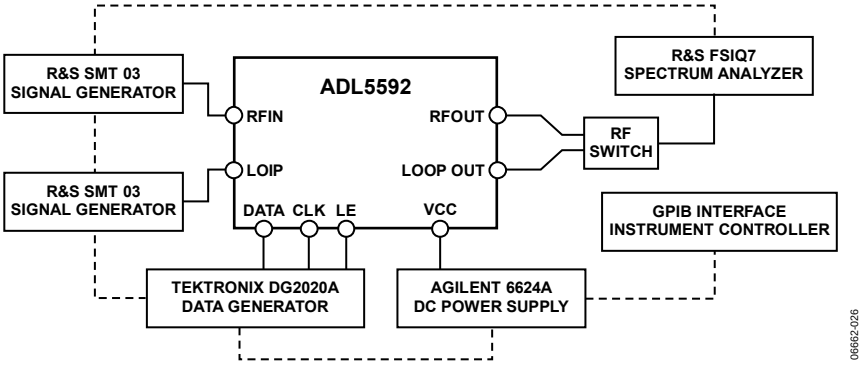


Figure 23. Characterization Bench Setup

SCHEMATIC AND LAYOUT

Figure 24 shows the schematic and Figure 25 and Figure 26 show the layout of the ADL5592 evaluation board. The board is powered by a single supply in the 4.75 V to 5.25 V range. Each power supply pin should be decoupled using a 100 pF capacitor in addition to either a 0.1 µF or 10 µF capacitor. Table 6 details the various configuration options of the evaluation board.

The RFIN, RFOUT, and LOOP OUT pins have 50 Ω impedances and must be ac-coupled. One of the supply pins (Pin 21) requires supply biasing using an RF choke (Coilcraft 0603CS). The value of the inductor is dictated by the frequency band of operation: 270 nH for the 450 MHz, 850 MHz, and 900 MHz bands and 33 nH for the 1800 MHz and 1900 MHz bands.

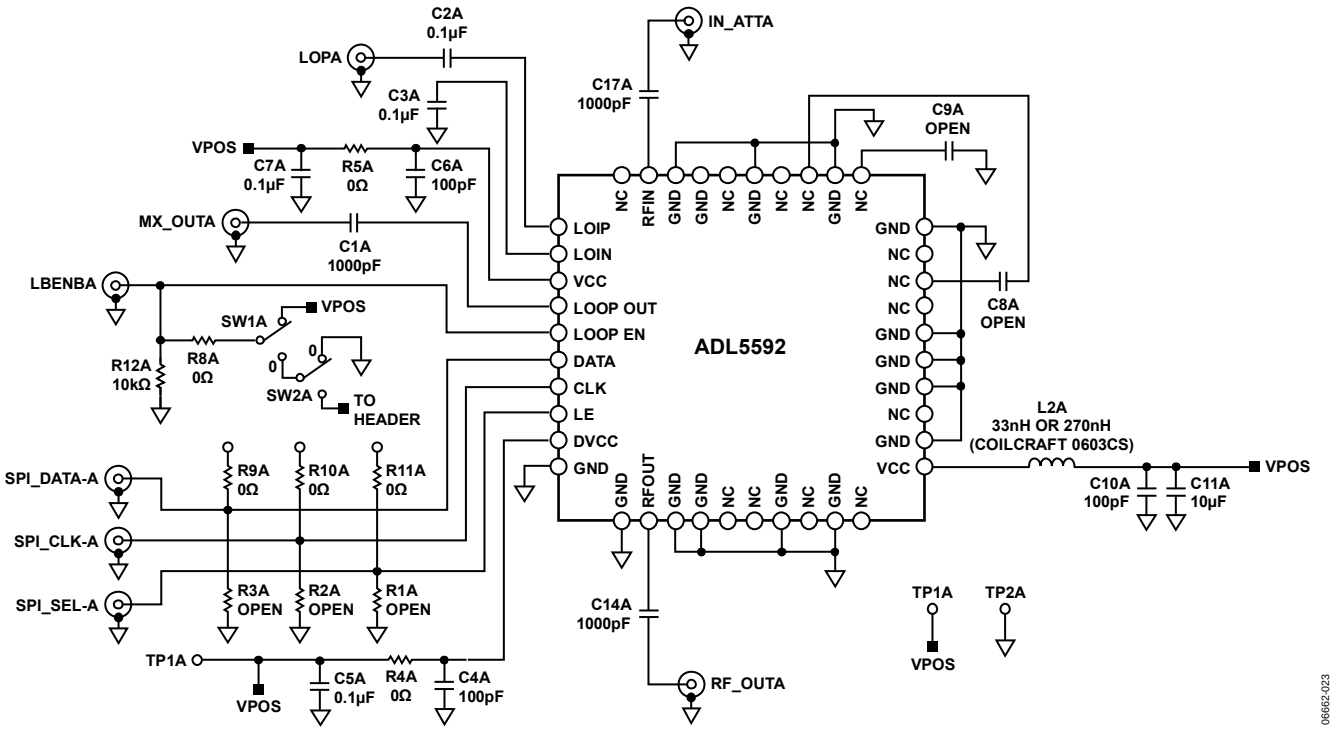


Figure 24. Evaluation Board Schematic

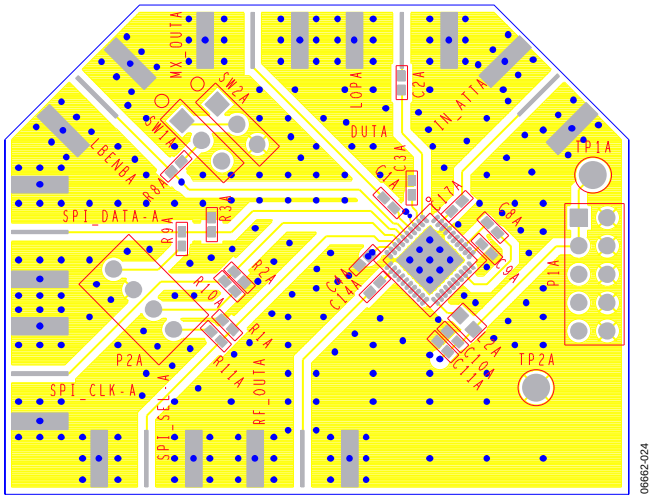


Figure 25. Evaluation Board Layout, Component Side

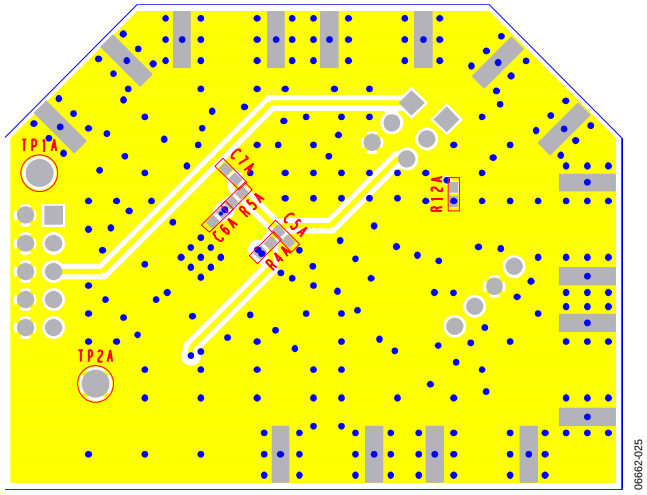


Figure 26. Evaluation Board Layout, Circuit Side

CONFIGURATION OPTIONS

Table 6. Evaluation Board Configuration Options

Component Designator	Component Name	Description	Default Conditions
TP1A, TP2A	Supply and ground vector pins		Not applicable
L1A, L2A, C4A to C11A, R4A, R5A	Power supply decoupling	The nominal power supply decoupling is accomplished by using a 100 pF (C4A, C6A, and C10A) in addition to either a 0.1 µF (C5A and C7A) or a 10 µF (C11A) capacitor at each power supply pin. A series inductor, L2A, is used to bias the open collector at Pin 21. To tune the ADL5592 for the low bands (450 MHz, 850 MHz, and 900 MHz), the value should be 270 nH. For the high bands (1800 MHz and 1900 MHz), the inductor should be changed to 33 nH.	L2A = 270 nH or 33 nH (Size 0603) (Coilcraft 0603CS); C4A, C6A, C10A = 100 pF (Size 0402); C5A, C7A = 0.1 µF (Size 0402); C11A = 10 µF (Size 0402); R4A, R5A = 0 Ω (Size 0402); C8A, C9A = open (Size 0402)
C14A, C17A	Input and output interfaces	C14A and C17A are dc blocks. The SMA labeled IN_ATTA is used to drive the RF input. The SMA labeled RF_OUTA corresponds to the RF output.	C14A, C17A = 1000 pF (Size 0402)
C1A to C3A	Mixer input and output interfaces	C1A to C3A are dc blocks. The SMA labeled LOPA drives the balanced differential mixer input with a single-ended LO source. The unused differential input is ac-coupled to ground. The SMA labeled MX_OUTA corresponds to the mixer output. To use this function, the loopback mode must be enabled.	C1A = 1000 pF (Size 0402); C2A, C3A = 0.1 µF (Size 0402)
SW1A, SW2A, R8A, R12A	Loopback enable interface	Normal transmit mode is exercised by applying a logic high voltage to the LOOP EN pin, setting Switch SW1A to the position opposite Label O. For loopback mode, a logic low voltage must be applied to the LOOP EN pin by setting both Switch SW1A and Switch SW2A to the positions closest to the O labels. To exercise the control function from an external source, Switch SW1A must be set to the position closest to the O label and Switch SW2A must be set to the opposite position. The signal is driven from the LBENBA SMA.	SW1A, SW2A = installed; R8A = 0 Ω (Size 0402); R12A = 10 kΩ (Size 0402)
R1A to R3A, R9A to R11A	Serial control interface	The evaluation board can be controlled using most PCs. Windows®-based control software is shipped with the evaluation kit. A 25-pin D-subadapter and cable are required to connect the PC to the SPI port test points on the evaluation board. In some cases, the quality of the PC port signals can be improved by adding capacitance to R1A to R3A. The addition of 50 Ω values for R1A to R3A allow for SPI port control from digital generators driven from the SMAs connectors, SPI_DATA-A, SPI_CLK-A, and SPI_SEL-A.	R1A, R2A, R3A = open (Size 0402); R9A, R10A, R11A = 0 Ω (Size 0402)

OUTLINE DIMENSIONS

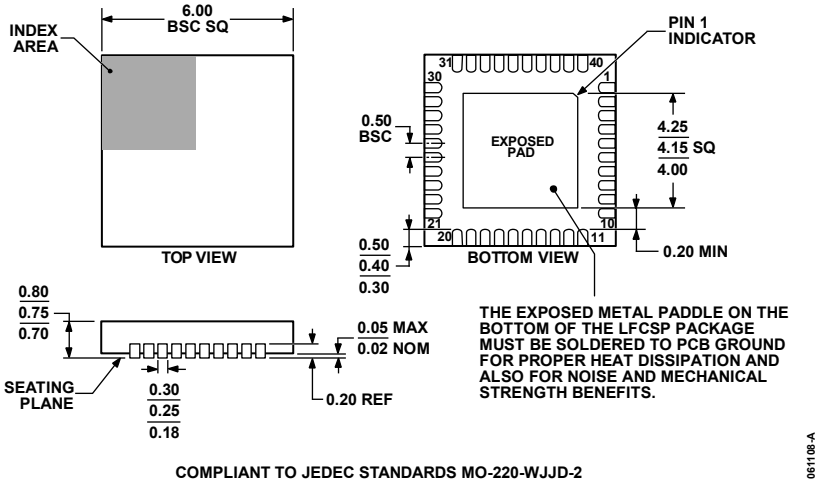


Figure 27. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5592ACPZ-R7[1]	−40°C to +85°C	40-Lead LFCSP_WQ, 7" Tape and Reel	CP-40-2	3,000
ADL5592-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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