400 MHz to 4000 MHz Low Noise Amplifier

Data Sheet

ADL5521

FEATURES

Operation from 400 MHz to 4000 MHz
Noise figure of 0.8 dB at 900 MHz
Requires few external components
Integrated active bias control circuit
Integrated dc blocking capacitors
Adjustable bias for low power applications
Single-supply operation from 3 V to 5 V
Gain of 20.8 dB at 900 MHz
OIP3 of 37.0 dBm at 900 MHz
P1dB of 21.8 dBm at 900 MHz
Small footprint LFCSP
Pin-compatible version with 21.5 dB gain available

FUNCTIONAL BLOCK DIAGRAM

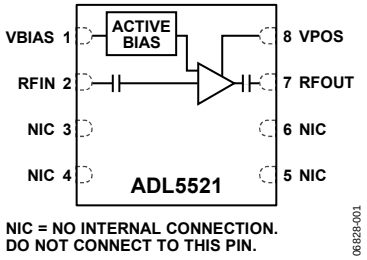


Figure 1.

GENERAL DESCRIPTION

The ADL5521 is a high performance GaAs pHEMT low noise amplifier. It provides high gain and low noise figure for single-downconversion IF sampling receiver architectures as well as direct-downconversion receivers.

The ADL5521 provides a high level of integration by incorporating the active bias and dc blocking capacitors, making it very easy to use while not sacrificing design flexibility.

The ADL5521 is easy to tune, requiring only a few external components. The device can support operation from 3 V to 5 V, and the current draw can be adjusted with the external bias resistor for applications requiring low power consumption.

The ADL5521 comes in a compact, thermally enhanced, 3 mm × 3 mm LFCSP and operates over the temperature range of −40°C to +85°C.

A fully populated evaluation board is also available.

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TABLE OF CONTENTS

Features ... 1
Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
AC Specifications ... 3
DC Specifications ... 4
De-Embedded S-Parameters, VPOS = 3 V to 5 V, RFIN = Port 1, VPOS = Port 2, RFOUT = Port 3 ... 4
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 7
900 MHz, VPOS = 5 V ... 7
1950 MHz, VPOS = 5 V ... 8
2600 MHz, VPOS = 5 V ... 9
3500 MHz, VPOS = 5 V ... 10
900 MHz, VPOS = 3 V ... 11
1950 MHz, VPOS = 3 V ... 12
2600 MHz, VPOS = 3 V ... 13
3500 MHz, VPOS = 3 V ... 14
DC Characteristics ... 15
Basic Connections ... 16
Evaluation Board ... 17
Soldering Information and Recommended PCB Land Pattern ... 17
Tuning the ADL5521 for Optimal Noise Figure ... 18
Tuning S22 ... 18
Tuning the LNA Input for Optimal Gain ... 19
Tuning the LNA Input for Optimal Noise Figure ... 19
S11 of the LNA with S22 Matched ... 20
Outline Dimensions ... 21
Ordering Guide ... 21

REVISION HISTORY

8/2017—Rev. B to Rev. C

Changed CP-8-2 to CP-8-13 ... Throughout
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 21

11/2013—Rev. A to Rev. B

Added Figure 52, Renumbered Sequentially ... 15

9/2009—Rev. 0 to Rev. A

Updated Maximum Junction Temperature Unit (Table 4) ... 5

10/2008—Revision 0: Initial Version

SPECIFICATIONS

AC SPECIFICATIONS

T_A = 25°C, R1 = 1.3 kΩ; parameters include matching circuit, matched for optimal noise, unless otherwise noted.

Table 1.

		3 V			5 V			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
FREQUENCY = 900 MHz								
Gain (S21)			20.3			20.8		dB
vs. Frequency	±50 MHz		±0.28			±0.33		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.53			±0.46		dB
Noise Figure[1]			0.8			0.9		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = 0 dBm per tone		28.0			37.0		dBm
Output 1 dB Compression Point (P1dB)			17.8			21.8		dBm
Input Return Loss (S11)			−8.0			−9.0		dB
Output Return Loss (S22)			−14.7			−15.3		dB
Isolation (S12)			−23.8			−25.0		dB
FREQUENCY = 1950 MHz								
Gain (S21)			15.4		14.7	15.8	17.0	dB
vs. Frequency	±30 MHz		±0.04			±0.06		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.43			±0.40		dB
Noise Figure[1]			1.0			1.0		dB
Output Third-Order Intercept (OIP3)	Δf = MHz, P_{OUT} = 0 dBm per tone		29.0			35.0		dBm
Output 1 dB Compression Point (P1dB)			17.6			21.8		dBm
Input Return Loss (S11)			−10.5			−12.5		dB
Output Return Loss (S22)			−25.5			−25.5		dB
Isolation (S12)			−20.2			−21.0		dB
FREQUENCY = 2600 MHz								
Gain (S21)			12.4			12.8		dB
vs. Frequency	±100 MHz		±0.35			±0.35		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.46			±0.45		dB
Noise Figure[1]			0.9			1.0		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = 0 dBm per tone		30.5			35.5		dBm
Output 1 dB Compression Point (P1dB)			17.1			21.5		dBm
Input Return Loss (S11)			−7.1			−7.7		dB
Output Return Loss (S22)			−14.1			−13.5		dB
Isolation (S12)			−20.0			−20.5		dB
FREQUENCY = 3500 MHz								
Gain (S21)			10.0			10.3		dB
vs. Frequency	±100 MHz		±0.56			±0.59		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.66			±0.63		dB
Noise Figure[1]			1.0			1.1		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = 0 dBm per tone		31.0			36.0		dBm
Output 1 dB Compression Point (P1dB)			17.0			20.9		dBm
Input Return Loss (S11)			−18.0			−18.3		dB
Output Return Loss (S22)			−10.5			−11.0		dB
Isolation (S12)			−17.8			−18.1		dB

[1] Noise figure de-embedded to first matching component on input side.

DC SPECIFICATIONS

Table 2.

		3 V			5 V			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Supply Current			30			60		mA
vs. Temperature	$-40°C \le T_A \le +85°C$		±4			±7		mA

DE-EMBEDDED S-PARAMETERS, VPOS = 3 V TO 5 V, RFIN = PORT 1, VPOS = PORT 2, RFOUT = PORT 3

Table 3.

Frequency (GHz)	S11 (dB/Ang)	S12 (dB/Ang)	S13 (dB/Ang)	S21 (dB/Ang)	S22 (dB/Ang)	S23 (dB/Ang)	S31 (dB/Ang)	S32 (dB/Ang)	S33 (dB/Ang)
0.125	−3.8/−11.3	−34.5/+8.9	−37.2/+51.8	+21.5/+161	−11.4/−133	−4.4/+32	+18.8/−155	+4.3/+32	−4.8/−80.9
0.25	−3.8/−24.5	−34.4/+26.6	−35.0/+50.5	+20.2/+158	−10.4/−153	−3.5/+19.8	+19.5/−178	−3.4/+20.1	−8.0/−111
0.375	−4.0/−37.1	−33.3/+39.6	−33.3/+54.2	+19.5/+154	−9.5/−158	−3.5/+16.5	+19.4/+170	−3.4/+17.0	−9.2/−126
0.5	−4.4/−48.9	−32.2/+48.9	−31.9/+57.7	+18.7/+150	−8.7/−158	−3.6/+16.2	+19.0/+161	−3.5/+16.7	−9.7/−133
0.625	−4.7/−60.0	−31.2/+55.8	−30.7/+60.2	+18.0/+146	−7.9/−155	−3.8/+17.2	+18.5/+153	−3.7/+17.7	−9.7/−137
0.75	−5.0/−70.2	−30.4/+61.3	−29.7/+61.9	+17.2/+143	−7.2/−150	−4.1/+19.1	+18.0/+147	−3.9/+19.5	−9.5/−139
0.875	−5.3/−79.1	−29.7/+66.6	−28.9/+63.5	+16.4/+141	−6.8/−144	−4.3/+21.6	+17.3/+141	−4.2/+22.1	−9.3/−139
1.0	−5.5/−86.9	−29.0/+71.2	−28.2/+64.7	+15.7/+140	−6.4/−137	−4.6/+24.8	+16.7/+137	−4.4/+25.1	−9.0/−138
1.125	−5.6/−93.3	−28.4/+75.6	−27.6/+65.6	+14.9/+138	−6.2/−129	−4.8/+28.0	+16.0/+132	−4.6/+28.3	−8.6/−137
1.25	−5.7/−98.0	−27.9/+79.8	−27.2/+66.9	+14.3/+138	−6.1/−121	−4.9/+31.9	+15.3/+129	−4.7/+32.1	−8.2/−135
1.375	−5.7/−102	−27.3/+84.0	−26.8/+68.0	+13.7/+138	−6.3/−113	−4.9/+35.7	+14.5/+126	−4.8/+35.8	−7.9/−133
1.5	−5.8/−104	−26.8/+87.8	−26.5/+69.4	+13.1/+138	−6.6/−105	−5.0/+39.4	+13.7/+123	−4.8/+39.4	−7.5/−131
1.625	−5.9/−104	−26.2/+91.6	−26.3/+71.5	+12.6/+138	−7.2/−97.2	−5.0/+43.5	+12.9/+122	−4.8/+43.5	−7.2/−129
1.75	−5.8/−104	−25.7/+94.8	−26.2/+73.9	+12.2/+138	−8.0/−91.0	−4.9/+47.0	+12.1/+121	−4.7/+47.0	−6.9/−127
1.875	−5.8/−103	−25.1/+98.2	−26.0/+76.8	+11.8/+139	−9.2/−86.4	−4.7/+50.5	+11.3/+122	−4.5/+50.5	−6.7/−126
2.0	−5.6/−101	−24.6/+101	−26.0/+80.1	+11.5/+139	−10.7/−85.8	−4.5/+53.6	+10.5/+123	−4.4/+53.6	−6.6/−125
2.125	−5.5/−99.3	−24.0/+104	−25.9/+85.1	+11.2/+139	−12.4/−92.3	−4.4/+56.6	+9.8/+125	−4.2/+56.6	−6.5/−125
2.25	−5.3/−97.2	−23.6/+106	−25.7/+91.0	+10.8/+139	−13.4/−110	−4.3/+59.1	+9.3/+129	−4.1/+59.1	−6.6/−125
2.375	−5.1/−95.9	−23.2/+109	−25.3/+96.7	+10.4/+139	−12.0/−129	−4.3/+61.6	+8.9/+132	−4.1/+61.7	−6.9/−127
2.5	−4.9/−94.8	−23.0/+111	−24.6/+103	+9.9/+140	−9.4/−136	−4.4/+64.3	+8.9/+136	−4.2/+64.4	−7.4/−128
2.625	−4.8/−94.4	−22.9/+114	−23.8/+108	+9.2/+141	−6.9/−135	−4.6/+67.3	+9.0/+139	−4.4/+67.4	−8.2/−130
2.75	−4.8/−94.8	−23.0/+118	−22.8/+111	+8.4/+143	−4.9/−127	−5.1/+70.9	+9.3/+140	−4.9/+71.0	−9.2/−132
2.875	−4.9/−95.4	−23.3/+122	−21.8/+114	+7.5/+146	−3.4/−117	−5.7/+75.0	+9.6/+141	−5.5/+75.2	−10.5/−133
3.0	−5.2/−96.9	−23.8/+127	−20.9/+114	+6.4/+149	−2.2/−104	−6.4/+79.7	+9.9/+140	−6.2/+79.8	−12.2/−133
3.125	−5.6/−98.9	−24.5/+133	−20.0/+114	+5.1/+153	−1.4/−89.0	−7.5/+85.2	+10.2/+138	−7.2/+85.0	−14.2/−132
3.25	−6.1/−102	−25.4/+139	−19.2/+114	+3.5/+157	−0.89/−73.4	−8.8/+90.4	+10.3/+136	−8.5/+90.4	−16.2/−126
3.375	−6.6/−105	−26.4/+144	−18.6/+112	+1.9/+162	−0.59/−57.8	−10.2/+95.5	+10.4/+133	−9.9/+95.4	−177/−116
3.5	−7.2/−110	−27.5/+149	−18.0/+111	+0.27/+165	−0.41/−42.6	−11.6/+100	+10.3/+130	−11.4/+99.7	−18.1/−104
3.625	−7.7/−115	−28.6/+154	−17.6/+109	−1.3/+169	−0.23/−27.6	−13.1/+104	+10.2/+127	−12.7/+104	−17.1/−93.5
3.75	−8.1/−123	−29.4/+158	−17.3/+106	−2.7/+172	+0.035/−12.8	−14.3/+109	+10.0/+124	−14.0/+108	−15.7/−88.0
3.875	−8.3/−132	−30.1/+163	−17.0/+103	−3.9/+175	+0.45/+2.3	−15.4/+114	+9.7/+119	−15.1/+113	−14.0/−87.7
4.0	−8.2/−140	−30.6/+168	−16.9/+99.8	−4.8/−180	+1.0/+18.9	−16.3/+120	+9.4/+115	−16.0/+120	−12.5/−89.2

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
RF Input Level	7 dBm
RF Input Level (with 8 Ω Series Resistor on VPOS)	20 dBm
Internal Power Dissipation	500 mW
θ_{JA} (Junction to Air)	50°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

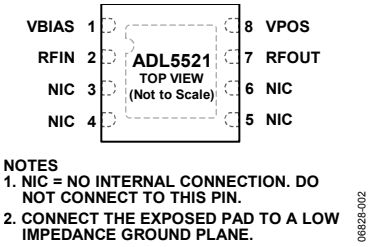


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VBIAS	Internal DC Bias. This pin should be connected to VPOS through the R1 resistor.
2	RFIN	RF Input. This is the input to the LNA.
3, 4, 5, 6	NC	No Connection. No internal connection.
7	RFOUT	RF Output.
8	VPOS	Supply Voltage. DC bias needs to be bypassed to ground using a low inductance capacitor. This pin is also used for output matching. See the Basic Connections section.
9 (EPAD)	Exposed Pad (EPAD)	GND. Connect the exposed pad to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

900 MHz, VPOS = 5 V

Matched for optimal noise figure, external matching circuit included.

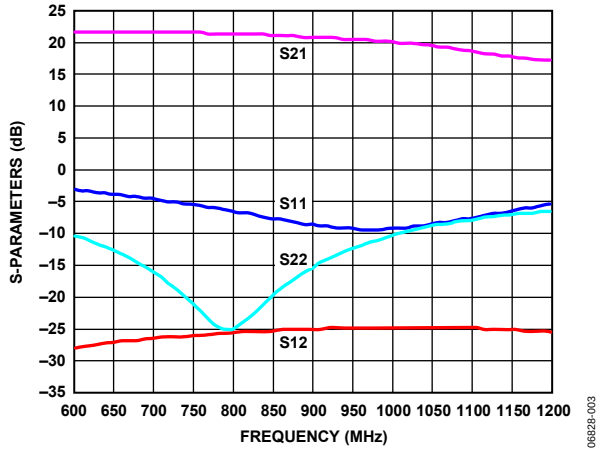


Figure 3. Typical S-Parameters, Log Magnitude

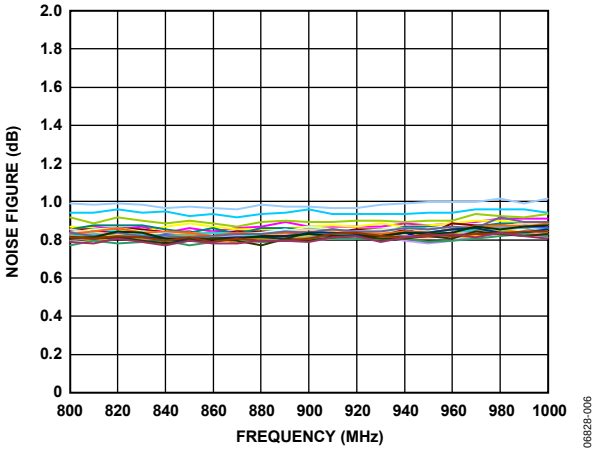


Figure 6. Noise Figure vs. Frequency at 25°C, Multiple Devices

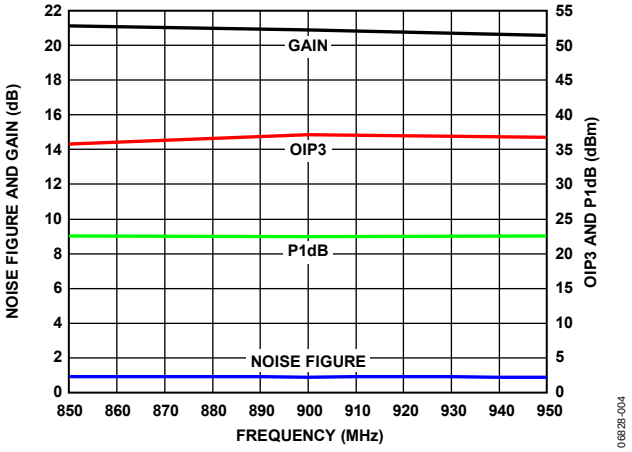


Figure 4. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

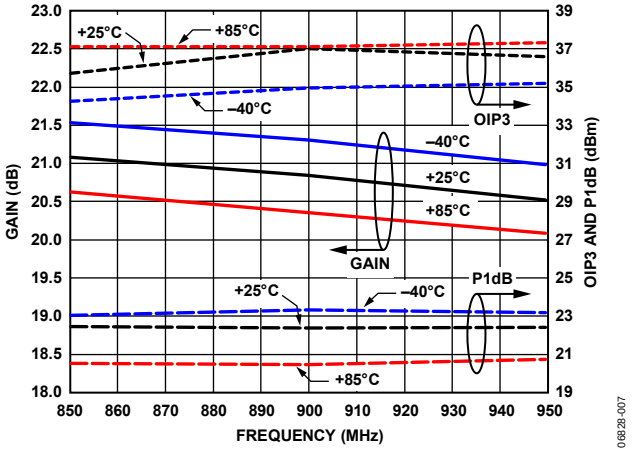


Figure 7. Gain, OIP3, and P1dB vs. Temperature

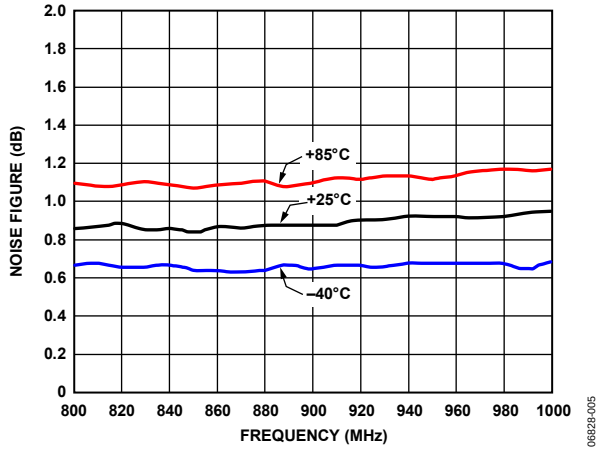


Figure 5. Noise Figure vs. Temperature

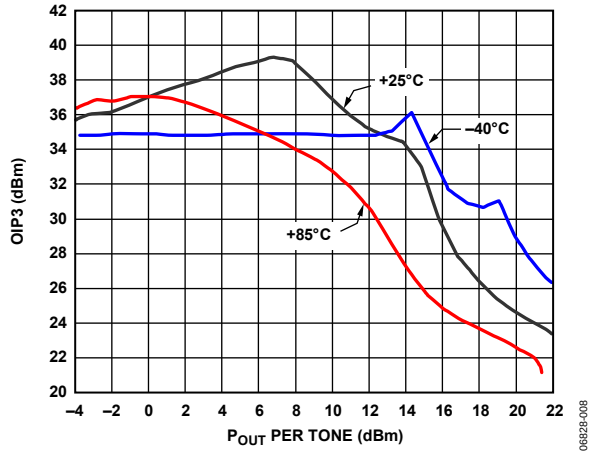


Figure 8. OIP3 vs. Output Power (P_{OUT}) and Temperature

1950 MHz, VPOS = 5 V

Matched for optimal noise figure, external matching circuit included.

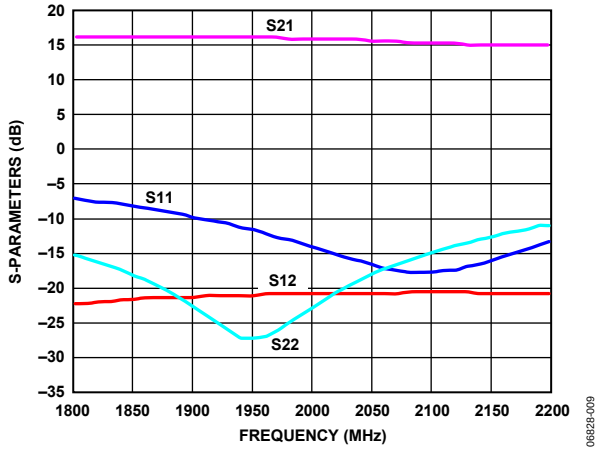


Figure 9. Typical S-Parameters, Log Magnitude

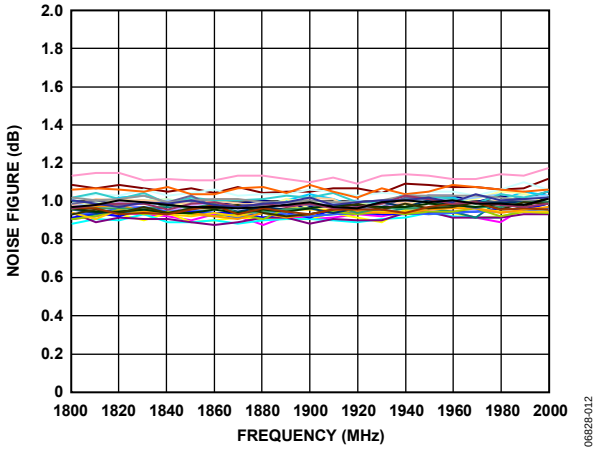


Figure 12. Noise Figure vs. Frequency at 25°C, Multiple Devices

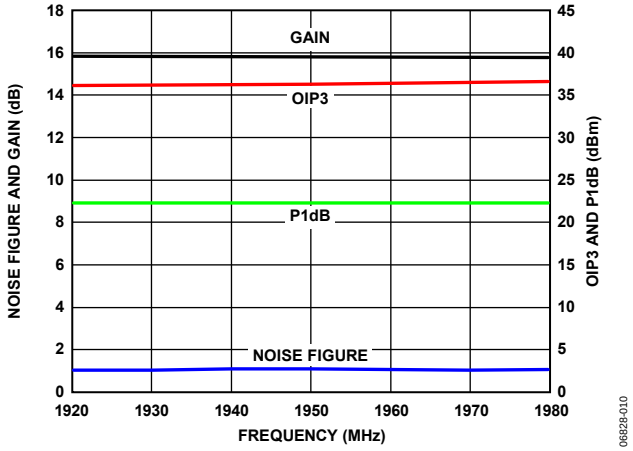


Figure 10. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

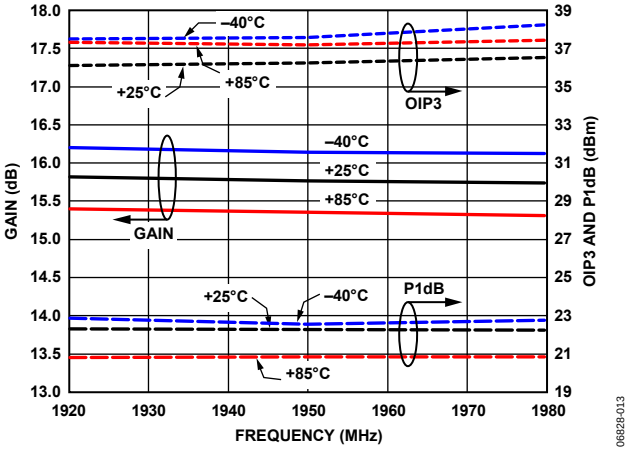


Figure 13. Gain, OIP3, and P1dB vs. Temperature

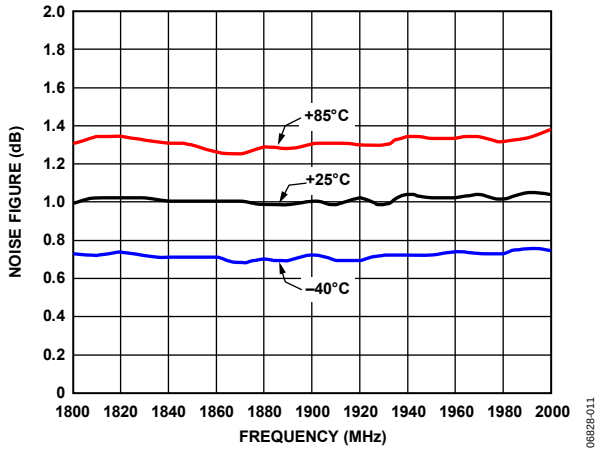


Figure 11. Noise Figure vs. Temperature

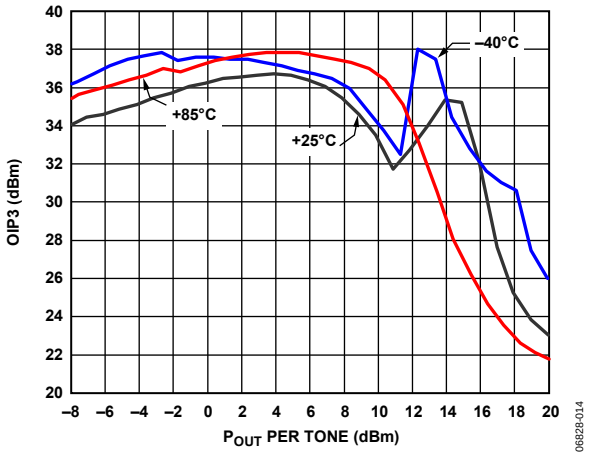


Figure 14. OIP3 vs. Output Power (P_{OUT}) and Temperature

2600 MHZ, VPOS = 5 V

Matched for optimal noise figure, external matching circuit included.

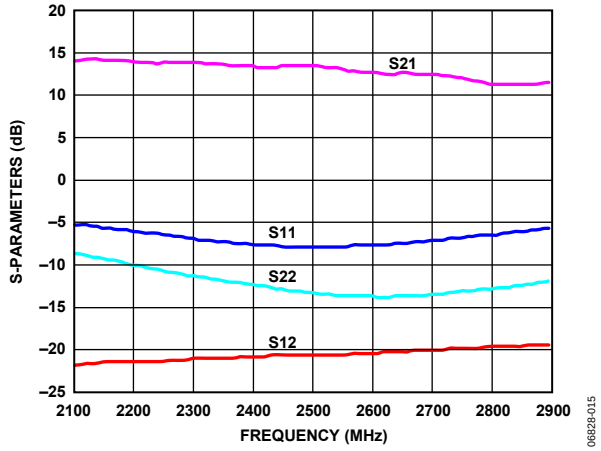


Figure 15. Typical S-Parameters, Log Magnitude

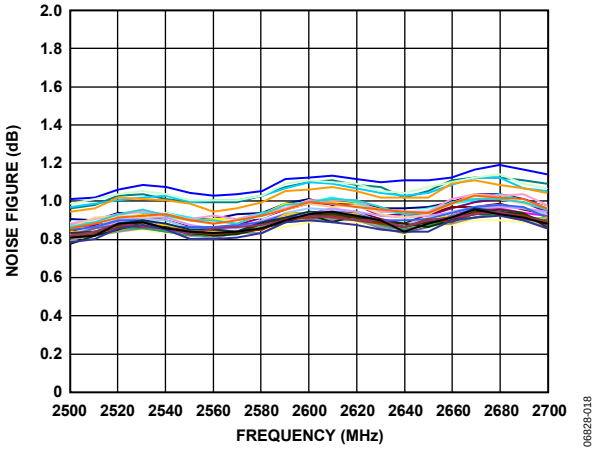


Figure 18. Noise Figure vs. Frequency at 25°C, Multiple Devices

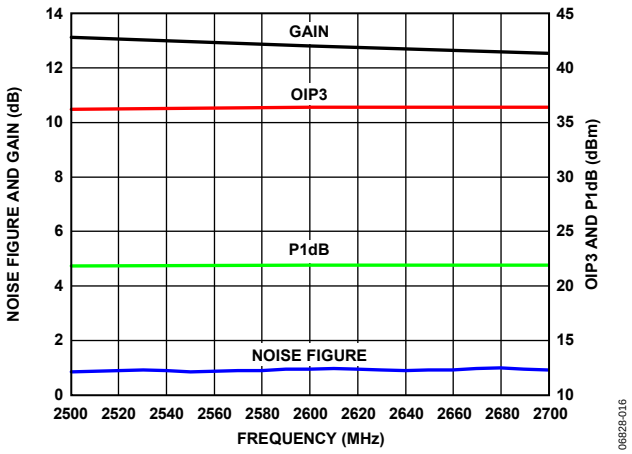


Figure 16. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

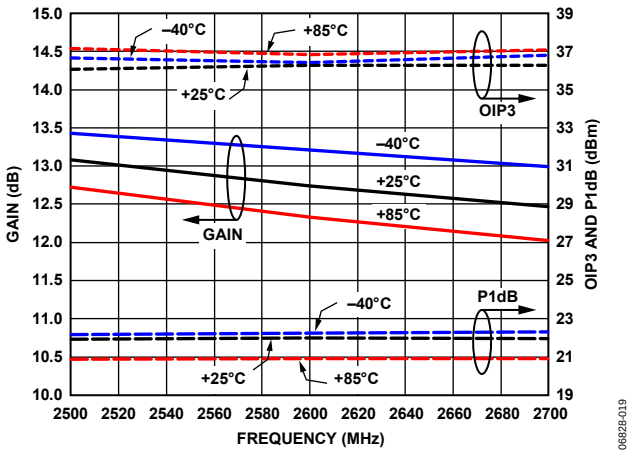


Figure 19. Gain, OIP3, and P1dB vs. Temperature

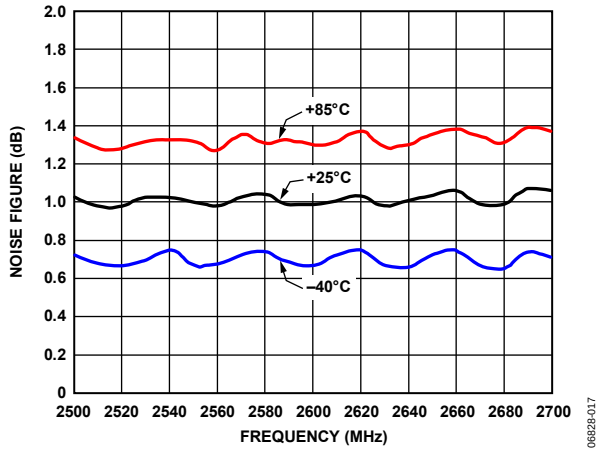


Figure 17. Noise Figure vs. Temperature

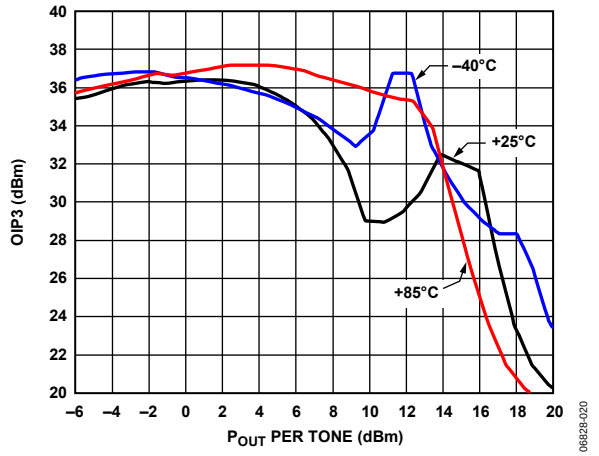


Figure 20. OIP3 vs. Output Power (P_{OUT}) and Temperature

3500 MHz, VPOS = 5 V

Matched for optimal noise figure, external matching circuit included.

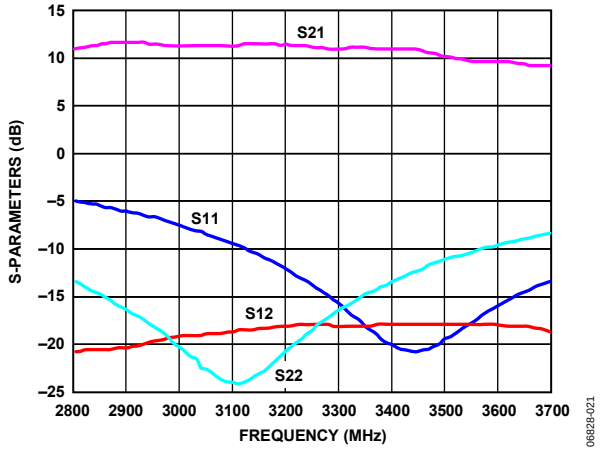


Figure 21. Typical S-Parameters, Log Magnitude

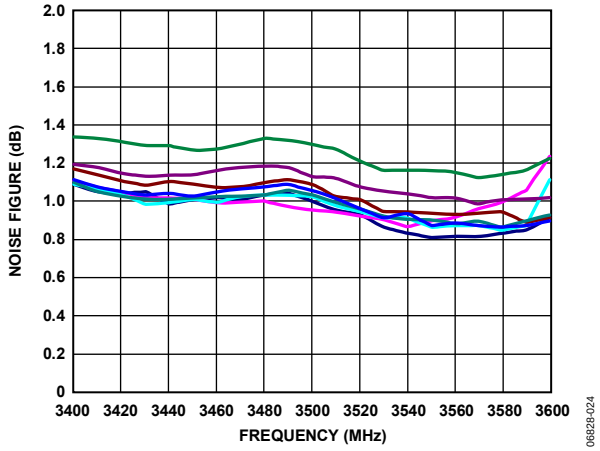


Figure 24. Noise Figure vs. Frequency at 25°C, Multiple Devices

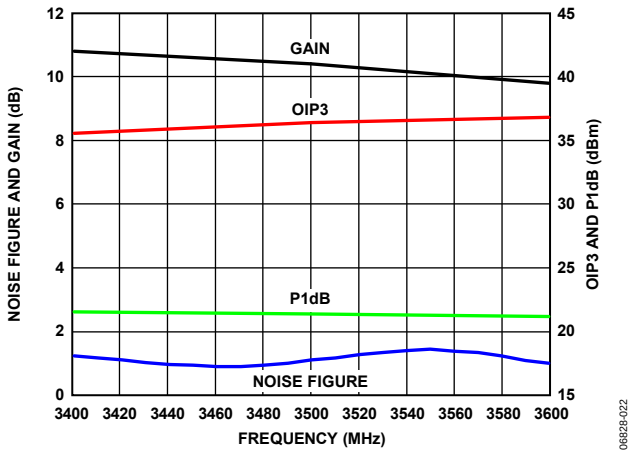


Figure 22. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

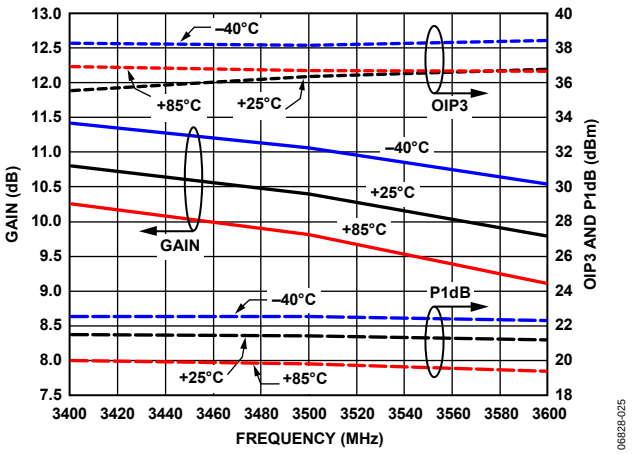


Figure 25. Gain, OIP3, and P1dB vs. Temperature

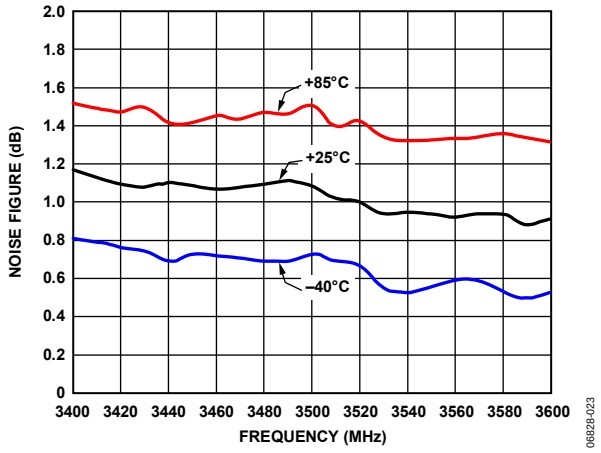


Figure 23. Noise Figure vs. Temperature

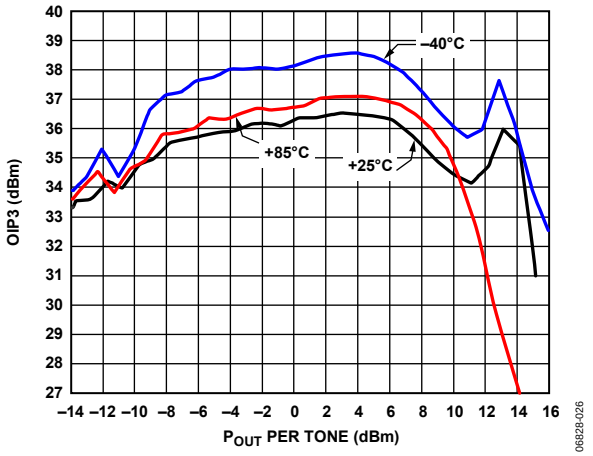


Figure 26. OIP3 vs. Output Power (P_{OUT}) and Temperature

900 MHz, VPOS = 3 V

Matched for optimal noise figure, external matching circuit included.

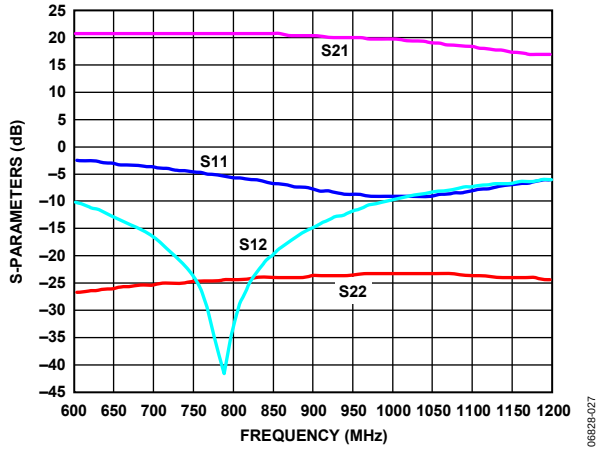


Figure 27. Typical S-Parameters, Log Magnitude

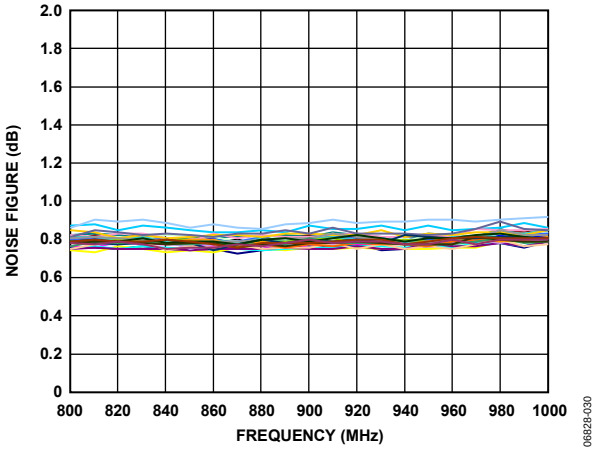


Figure 30. Noise Figure vs. Frequency at 25°C, Multiple Devices

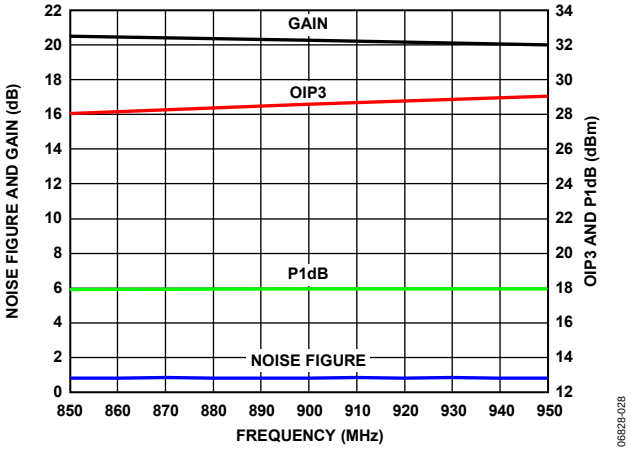


Figure 28. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

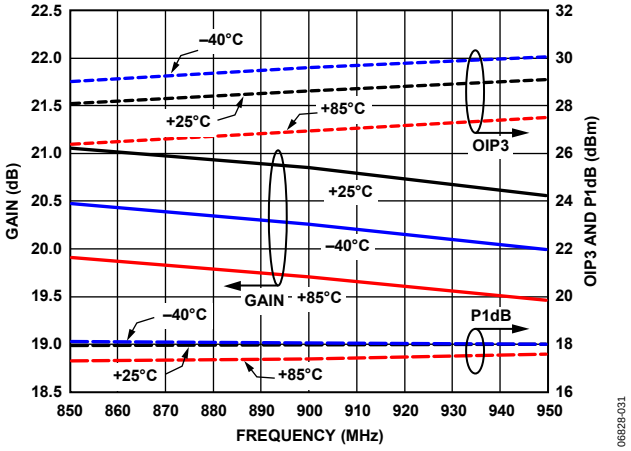


Figure 31. Gain, OIP3, and P1dB vs. Temperature

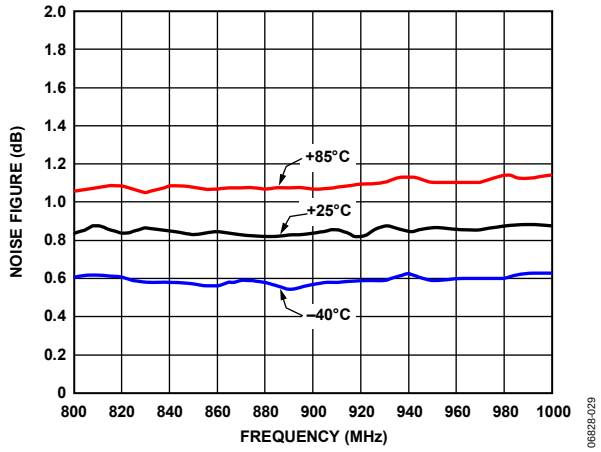


Figure 29. Noise Figure vs. Temperature

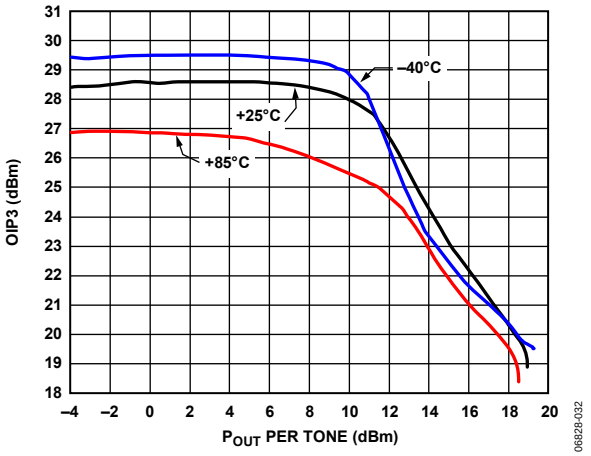


Figure 32. OIP3 vs. Output Power (P_{OUT}) and Temperature

1950 MHz, VPOS = 3 V

Matched for optimal noise figure, external matching circuit included.

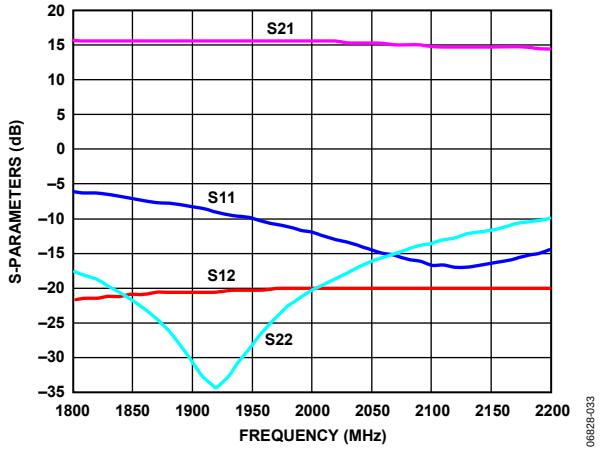


Figure 33. Typical S-Parameters, Log Magnitude

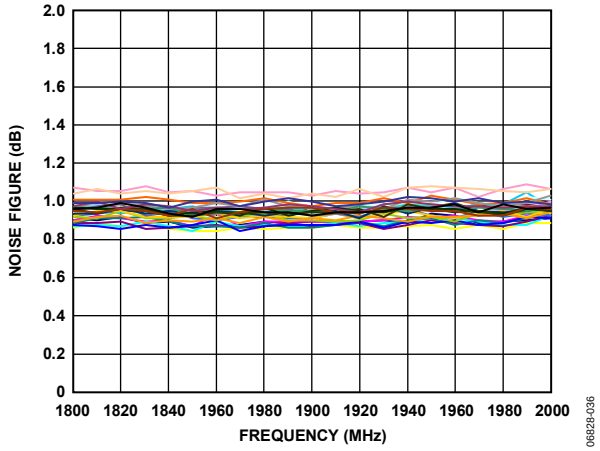


Figure 36. Noise Figure vs. Frequency at 25°C, Multiple Devices

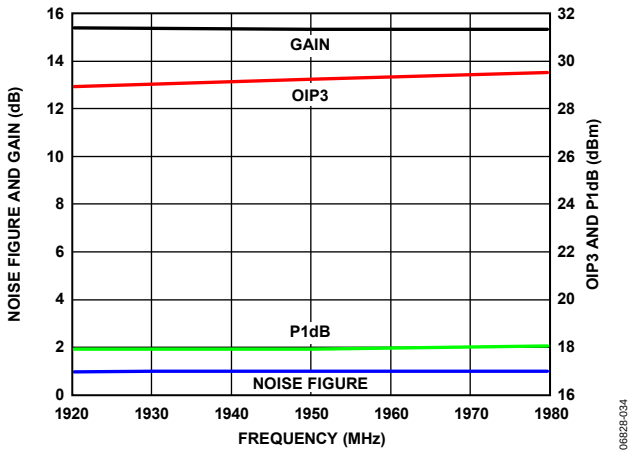


Figure 34. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

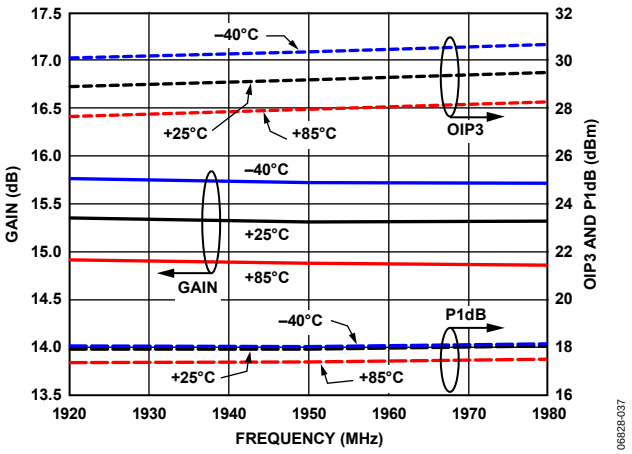


Figure 37. Gain, OIP3, and P1dB vs. Temperature

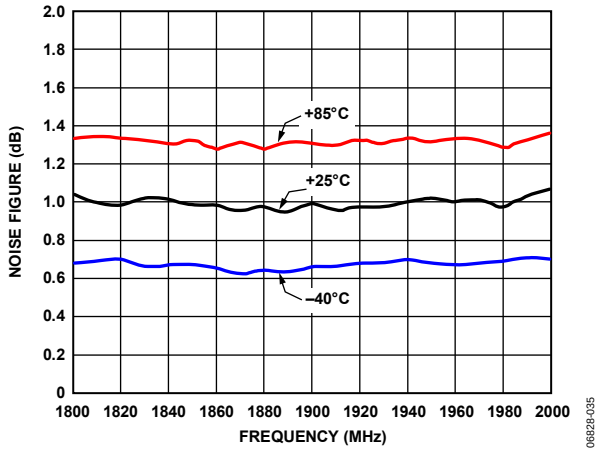


Figure 35. Noise Figure vs. Temperature

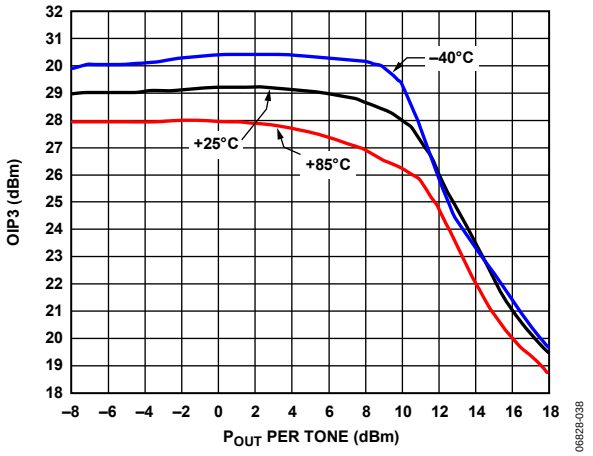


Figure 38. OIP3 vs. Output Power (P_{OUT}) and Temperature

2600 MHZ, VPOS = 3 V

Matched for optimal noise figure, external matching circuit included.

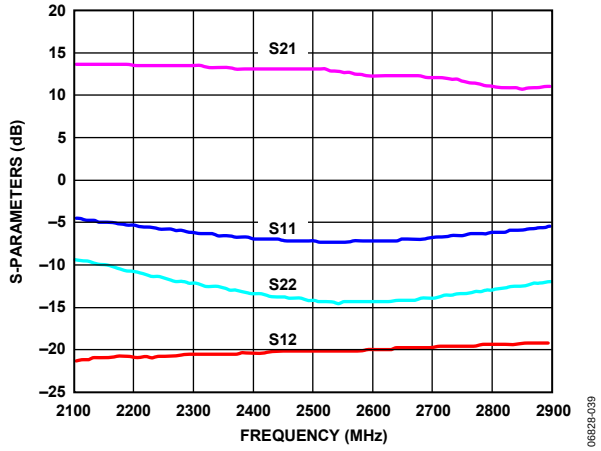


Figure 39. Typical S-Parameters, Log Magnitude

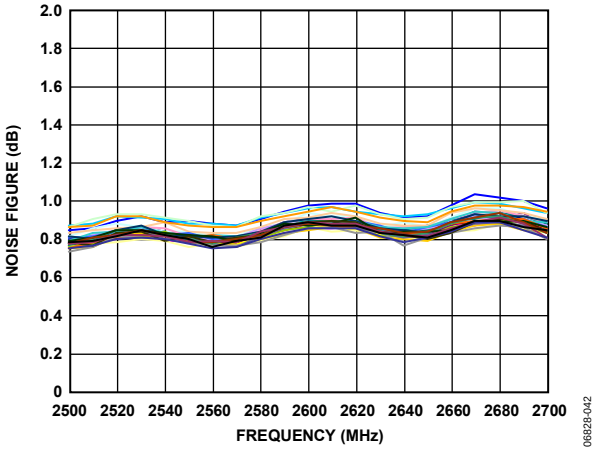


Figure 42. Noise Figure vs. Frequency at 25°C, Multiple Devices

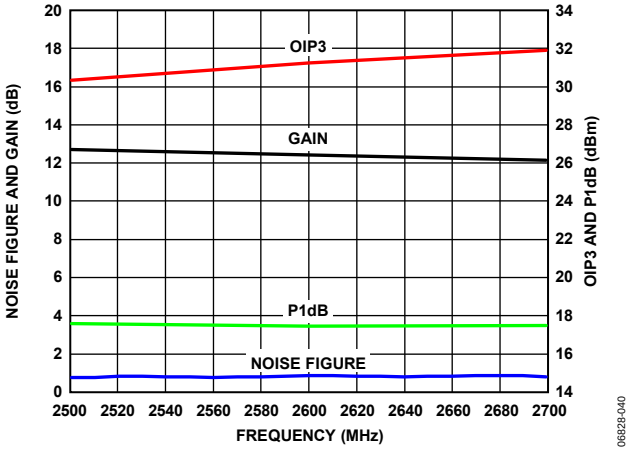


Figure 40. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

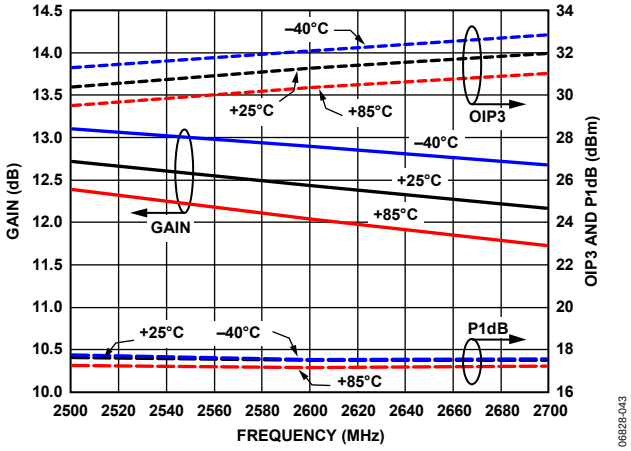


Figure 43. Gain, OIP3, and P1dB vs. Temperature

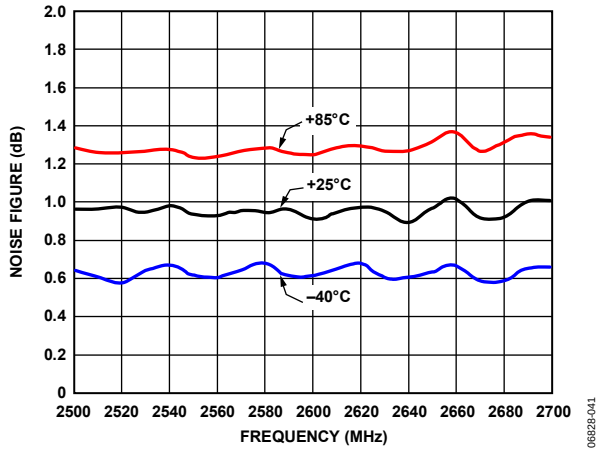


Figure 41. Noise Figure vs. Temperature

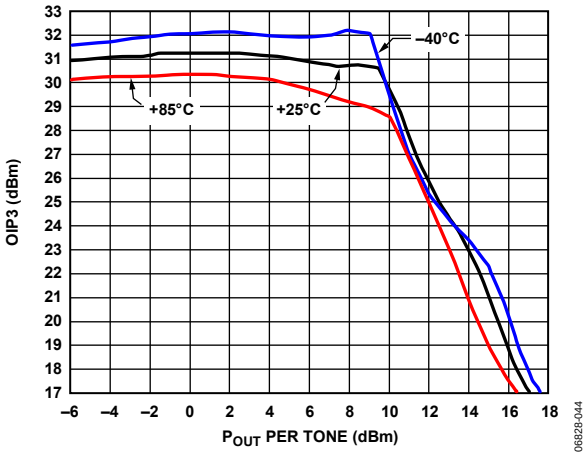


Figure 44. OIP3 vs. Output Power (P_{OUT}) and Temperature

3500 MHZ, VPOS = 3 V

Matched for optimal noise figure, external matching circuit included.

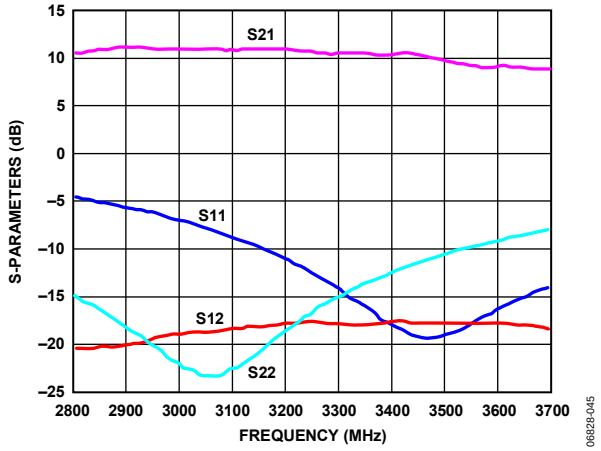


Figure 45. Typical S-Parameters, Log Magnitude

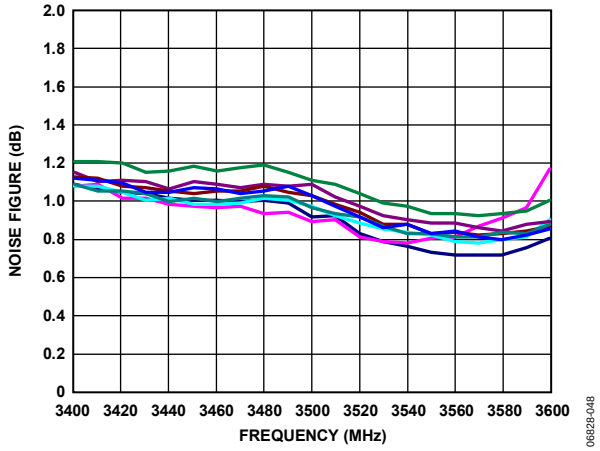


Figure 48. Noise Figure vs. Frequency at 25°C, Multiple Devices

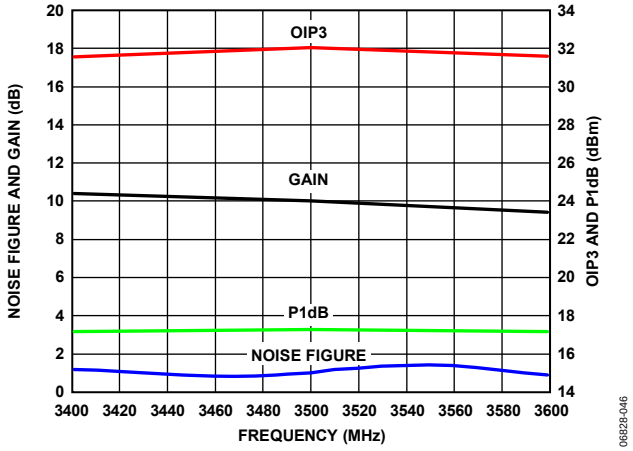


Figure 46. Noise Figure, Gain, OIP3, and P1dB vs. Frequency

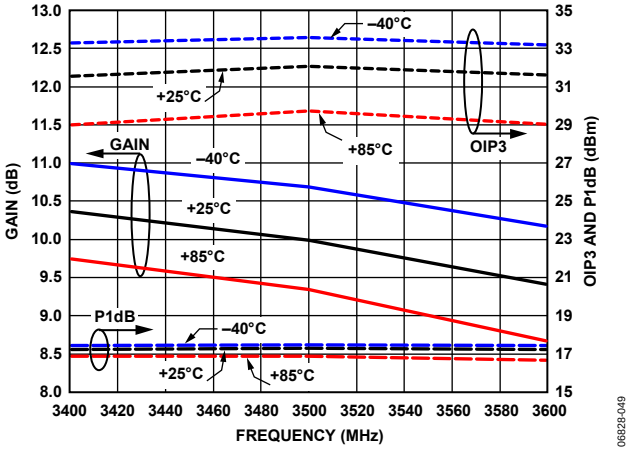


Figure 49. Gain, OIP3, and P1dB vs. Temperature

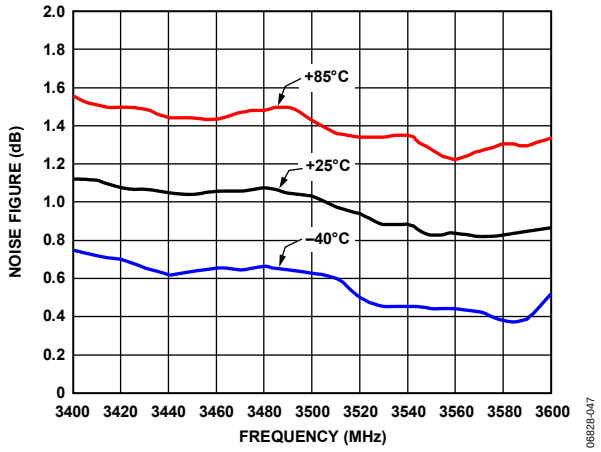


Figure 47. Noise Figure vs. Temperature

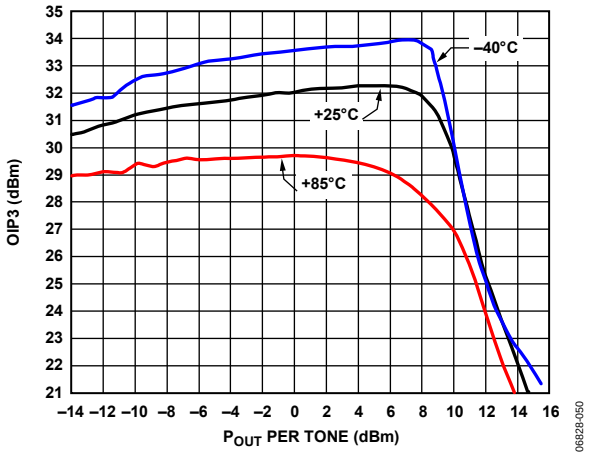


Figure 50. OIP3 vs. Output Power (P_{OUT}) and Temperature

DC CHARACTERISTICS

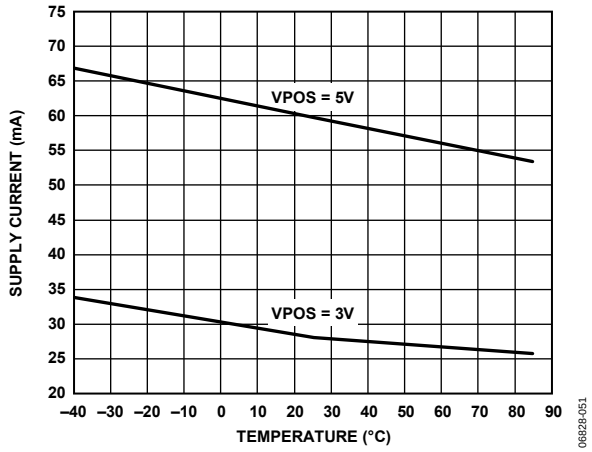


Figure 51. Supply Current vs. Temperature, 3 V and 5 V

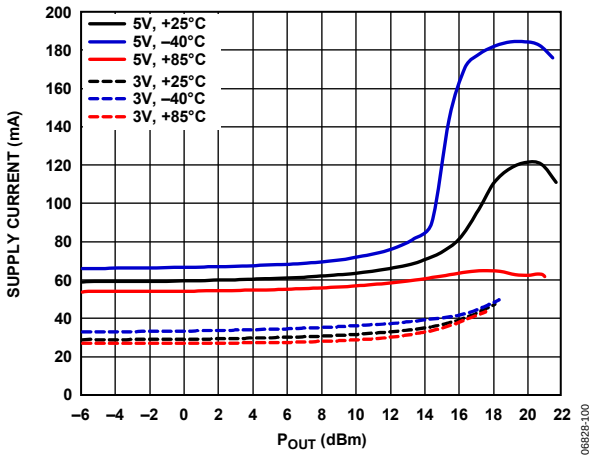


Figure 52. Supply Current vs. P_{OUT} and Temperature, 3 V and 5 V

BASIC CONNECTIONS

The basic connections for operating the ADL5521 are shown in Figure 53. Capacitor C5 provides the power supply decoupling. Inductor L1 (Coilcraft 0403HQ or 0402HP series) and Capacitor C1 (Murata High-Q GJM series or equivalent) provide the input impedance matching, and the output impedance matching is provided by either L2 or C3. Resistor R1 is used to set the supply current, and the value of R1 is indirectly proportional to the supply current (that is, increasing the value of R1 reduces the supply current). The recommended external components for the selected frequencies are listed in Table 7.

For 5 V applications where the input power exceeds the input compression point of approximately 7 dBm, a series resistor (R2) of at least 8 Ω, with a high power rating (0.2 W minimum), should be inserted on the VPOS line to protect the device from the input power overdrive. In this case, reduce resistor R1 from 1.3 kΩ to 600 Ω to keep the supply current at around 60 mA. With R2 = 8.2 Ω (Susumu RP1608S-8R2-F) and R1 = 600 Ω, the gain and noise figure for the ADL5521 are mostly unchanged. Table 6 lists OIP3 and P1dB at selected frequencies. For 3 V power supply applications, a series resistor is not necessary for the expected input overdrive powers up to 20 dBm.

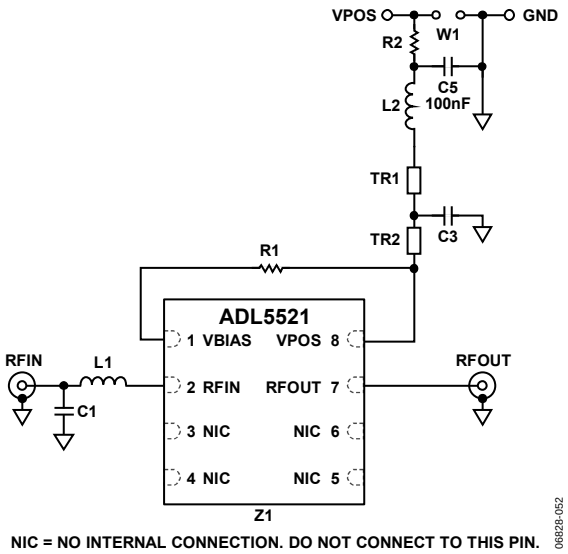


Figure 53. ADL5521 Basic Connections

Table 6. ADL5521 Performance at VPOS = 5 V, 25°C with R2 = 8.2 Ω and R1 = 600 Ω

Frequency (MHz)	Noise Figure (dB)	Gain (dB)	P1dB (dBm)	OIP3 (dBm) (P_{OUT} = 0 dBm)
900	0.9	20.8	20.8	34.0
1950	1.0	15.8	21.0	35.0
2600	1.0	13.0	20.6	35.0
3500	1.1	10.5	20.3	36.0

EVALUATION BOARD

Figure 54 shows the schematic of the ADL5521 evaluation board. The board is powered by a single supply, and dc bias can be applied to the board through clip-on leads at VPOS and GND or through a 2-pin connector, W1.

The evaluation board comes optimized at 1950 MHz from the factory, but it can be easily modified to work at any frequency between 400 MHz and 4 GHz. Table 7 lists the recommended components at various frequencies.

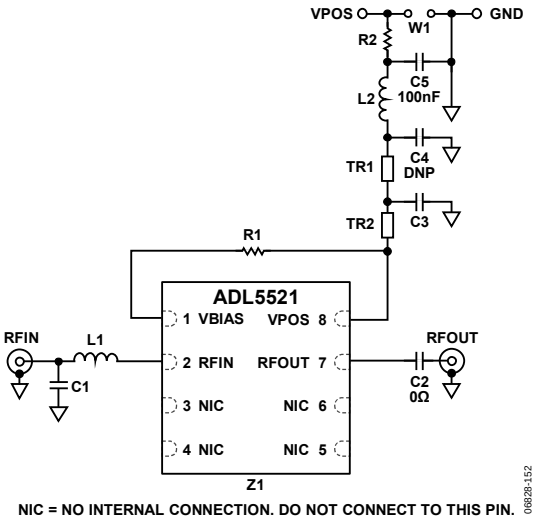


Figure 54. Evaluation Board Schematic

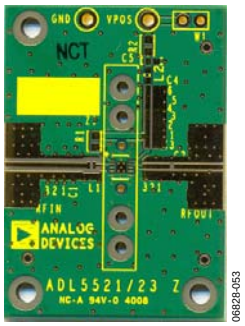


Figure 55. Evaluation Board Layout (Top View)

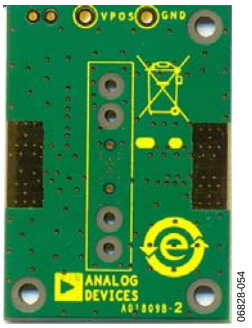


Figure 56. Evaluation Board Layout (Bottom View)

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 57 shows the recommended land pattern for ADL5521. To minimize thermal impedance, the exposed pad on the package underside is soldered down to a ground plane. If multiple ground layers exist, they are stitched together using vias (a minimum of five vias is recommended). Pin 3 to Pin 6 can be left unconnected or can be connected to ground. For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP).*

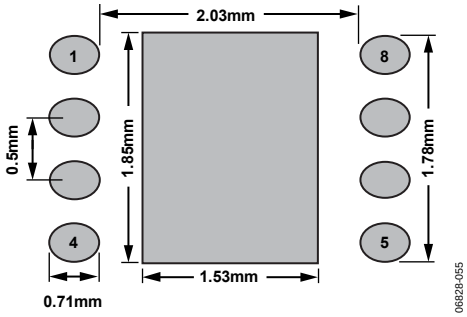


Figure 57. Recommended Land Pattern

Table 7. Recommended Components and Positions of Matching Components for Basic Connections Tuned for Optimal Noise

Frequency (MHz)	C1[1] (Size 0402)	C2 (Size 0402)	C3 (Size 0402)	C4 (Size 0402)	C5 (Size 0402)	L1[2] (Size 0403)	L2[2] (Size 0403)	R1[3] (Size 0603)	R2[4] (Size 0603)	TR1 (mm)	TR2 (mm)	C1 Position	C3 Position
500	Open	0 Ω	Open	Open	100 nF	9 nH	12 nH	1.3 kΩ	0 Ω	0	0	C1	N/A
900	2.4 pF	0 Ω	Open	Open	100 nF	8.2 nH	3.4 nH	1.3 kΩ	0 Ω	0	0	C1	N/A
1300	2.7 pF	0 Ω	1.0 nF	Open	100 nF	3.4 nH	0 Ω	1.3 kΩ	0 Ω	0	8.0 × 0.6	C1	6
1950	1.6 pF	0 Ω	1.0 nF	Open	100 nF	1.0 nH	0 Ω	1.3 kΩ	0 Ω	2.5 × 0.6	5.5 × 0.6	C1	4
2140	1.6 pF	0 Ω	1.0 nF	Open	100 nF	1.0 nH	0 Ω	1.3 kΩ	0 Ω	5.0 × 0.6	3.0 × 0.6	C1	2
2600	0.75 pF	0 Ω	1.0 nF	Open	100 nF	1.0 nH	0 Ω	1.3 kΩ	0 Ω	8.0 × 0.6	0	C1	C3
3500	0.5 pF	0 Ω	1.0 nF	Open	100 nF	2.4 pF[5]	0 Ω	1.3 kΩ	0 Ω	7.0 × 0.6	1 × 0.6	C1	1

[1] The Murata High-Q GJM series capacitor is recommended for C1.
[2] Coilcraft High Q 0403HQ or 0402HP inductors are recommended for L1 and L2.
[3] If R2 = 8 Ω, reduce R1 to 600 Ω.
[4] If R2 = 8 Ω, use a high power resistor (0.2 W rating minimum).
[5] Note that at 3500 MHz, a capacitor, not an inductor, is used at L1.

TUNING THE ADL5521 FOR OPTIMAL NOISE FIGURE

The ADL5521 is a monolithic low noise amplifier (LNA) in a 3 mm × 3 mm LFCSP. The evaluation board, as shipped from the factory, gives a noise figure of 0.9 dB over a bandwidth of several hundred megahertz. The specific frequency where optimal noise is reached depends on the tuning.

The bandwidth of the ADL5521 is 400 MHz to 4 GHz, although noise figure degrades above 2.5 GHz as the gain begins to roll off.

This section is based on Analog Devices, Inc., lab measurements. Although there are plots in which the Agilent Advanced Design System (ADS) environment is used, the data in these plots comes from Analog Devices lab measurements.

TUNING S22

Tuning of the LNA begins with S22 (output tuning). Tuning of the LNA output is done by placing reactive components on the bias line, referred to in the schematic in Figure 54 as VPOS.

On the LNA evaluation board, S22 tuning is achieved by either the use of an inductor (L2) on the bias line or a shunt capacitor (C3) on the bias line to ground. Typically, either L2 is required or C3, but not both.

The evaluation board uses a slider on the bias line to make tuning for S22 as easy as possible. The slider is an area of ground etch adjacent to the bias line that is clear of solder mask. The bias line in this area is also free of solder mask. This allows a capacitor (C3) to be placed anywhere on the bias line to ground, which provides easy and accurate tuning for S22.

Note that the PCB layout shows two capacitors, C3 and C4. Typically, only one of these capacitors is needed for good S22 tuning.

The slider can be seen in the LNA PCB layout in Figure 58 as the area near the red arrows to the right of the bias line. With a 0 Ω resistor in place of L2, moving a 1 nF capacitor from the top to the bottom effectively tunes S22 from 1400 MHz to 3500 MHz. Table 8 shows the component values and placement required for S22 tuning from 800 MHz to 3200 MHz. For lower frequencies, higher values of L2 can be used to tune S22, and for frequencies from 3.2 GHz to 4.0 GHz, smaller values of capacitors can be used on the slider.

Table 8. Capacitor and Inductor Tuning and Placement for LNA S22 Tuning

Frequency (MHz)	L2	C3	C3 Placement
800	3.4 nH	Open	N/A
1400	0 Ω	1 nF	6
2000	0 Ω	1 nF	4
2400	0 Ω	1 nF	3
2800	0 Ω	1 nF	2
3200	0 Ω	1 nF	1

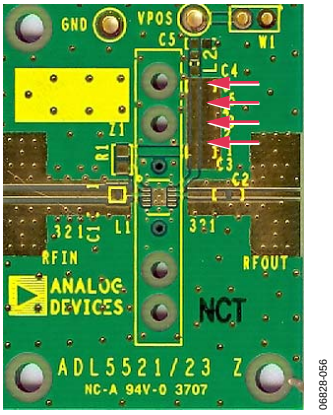


Figure 58. PCB Layout for LNA Evaluation Board (Note Slider on Bias Line with Capacitor Placement for S22 Tuning Noted by Arrows)

TUNING THE LNA INPUT FOR OPTIMAL GAIN

LNAs are generally tuned for either gain or noise optimization, or some trade-off between the two. One figure of merit of an LNA is how much trade-off must be made for one of these parameters to optimize the other. With the ADL5521, an S11 of 6 dB to 8 dB at the input to the matching network can still be achieved typically when optimizing for noise.

For optimal gain matching, the goal is to use a matching network that converts the input impedance of the LNA to the characteristic impedance of the system, typically 50 Ω. Correct tuning for gain matching results in a conjugate match. That is, the impedance of the matching network at the LNA input, looking back toward the generator, is always the complex conjugate of the LNA input impedance when matched for gain.

Once S11*, the complex conjugate of S11, is known, a matching circuit must be found that transforms the 50 Ω system impedance into the conjugate S11 impedance. To do this, the designer starts at the origin of the Smith Chart circle and finds components that move the 50 Ω match to S11*.

The related impedances for gain matching are shown in Figure 59. A Smith Chart representation of the conjugate match is shown in Figure 60.

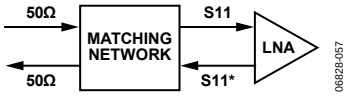


Figure 59. Matching LNA Input for Gain

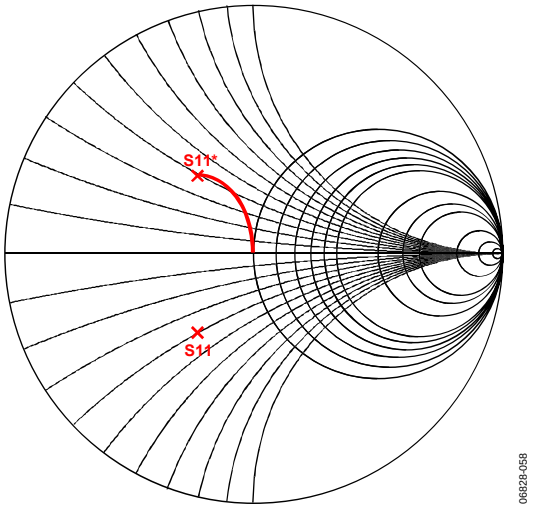


Figure 60. Smith Chart Representation of Conjugate Match

TUNING THE LNA INPUT FOR OPTIMAL NOISE FIGURE

The point in the Smith Chart at which matching for optimal noise occurs is typically referred to as gamma optimal or Γ_{OPT}. Typically, it is significantly different from the gain matching point; finding Γ_{OPT} is not as obvious as the gain match. Γ_{OPT} is a function of the semiconductor structure and characteristics of the LNA. The fabrication facility that produces the LNA typically has this information. Γ_{OPT} can also be determined by doing source pull testing in the lab.

Noise matching for the ADL5521 is very easy because the area of the Smith Chart where the noise figure is optimal or near optimal is not confined to a narrow area around Γ_{OPT}. This is very advantageous because it means that component variations play a smaller part in the board-to-board variation of noise figure.

The matching area for optimal noise for the ADL5521 is shown in Figure 61. Note that textbooks usually define noise circles as a conjugate match. However, for the purpose of this data sheet, the circle is a direct match. To find the correct matching circuit, the designer must start with the S11 of the LNA and select components that move the S11 to within this circle.

An important aspect of the overall ADL5521 ease of tuning is that as long as S22 is matched for a particular frequency, the noise matching area remains very consistent in its placement for that frequency. If S22 is matched, take the measured S11 and move it into the red circle shown in Figure 61 for optimal noise matching.

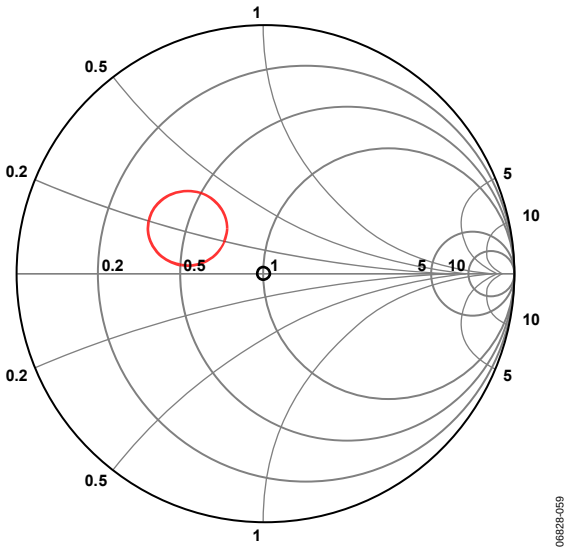


Figure 61. Area of Optimal Noise Matching for ADL5521

S11 OF THE LNA WITH S22 MATCHED

To determine the correct matching circuit for optimal noise, look at the results of S11 for the various frequencies at which S22 was tuned earlier in the Tuning S22 section. Once S11 is determined for a particular frequency, find the matching components that provided that match. Figure 63 and Figure 64 show S11 for the various frequencies. Again, these measurements are all based on S22 being matched at that particular frequency. Note that, for the examples shown in Figure 63 and Figure 64, S11 is either in the lower left quadrant of the Smith Chart or slightly into the upper left. To move the impedance in the given noise circle, a series L component at the LNA input is required. The L values in the examples differ, but a correct L value moves the match along the constant R circle up into the upper left quadrant of the Smith Chart.

A shunt capacitor can then be added to move the match along a constant admittance line, down and to the right, directly into the center of the noise circle given in Figure 61.

The solution for the structure of the match for the examples in Figure 63 and Figure 64 is a series L to the input of the LNA and a shunt capacitor at the generator end of this inductor. The recommended components for matching at various frequencies are shown in Table 7.

An example of the effect of the series L, shunt C match, based on the 800 MHz example, is given in Figure 62. This example uses the output from the Agilent ADS Smith Chart tool.

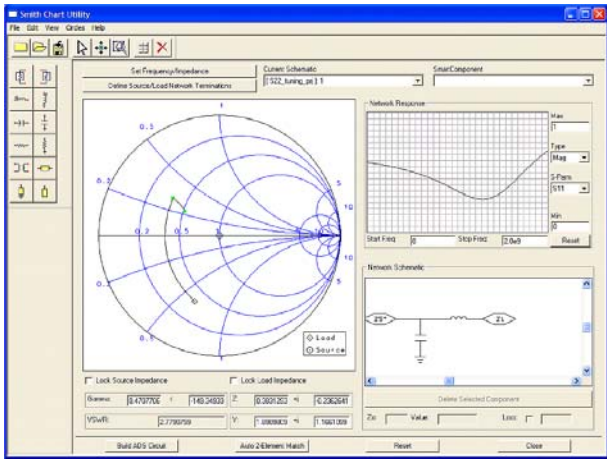


Figure 62. Example of Series L, Shunt C Matching Network for Γ_{OPT}

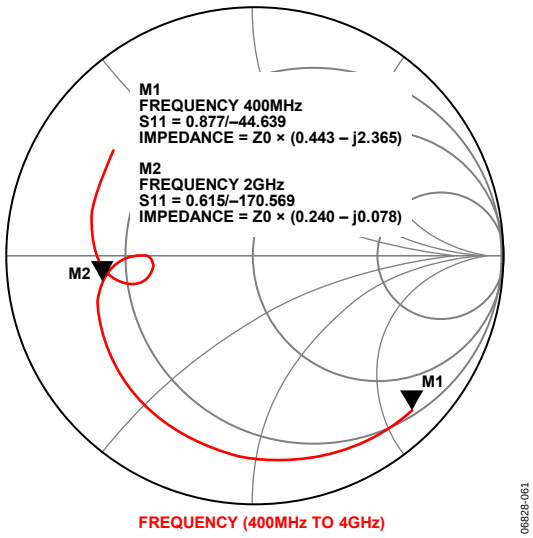


Figure 63. S11 of ADL5521 with S22 Matched at 2 GHz

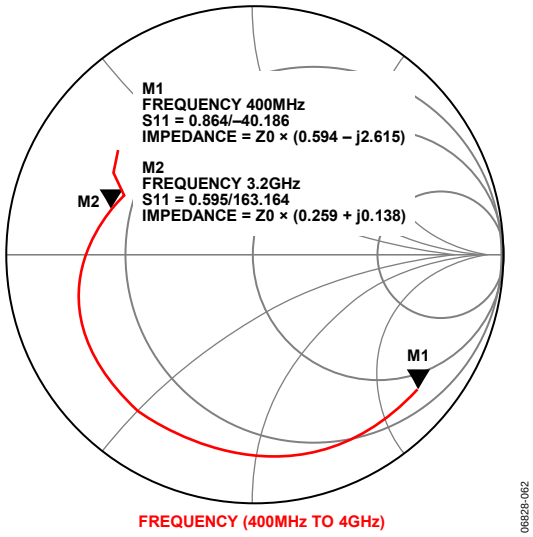


Figure 64. S11 of ADL5521 with S22 Matched at 3.2 GHz

OUTLINE DIMENSIONS

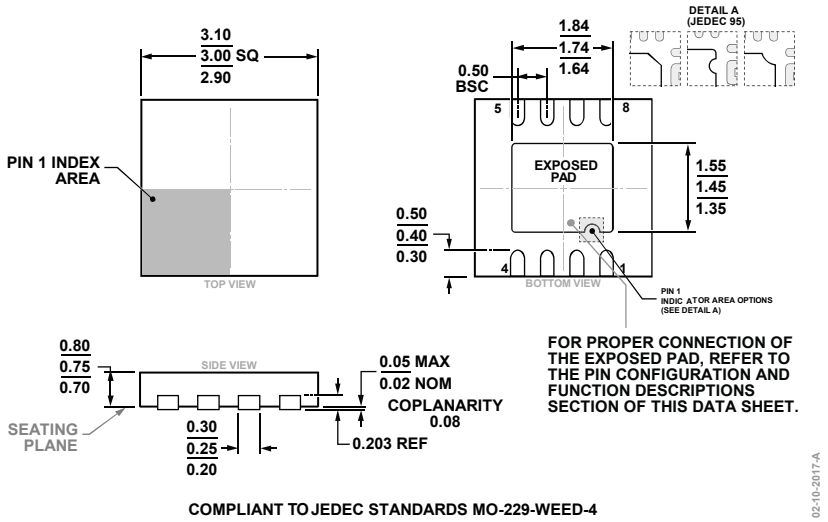


Figure 65. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADL5521ACPZ-R7	−40°C to +85°C	8-Lead LFCSP, 7″ Tape and Reel	CP-8-13	Q1G
ADL5521-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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