DC to 6 GHz Envelope and TruPwr RMS Detector

Data Sheet

ADL5511

FEATURES

- Envelope tracking RF detector with output proportional to input voltage
- Separate TruPwr rms output
- No balun or external tuning required
- Excellent temperature stability
- Input power dynamic range of 47 dB
- Input frequency range from dc to 6 GHz
- 130 MHz envelope bandwidth
- Envelope delay: 2 ns
- Single-supply operation: 4.75 V to 5.25 V
- Supply current: 21.5 mA
- Power-down mode: 130 µW

APPLICATIONS

- RMS power and envelope detection of W-CDMA, CDMA2000, LTE, and other complex waveforms
- Drain modulation based power amplifier linearization
- Power amplifier linearization employing envelope-tracking methods

FUNCTIONAL BLOCK DIAGRAM

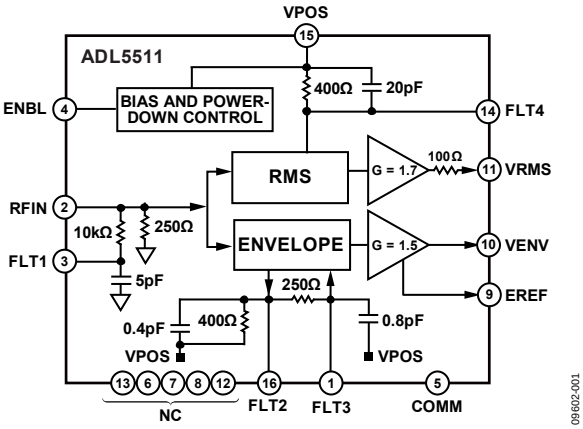

Figure 1.

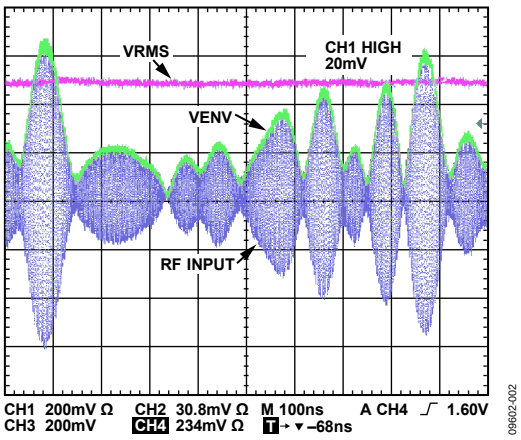

Figure 2. RMS and Envelope Response to a 20 MHz QPSK-Based LTE Carrier (Test Model E-TM1_1_20MHz)

GENERAL DESCRIPTION

The ADL5511 is an RF envelope and TruPwr™ rms detector. The envelope output voltage is presented as a voltage that is proportional to the envelope of the input signal. The rms output voltage is independent of the peak-to-average ratio of the input signal.

The rms output is a linear-in-V/V voltage with a conversion gain of 1.9 V/V rms at 900 MHz. The envelope output has a conversion gain of 1.46 V/V at 900 MHz and is referenced to an internal 1.1 V reference voltage, which is available on the EREF pin.

The ADL5511 can operate from dc to 6 GHz on signals with envelope bandwidths up to 130 MHz.

The extracted envelope can be used for RF power amplifier (PA) linearization and efficiency enhancements and the rms output can be used for rms power measurement. The high rms accuracy and fast envelope response are particularly useful for envelope detection and power measurement of broadband, high peak-to-average signals that are used in CDMA2000, W-CDMA, and LTE systems.

The ADL5511 operates from −40°C to +85°C and is available in a 16-lead, 3 mm × 3 mm LFCSP package.

Rev. D
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REVISION HISTORY

7/2018—Rev. C to Rev. D

Changes to Figure 55 and Figure 56 ... 23

7/2017—Rev. B to Rev. C

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5/2014—Rev. A to Rev. B

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2/2012—Rev. 0 to Rev. A

Changes to Equation 4 ... 19
Updated Outline Dimensions ... 26

7/2011—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{POS} = 5 V, C_{FLT4} = 100 nF, 75 Ω shunt termination resistor to ground on (ac-coupled) RFIN, three-point calibration on V_{ENV} and V_{RMS} at +5 dBm, −15 dBm, and −26 dBm, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	DC		6	GHz
ENVELOPE CONVERSION (100 MHz)	Input RFIN to output ($V_{ENV} - V_{EREF}$)				
Input Range (±1 dB Error)	CW input		46		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−29		dBm
Conversion Gain	V_{ENV} = (Gain × V_{IN}) + Intercept		1.42		V/V rms
Intercept			−5		mV
Output Voltage	$V_{ENV} - V_{EREF}$				
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.00		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		26		mV
RMS Conversion	Input RFIN to output (V_{RMS})				
Input Range (±1 dB Error)	CW input		46		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−29		dBm
Conversion Gain	V_{RMS} = (Gain × V_{IN}) + Intercept		1.92		V/V rms
Intercept			11		mV
Output Voltage					
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.38		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		53		mV
ENVELOPE CONVERSION (900 MHz)	Input RFIN to output ($V_{ENV} - V_{EREF}$)				
Input Range (±1 dB Error)	CW input		46		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−29		dBm
Conversion Gain	V_{ENV} = (Gain × V_{IN}) + Intercept		1.46		V/V rms
Intercept			−5		mV
Output Voltage	$V_{ENV} - V_{EREF}$				
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.02		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		26		mV
RMS Conversion	Input RFIN to output (V_{RMS})				
Input Range (±1 dB Error)	CW input		46		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−29		dBm
Conversion Gain	V_{RMS} = (Gain × V_{IN}) + Intercept		1.9		V/V rms
Intercept			13		mV
Output Voltage					
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.35		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		54		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ENVELOPE CONVERSION (1900 MHz)	Input RFIN to output ($V_{ENV} - V_{EREF}$)				
Input Range (±1 dB Error)	CW input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	$V_{ENV} = (Gain \times V_{IN}) + Intercept$		1.5		V/V rms
Intercept			−5		mV
Output Voltage	$V_{ENV} - V_{EREF}$				
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.05		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		28		mV
RMS Conversion	Input RFIN to output (V_{RMS})				
Input Range (±1 dB Error)	CW input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	$V_{RMS} = (Gain \times V_{IN}) + Intercept$		1.96		V/V rms
Intercept			14		mV
Output Voltage					
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.40		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		56		mV
ENVELOPE CONVERSION (2140 MHz)	Input RFIN to output ($V_{ENV} - V_{EREF}$)				
Input Range (±1 dB Error)	CW Input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	$V_{ENV} = (Gain \times V_{IN}) + Intercept$		1.53		V/V rms
Intercept			−5		mV
Output Voltage	$V_{ENV} - V_{EREF}$				
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.07		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		28		mV
RMS Conversion	Input RFIN to output (V_{RMS})				
Input Range (±1 dB Error)	CW input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	$V_{RMS} = (Gain \times V_{IN}) + Intercept$		1.99		V/V rms
Intercept			13		mV
Output Voltage					
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.42		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		56		mV
ENVELOPE CONVERSION (2600 MHz)	Input RFIN to output ($V_{ENV} - V_{EREF}$)				
Input Range (±1 dB Error)	CW Input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	$V_{ENV} = (Gain \times V_{IN}) + Intercept$		1.56		V/V rms
Intercept			−3		mV
Output Voltage	$V_{ENV} - V_{EREF}$				
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.10		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		30		mV
RMS Conversion	Input RFIN to output (V_{RMS})				
Input Range (±1 dB Error)	CW input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	$V_{RMS} = (Gain \times V_{IN}) + Intercept$		2.04		V/V rms
Intercept			15		mV
Output Voltage					

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.46		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		58		mV
ENVELOPE CONVERSION (3500 MHz)	Input RFIN to output ($V_{ENV} - V_{EREF}$)				
Input Range (±1 dB Error)	CW Input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	V_{ENV} = (Gain × V_{IN}) + Intercept		1.56		V/V rms
Intercept			−5		mV
Output Voltage	$V_{ENV} - V_{EREF}$				
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.10		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		28		mV
RMS Conversion	Input RFIN to output (V_{RMS})				
Input Range (±1 dB Error)	CW input		47		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−30		dBm
Conversion Gain	V_{RMS} = (Gain × V_{IN}) + Intercept		2.03		V/V rms
Intercept			12		mV
Output Voltage					
High Power In	P_{IN} = +10 dBm, +707 mV rms		1.46		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		57		mV
ENVELOPE CONVERSION (6000 MHz)	Input RFIN to output ($V_{ENV} - V_{EREF}$)				
Input Range (±1 dB Error)	CW Input		45		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−28		dBm
Conversion Gain	V_{ENV} = (Gain × V_{IN}) + Intercept		0.85		V/V rms
Intercept			−10		mV
Output Voltage	$V_{ENV} - V_{EREF}$				
High Power In	P_{IN} = +10 dBm, +707 mV rms		0.60		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		11		mV
RMS Conversion	Input RFIN to output (V_{RMS})				
Input Range (±1 dB Error)	CW input		45		dB
Maximum Input Level	±1 dB error		17		dBm
Minimum Input Level	±1 dB error		−28		dBm
Conversion Gain	V_{RMS} = (Gain × V_{IN}) + Intercept		1.11		V/V rms
Intercept			7		mV
Output Voltage					
High Power In	P_{IN} = +10 dBm, +707 mV rms		0.80		V
Low Power In	P_{IN} = −20 dBm, +22.4 mV rms		35		mV
ENVELOPE OUTPUT	Pin VENV				
Maximum Output Voltage	V_{POS} = 5 V, R_{LOAD} ≥ 500 Ω, C_{LOAD} ≤ 10 pF		3.5		V
Output Offset	No signal at RFIN		2		mV
Envelope Bandwidth	3 dB		130		MHz
Pulse Response Time	Input level = no signal to 5 dBm, 10% to 90% response time		4		ns
Envelope Delay	RFIN to VENV		2		ns
Output Current Drive	Load = 500 Ω||10 pF		15		mA
RMS OUTPUT	Pin VRMS				
Maximum Output Voltage	V_{POS} = 5 V, R_{LOAD} ≥ 10 kΩ		3.8		V
Output Offset	No signal at RFIN		23		mV
Output Current Drive	Load = 1.3 kΩ		3		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power	4.75 V ≤ V_{POS} ≤ 5.25 V	3.6			V
Logic Level to Disable Power	4.75 V ≤ V_{POS} ≤ 5.25 V			2.0	V
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	4.75		5.25	V
Quiescent Current	RFIN < −10 dBm, ENBL high		21.5		mA
	RFIN < −10 dBm, ENBL low		26		µA
	RFIN = 15 dBm, ENBL high		43.8		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
ENBL	0 V, VPOS
RFIN (RFIN AC-Coupled)	5.6 V p-p
Equivalent RF Power (Peak Envelope Power or CW), re: 50 Ω	19 dBm
Internal Power Dissipation	580 mW
θ_{JA}	68.9°C/W
θ_{JC}	17.5°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
ESD (FICDM)	1250 V
ESD (HBM)	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

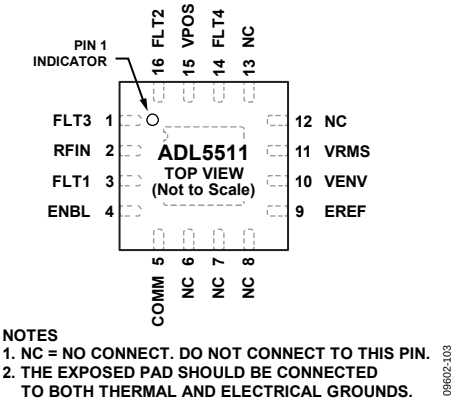


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 16	FLT3, FLT2	External Envelope Filter. With the FLT3 and FLT2 pins not connected, two internal low-pass filters (operating in series) with corner frequencies of approximately 1000 MHz and 800 MHz remove the residual RF carrier (at two times the original input frequency) from the envelope signal. External, supply-referenced capacitors connected to FLT3 and FLT2 can be used to reduce this corner frequency. See the Basic Connections section for more information.
2	RFIN	RF Input. RFIN should be externally ac-coupled. RFIN has a nominal input impedance of 250 Ω. To achieve a broadband 50 Ω input impedance, an external 75 Ω shunt resistor should be connected between the source side of the ac coupling capacitor and ground.
3	FLT1	External Envelope Filter. A capacitor to ground on this pin can be used to reduce the nominal minimum input frequency. The capacitance on this pin helps to reduce any residual RF carrier presence on the EREF output pin. See the Basic Connections section for more information.
4	ENBL	Device Enable/Disable. A logic high on this pin enables the device. A logic low on this pin disables the device.
5	COMM	Device Ground. Connect to a low impedance ground plane.
6, 7, 8, 12, 13	NC	Do not connect to these pins.
9	EREF	Reference Voltage for Envelope Output. The nominal value is 1.1 V.
10	VENV	Envelope Output. The voltage on this pin represents the envelope of the input signal and is referred to EREF. VENV can source a current of up to 15 mA. Capacitive loading should not exceed 10 pF to achieve the specified envelope bandwidth. Lighter loads should be chosen when possible. The nominal output voltages on EREF and VENV with no signal present track with temperature. For dc-coupled envelope output, EREF should be used as a reference giving the true envelope voltage of $V_{ENV} - V_{EREF}$. For ac coupling of the envelope output, the VENV pin can drive a 50 Ω load, if maximum current drive capability of 15 mA is not exceeded. See the Output Drive Capability and Buffering section for more information.
11	VRMS	RMS Output Pin. This voltage is ground referenced and has a nominal swing of 0 V to 3.8 V. V_{RMS} has a linear-in-V/V transfer function with a nominal slope of 2 V/V.
14	FLT4	RMS Averaging Capacitor. Connect between FLT4 and VPOS.
15	VPOS	Supply Voltage Pin. Operational range is 4.75 V to 5.25 V with a supply current of 21.5 mA.
0	EP	Exposed Pad. The exposed pad should be connected to both thermal and electrical grounds.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{POS} = 5 V, C_{FLT4} = 100 nF, 75 Ω shunt termination resistor to ground on (ac-coupled) RFIN, T_A = +25°C (black), −40°C (blue), +85°C (red), three-point calibration on V_{ENV} and V_{RMS} at +5 dBm, −15 dBm, and −26 dBm, unless otherwise noted.

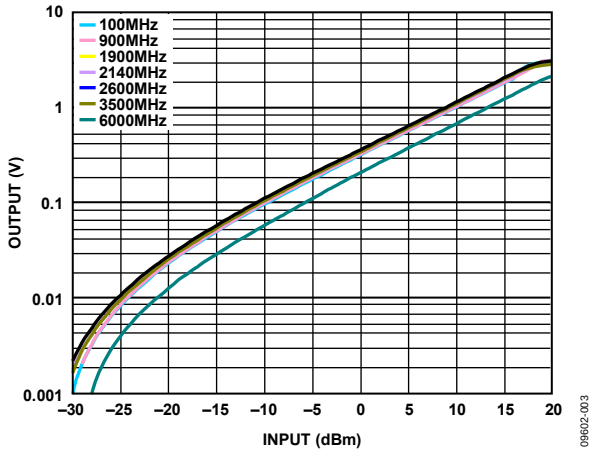


Figure 4. $V_{ENV} - V_{EREF}$ Output vs. Input Level, at Various Frequencies at 25°C, Supply 5 V

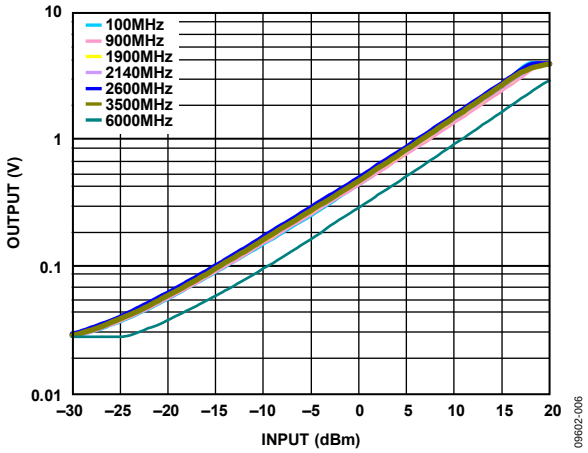


Figure 7. V_{RMS} Output vs. Input Level, at Various Frequencies at 25°C, Supply 5 V

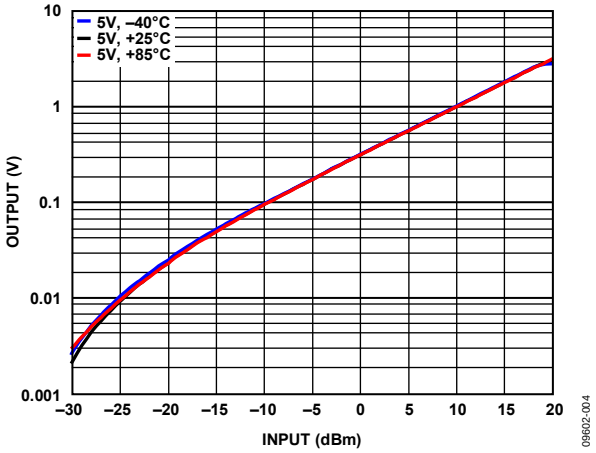


Figure 5. $V_{ENV} - V_{EREF}$ Output vs. Input Level and Temperature at 1900 MHz, Supply 5 V

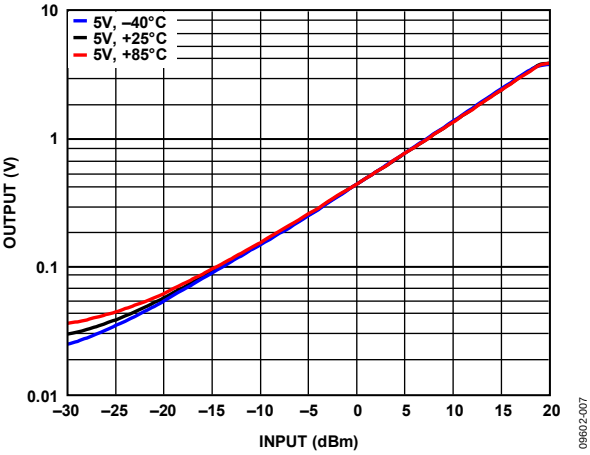


Figure 8. V_{RMS} Output vs. Input Level and Temperature at 1900 MHz, Supply 5 V

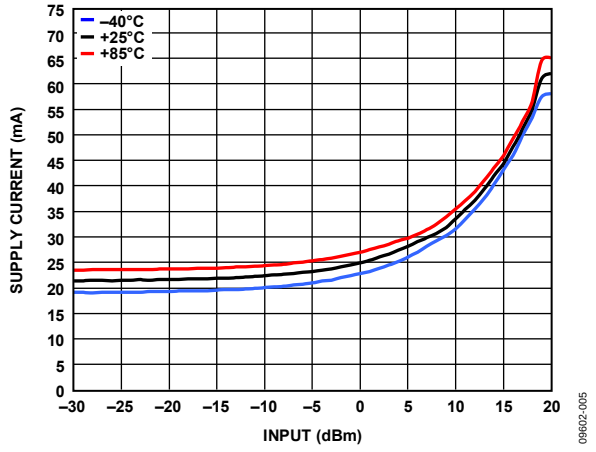


Figure 6. Supply Current vs. Input Level and Temperature

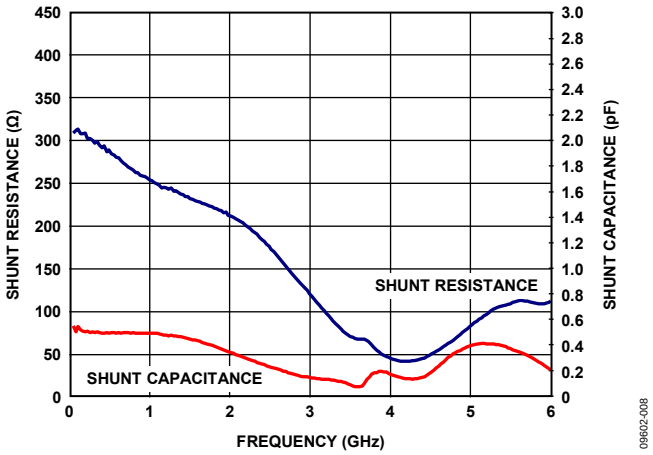


Figure 9. Input Impedance vs. Frequency

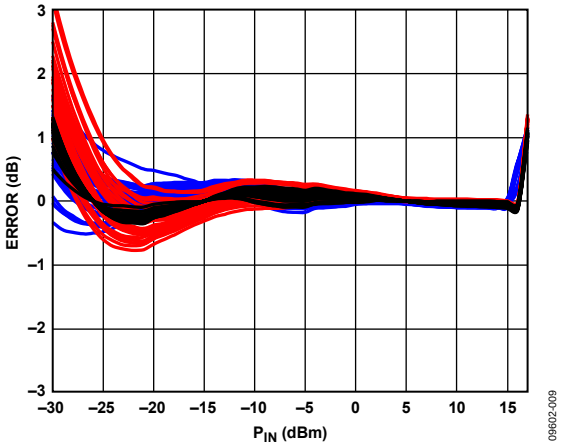


Figure 10. V_{ENV} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 100 MHz

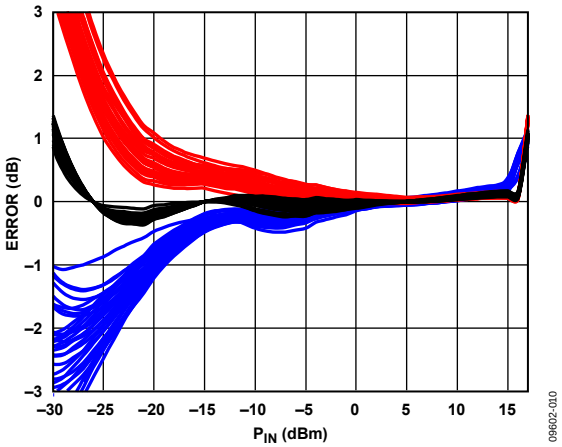


Figure 11. V_{RMS} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 100 MHz

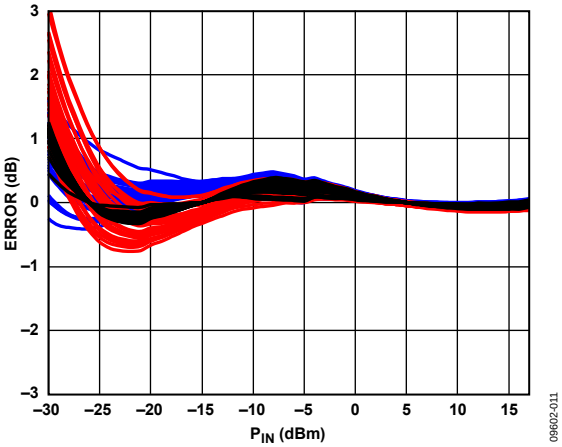


Figure 12. V_{ENV} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 900 MHz

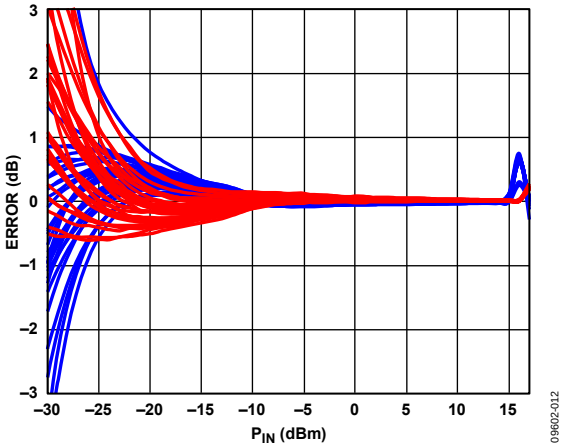


Figure 13. V_{ENV} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 100 MHz

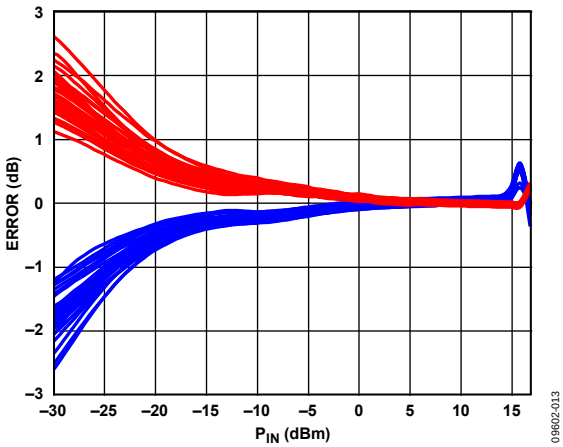


Figure 14. V_{RMS} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 100 MHz

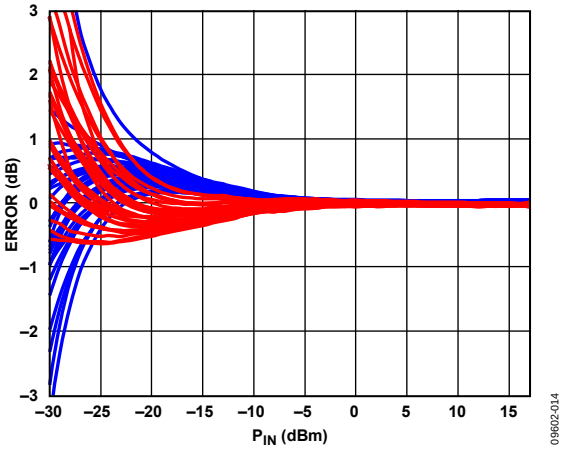


Figure 15. V_{ENV} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 900 MHz

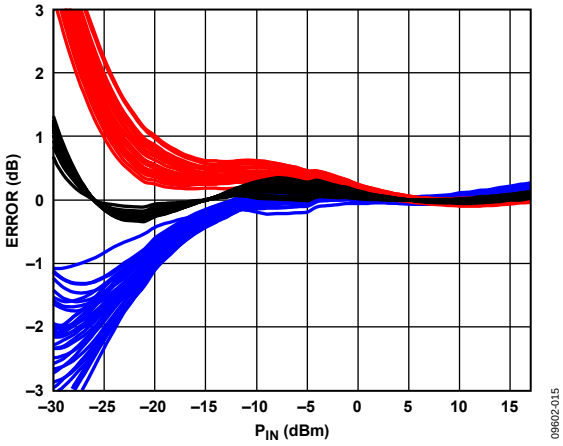


Figure 16. V_{RMS} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 900 MHz

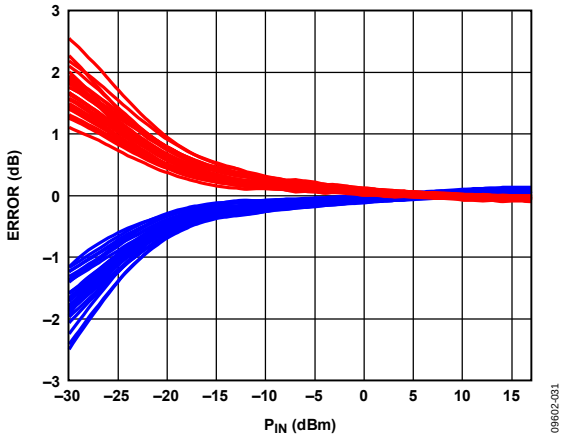


Figure 19. V_{RMS} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 900 MHz

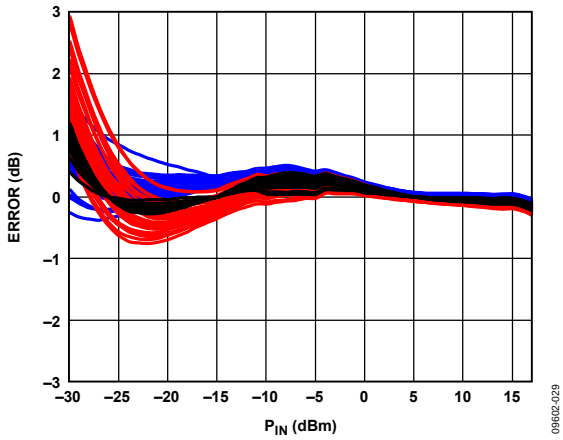


Figure 17. V_{ENV} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 1900 MHz

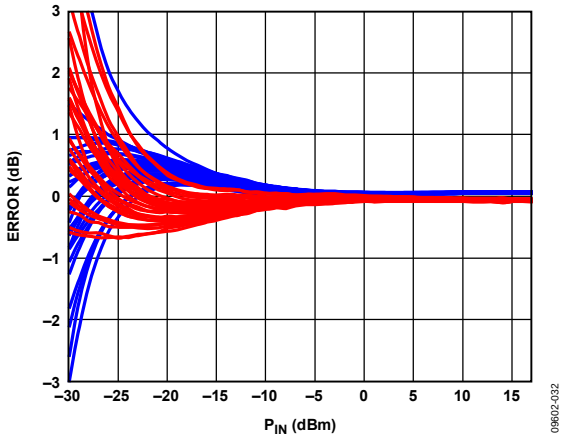


Figure 20. V_{ENV} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 1900 MHz

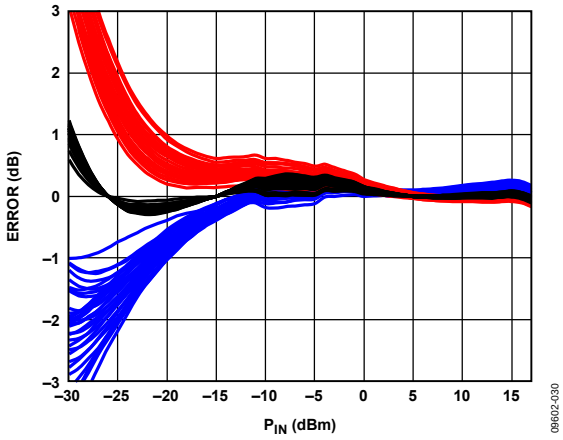


Figure 18. V_{RMS} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 1900 MHz

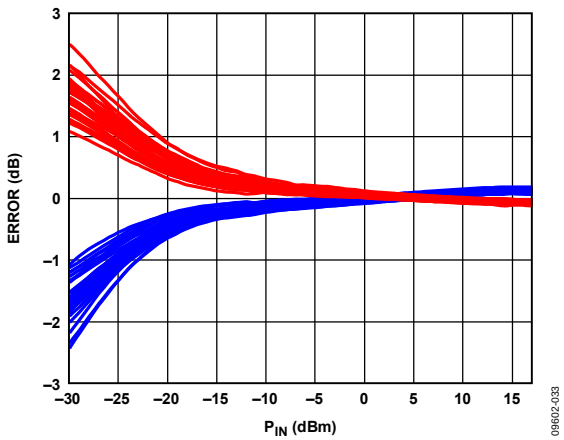


Figure 21. V_{RMS} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 1900 MHz

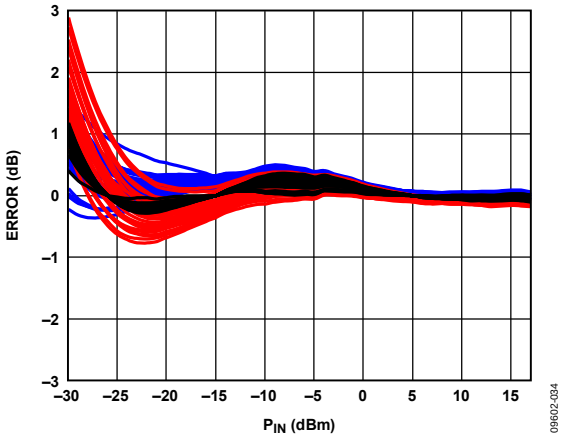


Figure 22. V_{ENV} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 2140 MHz

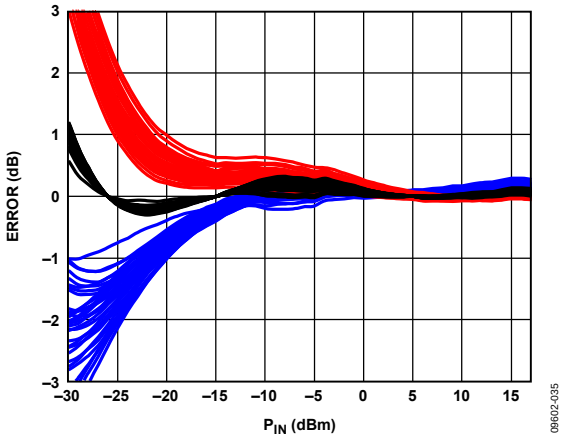


Figure 23. V_{RMS} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 2140 MHz

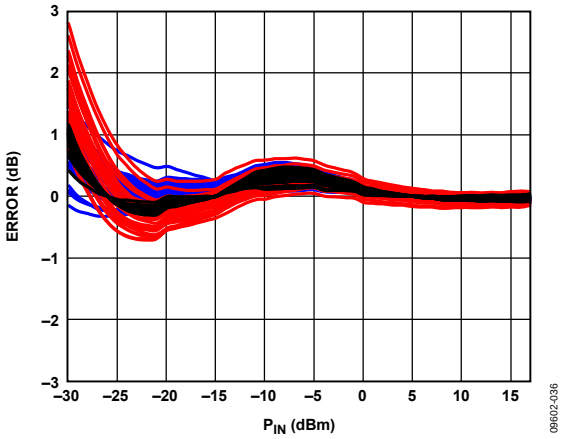


Figure 24. V_{ENV} Output Temperature Drift from +25°C, Three-Point Calibration for Multiple Devices at −40°C, +25°C, and +85°C at 2600 MHz

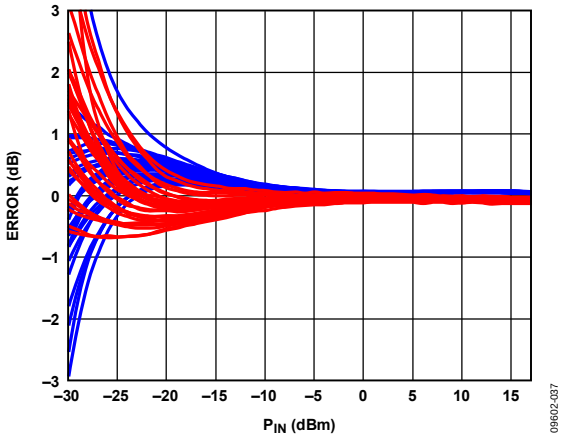


Figure 25. V_{ENV} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 2140 MHz

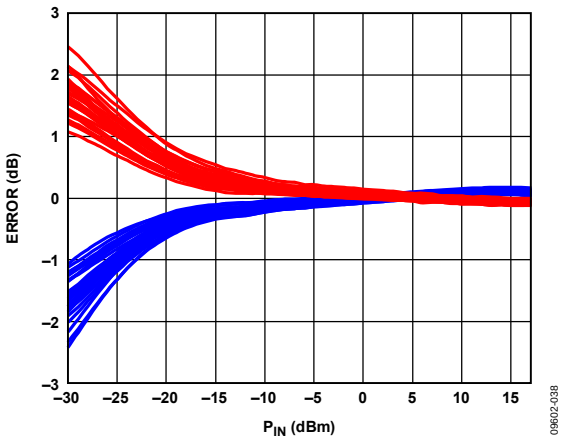


Figure 26. V_{RMS} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 2140 MHz

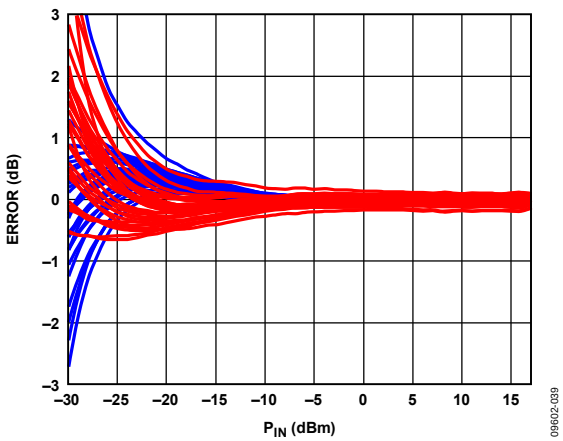


Figure 27. V_{ENV} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 2600 MHz

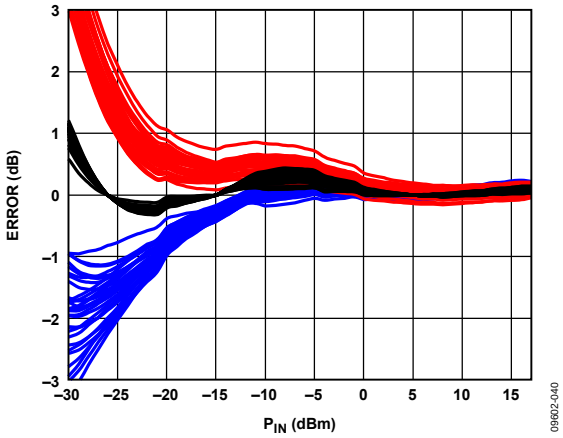


Figure 28. V_{RMS} Output Temperature Drift from +25°C Linear Reference for Multiple Devices at −40°C, +25°C, and +85°C, 2600 MHz Frequency

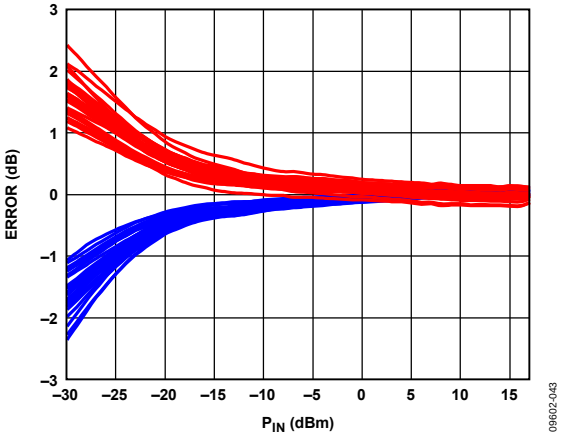


Figure 31. V_{RMS} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 2600 MHz

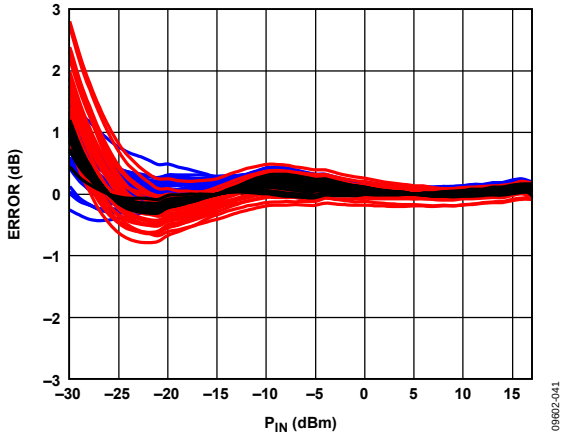


Figure 29. V_{ENV} Output Temperature Drift from +25°C Linear Reference for Multiple Devices at −40°C, +25°C, and +85°C, 3500 MHz Frequency

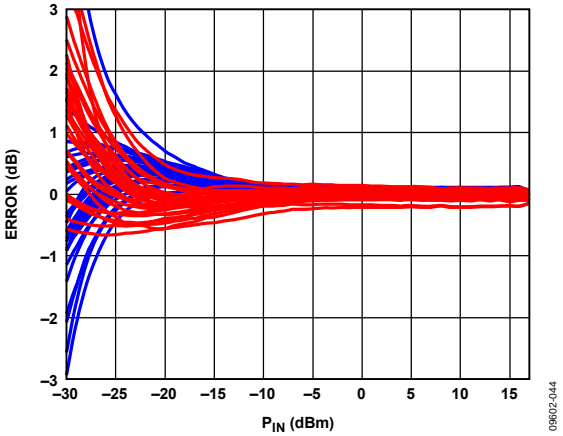


Figure 32. V_{ENV} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 3500 MHz

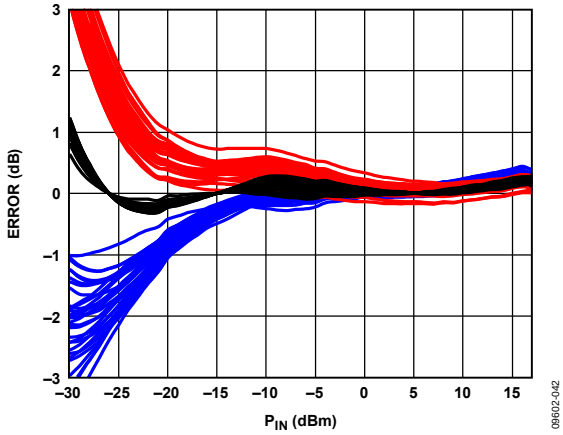


Figure 30. V_{RMS} Output Temperature Drift from +25°C Linear Reference for Multiple Devices at −40°C, +25°C, and +85°C, 3500 MHz Frequency

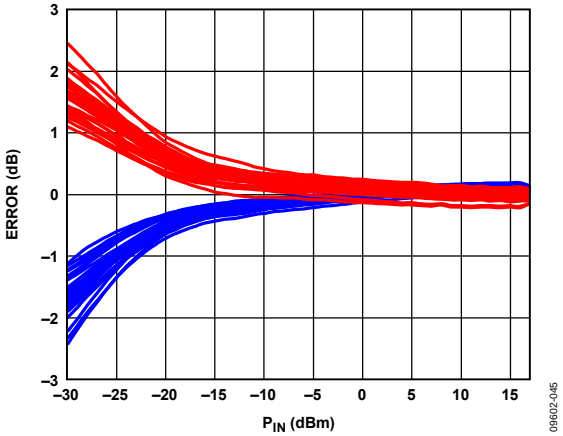


Figure 33. V_{RMS} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 3500 MHz

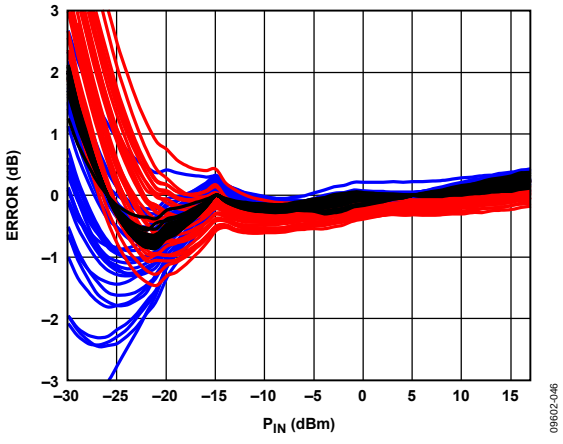


Figure 34. V_{ENV} Output Temperature Drift from +25°C Linear Reference for Multiple Devices at −40°C, +25°C, and +85°C, 6000 MHz Frequency

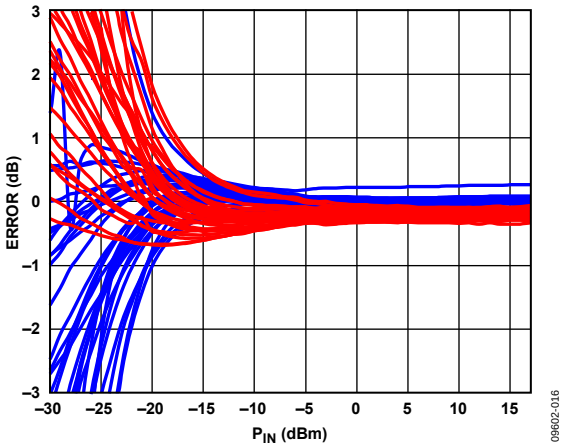


Figure 37. V_{ENV} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 6000 MHz

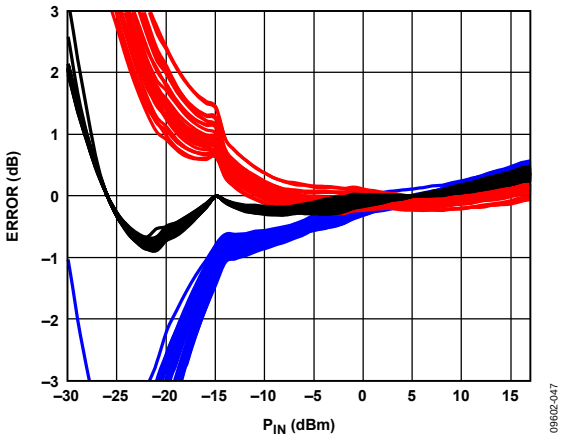


Figure 35. V_{RMS} Output Temperature Drift from +25°C Linear Reference for Multiple Devices at −40°C, +25°C, and +85°C, 6000 MHz Frequency

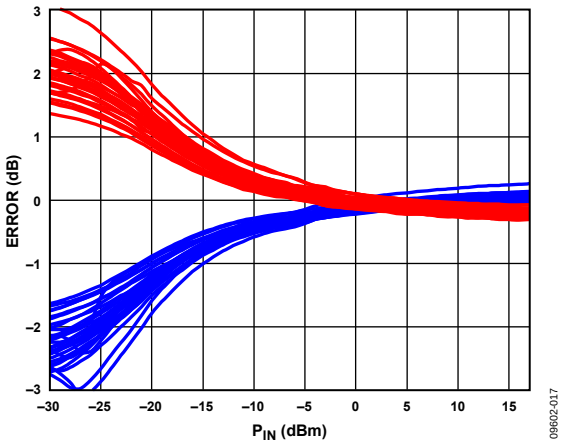


Figure 38. V_{RMS} Output Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C at 6000 MHz

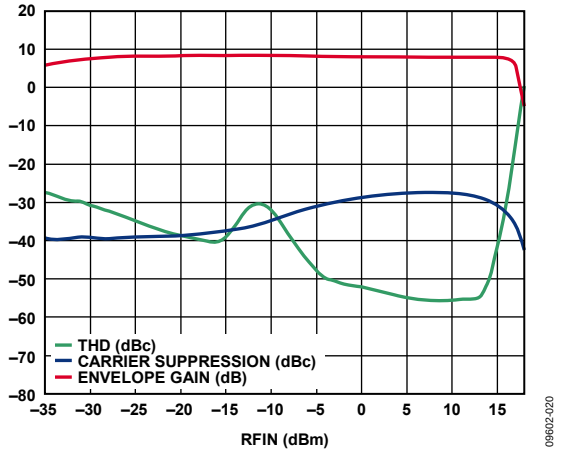


Figure 36. THD on V_{ENV} vs. RF Input Level; 1900 MHz RF Input, AM Modulated by a 20 MHz Sine Wave (Modulation Index = 0.25), V_{ENV} Output AC-Coupled into a 50 Ω Spectrum Analyzer Load

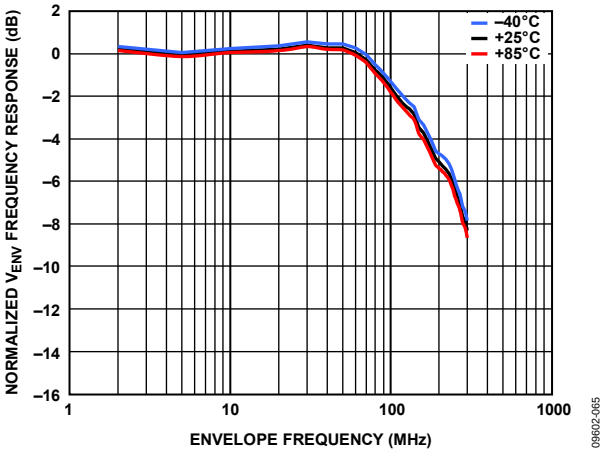


Figure 39. Normalized V_{ENV} Frequency Response, VENV AC-Coupled into a 50 Ω Spectrum Analyzer Load

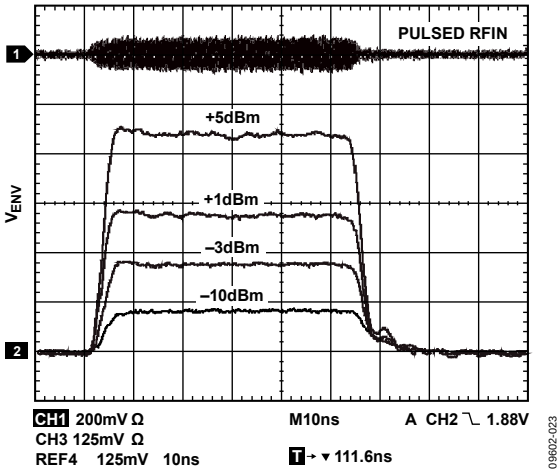


Figure 40. V_{ENV} Output Response to Various RF Input Pulse Levels 900 MHz Frequency

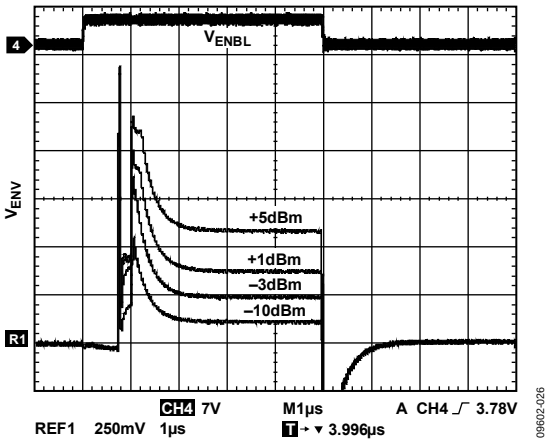


Figure 43. V_{ENV} Output Response to Enable Gating at Various RF Input Levels, 900 MHz Frequency

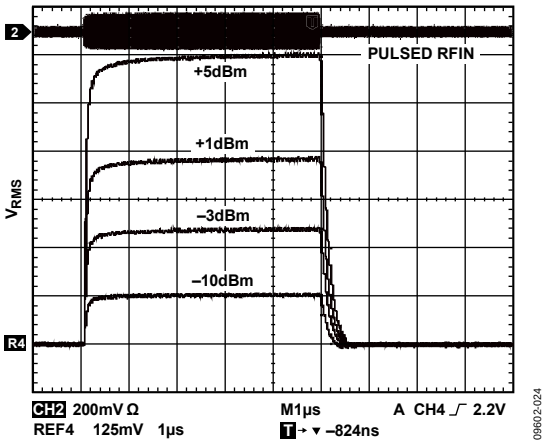


Figure 41. V_{RMS} Output Response to Various RF Input Pulse Levels 900 MHz Frequency, C_{FLT4} = Open

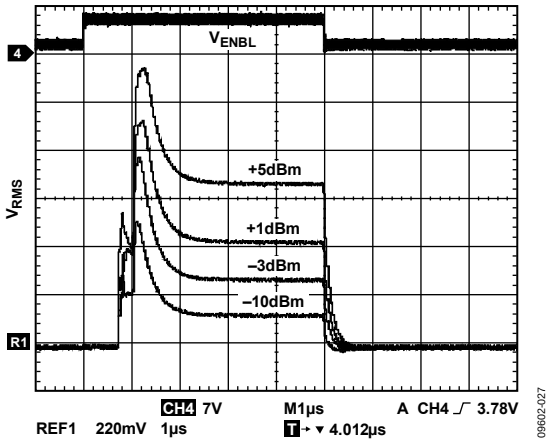


Figure 44. V_{RMS} Output Response to Enable Gating at Various RF Input Levels, 900 MHz Frequency, C_{FLT4} = Open

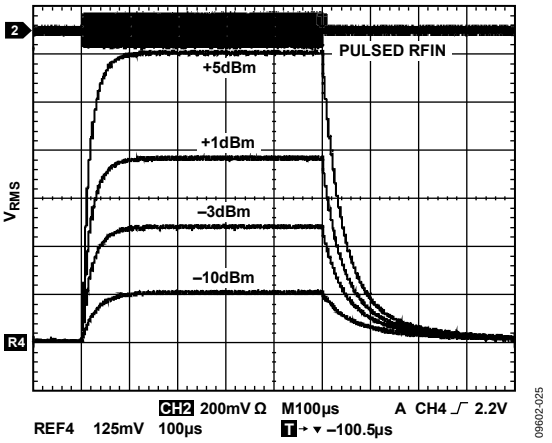


Figure 42. V_{RMS} Output Response to Various RF Input Pulse Levels, 900 MHz Frequency, C_{FLT4} = 100 nF

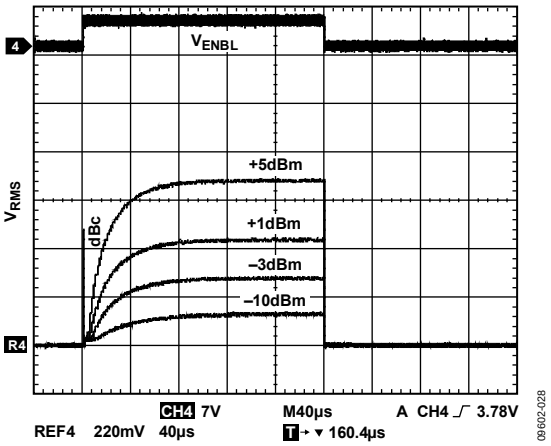


Figure 45. V_{RMS} Output Response to Enable Gating at Various RF Input Levels, 900 MHz Frequency, C_{FLT4} = 100 nF

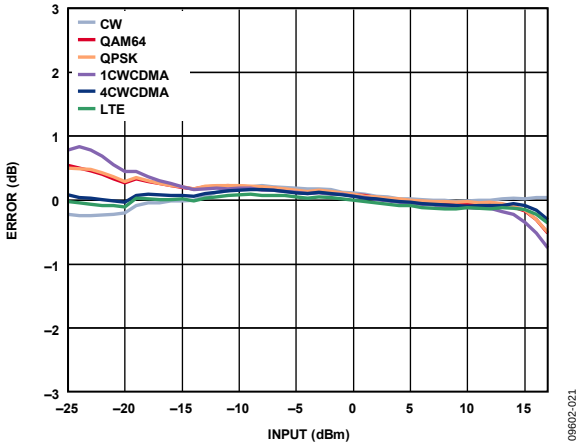


Figure 46. V_{RMS} Error from CW Linear Reference vs. Signal Modulation, Frequency = 900 MHz, C_{LPF} = 0.1 µF (CW, QPSK, QAM64, 1CW-CDMA, 4CW-CDMA, LTE Test Model E-TM1_1_20MHz)

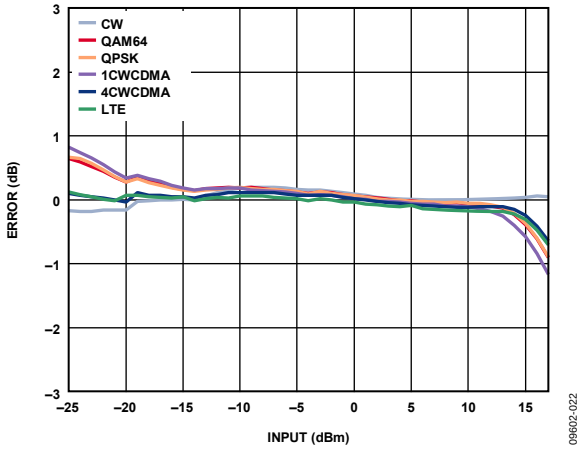


Figure 47. V_{RMS} Error from CW Linear Reference vs. Signal Modulation, Frequency = 2140 MHz, C_{LPF} = 0.1 µF (CW, QPSK, QAM64, 1CW-CDMA, 4CW-CDMA, LTE Test Model E-TM1_1_20MHz)

CIRCUIT DESCRIPTION

The ADL5511 employs a proprietary rectification technique to strip off the carrier of an input signal to reveal the true envelope. In this first detection stage, the carrier frequency is doubled and an on-chip two-pole passive low-pass filter accurately preserves the envelope and filters out the carrier. The poles of this filter, as defined by the on-chip RC filters (0.4 pF, 400 Ω, 0.8 pF, 250 Ω) values allow some carrier leakthrough for common RF frequencies. This is to ensure that maximum envelope bandwidth can be maintained. For more details, see the Basic Connections section.

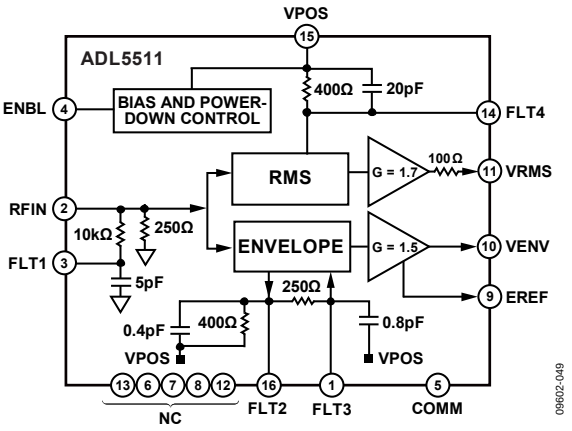


Figure 48. Block Diagram

The extracted envelope is further processed in two parallel channels, one computing the rms value of the envelope and the other transferring the envelope with appropriate scaling to the envelope output.

ENVELOPE PROPAGATION DELAY

The delay specified in this data sheet is with no external capacitor at the FLT2 and FLT3 pins. The delay through the ADL5511, although very small, depends upon a number of factors, notable of which are internal filter component values and op amp compensation capacitors. The delay will vary from part to part by approximately ±15% due to process variations.

In addition, the choice of external FLT2 and FLT3 values, as well as load on the VNEV pin will increase the delay. In this case, the delay variation will be dominated by the part-to-part tolerance of the external capacitors.

RMS CIRCUIT DESCRIPTION

The rms processing is done using a proprietary translinear technique. This method is a mathematically accurate rms computing approach and achieves unprecedented rms accuracies for complex modulation signals irrespective of the crest factor of the input signal. An integrating filter capacitor does the square-domain averaging. The VRMS output can be expressed as

$$VRMS = A \times \sqrt{\frac{\int_{T1}^{T2} V_{IN}^2 \times dt}{T2 - T1}} \quad (1)$$

Note that A is a scaling parameter that is decided on by the on-chip resistor ratio, and there are no other scaling parameters involved in this computation, which means that the rms output is inherently free from any sources of error due to temperature, supply, and process variation.

RMS FILTERING

The on-chip rms filtering corner is internally set by a 400 Ω resistor and a 20 pF capacitor, yielding a corner frequency of approximately 20 MHz. Whereas this filters out all carrier frequencies, most of the modulation envelope is not filtered. For adequate rms filtering, connect an external filter capacitor between FLT4 (Pin 14) and VPOS (Pin 15). This capacitance acts on the internal 400 Ω resistor (see Figure 48) to yield a new corner frequency for the rms filter given by

$$C_{FLT4} = \frac{1}{(2\pi \times f_{RMS} \times 400\ \Omega)} - 20\ \text{pF} \quad (2)$$

For example, a supply-referenced 0.1 µF capacitor on FLT4 reduces the corner frequency of the rms averaging circuit to approximately 4 kHz.

RMS filtering has a direct impact on rms accuracy. For most accurate detection, the rms filter corner should be low enough to filter out most of the modulation content. This will correspond to a corner frequency that is significantly lower than the bandwidth of the signal being measured. See the Choosing a Value for the RMS Averaging Capacitor (C_{FLT4}) section for more details and filtering options.

OUTPUT DRIVE CAPABILITY AND BUFFERING

The envelope output of the ADL5511 is presented on the VENV pin as a single-ended buffered output with low output impedance. To achieve high envelope bandwidth, this output is not ground referenced, unlike the VRMS output, which is ground referenced.

The VENV output has a no signal dc value of about 1.1 V. This dc reference is temperature dependent and is presented as a standalone reference voltage on the EREF pin and as a buffered output. The true envelope at any instant of time is simply (V_{ENV} – V_{EREF}), but these two pins do not constitute a differential output. EREF is a fixed dc voltage and V_{ENV} carries all the envelope information.

The VENV output is capable of supporting a parallel load of 500 Ω and 10 pF at full-scale envelope output and maximum bandwidth. Lighter loads (higher R and lower C) are always recommended whenever possible to minimize power consumption and achieve maximum possible bandwidth. The maximum source/sink current capacity of the VNEV output is 15 mA peak and load conditions should be such that this is not exceeded. The maximum output voltage at this pin is approximately (VPOS – 1.5) V.

For the case of ac coupling only, the VENV output can drive a 50 Ω load, as long as the maximum signal swing does not exceed an amplitude of approximately 1.5 V p-p. This corresponds to the peak signal current of 15 mA into the 50 Ω load. If a 50 Ω drive capability is desired, the maximum input signal to ADL5511 should be adjusted, such that this output swing condition is not exceeded.

A 50 Ω load should never be dc coupled to the VENV output, as it presents a current draw of >20 mA even for no-signal condition corresponding to 1.1 V nominal dc voltage at the VENV pin.

The VRMS buffered output can source a maximum current of 3 mA, but is not designed to sink any appreciable amount of current. If current sink capability is desired at this pin, a shunt resistance to ground can be connected. The VRMS output has an on-chip series resistance of 100 Ω, to allow a low-pass filtering of the residual ripple using a single shunt capacitor at this pin. Large shunt capacitors at this pin may also require a shunt resistor to be placed to allow fast discharging of the capacitor. The internal shunt resistance on the VRMS pin is 10 kΩ. Note that any shunt resistance placed on this pin creates a resistive divider with the on-chip 100 Ω series resistance.

The EREF output buffer also has 3 mA current sourcing capability. The internal shunt resistance on this pin through which any current must be sunk, is 12 kΩ. A capacitor to ground can be placed on this pin to eliminate any RF or envelope ripple at this pin to ensure that voltage at this pin acts as a clean reference for the VENV output for all possible carrier and envelope frequencies.

Viewing the Envelope on an Oscilloscope

When viewing the VENV output on an oscilloscope, use a low capacitive FET probe. This reduces the capacitance presented to the VENV output and avoids the corresponding effects of larger capacitive loads.

APPLICATIONS INFORMATION

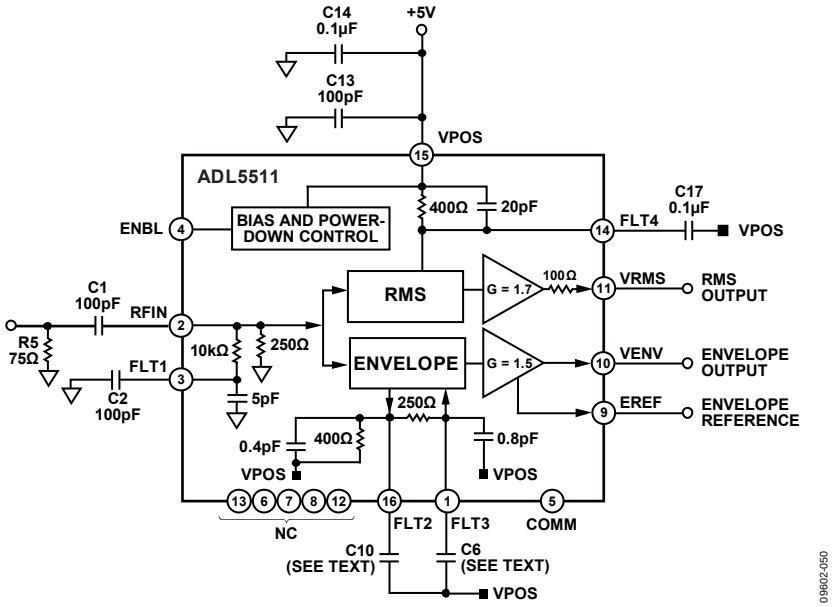


Figure 49. Basic Connections

BASIC CONNECTIONS

Basic connections for operation of the ADL5511 are shown in Figure 49. The ADL5511 requires a single supply of 5 V. The supply is connected to the VPOS supply pin. Decouple this pin using two capacitors with values equal or similar to those shown in Figure 49. Place these capacitors as close as possible to the VPOS pin.

An external 75 Ω resistor combines with the relatively high RF input impedance of the ADL5511 to provide a broadband 50 Ω match. Place an ac coupling capacitor between this resistor and RFIN.

The envelope output is available on Pin 10 (VENV) and is referenced to the 1.1 V dc voltage on Pin 9 (EREF).

The rms output voltage is available at the VRMS pin with rms averaging provided by the supply-referenced capacitance on Pin 14 (FLT4).

OPERATION BELOW 1 GHZ/ENVELOPE FILTERING

To operate the ADL5511 at frequencies below 1 GHz, a number of external capacitors must be added to the FLT3, FLT2, and FLT1 pins. These changes are in addition to the choice of an appropriate rms averaging capacitor, see the Choosing a Value for the RMS Averaging Capacitor (C_{FLT4}) section.

As part of the internal signal processing algorithm, the RF input signal passes through a low-pass filter comprising of a 10 kΩ resistor and a 5 pF capacitor (see Figure 49). This corresponds to a corner frequency of approximately 3.2 MHz. If the carrier frequency is less than approximately ten times this value (32 MHz), this corner frequency must be reduced.

The internal 5 pF capacitance can be augmented by connecting a ground referenced capacitor to Pin 3 (FLT1). The value of the external capacitance is set using the following equation:

$$C_{FLT1} = \frac{1}{(2\pi \times f_{3dB} \times 10{,}000\ \Omega)} - 5\ \text{pF} \quad (3)$$

For example, a 100 pF capacitance on FLT1 will reduce the corner frequency to 150 kHz. As a general guideline, this corner frequency should be set to be at least one tenth of the minimum expected carrier frequency. This ensures a flat frequency response around the frequency of interest.

The envelope detection path of the ADL5511 includes internal carrier-suppression low-pass filtering. With the FLT2 and FLT3 pins not connected, two internal 1 GHz and 800 MHz low-pass filters (operating in series) remove the RF carrier from the envelope output signal.

The equations for these filters are as follows:

$$\frac{1}{(2\pi \times 0.4\ \text{pF} \times 400\ \Omega)} \cong 1\ \text{GHz} \quad (4)$$

and

$$\frac{1}{(2\pi \times 0.8\ \text{pF} \times 250\ \Omega)} \cong 800\ \text{MHz} \quad (5)$$

Because the envelope detection circuitry includes a full-wave rectifier, this filter has to primarily suppress the signal at twice the original input frequency.

For input frequencies in the 900 MHz range, there will still be significant carrier content on the envelope output. With the two filters providing a combined 6 dB roll-off at approximately 900 MHz and with the residual carrier at 1.8 GHz, carrier filtering of approximately 18 dB can be expected (the two single-pole filters provide a combined roll-off of 12 dB per octave.

The internal filtering of the carrier in the envelope detection path can be augmented by adding additional supply-referenced capacitance to the FLT2 and FLT3 pins. The required capacitance can be calculated using the following equations:

$$C_{FLT2} = \frac{1}{(2\pi \times f_{FLT2} \times 400\ \Omega)} - 0.4\ \text{pF} \quad (6)$$

and

$$C_{FLT3} = \frac{1}{(2\pi \times f_{FLT3} \times 250\ \Omega)} - 0.8\ \text{pF} \quad (7)$$

where f_{LT2} and f_{LT3} are the desired corner frequencies.

For example, to set the corner frequency to 200 MHz, C_{FLT2} and C_{FLT3} should be set to 1.6 pF and 2.4 pF, respectively. The two corner frequencies should be set so that they are approximately equal.

Care should be taken not to set the corner frequency of this carrier suppression filter too low as it will start to degrade envelope bandwidth. The ADL5511 has an envelope bandwidth of 130 MHz. Thus, if the capacitors on FLT2 and FLT3 are so big that the carrier-suppression corner frequency approaches 130 MHz, the carrier filtering effort will directly impact the envelope bandwidth. Thus, the corner frequency should be set low enough so that the RF carrier is adequately removed from the envelope output while still maintaining the desired envelope bandwidth. An alternative option would be to filter the carrier at the VENV output using a higher order filter.

CHOOSING A VALUE FOR THE RMS AVERAGING CAPACITOR (C_{FLT4})

C_{FLT4} provides the averaging function for the internal rms computation, the result of which is available at the VRMS output. As already noted, the on-chip rms filtering corner is internally set by a 400 Ω resistor and a 20 pF capacitor, yielding a corner frequency of approximately 20 MHz.

For adequate rms filtering, connect an external filter capacitor between FLT4 (Pin 14) and VPOS (Pin 15). This capacitance acts on the internal 400 Ω resistor to yield a new corner frequency for the rms filter given by the following equation:

$$C_{FLT4} = \frac{1}{(2\pi \times f_{FLT4} \times 400\ \Omega)} - 20\ \text{pF} \quad (8)$$

For example, a supply-referenced 0.1 µF capacitor on FLT4 reduces the corner frequency of the rms averaging circuit to approximately 4 kHz.

The size of the rms filtering capacitor has a direct impact on the rms accuracy up to a point. For most accurate detection, the rms filter corner should be low enough to filter out most of the modulation content. This corresponds to a corner frequency that is significantly less than the bandwidth of the signal being measured.

Table 4 shows recommended minimum values of C_{FLT4} for popular modulation schemes. Using smaller capacitor values than these will result in rms measurement errors; using higher values will not further improve rms accuracy but will reduce the output noise on VRMS at the expense of increased rise and fall times. In Table 4, rise and fall times are also shown along with residual output noise.

The recommended minimum values for C_{FLT4} were experimentally determined by starting out with a large capacitance value on the FLT4 pin (for example, 10 µF). The value of V_{RMS} was noted for a fixed input power level (for example, 0 dBm). The value of C_{FLT4} was then progressively reduced (this can be done with press-down capacitors) until the value of V_{RMS} started to deviate from its original value (this indicates that the accuracy of the rms computation is degrading and that C_{FLT4} is becoming too small).

The recommended minimum value for C_{FLT4} is roughly inversely proportional to the bandwidth of the input signal, that is, wider bandwidth signals tend to require smaller minimum filter capacitances. As already noted, the value of C_{FLT4} sets up an internal low pass corner frequency, which filters the rms voltage. As carrier bandwidth increases, a larger proportion of the residual noise (which has been effectively mixed down to baseband) is filtered away. This results in smaller capacitances being required as carrier bandwidths increase.

Table 4. Recommended Minimum CFLT4 Values for Various Modulation Schemes (Pin = 0 dBm)

Modulation/Standard	PEP to RMS Ratio	Signal Bandwidth	C_{FLT4} (Min)	Output Noise	Rise/Fall Time (10% to 90%)
W-CDMA, One-Carrier, TM1-64	9.83 dB	3.84 MHz	220 nF	98 mV p-p	82 µs/310 µs
W-CDMA Four-Carrier, TM1-64, TM1-32, TM1-16, TM1-8	12.08 dB	18.84 MHz	100 nF	140 mV p-p	40 µs/140 µs
LTE Test Model E-TM1_1_4MHz	9.83 dB	4 MHz	220 nF	135 mV p-p	82 µs/310 µs
LTE Test Model E-TM1_1_10MHz	11.99 dB	10 MHz	100 nF	89 mV p-p	40 µs/140 µs
LTE Test Model E-TM1_1_20MHz	11.58 dB	20 MHz	47 nF	90 mV p-p	20 µs/70 µs

For applications that are not response time critical, a relatively large capacitor can be placed on the FLT4. There is no maximum capacitance limit for C_{FLT4}.

Figure 50 shows how output noise, rise time and fall time vary vs. C_{FLT4} when the ADL5511 is driven by an 1.9 GHz LTE carrier with a bandwidth of 10 MHz (LTE Test Model E-TM1_1_10MHz, peak-to-average ratio = 11.99 dB).

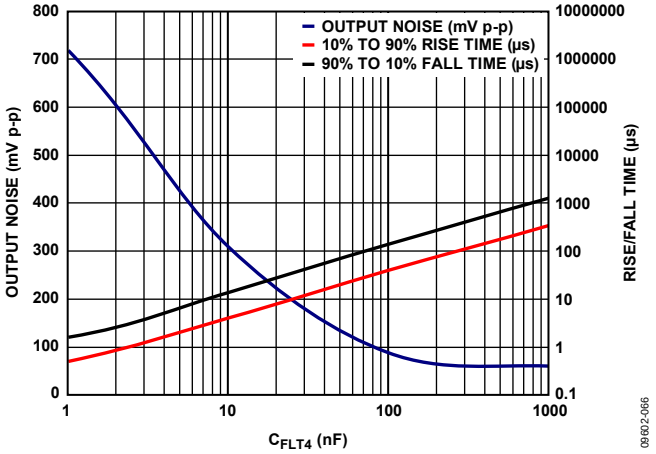


Figure 50. Output Noise, Rise and Fall Times vs. C_{FLT4} Capacitance, 10 MHz BW LTE Carrier (LTE Test Model E-TM1_1_10MHz) at 1.9 GHz with P_{IN} = 0 dBm

ENVELOPE TRACKING ACCURACY

The envelope tracking accuracy of the ADL5511 is measured in terms of the higher order distortion of the envelope output when the RF input signal is AM modulated using a low-harmonic sinusoid at a given frequency. Such an input sinusoidal envelope has been generated using the ADL5390 multiplier modulator. This generates a double sideband AM modulated signal of a known modulation index. In this measurement, the ADL5511 acts as free-running AM demodulator without requiring a local oscillator to demodulate the signal.

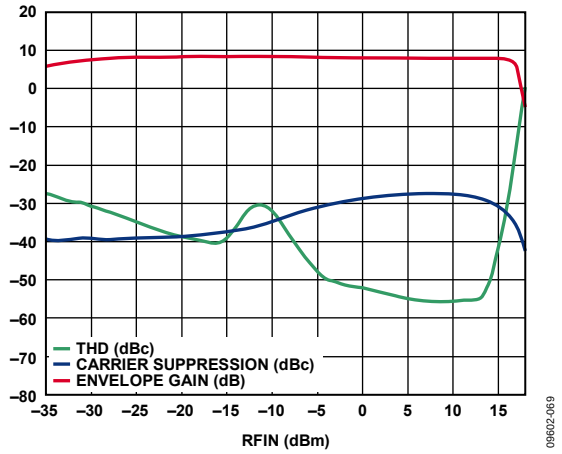


Figure 51. THD on V_{ENV} vs. RF Input Level; 1900 MHz RF Input, AM Modulated by a 20 MHz Sine Wave (Modulation Index = 0.25), V_{ENV} Output AC-Coupled into a 50 Ω Spectrum Analyzer Load

Figure 51 shows such a plot total harmonic distortion (THD) of the VENV output vs. RF input power for the modulation index of 0.25.

As the input power level increases, the THD improves until it sharply degrades at an input power level of approximately 13 dBm. This sharp decrease is caused by the clipping of the AM signal's peak envelope. Figure 51 also shows carrier leakage at VENV in dBc with respect to the input carrier amplitude.

This measurement, when conducted over the full input power range of the ADL5511, suffers from measurement inaccuracies of the input modulated signal due to the spectrum analyzer's noise floor and therefore does not accurately reveal the ADL5511's limitations at the lower end of the measurement range. In addition to this, the process of generating an AM signal for this test (using the ADL5390 multiplier) is not perfect and resulted in a source signal whose envelope was not harmonically pure.

TIME DOMAIN ENVELOPE TRACKING ACCURACY

The envelope tracking accuracy of the ADL5511 can also be assessed in the time domain by looking at the input peak power levels that cause clipping.

The usable rms input power range of the ADL5511 varies depending on the desired accuracy level and the peak-to-average ratio of the input signal. Figure 4 shows the linear operating range of the VENV output when the RF input is driven by unmodulated sine waves at various frequencies. This shows operation up to rms input levels of approximately 19 dBm. If the signal has a peak-to-average ratio that is greater than the square root of two, the usable input range on RFIN will decrease. In general, the maximum input power for linear operation should be determined by the peak envelope power (PEP) of the input signal. Figure 52 shows the time-domain response of the VENV output to a 900 MHz LTE carrier with a bandwidth of 20 MHz (Test Model E-TM1_2_20MHz). The signal level of the carrier (7 dBm rms, 19 dBm PEP) was deliberately increased until clipping was observed at the VENV output.

Note that the peak envelope power of a signal is derived based on the rms level of the signal during a peak cycle, that is V p-p/√2. For example, a signal that achieves a peak voltage of 10 V (or 20 V p-p) has a PEP of 30 dBm. According to this definition, the PEP of a sine wave is equal to its rms power level because it has a constant envelope.

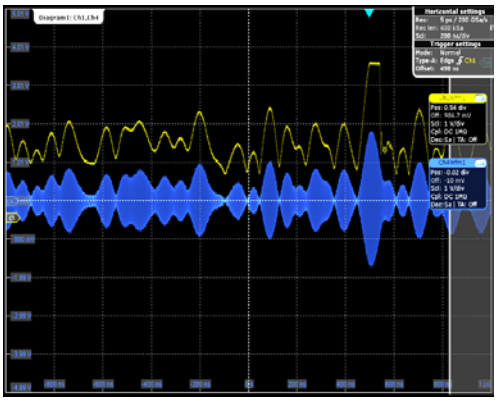


Figure 52. VENV Response to a 20 MHz LTE Carrier with a PEP of 19 dBm that has been Triggered to Capture the Envelope's Peak Level

VRMS AND VENV OUTPUT OFFSET

The 900 MHz RF power sweeps in Figure 53 and Figure 54 show distributions of the VRMS and VENV outputs voltages for multiple devices at 25°C. The VRMS output response flattens out at approximately −30 dBm while the various VENV response traces begin to fanout unpredictably (Figure 4 and Figure 7 show this behavior at other frequencies). While these plots suggest that operation at input levels down to −30 dBm is feasible, account must also be taken for variations over temperature. Figure 10 to Figure 38 show how the linearity error starts to increase below input levels of −20 dBm (the size of the error varies between VENV and VRMS and with frequency).

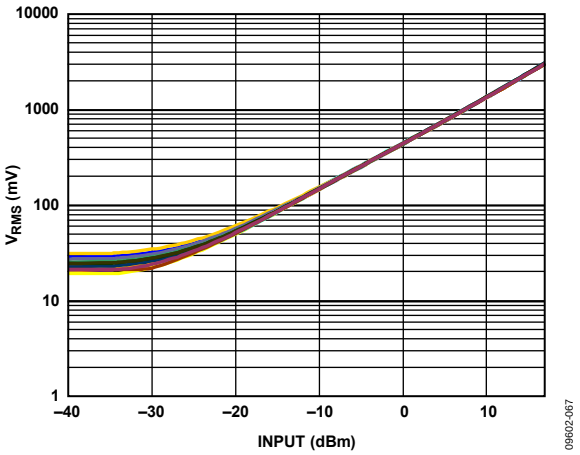


Figure 53. VRMS Output vs. Input Level Distribution of 50 Devices, 900 MHz Frequency

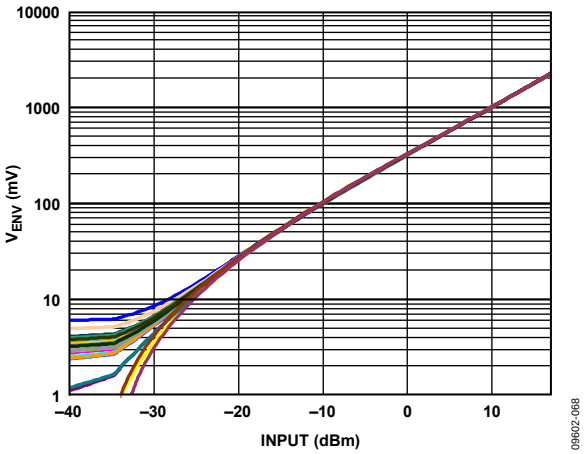


Figure 54. VENV Output vs. Input Level Distribution of 50 Devices, 900 MHz Frequency

DEVICE CALIBRATION AND ERROR CALCULATION

Because slope and intercept vary from device to device, calibration must be performed to achieve high accuracy. In general, calibration is performed by applying two or more known input power levels to the ADL5511 and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear operating range of the device. For a two-point calibration, the conversion gain (or slope) and intercept are calculated for V_{RMS} and V_{ENV} using the following equations:

$$Slope = (V_{OUT2} - V_{OUT1})/(V_{IN2} - V_{IN1}) \quad (9)$$

$$Intercept = V_{OUT1} - (Slope \times V_{IN1}) \quad (10)$$

where:
V_{IN} is the rms input voltage to RFIN.
V_{OUT} is the voltage output at VRMS or VENV.

Because the gain and intercept of the rms and envelope paths will be different, both paths should be calibrated, that is, with a measured signal applied to RFIN, V_{ENV}, and V_{RMS}. To ensure that the voltage at VENV and VRMS is a steady-state value, a constant envelope signal such as a sine wave should be used as the source during calibration.

Once slope and intercept are calculated, an equation can be written that allows calculation of the input rms or envelope level using the following equations:

$$V_{INRMS} = (V_{RMS} - Intercept_{VRMS})/Slope_{RMS} \quad (11)$$

$$V_{INENV} = (V_{ENV} - Intercept_{VENV})/Slope_{VENV} \quad (12)$$

The law conformance error, that is, the difference between the actual input level (V_{IN_IDEAL}) and the measured/calculated input level ($V_{MEASURED}$), of these calculations can be calculated using the following equation:

$$Error\ (\text{dB}) = 20 \times \log\left[(V_{MEASURED} - Intercept)/(Slope \times V_{IN_IDEAL})\right] \quad (13)$$

Figure 55 is a plot of this error for VENV at 1900 MHz for a multiple devices at +25°C, +85°C, and −40°C with calibration performed at two points, −14 dBm and +5 dBm (notice how the error at 25°C at the calibration points is zero). These error plots for all temperatures are calculated using the 25°C slope and intercept. This is consistent with calibration in a mass production environment where calibration at temperature is generally not practical.

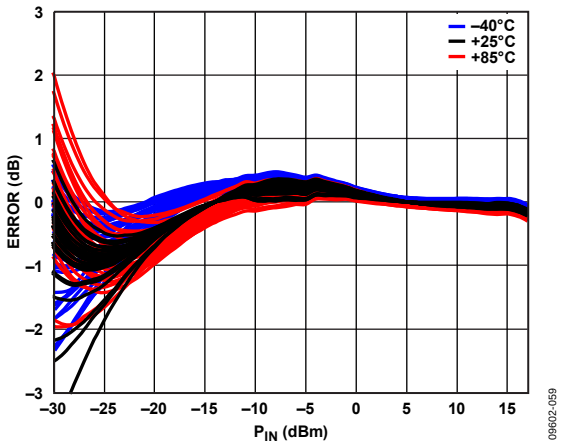


Figure 55. VENV Linearity Error vs. Input Level and Temperature Using a Two-Point Calibration at 1900 MHz

By adding a third calibration point, the linearity of the ADL5511 can be enhanced at lower power levels. With a three-point calibration, calibration coefficients (slope and intercept) are calculated for each segment (thus, there will be two slopes and two intercepts).

Figure 56 shows the same data as Figure 55, but with a three-point calibration (calibration points at −26 dBm, −15 dBm, and +5 dBm. This helps to extend the usable operating range of the ADL5511 well below −25 dBm.

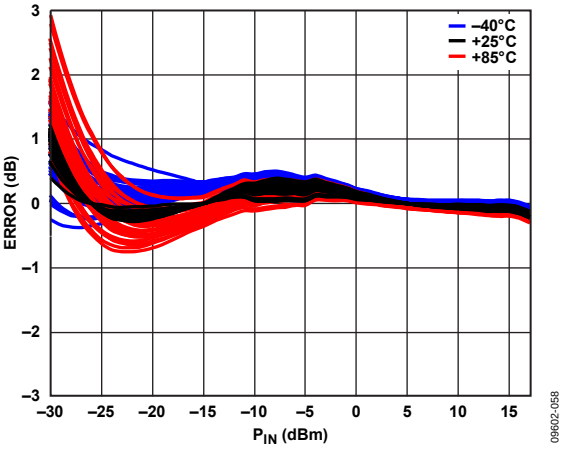


Figure 56. VENV Linearity Error vs. Input Level and Temperature Using a Three-Point Calibration at 1900 MHz

ERROR VS. FREQUENCY

Figure 57 and Figure 58 show how the V_{RMS} and V_{ENV} output voltages and error vary with input frequency when the ADL5511 is calibrated at a single frequency. In this example, the ADL5511 has been calibrated at 25°C at 1.9 GHz. The plots also show how the output voltage and error vary above and below this frequency.

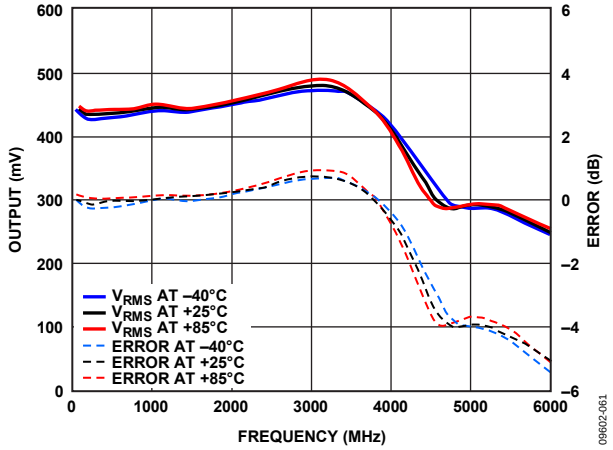


Figure 57. VRMS Output vs. Frequency for a Fixed Input Power, P_{IN} = 0 dBm, Calibration at 1.9 GHz, 25°C

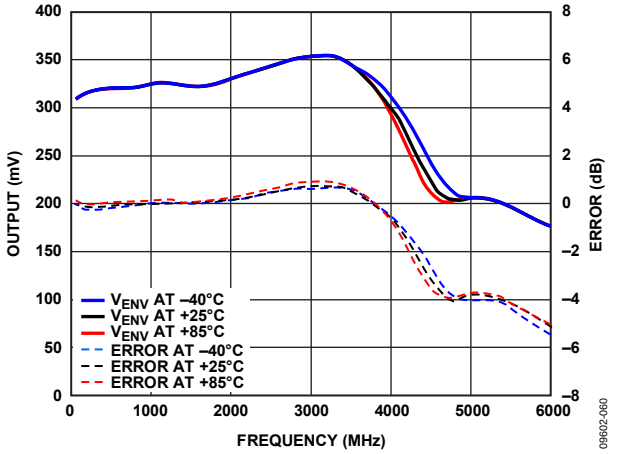


Figure 58. VENV Output vs. Frequency for a Fixed Input Power, P_{IN} = 0 dBm, Calibration at 1.9 GHz, 25°C

EVALUATION BOARD

Figure 59 shows the schematic of the ADL5511 evaluation board. This 4-layer board is powered by a single supply in the 4.75 V to 5.25 V range. The power supply is decoupled by 100 pF and 0.1 µF capacitors.

Table 5 details the various configuration options of the evaluation board. Figure 60 and Figure 61 show the bottom side and top side layouts, respectively.

The RF input has a broadband match of 50 Ω using a single 75 Ω resistor at R5.

The VRMS output is accessible via a clip lead (a pad is also available where an SMA connector is installed). The VENV output is accessible via an SMA connector. For response-time critical measurements where stray capacitance must be minimized, R2 can be removed and a FET probe can be attached to JP1 (JP1 must be installed).

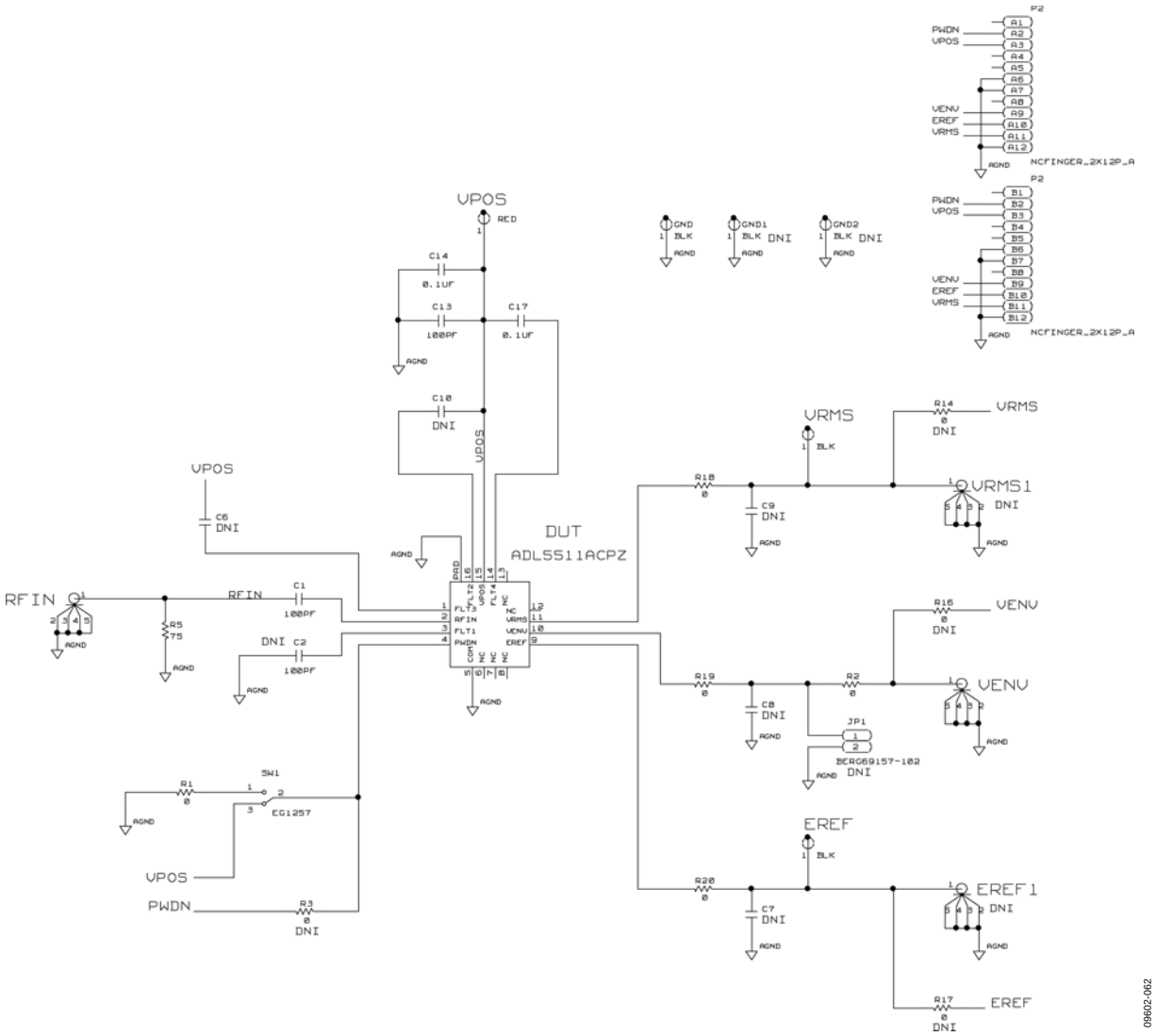


Figure 59. Evaluation Board Schematic

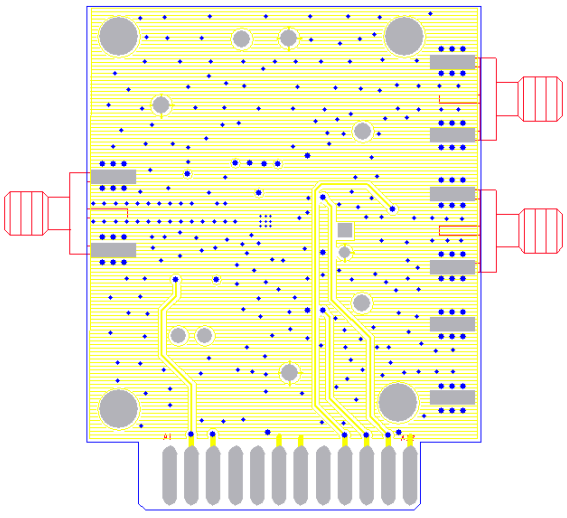


Figure 60. Layout of Evaluation Board, Bottom Side

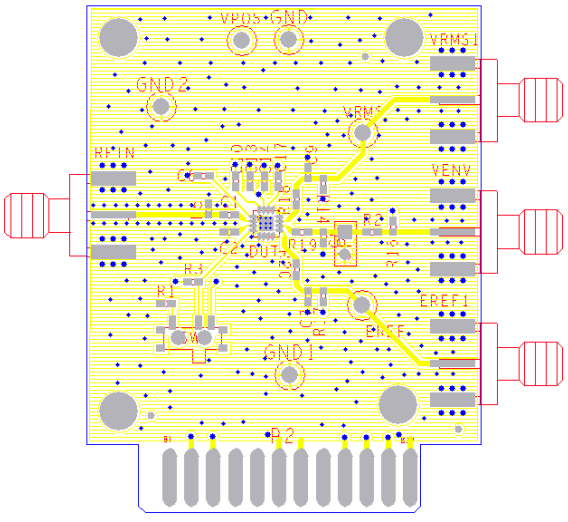
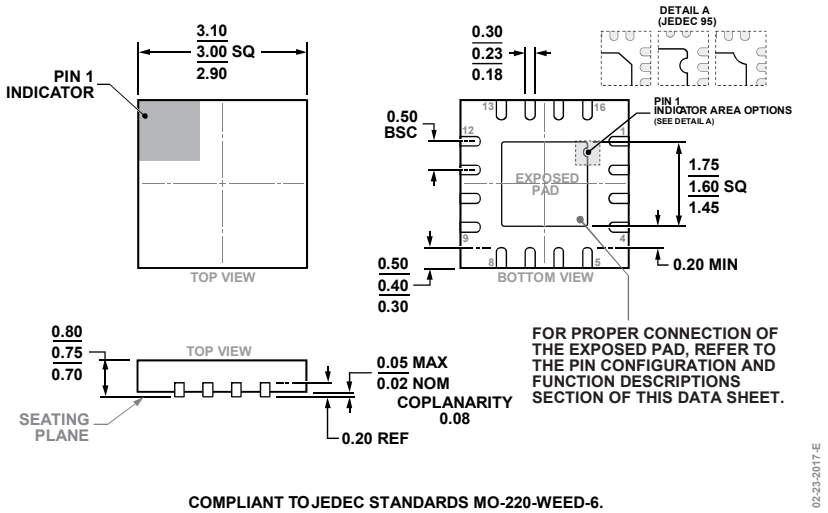


Figure 61. Layout of Evaluation Board, Top Side

Table 5. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and supply vector pins.	Not applicable
C13, C14	Power supply decoupling. Nominal supply decoupling of 0.01 µF and 100 pF.	C13 = 100 pF (Size 0402) C14 = 0.1 µF (Size 0402)
C17	RMS filter capacitor (FLT4). The internal rms averaging capacitor can be augmented by placing additional capacitance in C17.	C17 = 0.1 µF (Size 0402)
R5, C1	RF input interface. The 75 Ω resistor at R5 combines with the ADL5511 internal input impedance to give a broadband input impedance of around 50 Ω. C1 is an ac coupling capacitor, which should be chosen according to nominal carrier frequency.	R5 = 75 Ω (Size 0402) C1 = 100 pF (Size 0402)
R18, C9	RMS output and output filtering. The combination of C9 and the internal 100 Ω output resistance can be used to form a low-pass filter to reduce the output noise on the VRMS output beyond the reduction due to C17 (capacitor on FLT4). The rms output is available on the VRMS clip-on test point. To observe VRMS using an SMA cable, an SMA connector can be soldered on to the pad labeled VRMS1.	R18 = 0 Ω (Size 0402) C9 = open (Size 0402) VRMS clip-on test point = installed VRMS1 SMA connector = open
R19, C8, R2, JP1	VENV output and output filtering. The VENV output is available on the VENV SMA connector. If post-envelope filtering is desired, R19 and C8 can be used to form a low-pass filter at the VENV output. R2 can be removed to isolate the JP1 jumper from the VENV SMA connector and JP1 can be installed and used to interface to a FET probe. This helps to eliminate any excessive trace and connector capacitance.	VENV SMA connector = installed R19, R2 = 0 Ω (Size 0402) C8 = open (Size 0402) JP1 = open
R20, C7	Envelope reference output and output filtering. The EREF output is available on the EREF clip-on test point. The dc reference voltage at Pin EREF can be filtered by the low-pass filter formed by the combination of R20 and C7. To observe the EREF voltage using an SMA cable, an SMA connector can be soldered onto the pad labeled EREF1.	R20 = 0 Ω (Size 0402) C7 = open (Size 0402) EREF clip-on test point = installed EREF1 SMA connector = open
R1, SW1	Device enable. When the switch is set toward the SW1 label, the ENBL pin is connected to VPOS, which enables the ADL5511. In the opposite switch position, the ENBL pin is grounded which disables the ADL5511.	R1 = 0 Ω (Size 0402) SW1 = towards SW1 label
C6, C10	Envelope carrier-removal filters (FLT2, FLT3). The corner frequency of the internal VENV two-pole carrier-removal filter can be reduced by placing additional capacitors in C6 and C10.	C6, C10 = open (Size 0402)
C2	Envelope reference carrier-removal filter (FLT1). The internal filter that removes the carrier from the envelope reference dc voltage can be augmented by placing a capacitor in C2.	C2 = 100 pF (Size 0402)
R3, R14, R15, R16, R17	Alternate interface. The P2 edge connector provides an alternate access point to the various ADL5511 signals.	R3, R14, R15, R16, R17 = open (Size 0402)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 62. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADL5511ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	1500	Q1Y
ADL5511-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

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D09602-0-7/18(D)