RF/IF Vector Multiplier

Data Sheet

ADL5390

FEATURES

Matched pair of multiplying VGAs
Broad frequency range 20 MHz to 2.4 GHz
Continuous magnitude control from +5 dB to −30 dB
Output third-order intercept 24 dBm
Output 1 dB compression point 11 dBm
Output noise floor −148 dBm/Hz
Adjustable modulation bandwidth up to 230 MHz
Fast output power disable
Single-supply voltage 4.75 V to 5.25 V

APPLICATIONS

PA linearization and predistortion
Amplitude and phase modulation
Variable matched attenuator and/or phase shifter
Cellular base stations
Radio links
Fixed wireless access
Broadband/CATV
RF/IF analog multiplexer

FUNCTIONAL BLOCK DIAGRAM

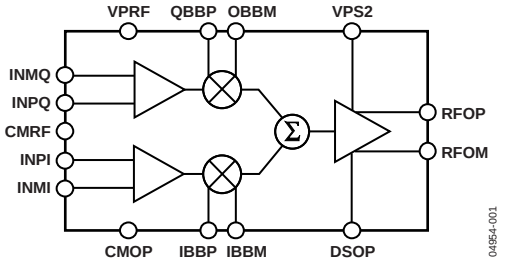


Figure 1.

GENERAL DESCRIPTION

The ADL5390 vector multiplier consists of a matched pair of broadband variable gain amplifiers whose outputs are summed. The separate gain controls for each amplifier are linear-in-magnitude. If the two input RF signals are in quadrature, the vector multiplier can be configured as a vector modulator or as a variable attenuator/phase shifter by using the gain control pins as Cartesian variables. In this case, the output amplitude can be controlled from a maximum of +5 dB to less than −30 dB, and the phase can be shifted continuously over the entire 360° range. Since the signal paths are linear, the original modulation on the inputs is preserved. If the two signals are independent, then the vector multiplier can function as a 2:1 multiplexer or can provide fading from one channel to another.

The ADL5390 operates over a wide frequency range of 20 MHz to 2400 MHz. For a maximum gain setting on one channel at 380 MHz, the ADL5390 delivers an OP1dB of 11 dBm, an OIP3 of 24 dBm, and an output noise floor of −148 dBm/Hz. The gain and phase matching between the two VGAs is better than 0.5 dB and 1°, respectively, over most of the operating range.

The gain control inputs are dc-coupled with a ±500 mV differential full-scale range centered about a 500 mV common mode. The maximum modulation bandwidth is 230 MHz, which can be reduced by adding external capacitors to limit the noise bandwidth on the control lines.

Both the RF inputs and outputs can be used differentially or single-ended and must be ac-coupled. The impedance of each VGA RF input is 250 Ω to ground, and the differential output impedance is nominally 50 Ω over the operating frequency range. The DSOP pin allows the output stage to be disabled quickly to protect subsequent stages from overdrive. The ADL5390 operates off supply voltages from 4.75 V to 5.25 V while consuming 135 mA.

The ADL5390 is fabricated on Analog Devices' proprietary, high performance 25 GHz SOI complementary bipolar IC process. It is available in a 24-lead, Pb-free CSP package and operates over a −40°C to +85°C temperature range. Evaluation boards are available.

Rev. A Document Feedback
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REVISION HISTORY

10/2017—Rev. 0 to Rev. A

Changed CP-24-2 to CP-24-10 ... Throughout
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

10/2004—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_O = 50 Ω, F_{RF} = 380 MHz, single-ended source drive to INPI and INPQ, and INMI and INMQ are ac-coupled to common, unless otherwise noted. 66.5 Ω termination resistors before ac-coupling capacitors on INPI and INPQ. The specifications refer to one active channel with the other channel input terminated in 50 Ω. The common-mode level for the gain control inputs is 0.5 V. A maximum gain setpoint of 1.0 refers to a differential gain control voltage of 0.5 V.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		20		2400	MHz
Gain Control Range	Relative to maximum gain		35		dB
GAIN CONTROL INTERFACE (I and Q)	QBBP, QBBM, IBBM, IBBP (Pins 4, 5, 14, 15)				
Gain Scaling			3.5		1/V
Modulation Bandwidth	500 mV p-p, sinusoidal baseband input single-ended		230		MHz
Second Harmonic Distortion	500 mV p-p, 1 MHz, sinusoidal baseband input differential		45		dBc
Third Harmonic Distortion	500 mV p-p, 1 MHz, sinusoidal baseband input differential		55		dBc
Step Response	For gain from −15 dB to +5 dB		45		ns
	For gain from +5 dB to −15 dB		47		ns
F_{RF} = 70 MHz					
Maximum Gain	Maximum gain setpoint		4.6		dB
Gain Conformance	Over gain setpoint of 0.2 to 1.0		0.25		dB
Output Noise Floor	Maximum gain setpoint, no RF input		−149		dBm/Hz
	RF P_{IN} = −5 dBm, frequency offset = 20 MHz		−146		dBm/Hz
Output IP3	F_{RF1} = 70 MHz, F_{RF2} = 72.5 MHz, maximum gain setpoint		23		dBm
Output 1 dB Compression Point	Maximum gain setpoint		10.7		dBm
Input 1 dB Compression Point	Gain setpoint = 0.1		6.7		dBm
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Gain Matching	At maximum gain setpoint		0.5		dB
Phase Matching	At maximum gain setpoint		±0.25		Degrees
Input Impedance	INPI, INMI, INMQ, INMP (Pins 20, 21, 22, 23)		250‖1		Ω‖pF
Output Return Loss	RFOP, RFOM (Pins 9, 10) measured through balun		9.7		dB
F_{RF} = 140 MHz					
Maximum Gain	Maximum gain setpoint		4.5		dB
Gain Conformance	Over gain setpoint of 0.2 to 1.0		0.25		dB
Output Noise Floor	Maximum gain setpoint, no RF input		−144		dBm/Hz
	RF P_{IN} = −5 dBm, frequency offset = 20 MHz		−145		dBm/Hz
Output IP3	F_{RF1} = 140 MHz, F_{RF2} = 142.5 MHz, maximum gain setpoint		24.4		dBm
Output 1 dB Compression Point	Maximum gain setpoint		11		dBm
Input 1 dB Compression Point	Gain setpoint = 0.1		7.1		dBm
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Gain Matching	At maximum gain setpoint		0.5		dB
Phase Matching	At maximum gain setpoint		±0.25		Degrees
Input Impedance	INPI, INMI, INMQ, INMP (Pins 20, 21, 22, 23)		250‖1		Ω‖pF
Output Return Loss	RFOP, RFOM (Pins 9, 10) measured through balun		9.6		dB
F_{RF} = 380 MHz					
Maximum Gain	Maximum gain setpoint		4.1		dB
Gain Conformance	Over gain setpoint of 0.2 to 1.0		0.25		dB

Parameter	Conditions	Min	Typ	Max	Unit
Output Noise Floor	Maximum gain setpoint, no RF input		−147.5		dBm/Hz
	RF P_{IN} = −5 dBm, frequency offset = 20 MHz		−146		dBm/Hz
Output IP3	F_{RF1} = 380 MHz, F_{RF2} = 382.5 MHz, maximum gain setpoint		24.2		dBm
Output 1 dB Compression Point	Maximum gain setpoint		11.3		dBm
Input 1 dB Compression Point	Gain setpoint = 0.1		8.3		dBm
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Gain Matching	At maximum gain setpoint		0.5		dB
Phase Matching	At maximum gain setpoint		±0.5		Degrees
Input Impedance	INPI, INMI, INMQ, INMP (Pins 20, 21, 22, 23)		200||1		Ω||pF
Output Return Loss	RFOP, RFOM (Pins 9, 10) measured through balun		8.5		dB
F_{RF} = 900 MHz					
Maximum Gain	Maximum gain setpoint		4.5		dB
Gain Conformance	Over gain setpoint of 0.2 to 1.0		0.4		dB
Output Noise Floor	Maximum gain setpoint, no RF input		−149.5		dBm/Hz
	RF P_{IN} = −5 dBm, frequency offset = 20 MHz		−148		dBm/Hz
Output IP3	F_{RF1} = 900 MHz, F_{RF2} = 902.5 MHz, maximum gain setpoint		23.3		dBm
Output 1 dB Compression Point	Maximum gain setpoint		11.5		dBm
Input 1 dB Compression Point	Gain setpoint = 0.1		8.5		dBm
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Gain Matching	At maximum gain setpoint		0.6		dB
Phase Matching	At maximum gain setpoint		±1		Degrees
Input Impedance	INPI, INMI, INMQ, INMP (Pins 20, 21, 22, 23)		180||0.6		Ω||pF
Output Return Loss	RFOP, RFOM (Pins 9, 10) measured through balun		6.8		dB
F_{RF} = 2400 MHz					
Maximum Gain	Maximum gain setpoint		7.0		dB
Gain Conformance	Over gain setpoint of 0.2 to 1.0		0.5		dB
Output Noise Floor	Maximum gain setpoint, no RF input		−147		dBm/Hz
	RF P_{IN} = −5 dBm, frequency offset = 20 MHz		−144		dBm/Hz
Output IP3	F_{RF1} = 2400 MHz, F_{RF2} = 2402.5 MHz, maximum gain setpoint		18.7		dBm
Output 1 dB Compression Point	Maximum gain setpoint		9.6		dBm
Input 1 dB Compression Point	Gain setpoint = 0.1		4.3		dBm
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Gain Matching	At maximum gain setpoint		0.8		dB
Phase Matching	At maximum gain setpoint		±2.5		Degrees
Input Impedance	INPI, INMI, INMQ, INMP (Pins 20, 21, 22, 23)		140||0.5		Ω||pF
Output Return Loss	RFOP, RFOM (Pins 9, 10) measured through balun		13.5		dB
POWER SUPPLY	VPRF, VPS2 (Pin 1, 18, 6); RFOP, RFOM (Pins 9, 10)				
Positive Supply Voltage		4.75	5	5.25	V
Total Supply Current	Includes load current		135		mA
OUTPUT DISABLE	DSOP (Pin 13)				
Disable Threshold			2.5		V
Maximum Attenuation	DSOP = 5 V		40		dB
Enable Response Time	Delay following high-to-low transition until device meets full specifications		15		ns
Disable Response Time	Delay following low-to-high transition until device produces full attenuation		10		ns

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Rating
Supply Voltage VPRF, VPS2	5.5 V
DSOP	5.5 V
IBBP, IBBM, QBBP, QBBM	2.5 V
RFOP, RFOM	5.5 V
RF Input Power at Maximum Gain (INPI or INPQ, Single-Ended Drive) Equivalent Voltage	10 dBm for 50 Ω 2.0 V p-p
Internal Power Dissipation	825 mW
θ_{JA} (With Pad Soldered to Board)	59°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

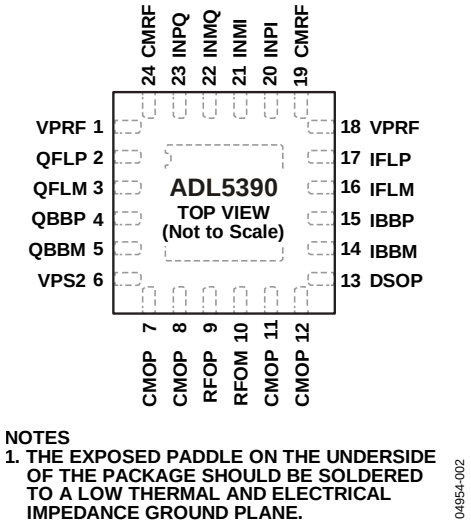


Figure 2. LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
2, 3	QFLP, QFLM	Q Baseband Input Filter Pins. Connect optional capacitor to reduce Q baseband gain control channel low-pass corner frequency.
4, 5	QBBP, QBBM	Q Channel Differential Baseband Gain Control Inputs. Typical common-mode bias level of 0.5 V.
6, 1, 18	VPS2, VPRF	Positive Supply Voltage. V_P of 4.75 V to 5.25 V.
7, 8, 11, 12, 19, 24	CMOP, CMRF	Device Common. Connect via lowest possible impedance to external circuit common.
9, 10	RFOP, RFOM	Differential RF Outputs. Must be ac-coupled. Differential impedance 50 Ω nominal.
13	DSOP	Output Disable. Pull high to disable output stage. Connect to common for normal operation.
14, 15	IBBM, IBBP	I Channel Differential Baseband Gain Control Inputs. Typical common-mode bias level of 0.5 V.
16, 17	IFLM, IFLP	I Baseband Input Filter Pins. Connect optional capacitor to reduce I baseband gain control channel low-pass corner frequency.
20, 21	INPI, INMI	I Channel Differential RF Inputs. Must be ac-coupled. 250 Ω impedance to common on each pin. These inputs can be driven single-ended without any performance degradation.
22, 23	INMQ, INPQ	Q Channel Differential RF Inputs. Must be ac-coupled. 250 Ωimpedance to common on each pin. These inputs can be driven single-ended without any performance degradation.
Exposed Paddle	GND	The exposed paddle on the underside of the package should be soldered to a low thermal and electrical impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

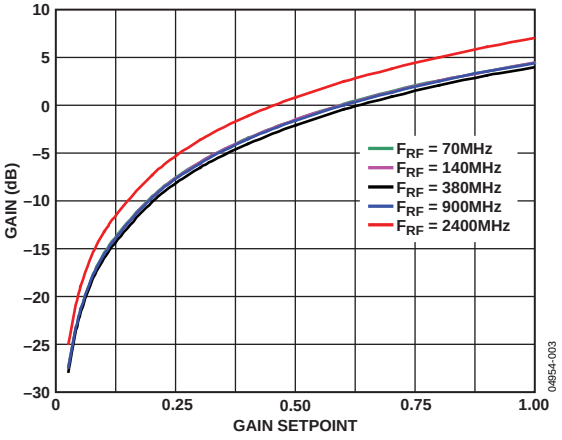


Figure 3. Gain Magnitude vs. Gain Setpoint, RF Frequency = 70 MHz, 140 MHz, 380 MHz, 900 MHz, 2400 MHz (Channel I or Channel Q)

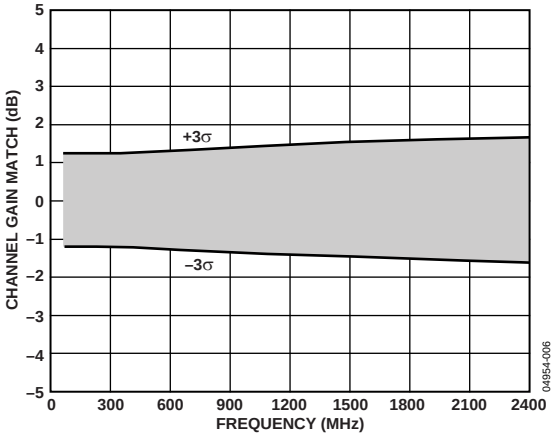


Figure 6. Channel Gain Matching (I to Q) vs. RF Frequency, Gain Setpoint = 1.0

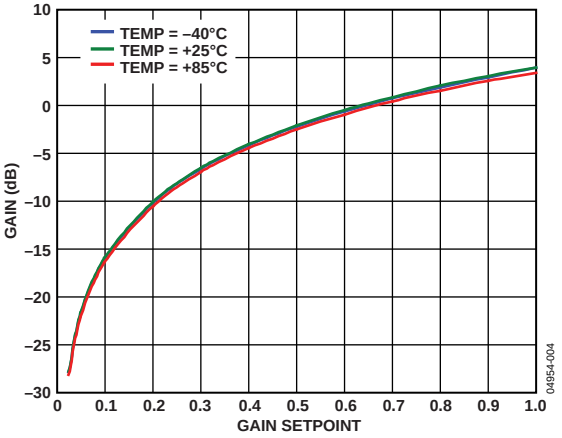


Figure 4. Gain Magnitude vs. Gain Setpoint, Temp = +85°C, +25°C, –40°C, RF Frequency = 380 MHz (Channel I or Channel Q)

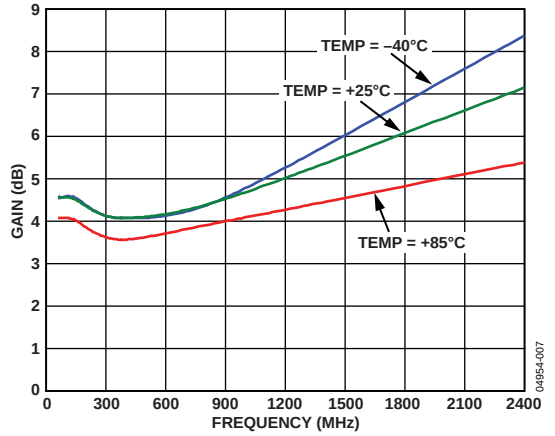


Figure 7. Channel Gain vs. RF Frequency, Temp = +85°C, +25°C, –40°C, Gain Setpoint = 1.0

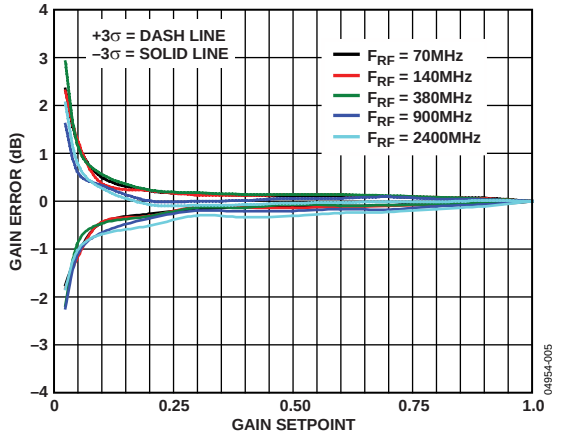


Figure 5. Gain Conformance Error vs. Gain Setpoint, RF Frequency = 70 MHz, 140 MHz, 380 MHz, 900 MHz, 2400 MHz

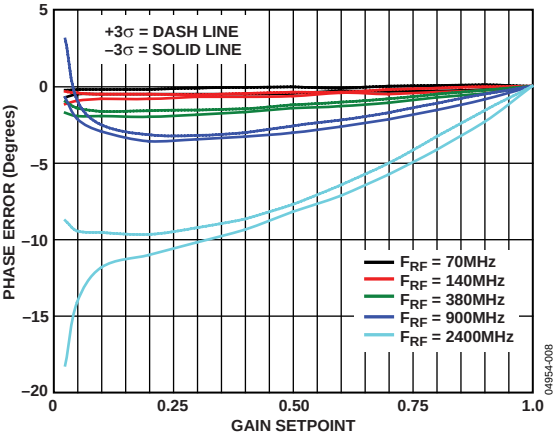


Figure 8. Single-Channel Phase Deviation vs. Gain Setpoint, Normalized to Gain Setpoint = 1.0, RF Frequency = 70 MHz, 140 MHz, 380 MHz, 900 MHz, 2400 MHz

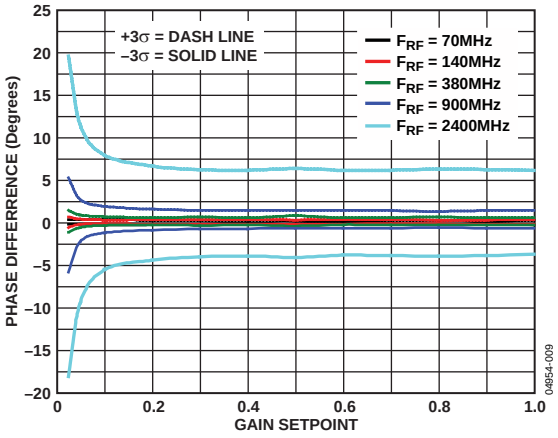


Figure 9. Channel-to-Channel Phase Matching vs. Gain Setpoint, RF Frequency = 70 MHz, 140 MHz, 380 MHz, 900 MHz, 2400 MHz

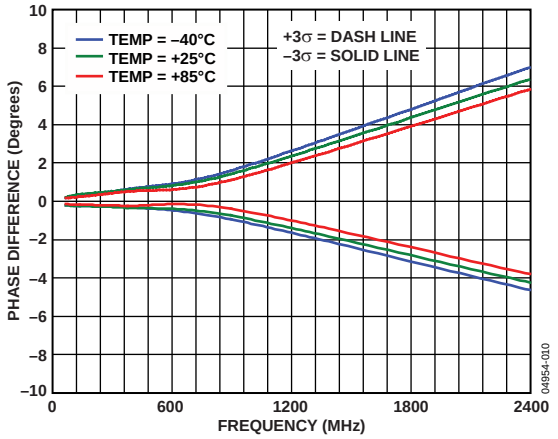


Figure 10. Channel-to-Channel Phase Matching vs. RF Frequency, Temp = +85°C, +25°C, –40°C, Gain Setpoint = 1.0

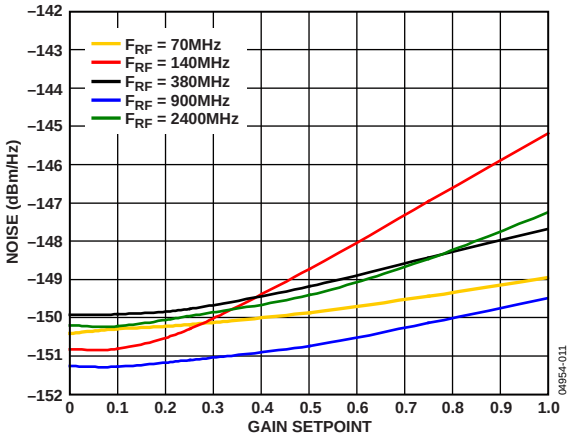


Figure 11. Output Noise Floor vs. Gain Setpoint, No RF Carrier, RF Frequency = 70 MHz, 140 MHz, 380 MHz, 900 MHz, 2400 MHz

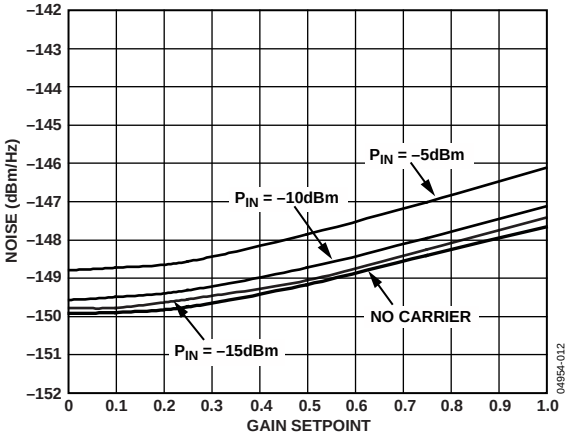


Figure 12. Output Noise Floor vs. Gain Setpoint, No Carrier, with Carrier (20 MHz Offset), RF P_{IN} = –5, –10, –15, No Carrier, RF Frequency = 380 MHz

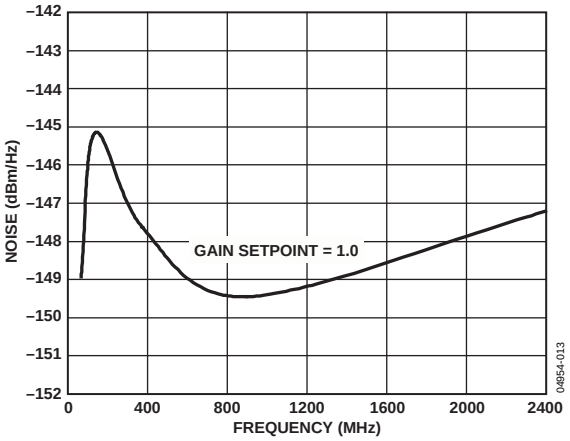


Figure 13. Output Noise Floor vs. RF Frequency, Gain Setpoint = 1.0, No RF Carrier

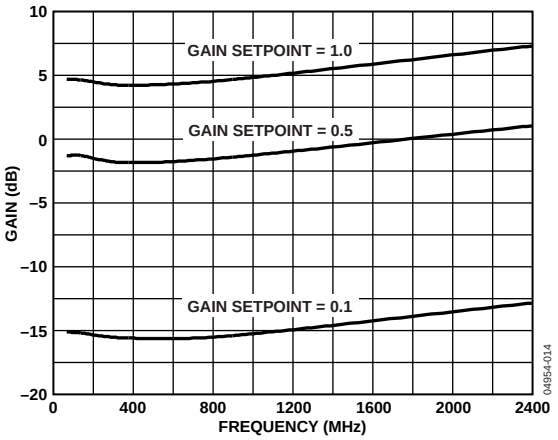


Figure 14. Gain vs. RF Frequency, Gain Setpoint = 1.0, 0.5, 0.1

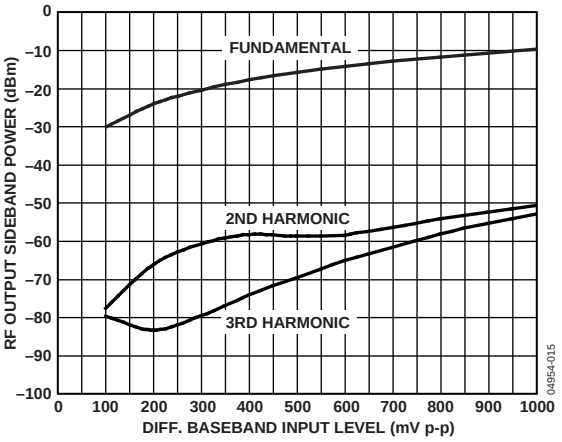


Figure 15. Baseband Harmonic Distortion, (Channel I and Channel Q), RF P_{IN} = −5 dBm, (Balun and Cable Losses Not Included)

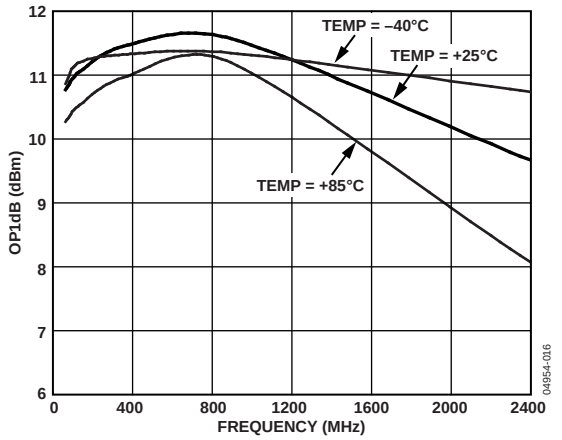


Figure 16. Output 1 dB Compression Point vs. RF Frequency, Temp = +85°C, +25°C, −40°C, Gain Setpoint = 1.0

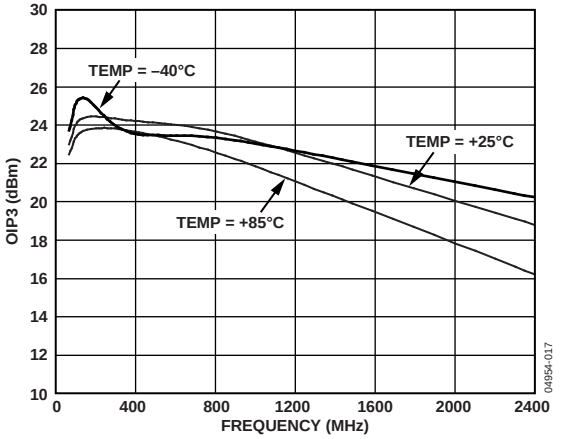


Figure 17. Output IP3 vs. RF Frequency, Temp = +85°C, +25°C, −40°C, Gain Setpoint = 1.0

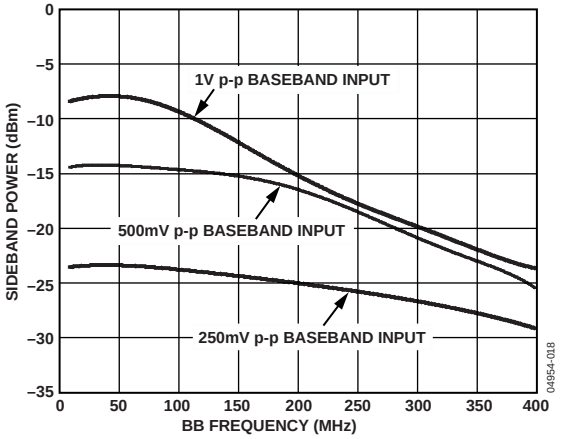


Figure 18. IQ Modulation Bandwidth vs. Baseband Magnitude

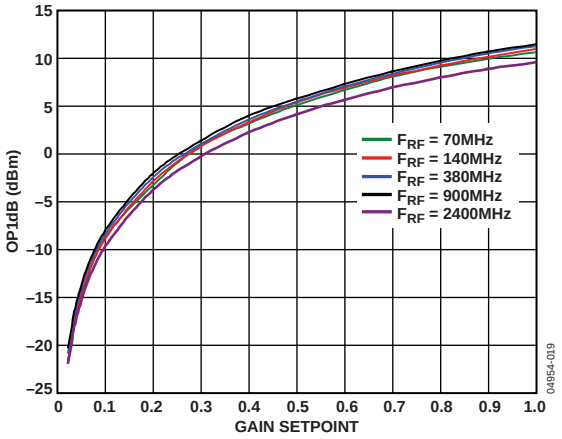


Figure 19. Output 1 dB Compression vs. Gain Setpoint, RF Frequency = 70 MHz, 140 MHz, 380 MHz, 900 MHz, 2400 MHz

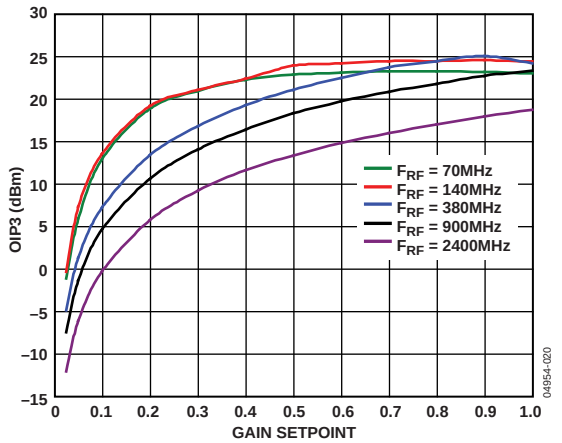


Figure 20. Output IP3 vs. Gain Setpoint, RF Frequency = 70 MHz, 140 MHz, 380 MHz, 900 MHz, 2400 MHz

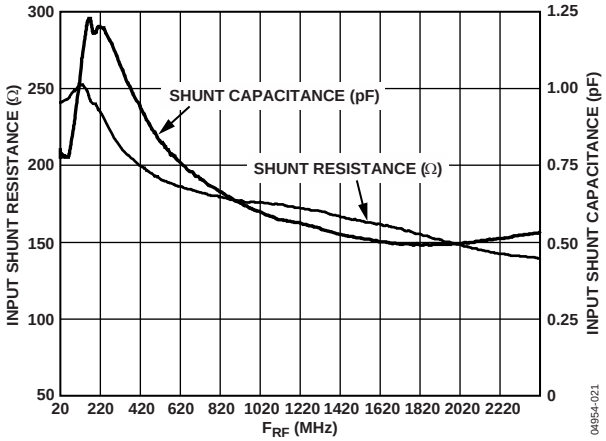


Figure 21. S11 of RF Input (Shunt R/C Representation)

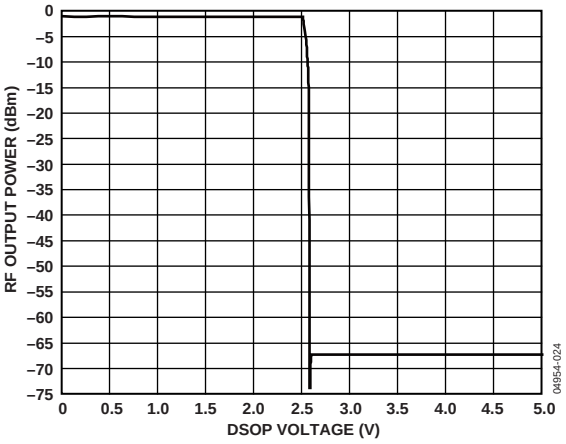


Figure 24. Power Shutdown Attenuation, RF = 380 MHz

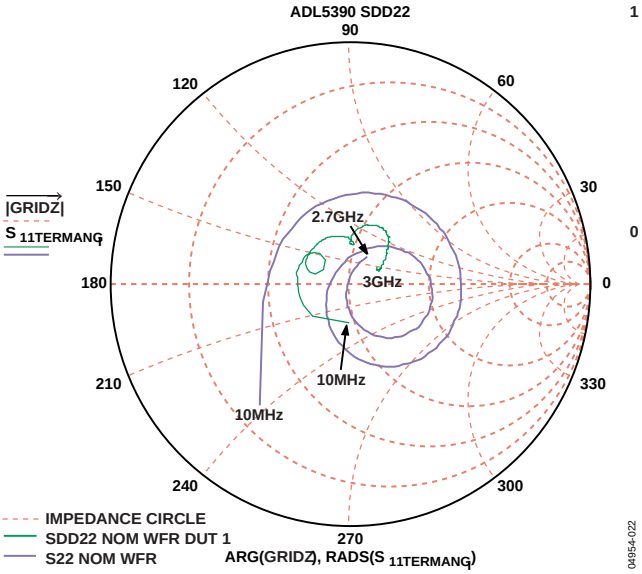


Figure 22. S22 of RF Output (Differential and Single-Ended through Balun)

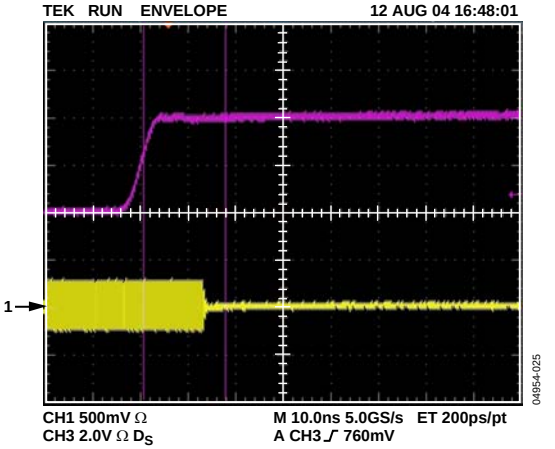


Figure 25. Power Shutdown Response Time, RF = 380 MHz

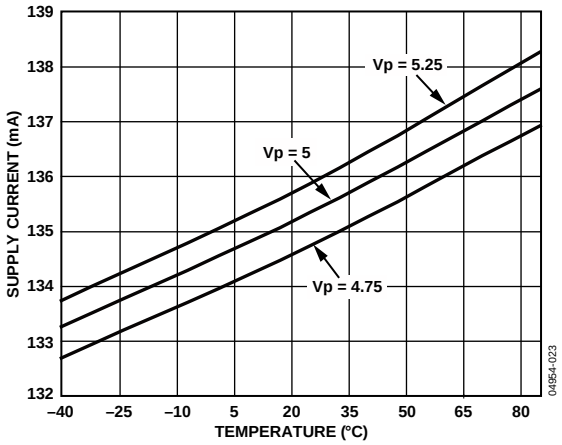


Figure 23. Supply Current vs. Temperature

GENERAL STRUCTURE

THEORY OF OPERATION

The simplified block diagram given in Figure 26 shows a matched pair of variable gain channels whose outputs are summed and presented to the final output. The RF/IF signals propagate from the left to the right, while the baseband gain controls are placed above and below. The proprietary linear-responding variable attenuators offer excellent linearity, low noise, and greater immunity from mismatches than other commonly used methods.

Since the two independent RF/IF inputs can be combined in arbitrary proportions, the overall function can be termed "vector multiplication" as expressed by

$$V_{OUT} = V_{IRF} \times (V_{IBB}/V_O) + V_{QRF} \times (V_{QBB}/V_O)$$

where:
V_{IRF} and V_{QRF} are the RF/IF input vectors.
V_{IBB} and V_{QBB} are the baseband input scalars.
V_O is the built-in normalization factor, which is designed to be 0.285 V (1/3.5 V).

The overall voltage gain, in linear terms, of the I and Q channels is proportional to its control voltage and scaled by the normalization factor, i.e., a full-scale gain of 1.75 (5 dB) for $V_{I\ (Q)BB}$ of 500 mV. A full-scale voltage gain of 1.75 defines a gain setpoint of 1.0.

Due to its versatile functional form and wide signal dynamic range, the ADL5390 can form the core of a variety of useful functions such as quadrature modulators, gain and phase adjusters, and multiplexers. At maximum gain on one channel, the output 1 dB compression point and noise floor referenced to 50 Ω are 11 dBm and −148 dBm/Hz, respectively. The broad frequency response of the RF/IF and gain control ports allows the ADL5390 to be used in a variety of applications at different frequencies. The bandwidth for the RF/IF signal path extends from approximately 20 MHz to beyond 2.4 GHz, while the gain controls signals allow for modulation rates greater than 200 MHz.

Matching between the two gain channels is ensured by careful layout and design. Since they are monolithic and arranged symmetrically on the die, thermal and process gradients are minimized. Typical gain and phase mismatch at maximum gain are <0.5 dB and <0.5°.

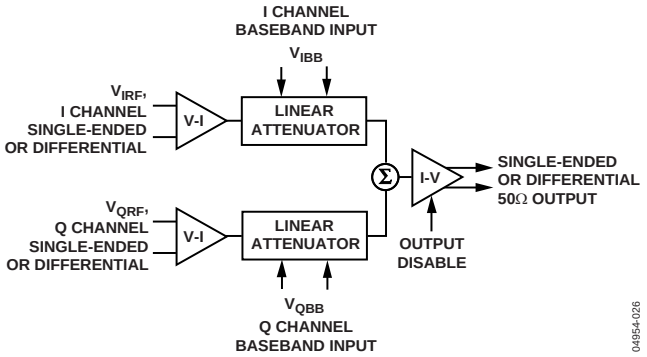


Figure 26. Simplified Architecture of the ADL5390

NOISE AND DISTORTION

The signal path for a particular channel of the ADL5390 consists basically of a preamplifier followed by a variable attenuator and then an output driver. Each subblock contributes some level of noise and distortion to the desired signal. As the channel gain is varied, these relative contributions change. The overall effect is a dependence of output noise floor and output distortion levels on the gain setpoint.

For the ADL5390, the distortion is always determined by the preamplifier. At the highest gain setpoint, the signal capacity, as described by the 1 dB compression point (P1dB) and the third-order intercept (OIP3), are at the highest levels. As the gain is reduced, the P1dB and OIP3 are reduced in exact proportion. At the higher gain setpoints, the output noise is dominated by the preamplifier as well. At lower gains, the contribution from the preamplifier is correspondingly reduced and eventually a noise floor, set by the output driver, is reached. As Figure 27 illustrates, the overall dynamic range defined as a ratio of OIP3 to output noise floor remains constant for the higher gain setpoints. At some gain level, the noise floor levels off and the dynamic range degrades commensurate with the gain reduction.

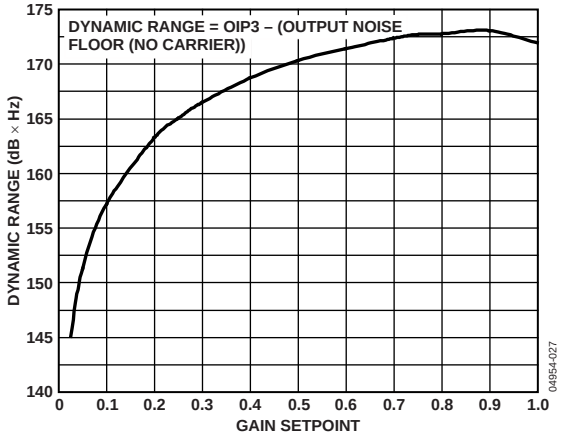


Figure 27. Dynamic Range Variation with Gain Setpoint

APPLICATIONS INFORMATION

USING THE ADL5390

The ADL5390 is designed to operate in a 50 Ω impedance system. Figure 29 illustrates an example where the RF/IF inputs are driven in a single-ended fashion, while the differential RF output is converted to a single-ended output with a RF balun. The baseband gain controls for the I and Q channels are typically driven from differential DAC outputs. The power supplies, VPRF and VPS2, should be bypassed appropriately with 0.1 µF and 100 pF capacitors. Low inductance grounding of the CMOP and CMRF common pins is essential to prevent unintentional peaking of the gain. The exposed paddle on the underside of the package should be soldered to a low thermal and electrical impedance ground plane.

RF INPUT AND MATCHING

The RF/IF inputs present 250 Ω resistive terminations to ground. In general, the input signals should be ac-coupled through dc-blocking capacitors. The inputs may be driven differentially or single-ended, in which case the unused inputs are connected to common via the dc-blocking capacitors. The ADL5390's performance is not degraded by driving these inputs single-ended. The input impedance can be reduced by placing external shunt termination resistors to common on the source side of the dc-blocking capacitors so that the quiescent dc-bias level of the ADL5390 inputs is not affected, as shown in Figure 29. Capacitive reactance at the RF inputs can be compensated for with series inductance. In fact, the customer evaluation board has high impedance line traces between the shunt termination pads and the device input pins, which provides series inductance and improves the return loss at 1.9 GHz to better than −15 dB with the shunt termination removed, as shown in Figure 28.

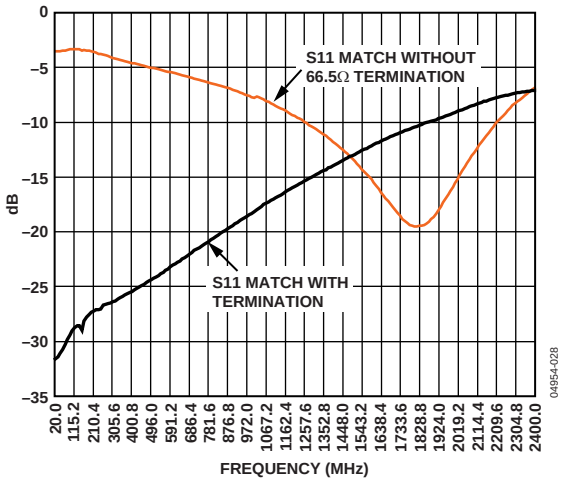


Figure 28. ADL5390 Customer Evaluation Board RF Input Return Loss.

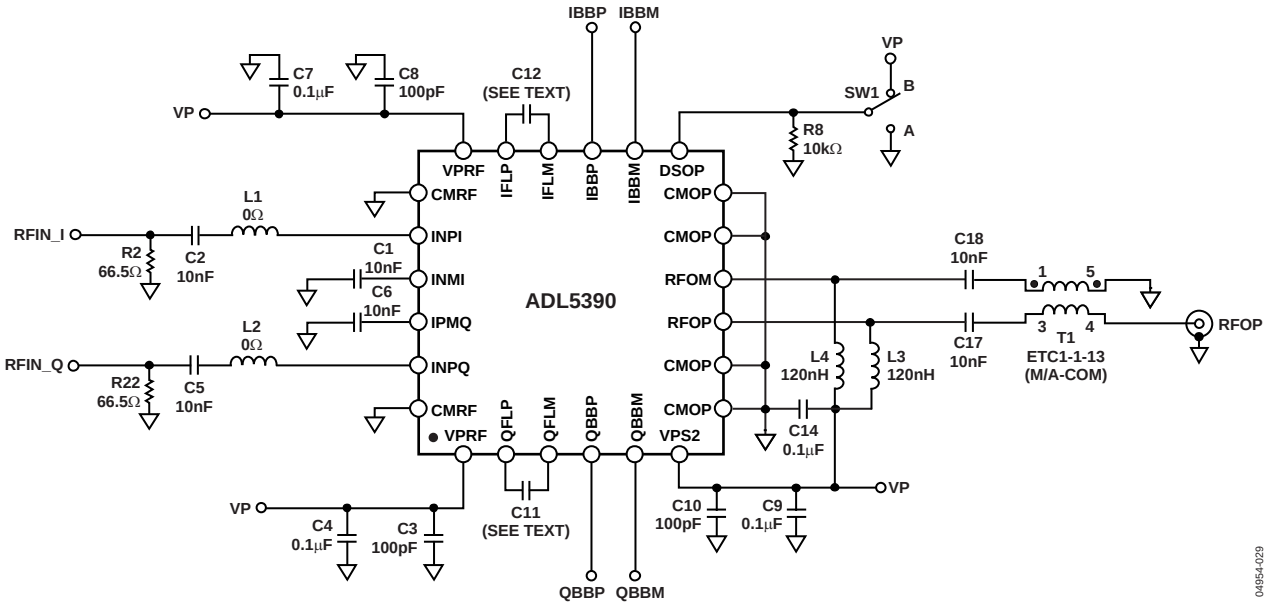


Figure 29. Basic Connections

RF OUTPUT AND MATCHING

The RF/IF outputs of the ADL5390, RFOP and RFOM, are open collectors of a transimpedance amplifier that need to be pulled up to the positive supply, preferably with RF chokes, as shown in Figure 30. The nominal output impedance looking into each individual output pin is 25 Ω. Consequently, the differential output impedance is 50 Ω.

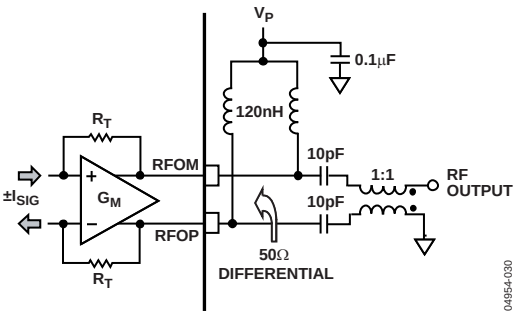


Figure 30. RF Output Interface to the ADL5390 Showing Coupling Capacitors, Pull-Up RF Chokes, and Balun

Since the output dc levels are at the positive supply, ac-coupling capacitors are usually needed between the ADL5390 outputs and the next stage in the system.

A 1:1 RF broadband output balun, such as the ETC1-1-13 (M/A-COM), converts the differential output of the ADL5390 into a single-ended signal. Note that the loss and balance of the balun directly impact the apparent output power, noise floor, and gain/phase errors of the ADL5390. In critical applications, narrowband baluns with low loss and superior balance are recommended.

If the output is taken in a single-ended fashion directly into a 50 Ω load through a coupling capacitor, there will be an impedance mismatch. This can be resolved with a 1:2 balun to convert the single-ended 25 Ω output impedance to 50 Ω. If loss of signal swing is not critical, a 25 Ω back termination in series with the output pin can also be used. The unused output pin must still be pulled up to the positive supply. The user may load it through a coupling capacitor with a dummy load to preserve balance. The mismatched gain of the ADL5390 when the output is single-ended varies slightly with dummy load value, as shown in Figure 31.

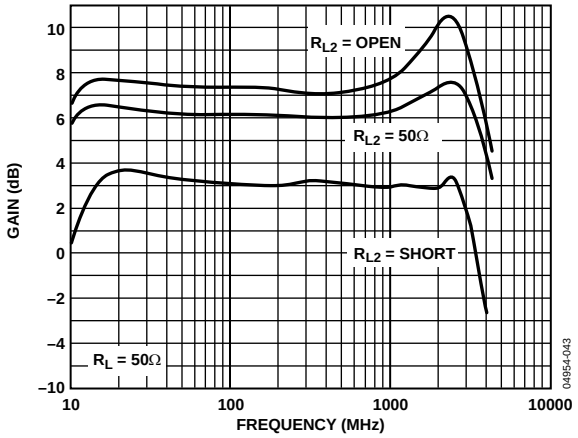


Figure 31. Gain of the ADL5390 Using a Single-Ended Output with Different Dummy Loads, R_{L2} on the Unused Output, Gain Setpoint = 1.0

The RF output signal can be disabled by raising the DSOP pin to the positive supply. The output disable function provides >40 dB attenuation of the input signal, even at full gain. The interface to DSOP is high impedance and the output disable and output enable response times are <100 ns. If the output disable function is not needed, the DSOP should be tied to ground.

DRIVING THE I-Q BASEBAND GAIN CONTROLS

The I and Q gain control inputs to the ADL5390 set the gain for each channel. These inputs are differential and should normally have a common-mode level of 0.5 V. However, when differentially driven, the common mode can vary from 250 mV to 750 mV while still allowing full gain control. Each input pair has a nominal input swing of ±0.5 V differential around the common-mode level. The maximum gain is achieved if the differential voltage is equal to +500 mV or −500 mV. So with a common-mode level of 500 mV, IBBP and IBBM will each swing between 250 mV and 750 mV.

The I and Q gain control inputs can also be driven with a single-ended signal. In this case, one side of each input should be tied to a low noise 0.5 V voltage source (a 0.1 µF decoupling capacitor located close to the pin is recommended), while the other input swings from 0 V to 1 V. Low speed, single-ended drive can easily be achieved using 12-bit voltage output DACs such as AD8303 (serial SPI® interface) or AD8582 (parallel interface) DACs. A reference voltage should also be supplied. Differential drive generally offers superior even-order distortion and lower noise than single-ended drive.

The bandwidth of the baseband controls exceeds 200 MHz even at full-scale baseband drive. This allows for very fast gain modulation of the RF input signal. In cases where lower modulation bandwidths are acceptable or desired, external filter capacitors can be connected across Pins IFLP to IFLM and Pins QFLP to QFLM to reduce the ingress of baseband noise and spurious signal into the control path.

The 3 dB bandwidth is set by choosing C_{FLT} according to the following equation:

$$f_{3\,dB} \approx \frac{45\ \text{kHz} \times 10\ \text{nF}}{C_{external} + 0.5\ \text{pF}}$$

This equation has been verified for values of C_{FLT} from 10 pF to 0.1 µF (bandwidth settings of approximately 4.5 kHz to 43 MHz).

INTERFACING TO HIGH SPEED DACs

The AD977x family of dual DACs is well suited to driving the I and Q gain controls of the ADL5390 with fast modulating signals. While these inputs can in general be driven by any DAC, the differential outputs and bias level of the ADI TxDAC® family allows for a direct connection between DAC and modulator.

The AD977x family of dual DACs has differential current outputs. The full-scale current is user programmable and is usually set to 20 mA, that is each output swings from 0 mA to 20 mA.

The basic interface between the AD9777 DAC outputs and the ADL5390 I and Q gain control inputs is shown in Figure 32. Resistors R1 and R2 (R1 = R2) set the dc bias level according to the following equation:

Bias Level = Average Output Current × R1

For example, if the full-scale current from each output is 20 mA, each output will have an average current of 10 mA. Therefore, to set the bias level to the recommended 0.5 V, R1 and R2 should be set to 50 Ω each. R1 and R2 should always be equal.

If R3 is omitted, this will result in an available swing from the DAC of 2 V p-p differential, which is twice the maximum voltage range required by the ADL5390. DAC resolution can be maximized by adding R3, which scales down this voltage according to the following equation:

Full Scale Swing =

$$2 \times I_{MAX}\left(R1 \,||\, \left(R2 + R3\right)\right) \times \left[1 - \frac{R2}{R2 + R3}\right]$$

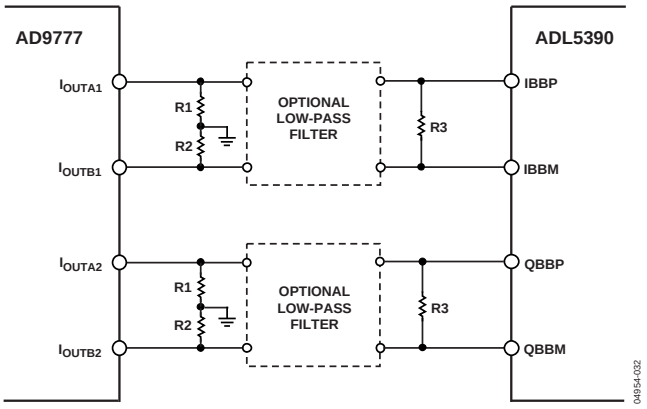


Figure 32. Basic AD9777-to-ADL5390 Interface

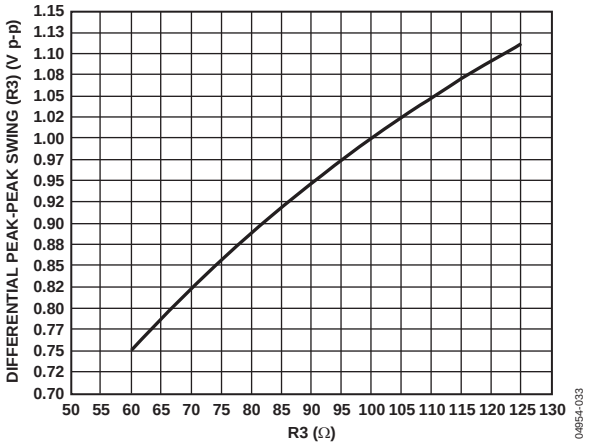


Figure 33. Peak-Peak DAC Output Swing vs. Swing Scaling Resistor R3 (R1 = R2 = 50 Ω)

Figure 33 shows the relationship between the value of R3 and the peak baseband voltage with R1 and R2 equal to 50 Ω. As shown in Figure 33, a value of 100 Ω for R3 will provide a peak-peak swing of 1 V p-p differential into the ADL5390's I and Q inputs.

When using a DAC, low-pass image reject filters are typically used to eliminate the Nyquist images produced by the DAC. They also provide the added benefit of eliminating broadband noise that might feed into the modulator from the DAC.

GENERALIZED MODULATOR

The ADL5390 can be configured as a traditional IQ quadrature modulator or as a linear vector modulator by applying signals that are in quadrature to the RF/IF input channels. Since the quadrature generation is performed externally, its accuracy and bandwidth are determined by the user. The user-defined bandwidth is attractive for multioctave or lower IF applications where on-chip, high accuracy quadrature generation is traditionally difficult or impractical. The gain control pins ($I_{BBP/M}$ and $Q_{BBP/M}$) become the in-phase (I) and quadrature (Q) baseband inputs for the quadrature modulator and the gain/phase control for the vector modulator. The wide modulation bandwidths of the gain control interface allow for high fidelity baseband signals to be generated for the quadrature modulator and for high speed gain and phase adjustments to be generated for the vector modulator.

RF/IF signals can be introduce to the ADL5390 in quadrature by using a two-way 90° power splitter such as the Mini-Circuits QCN-12. Each output of an ideal 90° power splitter is 3 dB smaller than the input and has a 90° phase difference from the other output. In reality, the 90° power splitter will have its own insertion loss, which can be different for each output, causing a magnitude imbalance. Furthermore, quadrature output will not be maintained over a large frequency range, introducing a phase imbalance. The type of 90° power splitter that should be used for a particular application will be determined by the frequency, bandwidth, and accuracy needed. In some applications minor magnitude and phase imbalances can be adjusted for in the I/Q gain control inputs.

VECTOR MODULATOR

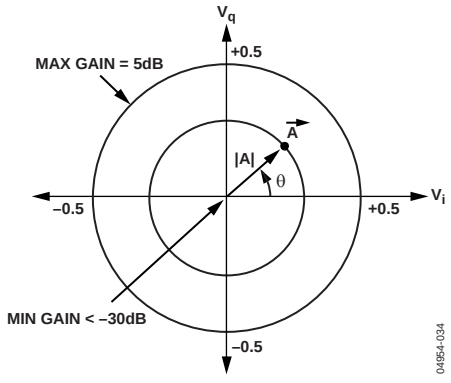


Figure 34. Vector Gain Representation

The ADL5390 can be used as a vector modulator by driving the RF I and Q inputs single-ended through a 90° power splitter. By controlling the relative amounts of I and Q components that are summed, continuous magnitude and phase control of the gain is possible. Consider the vector gain representation of the ADL5390 expressed in polar form in Figure 34. The attenuation factors for the RF I and Q signal components are represented on the x-axis and y-axis, respectively, by the baseband gain control inputs V_{IBB} and V_{QBB}. The resultant of their vector sum represents the vector gain, which can also be expressed as a magnitude and phase. By applying different combinations of baseband inputs, any vector gain within the unit circle can be programmed. The magnitude and phase (with respect to 90°) accuracy of the 90° power splitter will directly affect this representation and could be seen as an offset and skew of the circle.

A change in sign of V_{IBB} or V_{QBB} can be viewed as a change in sign of the gain or as a 180° phase change. The outermost circle represents the maximum gain magnitude. The circle origin implies, in theory, a gain of 0. In practice, circuit mismatches and unavoidable signal feedthrough limit the minimum gain to approximately −30 dB. The phase angle between the resultant gain vector and the positive x-axis is defined as the phase shift. Note that there is a nominal, systematic insertion phase through the ADL5390 to which the phase shift is added. In the following discussions, the systematic insertion phase is normalized to 0°.

The correspondence between the desired gain and phase and the Cartesian inputs V_{IBB} and V_{QBB} is given by simple trigonometric identities

$$Gain = \sqrt{\left[\left(V_{IBB}/V_O\right)^2 + \left(V_{QBB}/V_O\right)^2\right]}$$

$$Phase = arctan\left(V_{QBB}/V_{IBB}\right)$$

where:
V_O is the baseband scaling constant (285 mV).
V_{IBB} and V_{QBB} are the differential I and Q baseband voltages centered around 500 mV, respectively ($V_{IBB} = V_{IBBP} - V_{IBBM}$; $V_{QBB} = V_{QBBP} - V_{QBBM}$).

Note that when evaluating the arctangent function, the proper phase quadrant must be selected. For example, if the principal value of the arctangent (known as arctangent(x)) is used, quadrants 2 and 3 would be interpreted mistakenly as quadrants 4 and 1, respectively. In general, both V_{IBB} and V_{QBB} are needed in concert to modulate the gain and the phase.

Pure amplitude modulation is represented by radial movement of the gain vector tip at a fixed angle, while pure phase modulation is represented by rotation of the tip around the circle at a fixed radius. Unlike traditional I-Q modulators, the ADL5390 is designed to have a linear RF signal path from input to output. Traditional I-Q modulators provide a limited LO carrier path through which any amplitude information is removed.

VECTOR MODULATOR EXAMPLE—CDMA2000

The ADL5390 can be used as a vector modulator by driving the RF I and Q inputs (INPI and INPQ) single-ended through a 90° power splitter and controlling the magnitude and phase using the gain control inputs. To demonstrate operation as a vector modulator, an 880 MHz single-carrier CDMA2000 test model signal (forward pilot, sync, paging, and six traffic as per 3GPP2 C.S0010-B, Table 6.5.2.1) was applied to the ADL5390. A cavity-tuned filter was used to reduce noise from the signal

source being applied to the device. The 4.6 MHz pass band of this filter is apparent in the subsequent spectral plots.

Figure 35 shows the output signal spectrum for a programmed gain and phase of 5 dB and 45°. P_{OUT} is equal to 0 dBm and $V_{IBB} = V_{QBB} = 0.353$ V (centered around 500 mV), that is , $V_{IBBP} - V_{IBBM} = V_{QBBP} - V_{QBBM} = 0.353$ V. Adjacent channel power is measured in 30 kHz resolution bandwidth at 750 kHz and 1.98 MHz carrier offset. Noise floor is measured at ±4 MHz carrier offset in a 1 MHz resolution bandwidth.

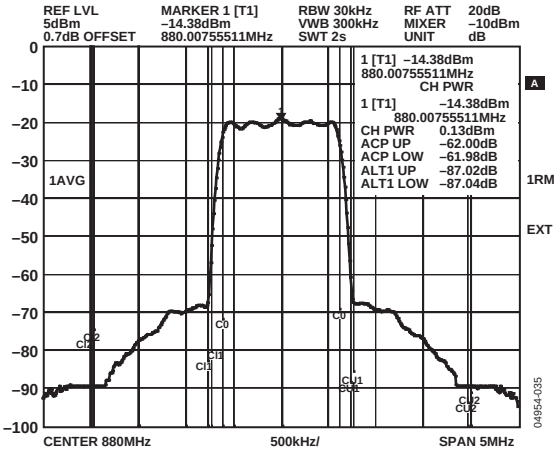


Figure 35. Output Spectrum, Single-Carrier CDMA2000 Test Model at −5 dBm, $V_I = V_Q = 0.353$ V, ACP Measured at 750 kHz and 1.98 MHz Carrier Offset, Input Signal–Filtered Using a Cavity-Tuned Filter (Pass Band = 4.6 MHz)

Holding the I and Q gain control voltages steady at 0.353 V, input power was swept. Figure 36 shows the resulting output power, noise floor, and adjacent channel power ratio. The noise floor is presented as noise in a 1 MHz bandwidth as defined by the 3GPP2 specification.

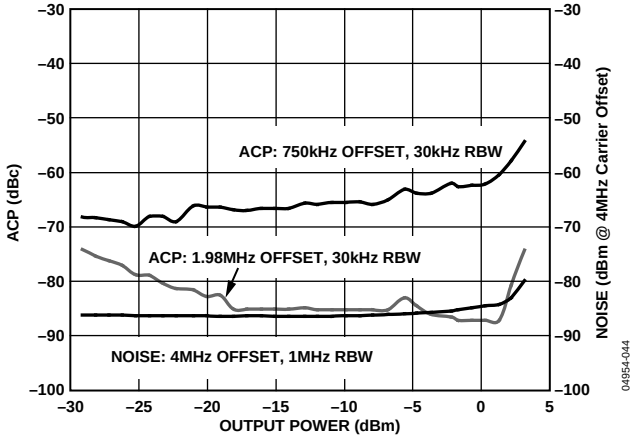


Figure 36. Noise and ACP vs. Output Power, Single-Carrier CDMA2000 Test Model, $V_I = V_Q = 0.353$, ACP Measured in 30 kHz RBW at ±750 kHz and ±1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset

ACP is still in compliance with the standard (<−45 dBc at 750 kHz and <−60 dBc at 1.98 MHz) even with output powers greater than +3 dBm. At low output power levels, ACP at 1.98 MHz carrier offset degrades as the noise floor of the ADL5390 becomes the dominant contributor to measured ACP.

Measured noise at 4 MHz carrier offset begins to increase sharply above 2 dBm output power. This increase is not due to noise, but results from increased carrier-induced distortion. As output power drops below 2 dBm, the noise floor drops towards −90 dBm.

With a fixed input power of 2.16 dBm, the output power was again swept by changing V_{IBB} and V_{QBB} from 0 V to 500 mV. The resulting output power, ACP, and noise floor are shown in Figure 37.

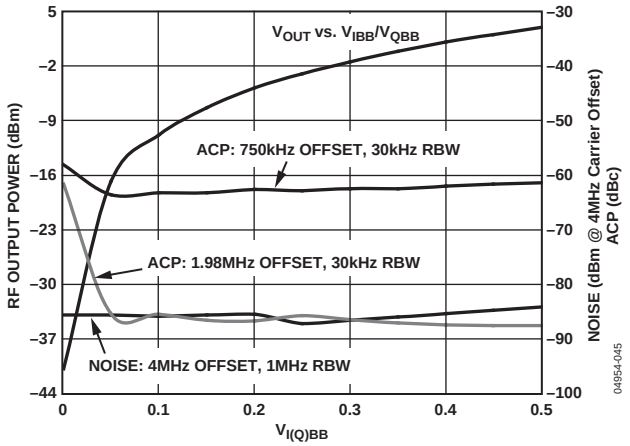


Figure 37. Output Power, Noise, and ACP vs. I and Q Control Voltages, CDMA2000 Test Model, $V_I = V_Q$, ACP Measured in 30 kHz RBW at ±750 MHz and ±1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset

In contrast to Figure 36, Figure 37 shows that for a fixed input power, ACP remains fairly constant as gain and phase are changed (this is not true for very high RF input powers) until the noise floor of the ADL5390 becomes the dominant contributor to the measured ACP.

QUADRATURE MODULATOR

The ADL5390 can be used as a quadrature modulator by driving the RF I and Q inputs (INPI and INPQ) single-ended through a 90° phase splitter to serve as the LO input. I/Q modulation is applied to the baseband I and Q gain control inputs (IBBP/IBBM and QBBP/QBBM). A simplified schematic is shown in Figure 38.

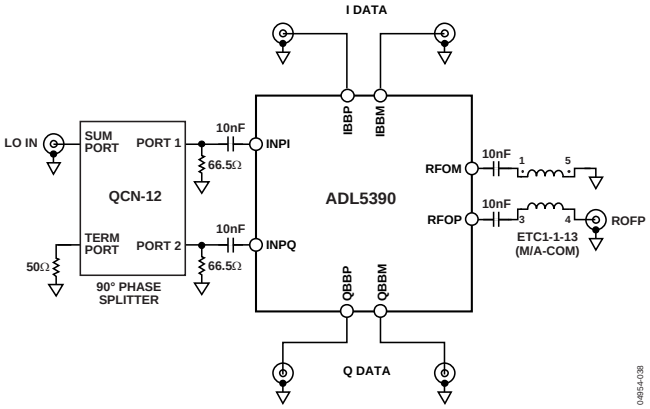


Figure 38. Quadrature Modulator Application

Single sideband performance of a quadrature modulator is determined by the magnitude and phase balance (compared to a 90° offset) at the summation point of the I and Q signals. Because the ADL5390 has matched amplifiers and mixers in the I and Q channel, most of the single sideband performance will be determined by the external 90° phase splitter. Good single sideband performance can be achieved by choosing a well-balanced 90° phase splitter. However, phase and magnitude differences in the 90° phase splitter can be corrected by adjusting the magnitude and phase of the I and Q data. Figure 39 shows the performance of the ADL5390 used in conjunction with sMini-Circuits QCN-12 90° power splitter. Figure 40 shows the single sideband improvement as the I and Q data is adjusted in magnitude and phase to achieve better single sideband performance.

For maximum dynamic range, the ADL5390 should be driven as close to the output 1 dB compression point as possible. The output power of the ADL5390 increases linearly with the RF (LO) input power and baseband gain control input voltage until the ADL5390 reaches compression. At the 1 dB compression point, the lower sideband starts to increase. Figure 41 demonstrates the output spectrum of a 3-carrier CDMA2000 signal applied to the I/Q baseband gain control inputs. As the RF (LO) power is increased, the relative amount of noise is reduced until the ADL5390 goes into compression. At this point, the relative noise increases, as shown in Figure 42.

Analog Devices has several quadrature/vector modulators that have highly accurate integrated 90° phase splitters—AD8340, AD8341, AD8345, AD8346, AD8349—that cover a variety of frequency bands.

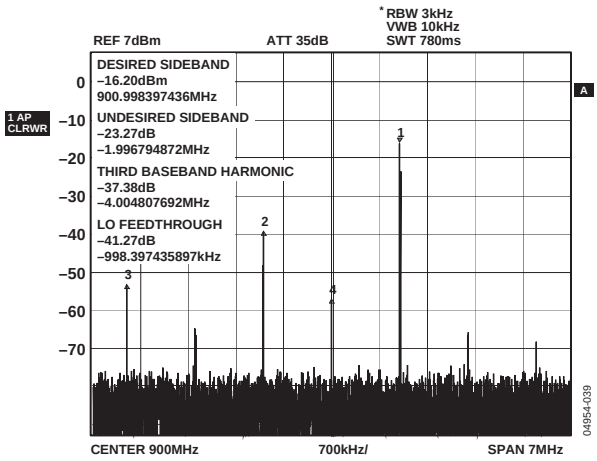


Figure 39. SSB Quadrature Modulator Result Using External 90° Phase Splitter, RF P_{IN} = −15 dBm, VIBB = VQBB = 0.5 V (With Reference to a Common-Mode Voltage of 0.5 V)

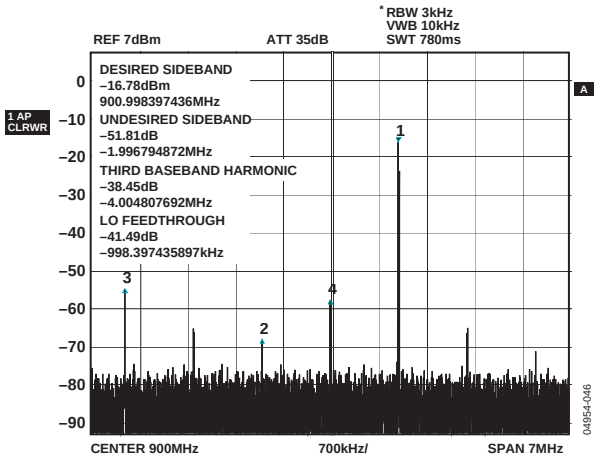


Figure 40. SSB Modulator Applications with Gain and Phase Errors Corrected, RF Pin = −15 dBm, VIBB = VQBB = 0.5 V (With Reference to a Common-Mode Voltage of 0.5 V), I/Q Phase Offset by 3°, and Magnitude Offset by 0.5 V

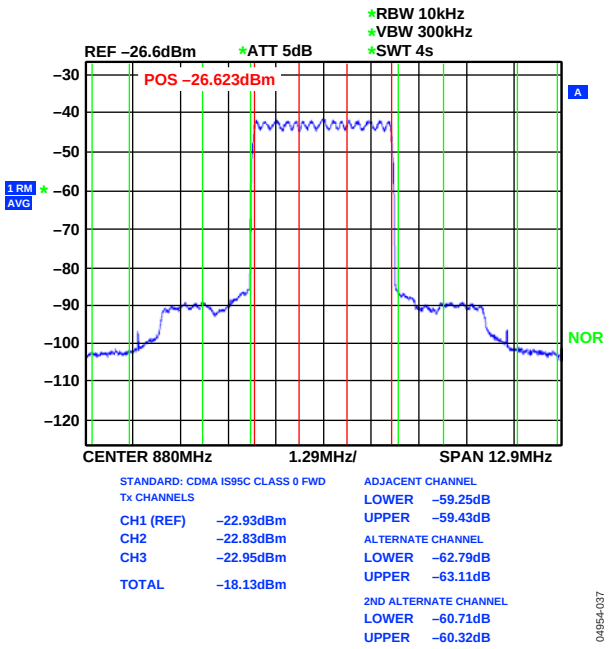


Figure 41. ADL5390 as a Quadrature Modulator with the Use of an External 90°Phase Splitter, RF/LO Power = −1 dBm and Gain Control Inputs Driven Differentially with 0.353 V_{P-P}, 3-Carrier CDMA2000 I/Q Data

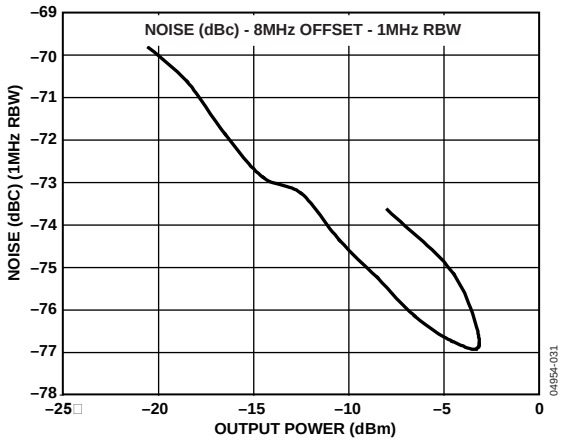


Figure 42. Noise vs. Output Power

RF MULTIPLEXER

The ADL5390 may also be used as an RF multiplexer. In this application, two RF signals are applied to the INPI and INPQ inputs, and the baseband voltages control which of the two RF signals appears at the output. Figure 43 illustrates this application and shows that with V_{IBB} = 0.5 and V_{QBB} = 0.0 (with reference to a common-mode voltage of 0.5 V). The INPI signal is presented to the output. Then, when V_{IBB} transitions to V_{IBB} = 0.0 and V_{QBB} remains equal to zero, there is no RF output. Lastly, as V_{QBB} transitions to 0.5 V, the INPQ signal appears at the output. With V_{IBB} = 0.0 and V_{QBB} = 0.0, the isolation to the output is typically >40 dB at 380 MHz.

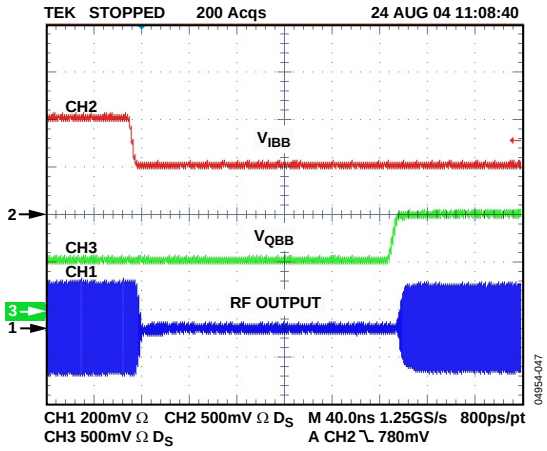


Figure 43. ADL5390 in RF Multiplexer Application

EVALUATION BOARD

The evaluation board circuit schematic for the ADL5390 is shown in Figure 44.

The evaluation board is configured to be driven from a single-ended 50 Ω source. Although the input of the ADL5390 is differential, it may be driven single-ended with no loss of performance.

The low-pass corner frequency of the baseband I and Q channels can be reduced by installing capacitors in the C11 and C12 positions. The low-pass corner frequency for either channel is approximated by

$$f_{3\text{ dB}} \approx \frac{45\text{ kHz} \times 10\text{ nF}}{C_{external} + 0.5\text{ pF}}$$

On this evaluation board, the I and Q baseband circuits are identical to each other, so the following description applies to each. The connections and circuit configuration for the I/Q baseband inputs are described in Table 4.

The baseband input of the ADL5390 requires a differential voltage drive. The evaluation board is set up to allow such a drive by connecting the differential voltage source to QBBP and QBBM. The common-mode voltage should be maintained at approximately 0.5 V. For this configuration, Jumpers W1 to W4 should be removed.

The baseband input of the evaluation board may also be driven with a single-ended voltage. In this case, a bias level is provided to the unused input from Potentiometer R10 by installing either W1 or W2.

Setting SW1 in Position B disables the ADL5390 output amplifier. With SW1 set to Position A, the output amplifier is enabled. With SW1 set to Position A, an external voltage signal, such as a pulse, can be applied to the DSOP SMA connector to exercise the output amplifier enable/disable function.

Table 4. Evaluation Board Configuration Options

Component	Function	Default Conditions
R7, R9, R11, R14, R15, R19, R20, R21, C15, C19, W3, W4	I Channel Baseband Interface. Resistors R7 and R9 may be installed to accommodate a baseband source that requires a specific terminating impedance. Capacitors C15 and C19 are bypass capacitors. For single-ended baseband drive, the Potentiometer R11 can be used to provide a bias level to the unused input (install either W3 or W4).	R7, R9 = not installed R11 = potentiometer, 2 kΩ, 10 turn (Bourns) R14 = 4 kΩ (Size 0603) R15 = 44 kΩ (Size 0603) R19, R20, R21 = 0 Ω (Size 0603) C15, C19 = 0.1 µF (Size 0603) W3 = jumper (installed) W4 = jumper (open)
R1, R3, R10, R12, R13, R16, R17, R18, C16, C20, W1, W2	Q Channel Baseband Interface. See the I Channel Baseband Interface section.	R1, R3 = not installed R10 = potentiometer, 2 kΩ, 10 turn (Bourns) R12 = 4 kΩ (Size 0603) R13 = 44 kΩ (Size 0603) R16, R17, R18 = 0 Ω (Size 0603) C16, C20 = 0.1 µF (Size 0603) W1 = jumper (installed) W2 = jumper (open)
C11, C12	Baseband Low-Pass Filtering. By adding capacitor C11 between QFLP and QFLM, and capacitor C12 between IFLP and IFLM, the 3 dB low-pass corner frequency of the baseband interface can be reduced from 230 MHz (nominal) as given by the equation in the Evaluation Board section.	C11, C12 = not installed
T1, C17, C18, L3, L4	Output Interface. The 1:1 balun transformer, T1, converts the 50 Ω differential output to 50 Ω single-ended. C17 and C18 are dc blocks. L3 and L4 provide dc bias for the output.	C17, C18 = 10 nF (Size 0603) T1 = ETC1-1-13 (M/A-COM) L3, L4 = 120 nH (size 0603)
C2, C1, R2 C5, C6, R22	I and Q Channel RF Input Interface. The single-ended impedance to the ADL5390 RF inputs is 200 Ω. Shunt terminations R2 and R22 of 66.5 Ω bring the impedances to 50 Ω. C2 and C5 are dc blocks. C1 and C6 are used to ac-couple the unused side of the differential inputs to common.	C2 = C1 = 10 nF (Size 0603) R2 = 66.5 Ω (Size 0603) C5 = C6 = 10 nF (Size 0603) R22 = 66.5 Ω (Size 0603)
R4, R6, R5, C4, C7 C9, C3, C8, C10	Power Supply Decoupling.	R4, R6, R5 = 0 Ω (Size 0603) C4, C7, C9 = 0.1 µF (Size 0603) C3, C8, C10 = 100 pF (Size 0603)
R8, SW1	Output Disable Interface. The output stage of the ADL5390 is disabled by applying a high voltage to the DSOP pin by moving SW1 to Position B. The output stage is enabled moving SW1 to Position A. The output disable function can also be exercised by applying an external high or low voltage to the DSOP SMA connector with SW1 in Position A.	R8 = 10 kΩ (Size 0603) SW1 = SPDT (Position A, output enabled)

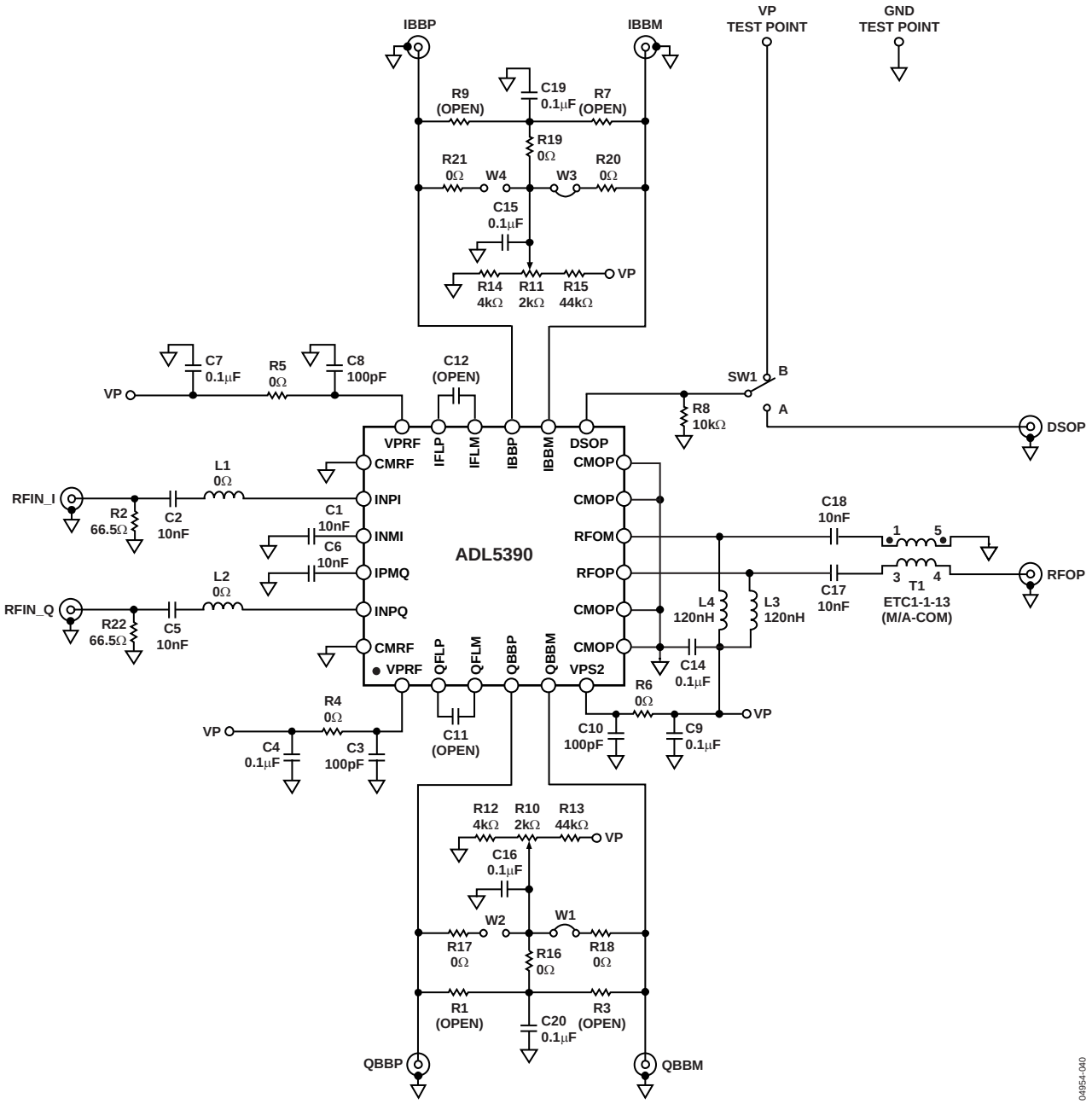


Figure 44. Evaluation Board Schematic

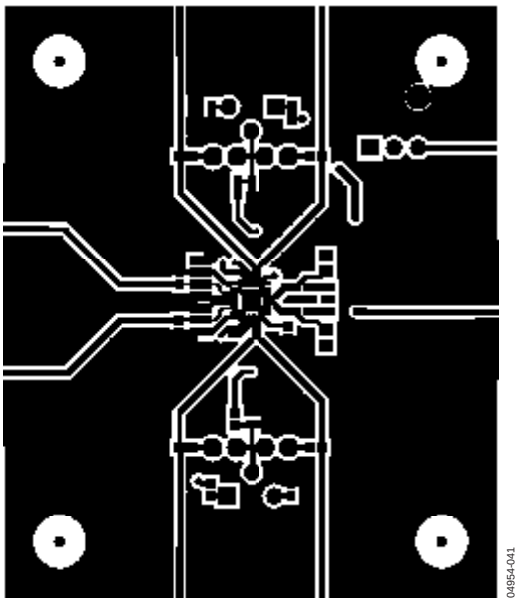


Figure 45. Component Side Layout

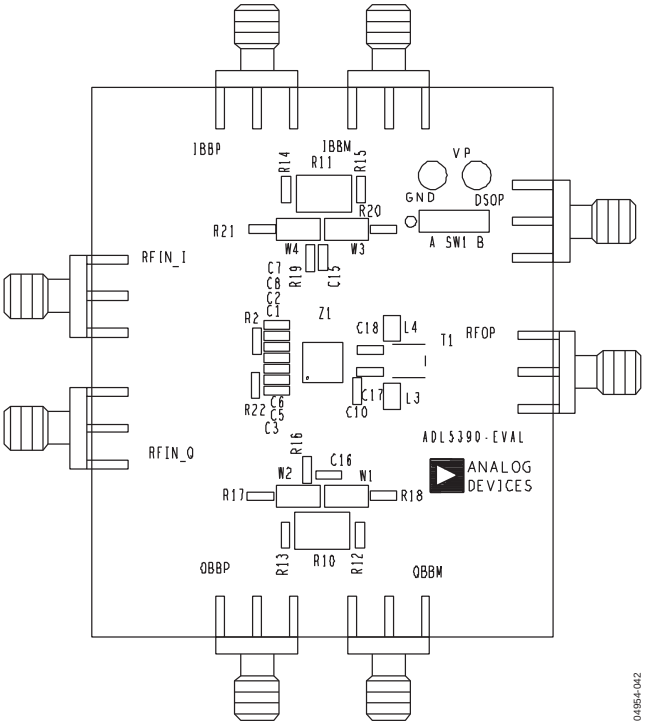
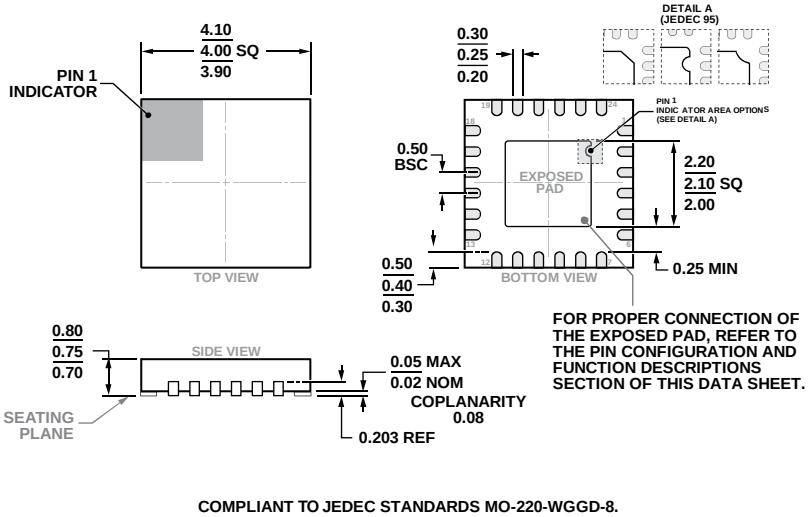


Figure 46. Component Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 47. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Models[1, 2]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5390ACPZ-WP	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10	64
ADL5390ACPZ-REEL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package[LFCSP]	CP-24-10	1,500
ADL5390-EVALZ		Evaluation Board		1

[1] Z = RoHS compliant part.
[2] WP = waffle pack.

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