300 MHz to 1100 MHz Balanced Mixer, LO Buffer, and RF Balun

Data Sheet

ADL5369

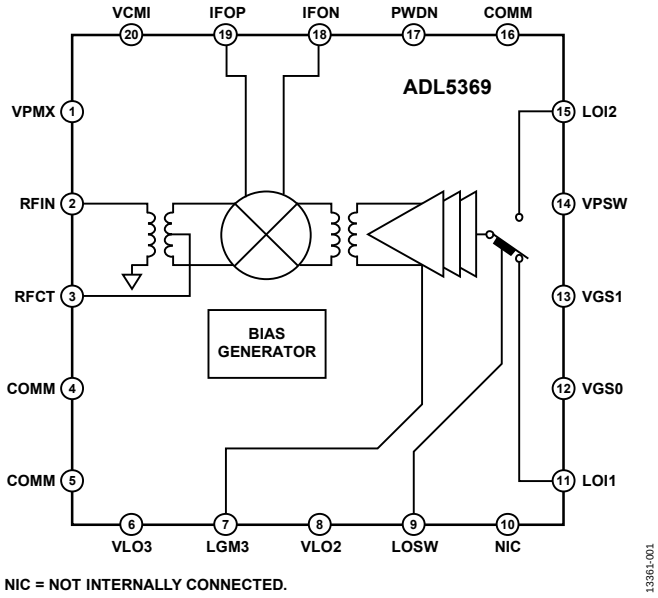
FEATURES

- RF frequency range of 300 MHz to 1100 MHz
- IF frequency range of 30 MHz to 450 MHz
- Power conversion loss: 6.2 dB
- SSB noise figure of 7.2 dB
- Input IP3 of 28 dBm
- Typical LO interface return loss of 0 dBm
- Single-ended, 50 Ω RF and LO input ports
- High isolation SPDT LO input switch
- Typical single-supply operation: 3.3 V to 5 V
- Exposed pad, 5 mm × 5 mm, 20-lead LFCSP

APPLICATIONS

- Cellular base station receivers
- Transmit observation receivers
- Radio link downconverters

FUNCTIONAL BLOCK DIAGRAM



NIC = NOT INTERNALLY CONNECTED.

Figure 1.

GENERAL DESCRIPTION

The ADL5369 uses a highly linear, doubly balanced passive mixer core along with integrated radio frequency (RF) and local oscillator (LO) balancing circuitry to allow single-ended operation. The ADL5369 incorporates an RF balun, allowing optimal performance over a 300 MHz to 1100 MHz RF input frequency range. The balanced passive mixer arrangement provides good LO to RF leakage, typically better than −25 dBm, and excellent intermodulation performance. The balanced mixer core also provides extremely high input linearity, allowing the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in the degradation of dynamic performance. The passive mixer core yields a typical power conversion loss of 6.2 dB.

The ADL5369 provides two switched LO paths that can be used in time division duplex (TDD) applications where it is desirable to rapidly switch between two local oscillators. LO current can be externally set using a resistor to minimize dc current commensurate with the desired level of performance. For low voltage applications, the ADL5369 is capable of operation at voltages down to 3.3 V with substantially reduced current. Under low voltage operation, an additional logic pin is provided to power down (<200 µA) the circuit when desired.

The ADL5369 is fabricated using a BiCMOS high performance IC process. The device is available in a 5 mm × 5 mm, 20-lead LFCSP and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Table 1. Passive Mixers

RF Frequency (MHz)	Single Mixer	Single Mixer and IF Amp	Dual Mixer and IF Amp
300 to 1100	ADL5369	Not applicable	Not applicable
500 to 1700	ADL5367	ADL5357	ADL5358
1200 to 2500	ADL5365	ADL5355	ADL5356
2200 to 2700	Not applicable	ADL5353	ADL5354
2300 to 2900	ADL5363	Not applicable	Not applicable

Rev. A
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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REVISION HISTORY

5/16—Rev. 0 to Rev. A

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1/16—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_S) = 5 V, supply current (I_S) = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, Z_O = 50 Ω, R9 = 1.7 kΩ, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		10		dB
Input Impedance			50		Ω
RF Frequency Range		300		1100	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 93 MHz		35.2||11.9		Ω||pF
IF Frequency Range		30		450	MHz
DC Bias Voltage[1]	Externally generated	3.3	5.0	5.5	V
LO INTERFACE					
LO Power		−6	0	+10	dBm
Return Loss			16.5		dB
Input Impedance			50		Ω
LO Frequency Range		330		1550	MHz
POWER-DOWN (PWDN) INTERFACE[2]					
PWDN Threshold			1.0		V
Logic 0 Level				0.4	V
Logic 1 Level		1.4			V
PWDN Response Time	Device enabled, IF output to 90% of its final level		160		ns
	Device disabled, supply current < 5 mA		220		ns
PWDN Input Bias Current	Device enabled		0.0		µA
	Device disabled		70		µA

[1] Apply the supply voltage from the external circuit through the choke inductors.
[2] PWDN function is intended for use with $V_S \leq 3.6$ V only.

5 V PERFORMANCE

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, R9 = 1.7 kΩ, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Loss	Including 1:1 IF port transformer and printed circuit board (PCB) loss		6.2		dB
Voltage Conversion Loss	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 50 Ω differential		1.4		dB
Single Sideband (SSB) Noise Figure			7.2		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 449.5 MHz, f_{RF2} = 451.5 MHz, f_{LO} = 543 MHz, each RF tone at 0 dBm		28		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 500 MHz, f_{RF2} = 450 MHz, f_{LO} = 543 MHz, each RF tone at −10 dBm		56		dBm
Input 1 dB Compression Point (IP1dB)[1]	Exceeding 20 dBm RF power results in damage to the device			20	dBm
LO to IF Leakage	Unfiltered IF output		−16		dBm
LO to RF Leakage			−27		dBm
RF to IF Isolation			−42		dBc
IF/2 Spurious	0 dBm input power		−57		dBc
IF/3 Spurious	0 dBm input power		−60		dBc
POWER SUPPLY					
Positive Supply Voltage		4.5	5	5.5	V
Total Quiescent Current	V_S = 5 V		84		mA

[1] Exceeding 20 dBm RF power results in damage to the device.

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 55 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, R9 = 226 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Loss	Including 1:1 IF port transformer and PCB loss		6.5		dB
SSB Noise Figure			7.4		dB
IIP3	f_{RF1} = 449.5 MHz, f_{RF2} = 451.5 MHz, f_{LO} = 543 MHz, each RF tone at −10 dBm		24		dBm
IIP2	f_{RF1} = 500 MHz, f_{RF2} = 450 MHz, f_{LO} = 543 MHz, each RF tone at −10 dBm		53		dBm
POWER INTERFACE					
Supply Voltage		3.0	3.3	3.6	V
Quiescent Current	Resistor programmable		55		mA
Power-Down Current	Device disabled		150		µA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_S	5.5 V
RF Input Level	20 dBm
LO Input Level	13 dBm
IFOP, IFON Bias Voltage	6.0 V
VGS0, VGS1, LOSW, PWDN	5.5 V
Internal Power Dissipation	0.6 W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is the junction to ambient thermal resistance (°C/W), θ_{JB} is the junction to board thermal resistance (°C/W), and θ_{JC} is the junction to case thermal resistance (°C/W). θ_{JC} is determined by the mechanical design of the ADL5369 and is optimized to the lowest possible value. θ_{JA} and θ_{JB} are functions of the design of the PCB, and are under the control of the user. The data shown in Table 6 is based on a JEDEC standard design and is provided for comparison purposes.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JB}[1]	θ_{JC}[1]	Unit
20-Lead LFCSP	25	14.74	1.08	°C/W

[1] See JEDEC Standard JESD51-2 for information on optimizing thermal impedance (PCB with 3 × 3 vias).

Junction to Board Thermal Impedance

The junction to board thermal impedance (θ_{JB}) is the thermal impedance from the die to or near the component lead of the ADL5369. For the ADL5369, θ_{JB} was determined experimentally to be 14.74°C/W with the device mounted on a 4-layer circuit board (two of the layers being ground planes) in a configuration similar to that of the ADL5369-EVALZ evaluation board. Board size and complexity (number of layers) affect θ_{JB}; more layers tend to reduce the thermal impedance slightly.

If the board temperature is known, use the junction to board thermal impedance to calculate die temperature (also known as junction temperature) to ensure that it does not exceed the specified limit of 150°C. For example, if the board temperature is 85°C, the die temperature is given by the equation

$$T_J = T_B + (P_{DISS} \times \theta_{JB})$$

where:
T_J is the junction temperature.
T_B is the board temperature measured at or near the component lead.
P_{DISS} is the power dissipated from the device.

The typical worst case power dissipation for the ADL5369 is 522 mW (5.5 V × 95 mA). Therefore, T_J is

$$T_J = 85°C + (0.522\ W \times 14.74°C/W) = 92.70°C$$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

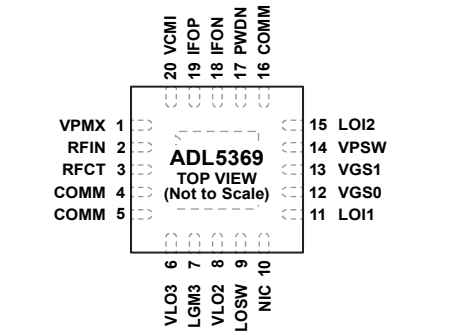


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPMX	Positive Supply Voltage for the IF Amplifier.
2	RFIN	RF Input. This pin must be ac-coupled.
3	RFCT	RF Balun Center Tap (AC Ground).
4, 5, 16	COMM	Device Common (DC Ground).
6, 8	VLO3, VLO2	Positive Supply Voltages for LO Amplifier.
7	LGM3	LO Amplifier Bias Control.
9	LOSW	LO Switch. LOI1 is selected for 0 V, or LOI2 is selected for 3 V.
10	NIC	Not Internally Connected.
11, 15	LOI1, LOI2	LO Inputs. These pins must be ac-coupled.
12, 13	VGS0, VGS1	Mixer Gate Bias Controls (3 V Logic). Ground these pins for the nominal setting.
14	VPSW	Positive Supply Voltage for LO Switch.
17	PWDN	Power-Down. Connect this pin to ground for normal operation or connect this pin to 3.0 V for disable mode.
18, 19	IFON, IFOP	Differential IF Outputs.
20	VCMI	No Connect. This pin can be grounded.
	EPAD (EP)	Exposed Pad. The exposed pad must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

5 V PERFORMANCE CHARACTERISTICS

RF Frequency

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

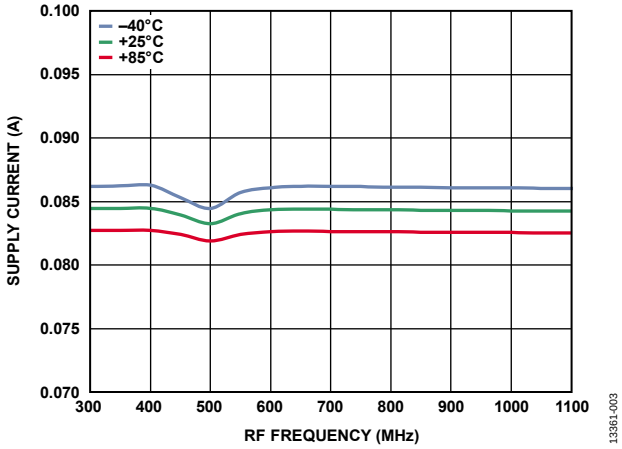


Figure 3. Supply Current vs. RF Frequency

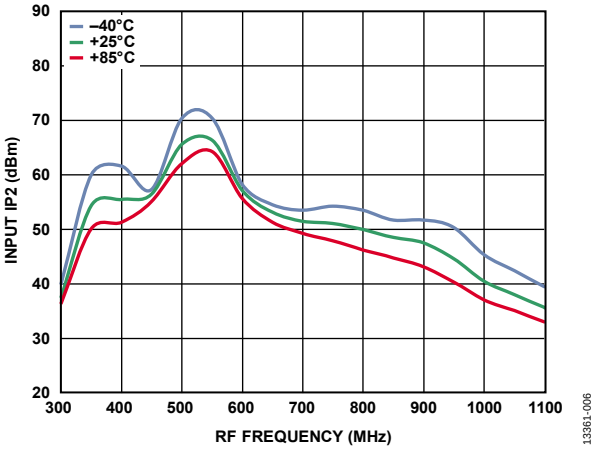


Figure 6. Input IP2 vs. RF Frequency

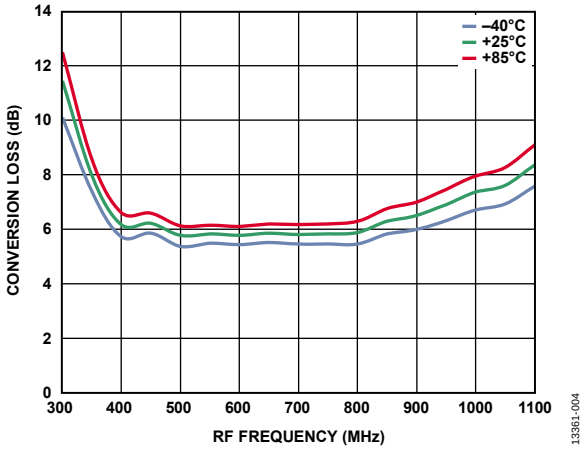


Figure 4. Power Conversion Loss vs. RF Frequency

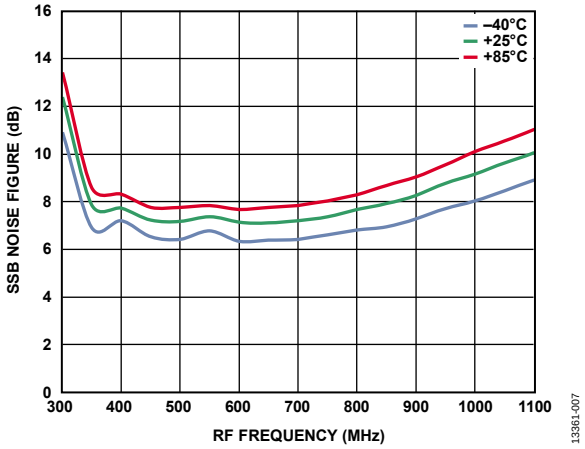


Figure 7. SSB Noise Figure vs. RF Frequency

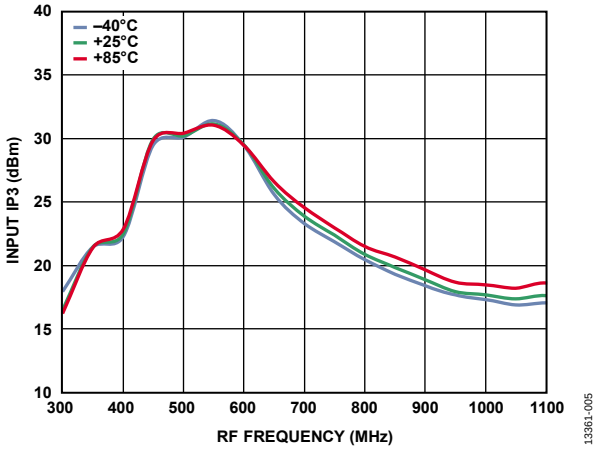


Figure 5. Input IP3 vs. RF Frequency

Temperature

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

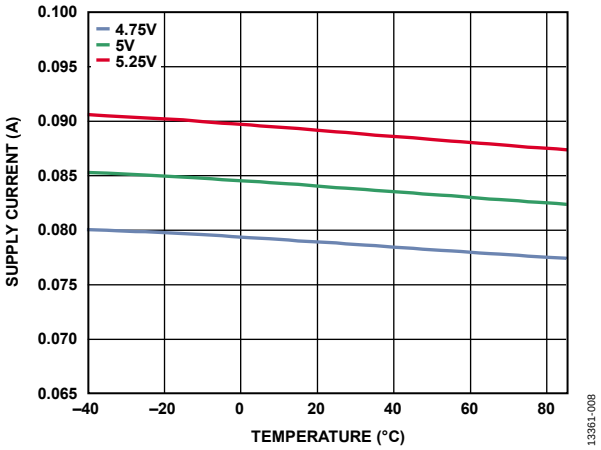


Figure 8. Supply Current vs. Temperature

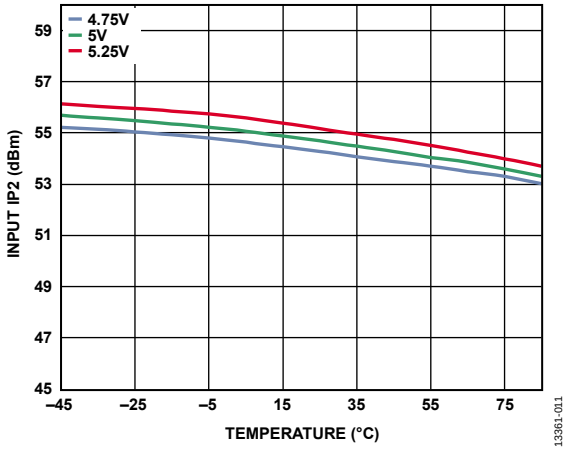


Figure 11. Input IP2 vs. Temperature

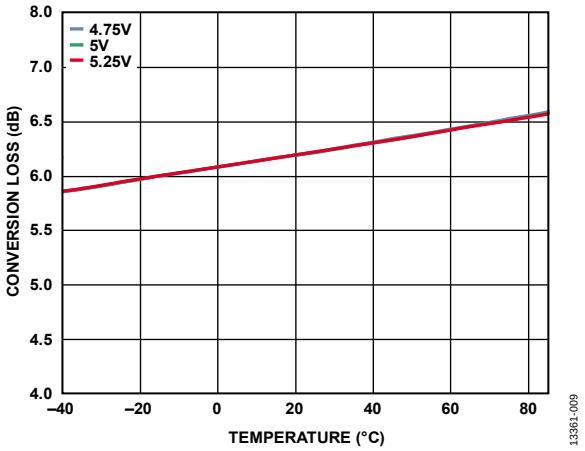


Figure 9. Power Conversion Loss vs. Temperature

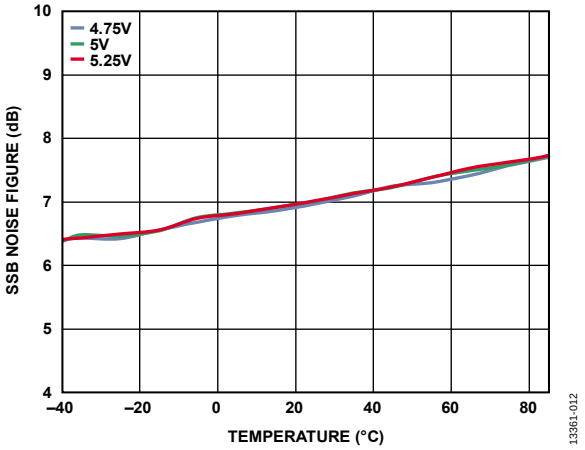


Figure 12. SSB Noise Figure vs. Temperature

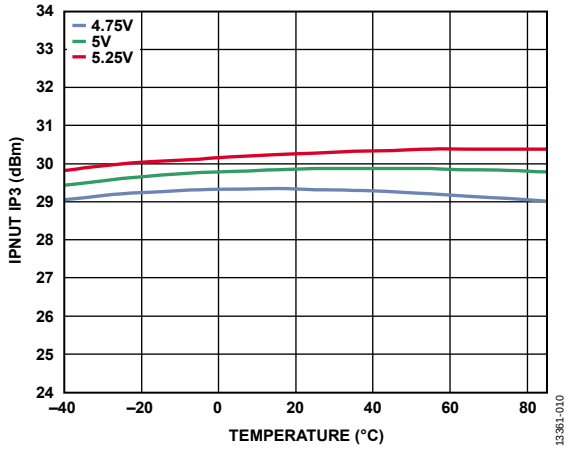


Figure 10. Input IP3 vs. Temperature

IF Frequency

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

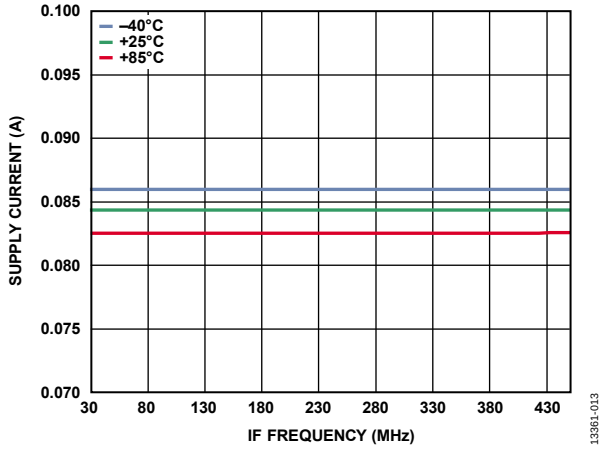


Figure 13. Supply Current vs. IF Frequency

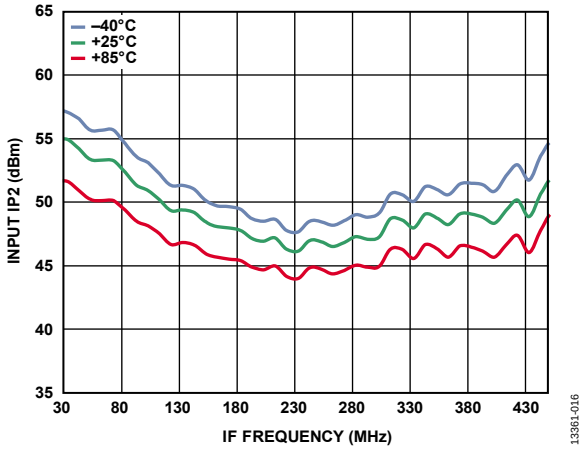


Figure 16. Input IP2 vs. IF Frequency

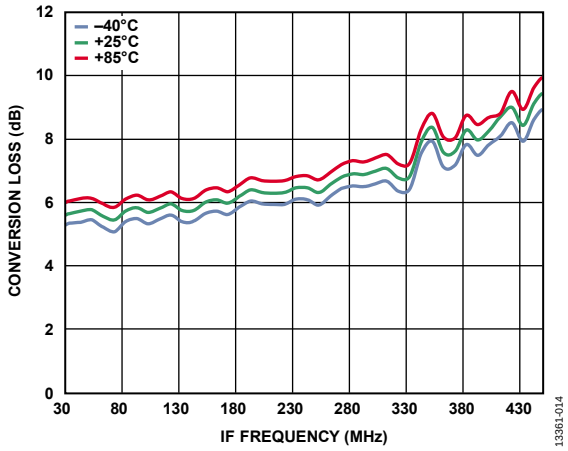


Figure 14. Power Conversion Loss vs. IF Frequency

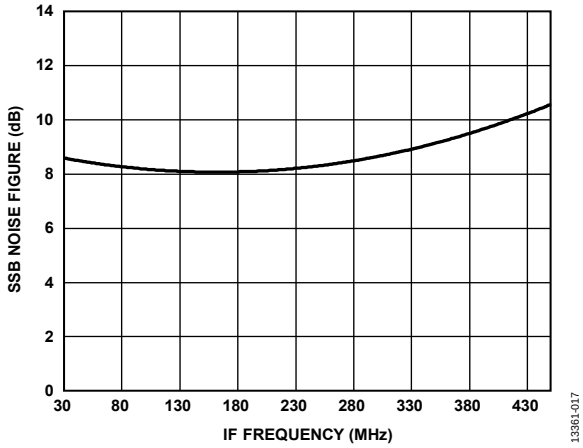


Figure 17. SSB Noise Figure vs. IF Frequency

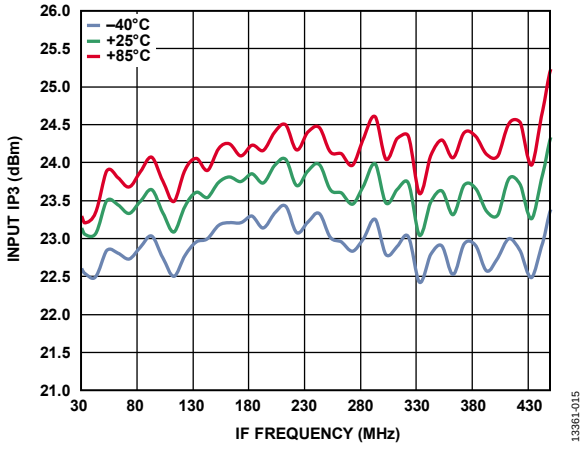


Figure 15. Input IP3 vs. IF Frequency

LO Power and Spurious Performance

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

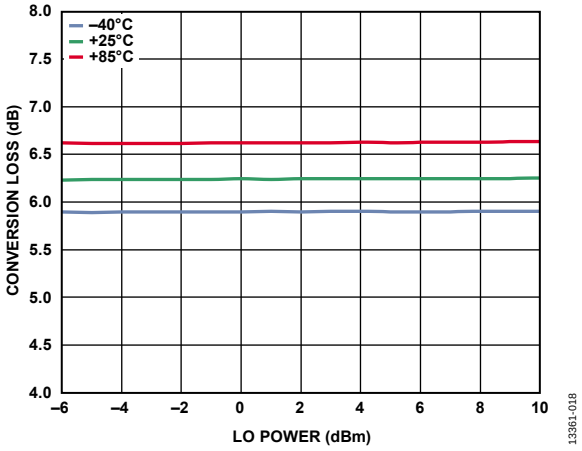


Figure 18. Power Conversion Loss vs. LO Power

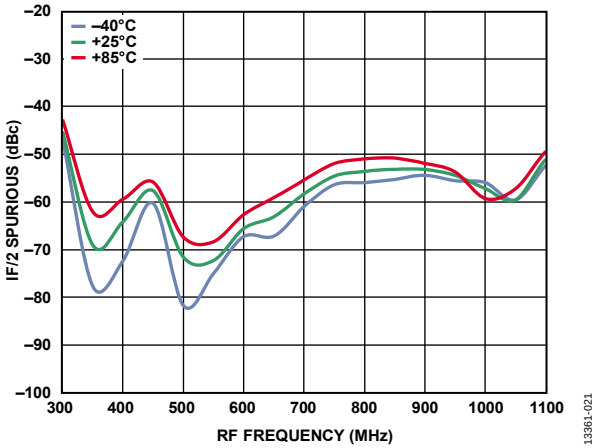


Figure 21. IF/2 Spurious vs. RF Frequency

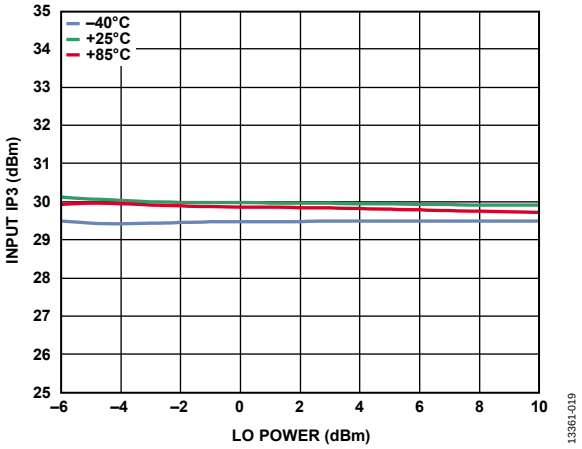


Figure 19. Input IP3 vs. LO Power

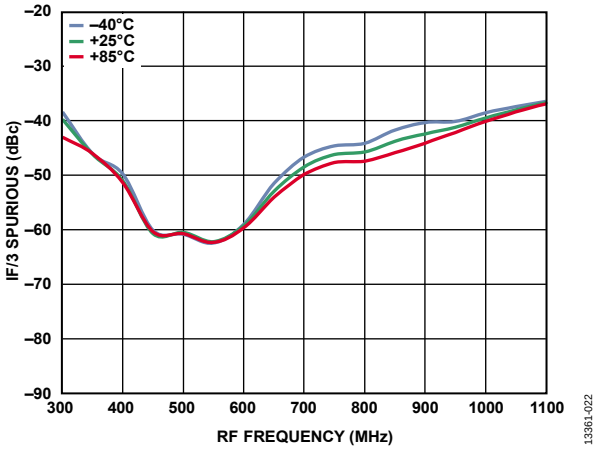


Figure 22. IF/3 Spurious vs. RF Frequency

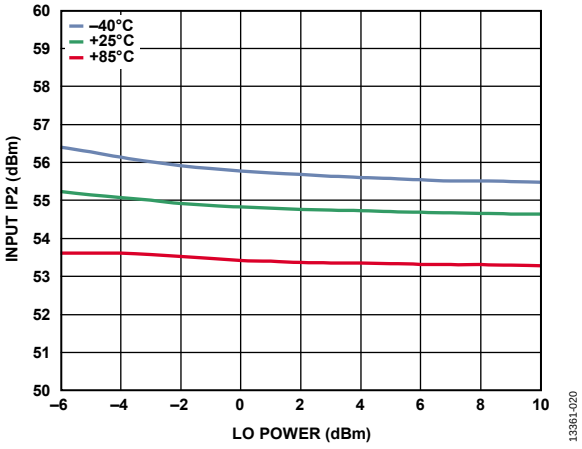


Figure 20. Input IP2 vs. LO Power

Conversion Loss Distribution, Input IP3 Distribution, and Return Loss

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

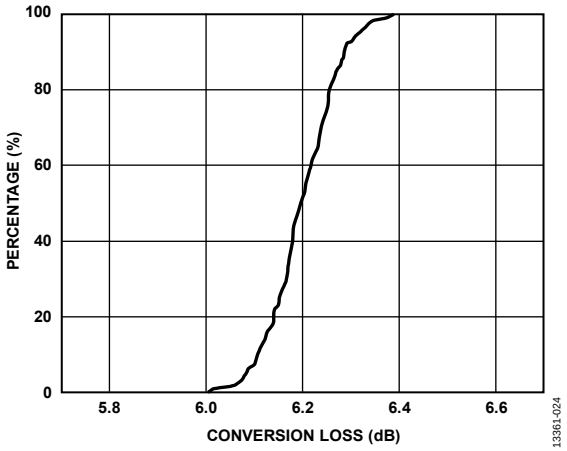


Figure 23. Conversion Loss Distribution

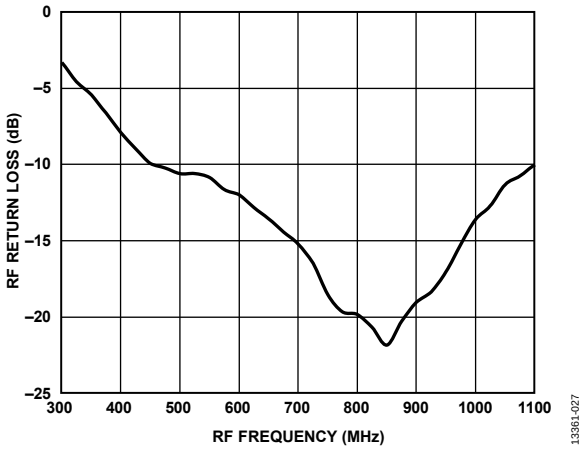


Figure 26. RF Port Return Loss, Fixed IF vs. Frequency

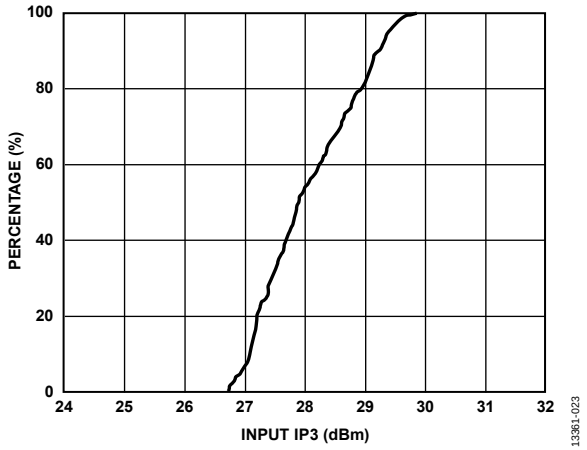


Figure 24. Input IP3 Distribution

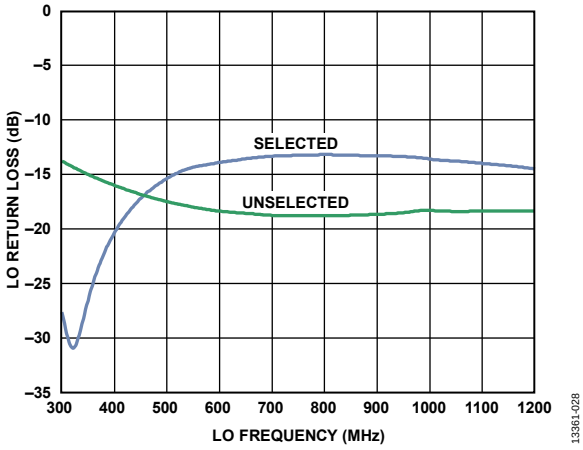


Figure 27. LO Return Loss vs. LO Frequency, Selected and Unselected

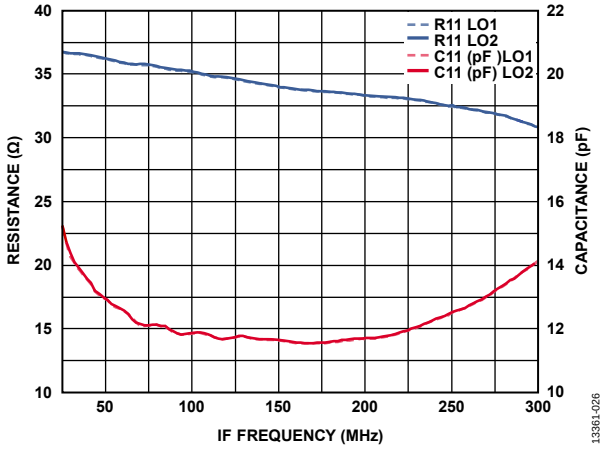


Figure 25. IF Port Return Loss

Isolation, Leakage, Power Conversion Loss, Input IP3, and SSB Noise Figure

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

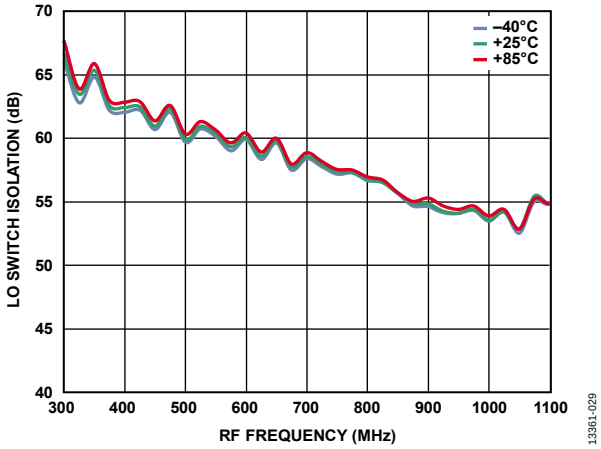


Figure 28. LO Switch Isolation vs. RF Frequency

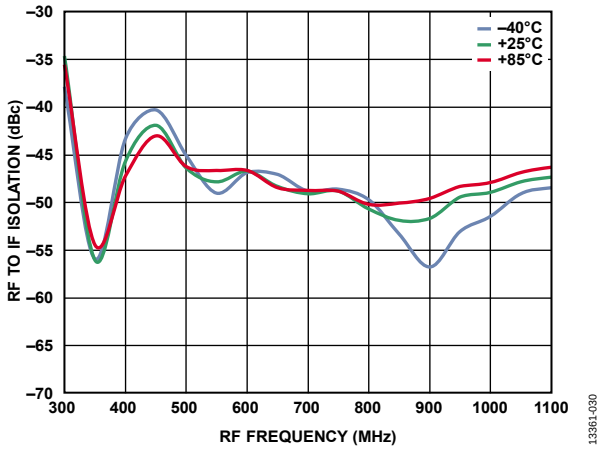


Figure 29. RF to IF Isolation vs. RF Frequency

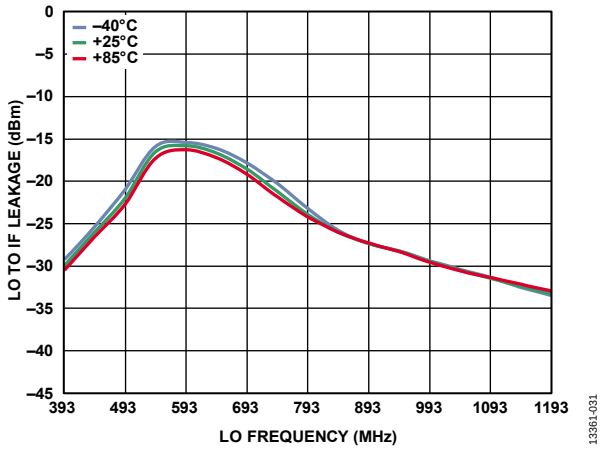


Figure 30. LO to IF Leakage vs. LO Frequency

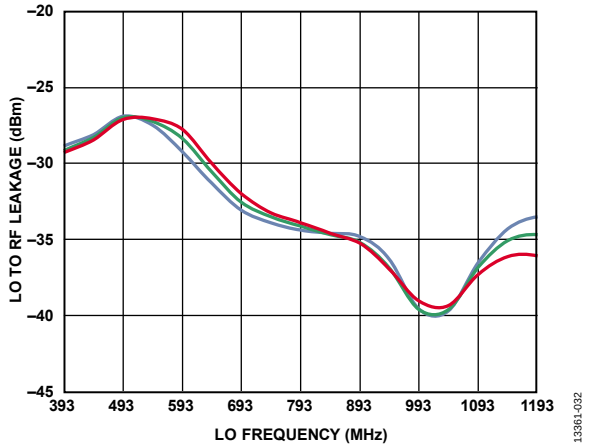


Figure 31. LO to RF Leakage vs. LO Frequency

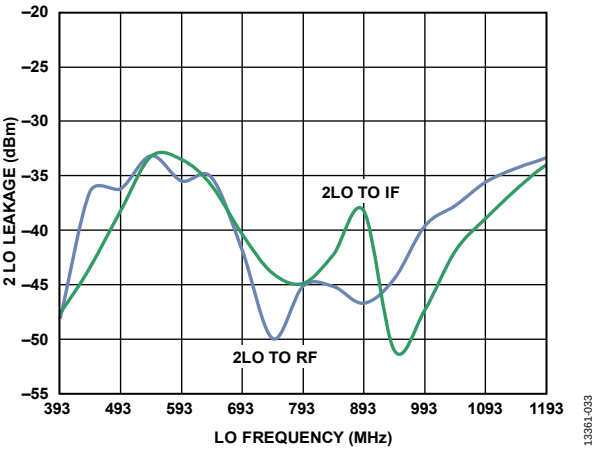


Figure 32. 2LO Leakage vs. LO Frequency

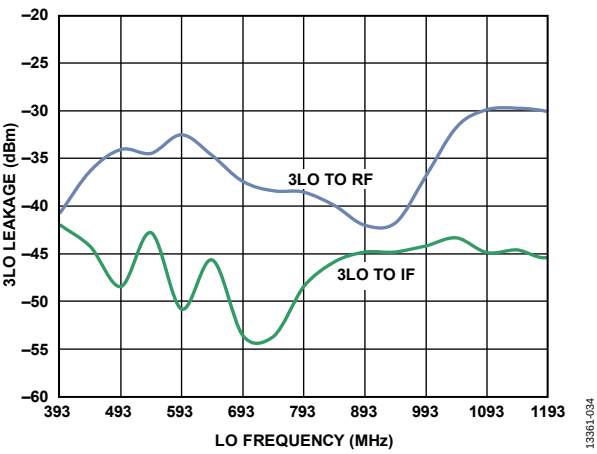


Figure 33. 3LO Leakage vs. LO Frequency

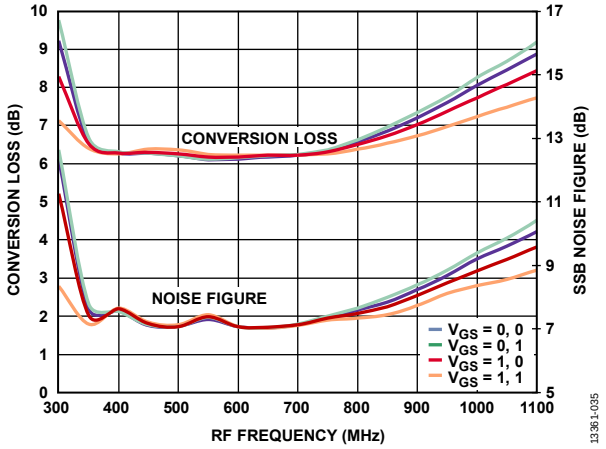


Figure 34. Power Conversion Loss and SSB Noise Figure vs. RF Frequency

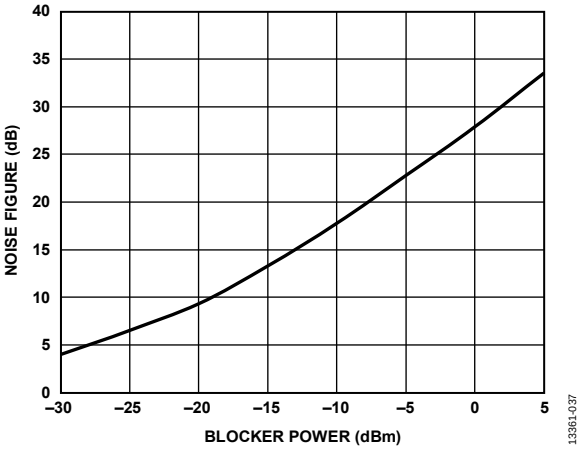


Figure 36. SSB Noise Figure vs.10 MHz Offset Blocker Level

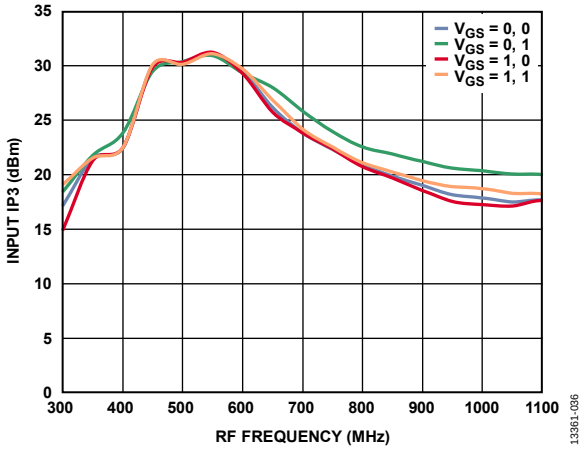


Figure 35. Input IP3 vs. RF Frequency

3.3 V PERFORMANCE CHARACTERISTICS

V_S = 3.3 V, I_S = 56 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, R9 = 226 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

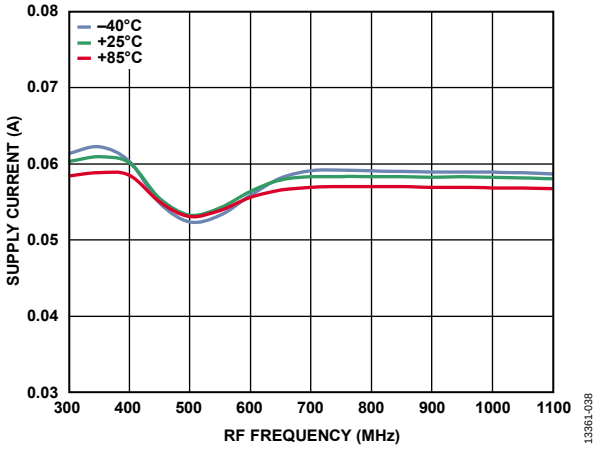


Figure 37. Supply Current vs. RF Frequency

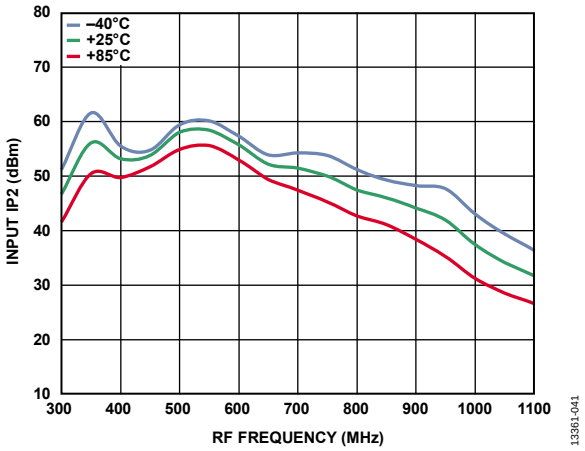


Figure 40. Input IP2 vs. RF Frequency

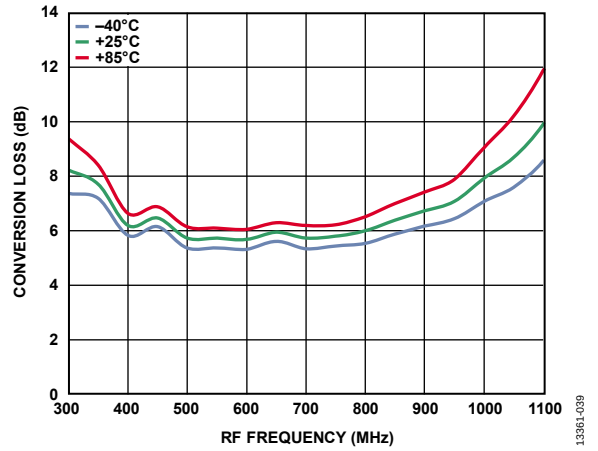


Figure 38. Power Conversion Loss vs. RF Frequency

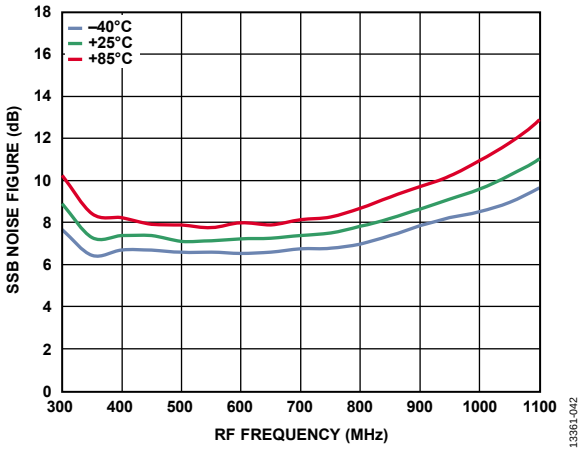


Figure 41. SSB Noise Figure vs. RF Frequency

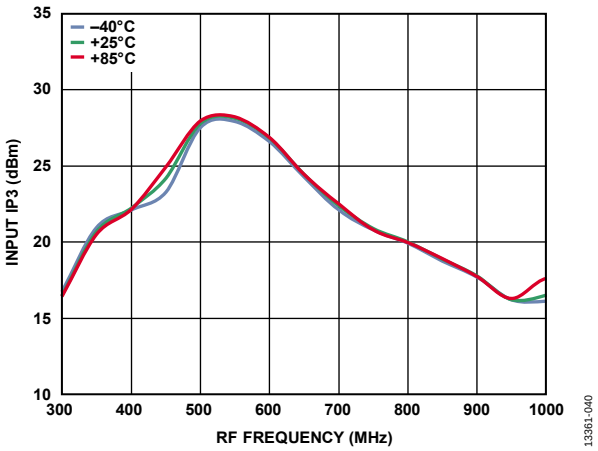


Figure 39. Input IP3 vs. RF Frequency

UPCONVERSION CHARACTERISTICS

T_A = 25°C, f_{IF} = 93 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

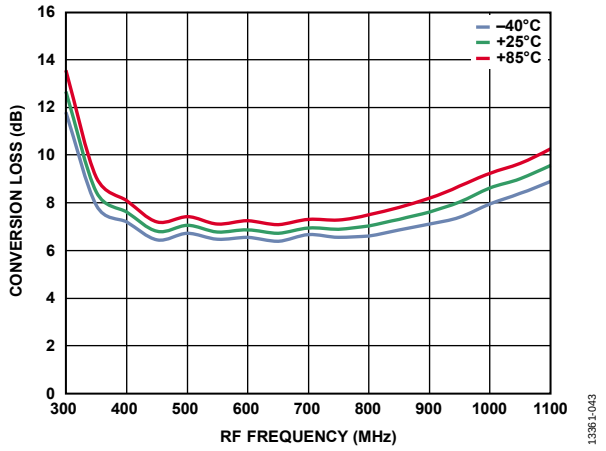


Figure 42. Power Conversion Loss vs. RF Frequency, V_S = 5 V, Upconversion

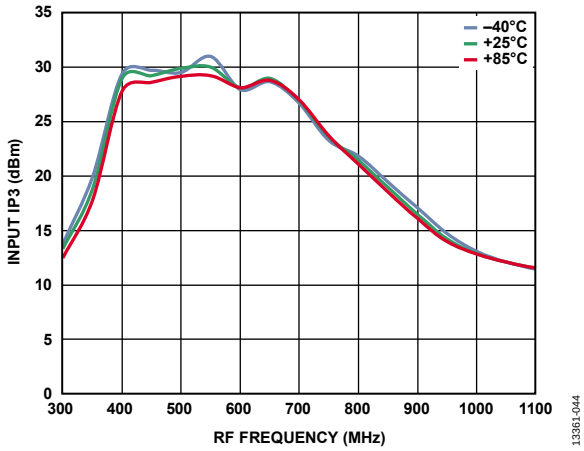


Figure 43. Input IP3 vs. RF Frequency, V_S = 5 V, Upconversion

SPURIOUS PERFORMANCE

All spur tables are (N × f_{RF}) − (M × f_{LO}) and were measured using the standard evaluation board. Mixer spurious products are measured in dBc from the IF output power level. Data was measured only for frequencies less than 6 GHz. Typical noise floor of the measurement system = −100 dBm.

5 V Performance

V_S = 5 V, I_S = 84 mA, T_A = 25°C, f_{RF} = 450 MHz, f_{LO} = 543 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, R9 = 1.7 kΩ, and Z_O = 50 Ω, unless otherwise noted.

		M											
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
N	**0**		−16.885	−33.42	−42.57	−38.358	−49.375	−61.446	−49.819	−51.873	−60.951	−52.666	−60.115	−61.09
	1	−41.537	0	−45.535	−17.948	−54.779	−32.507	−47.242	−42.403	−45.589	−45.324	−67.094	−47.641	−61.494
	2	−71.919	−50.753	−58.999	−60.289	−72.545	−70.273	−58.881	−73.383	−65.824	−78.819	−68.754	−97.834	−72.556
	3	−95.982	−72.895	−79.147	−64.17	−90.573	−70.476	−92.162	−81.353	−87.574	−89.786	−82.829	−93.849	−86.249
	4	<−100	−78.49	−93.128	−81.092	−99.503	−87.794	<−100	−99.13	−98.082	<−100	<−100	<−100	<−100
	5	<−100	<−100	<−100	<−100	−95.9	−90.504	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	6	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	7		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	8			<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	9			<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	10				<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	11					<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12					<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100

CIRCUIT DESCRIPTION

The ADL5369 consists of two primary components: the RF subsystem and the-LO subsystem. The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

The RF subsystem consists of an integrated, low loss RF balun, passive metal-oxide semiconductor field-effect transistor (MOSFET) mixer, sum termination network, and IF amplifier.

The LO subsystem consists of a single pole, double throw (SPDT)-terminated FET switch and a three-stage limiting LO amplifier. The purpose of the LO subsystem is to provide a large, fixed amplitude, balanced signal to drive the mixer independent of the level of the LO input.

A block diagram of the device is shown in Figure 44.

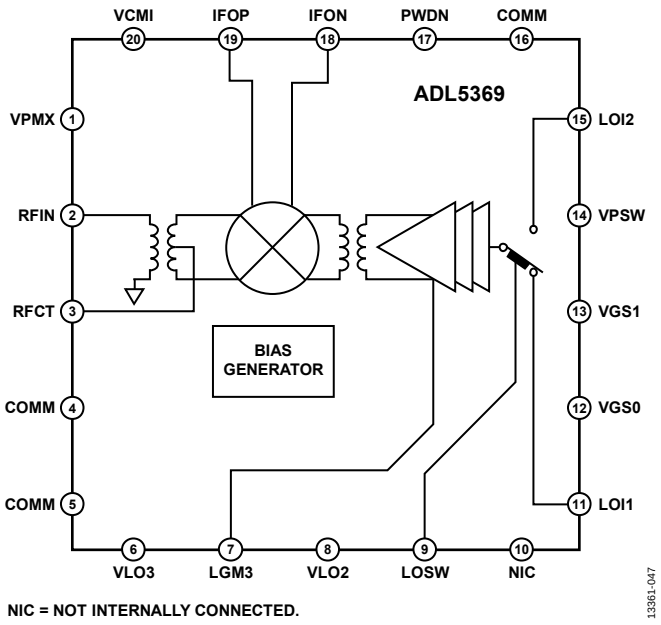


Figure 44. Simplified Schematic

RF SUBSYSTEM

The single-ended, 50 Ω RF input is internally transformed to a balanced signal using a low loss (<1 dB), unbalanced to balanced (balun) transformer. This transformer is made possible by an extremely low loss metal stack, which provides both excellent balance and dc isolation for the RF port. Although the port can be dc connected, using a blocking capacitor is recommended to avoid running excessive dc current through the device. The RF balun can easily support an RF input frequency range of 300 MHz to 1100 MHz.

The resulting balanced RF signal is applied to a passive mixer that commutates the RF input with the output of the LO subsystem. The passive mixer is essentially a balanced, low loss switch that adds minimum noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

Because the mixer is inherently broadband and bidirectional, it is necessary to properly terminate all the idler (M × N product) frequencies generated by the mixing process. Terminating the mixer avoids the generation of unwanted intermodulation products and reduces the level of unwanted signals at the IF output. This termination is accomplished by the addition of a sum network between the IF output and the mixer.

Additionally, dc current can be saved by reducing the dc supply voltage to as low as 3.3 V, further reducing the dissipated power of the device. Note that no performance enhancement is obtained by reducing the value of the resistors; reducing the value of the resistors may result in excessive dc power dissipation.

LO SUBSYSTEM

The LO amplifier provides a large signal level to the mixer to obtain optimum intermodulation performance. The resulting amplifier provides extremely high performance centered on an operating frequency of 700 MHz. The best operation is achieved with high-side LO injection for RF signals in the 300 MHz to 1100 MHz range. Operation outside these ranges is permissible, and conversion loss is extremely wideband, easily spanning 300 MHz to 1100 MHz, but intermodulation is optimal over the aforementioned ranges.

The ADL5369 has two LO inputs permitting multiple synthesizers to be rapidly switched with extremely short switching times (<40 ns) for frequency agile applications. The two inputs are applied to a high isolation SPDT switch that provides a constant input impedance, regardless of whether the port is selected, to avoid pulling the LO sources. This multiple section switch also ensures high isolation to the off input, minimizing any leakage from the unwanted LO input that may result in undesired IF responses.

The single-ended LO input is converted to a fixed amplitude differential signal using a multistage, limiting LO amplifier. This results in consistent performance over a range of LO input power. Optimum performance is achieved from −6 dBm to +10 dBm, but the circuit continues to function at considerably lower levels of LO input power.

The performance of this amplifier is critical in achieving a high intercept passive mixer without degrading the noise floor of the system. This is a critical requirement in an interferer rich environment, such as cellular infrastructure, where blocking interferers can limit mixer performance. The bandwidth of the intermodulation performance is somewhat influenced by the current in the LO amplifier chain. For dc current sensitive applications, it is permissible to reduce the current in the LO amplifier by raising the value of the external bias control resistor. For dc current critical applications, the LO chain can operate with a supply voltage as low as 3.3 V, resulting in substantial dc power savings.

In addition, when operating with supply voltages below 3.6 V, the ADL5369 has a power-down mode that permits the dc current to drop to <200 μA.

All of the logic inputs work with any logic family that provides a Logic 0 input level of less than 0.4 V and a Logic 1 input level that exceeds 1.4 V. All logic inputs are high impedance up to Logic 1 levels of 3.3 V. At levels exceeding 3.3 V, protection circuitry permits operation up to 5.5 V, although a small bias current is drawn.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5369 mixer is designed to upconvert or downconvert between radio frequencies (RF) from 300 MHz to 1100 MHz and intermediate frequencies (IF) from 30 MHz to 450 MHz. Figure 45 depicts the basic connections of the mixer. It is recommended to ac-couple the RF and LO input ports to prevent non-zero dc voltages from damaging the RF balun or LO input circuit. The RFIN capacitor value of 8 pF is recommended to provide the optimized RF input return loss for the desired frequency band.

For upconversion, drive the IF inputs, Pin 18 (IFON) and Pin 19 (IFOP), differentially or use a 1:1 ratio transformer for single-ended operation. An 8 pF capacitor is recommended for the RF output, Pin 2 (RFIN).

IF PORT

The real part of the output impedance is approximately 50 Ω, as seen in Figure 25, which matches many commonly used SAW filters without the need for a transformer. This results in a voltage conversion loss that is approximately the same as the power conversion loss, as shown in Table 3.

MIXER VGS CONTROL DAC

The ADL5369 features two logic control pins, Pin 12 (VGS0) and Pin 13 (VGS1), that allow programmability for internal gate to source voltages for optimizing mixer performance over desired frequency bands. The evaluation board defaults both VGS0 and VGS1 to ground. Power conversion loss, NF, and IIP3 can be optimized, as shown in Figure 34 and Figure 35.

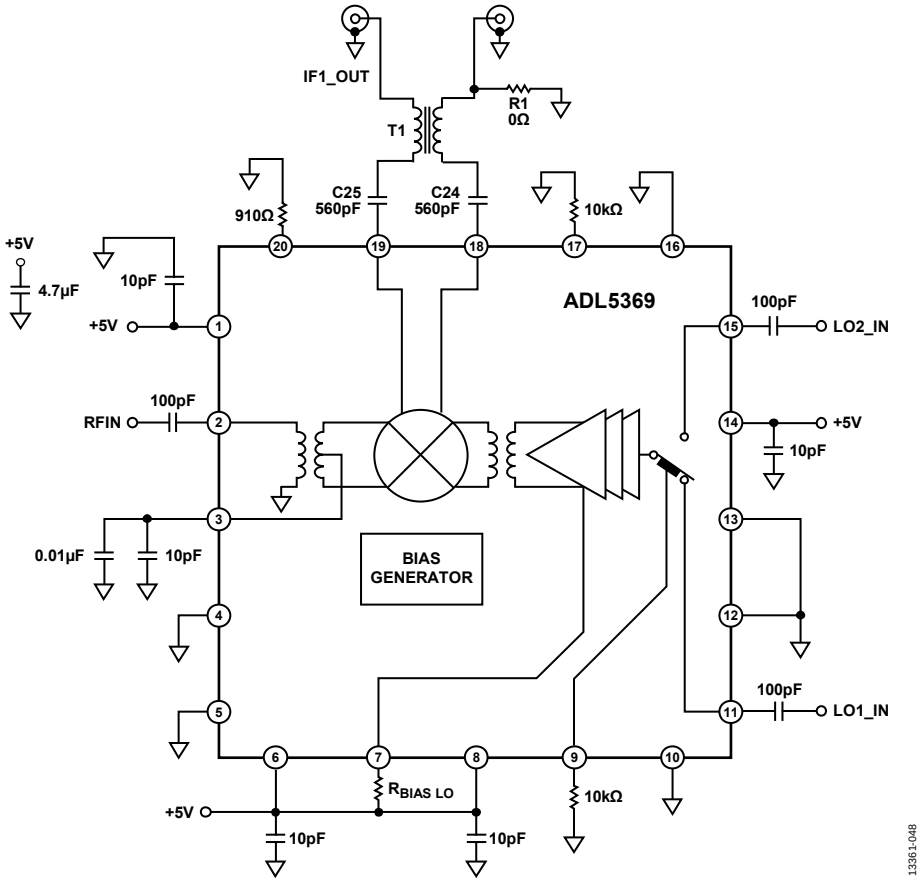


Figure 45. Typical Application Circuit

EVALUATION BOARD

An evaluation board is available for the family of double balanced mixers. The standard evaluation board schematic is shown in Figure 46. The evaluation board is fabricated using Rogers® RO3003 material.

Table 8 describes the various configuration options of the evaluation board. Evaluation board layout is shown in Figure 47 to Figure 50.

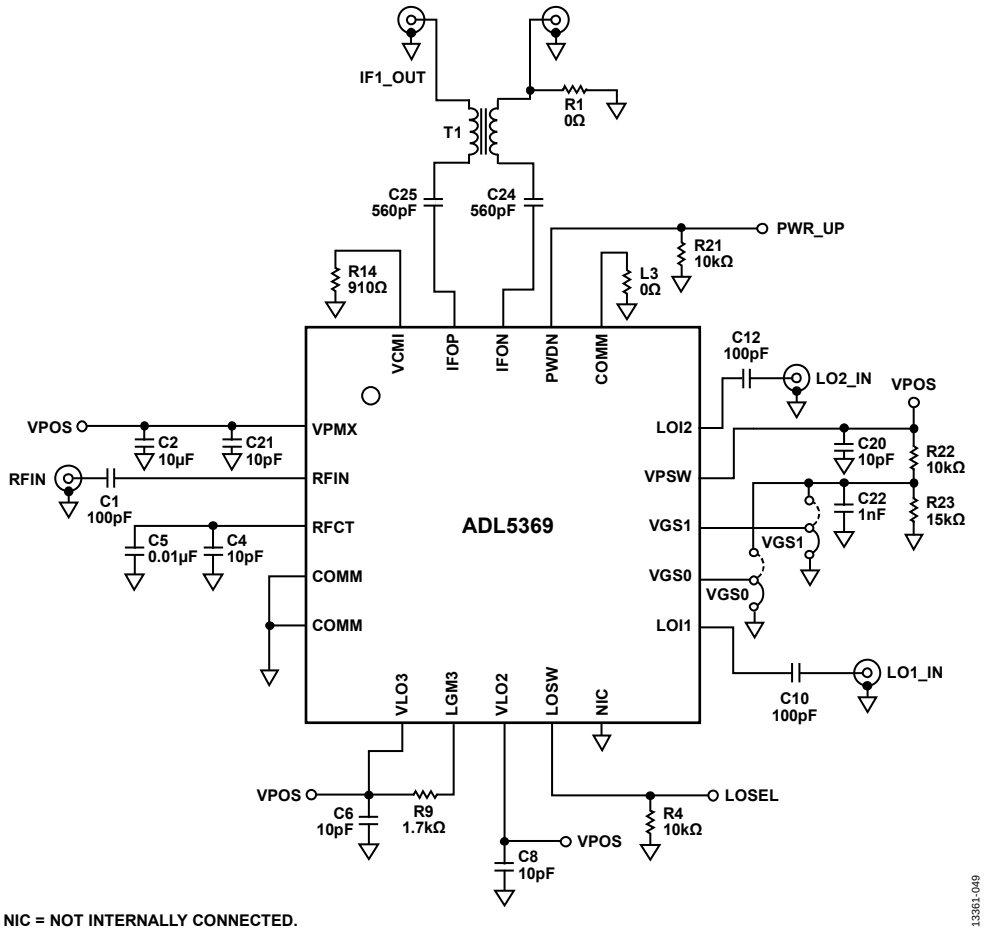


Figure 46. Evaluation Board Schematic

Table 8. Evaluation Board Configuration

Components	Description	Default Conditions
C2, C6, C8, C20, C21	Power supply decoupling. Nominal supply decoupling consists of a 10 µF capacitor to ground in parallel with a 10 pF capacitor to ground positioned as close to the device as possible.	C2 = 10 µF (Size 0603), C6, C8, C20, C21 = 10 pF (Size 0402)
C1, C4, C5	RF input interface. The input channels are ac-coupled through C1. C4 and C5 provide bypassing for the center taps of the RF input baluns.	C1 = 100 pF (Size 0402), C4 = 10 pF (Size 0402), C5 = 0.01 µF (Size 0402)
T1, R1, C24, C25	IF output interface. T1 is a 1:1 impedance transformer used to provide a single-ended IF output interface. Remove R1 for balanced output operation. C24 and C25 are used to block the dc bias at the IF ports.	T1 = TC1-1-13M+ (Mini-Circuits), R1 = 0 Ω (Size 0402), C24, C25 = 560 pF (Size 0402)
C10, C12, R4	LO interface. C10 and C12 provide ac coupling for the LO1_IN and LO2_IN local oscillator inputs. LOSEL selects the appropriate LO input for both mixer cores. R4 provides a pull-down to ensure that LO1_IN is enabled when the LOSEL test point is logic low. LO2_IN is enabled when LOSEL is pulled to logic high.	C10, C12 = 100 pF (Size 0402), R4 = 10 kΩ (Size 0402)
R21	PWDN interface. R21 pulls the PWDN logic low and enables the device. The PWR_UP test point allows the PWDN interface to be exercised using the an external logic generator. Grounding the PWDN pin for nominal operation is allowed. Using the PWDN pin when supply voltages exceed 3.3 V is not allowed.	R21 = 10 kΩ (Size 0402)
C22, L3, R9, R14, R22, R23, VGS0, VGS1	Bias control. R22 and R23 form a voltage divider to provide 3 V for logic control, bypassed to ground through C22. VGS0 and VGS1 jumpers provide programmability at the VGS0 and VGS1 pins. It is recommended to pull these two pins to ground for nominal operation. R9 sets the bias point for the internal LO buffers.	C22 = 1 nF (Size 0402), L3 = 0 Ω (Size 0603), R9 = 1.7 kΩ (Size 0402), R14 = 910 Ω (Size 0402), R22 = 10 kΩ (Size 0402), R23 = 15 kΩ (Size 0402), VGS0 = VGS1 = 3-pin shunt

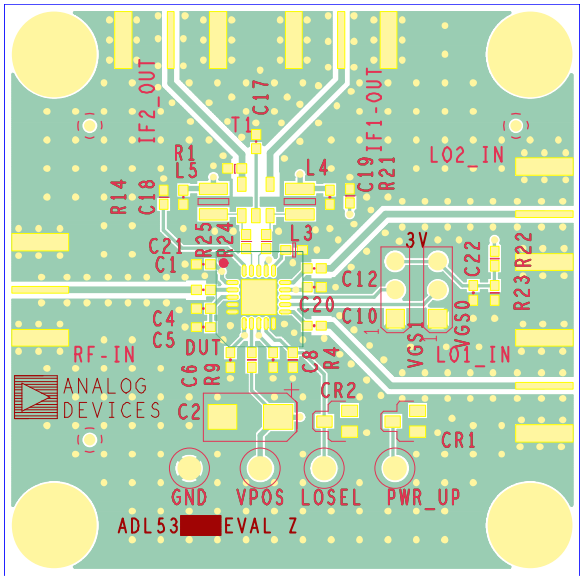


Figure 47. Evaluation Board Top Layer

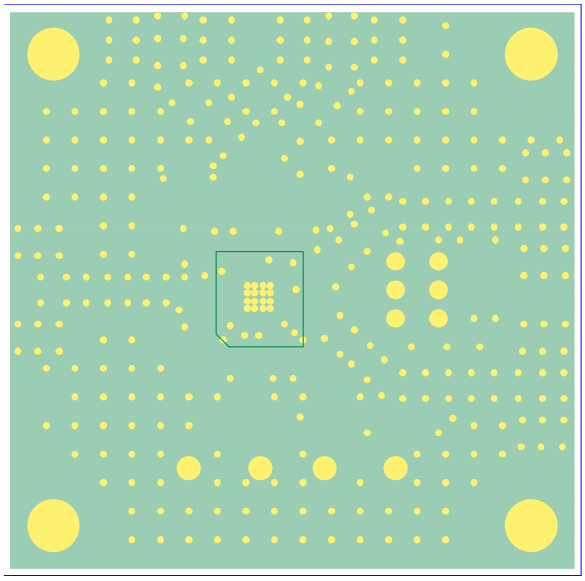


Figure 48. Evaluation Board Ground Plane, Internal Layer 1

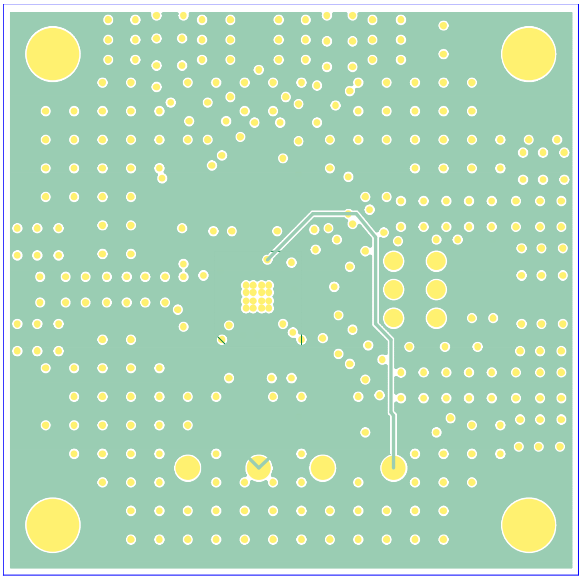


Figure 49. Evaluation Board Power Plane, Internal Layer 2

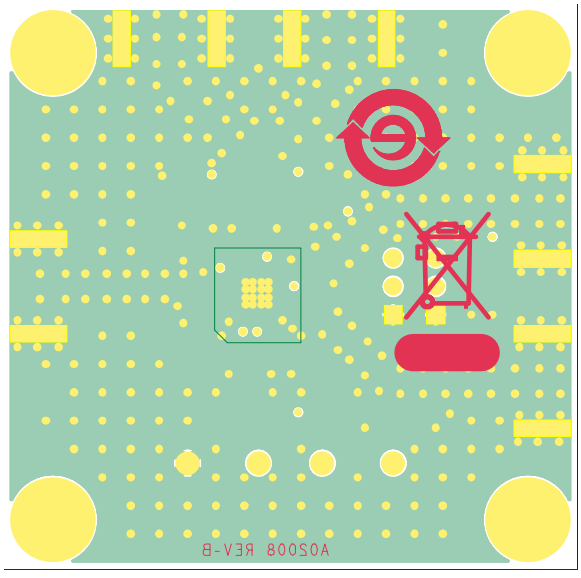


Figure 50. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

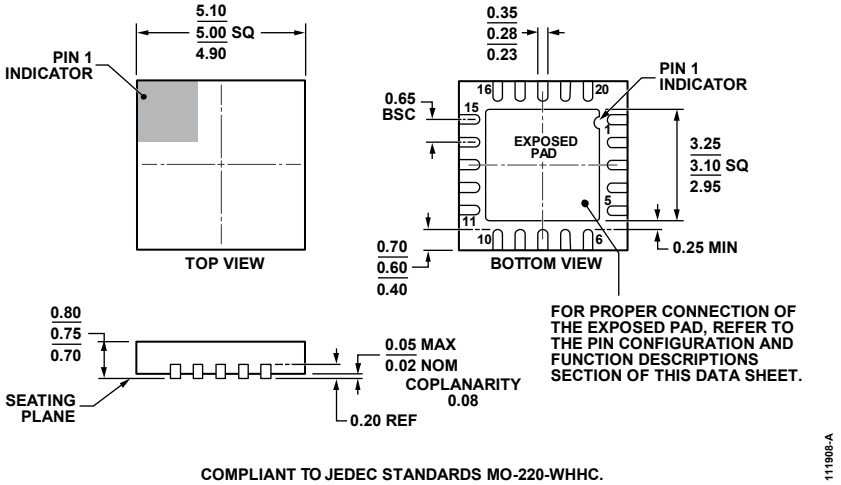


Figure 51. 20-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-20-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5369ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP], 7″ Tape and Reel	CP-20-9	1,500
ADL5369-EVALZ		Evaluation Board		1

[1] Z = RoHS Compliant Part.

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D13361-0-5/16(A)