Precision Wide Range (3 nA to 3 mA) High-Side Current Mirror

Data Sheet **ADL5315**

FEATURES

- Accurately mirrors input current (1:1 ratio) over 6 decades
  - Linearity 1% from 3 nA to 3 mA
- Stable mirror input voltage
  - Voltage held 1 V below supply using internal reference or can be set externally
- Adjustable input current limit
- 2.7 V to 8 V single-supply operation
- Miniature 8-lead LFCSP (2 mm × 3 mm)

APPLICATIONS

- Optical power monitoring from a single photodiode
- General voltage biasing with precision current monitoring
- Voltage-to-current conversion

FUNCTIONAL BLOCK DIAGRAM

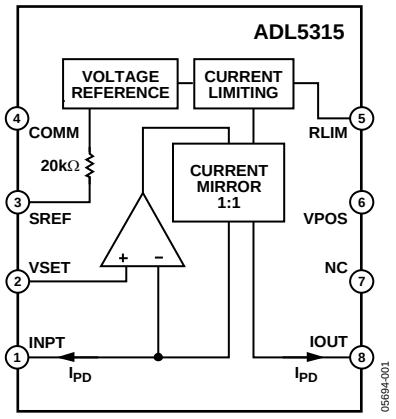


Figure 1.

GENERAL DESCRIPTION

The ADL5315 is a wide input current range, precision high-side current mirror featuring a stable and user-adjustable input voltage. It is optimized for use with PIN photodiodes, but its flexibility and wide operating range make it suitable for a broad array of additional applications. Over the 3 nA to 3 mA range, the current sourced from the INPT pin is accurately mirrored with a 1:1 ratio and sourced from the IOUT output pin. In a typical photodiode application, the output drives a current-input logarithmic amplifier to produce a linear-in-dB output representing the optical power incident upon the photodiode. For linear voltage output, a single resistor to ground is all that is required. The photodiode anode can be connected to a high speed transimpedance amplifier for the extraction of the data stream. The voltage at the INPT pin is temperature stable with respect to the voltage at the VSET input pin, which it tracks. A temperature stable reference voltage is provided at the SREF pin, which, when tied to VSET, fixes the voltage at INPT 1.0 V below VPOS. VSET can also be driven from an external source.

The VSET input has very low input current and can be driven as low as the bottom rail, facilitating nonloading voltage-to-current conversion as well as minimizing dark current in photodiode applications.

The ADL5315 also features adjustable input current limiting using an external resistor from RLIM to VPOS. The maximum current sourced by INPT (and IOUT) can be set between 1 mA and 16 mA, beyond which the voltage at INPT falls rapidly from its setpoint. Connecting RLIM directly to VPOS provides basic input short-circuit protection with the default current limit of 16 mA typical.

The ADL5315 is available in a 2 mm × 3 mm, 8-lead LFCSP and is specified for operation from −40°C to +85°C.

Rev. A
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REVISION HISTORY

9/2017—Rev. 0 to Rev. A

Changed CP-8-1 to CP-8-23 ... Throughout
Changes to Figure 2 ... 5
Updated Outline Dimensions ... 17
Changes to Ordering Guide ... 17

10/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{POS} = 5 V, V_{SET} = 4 V, I_{INPT} = 3 µA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
CURRENT MIRROR OUTPUT	IOUT (Pin 8)				
Current Gain from INPT to IOUT		0.99	1.00	1.01	
Current Gain from INPT to IOUT	−40°C < T_A < +85°C	0.97	1.00	1.03	A/A
Nonlinearity	3 nA < I_{PD} < 3 mA		0.25	1.00	%
Small Signal Bandwidth	I_{INPT} = 3 nA		1		kHz
	I_{INPT} = 3 µA		1		MHz
Wideband Noise at IPDM	I_{INPT} = 3 µA, C_{SET} = 2.2 nF		20		nA rms
Specified Output Voltage Range		0		V_{POS} − 1	V
$I_{OUT} \times R_{OUT}$ Product	I_{INPT} = 3 µA		900		V
MIRROR INPUT, VOLTAGE CONTROL	INPT (Pin 1), VSET (Pin 2), SREF (Pin 3)				
Specified Input Current Range, I_{INPT}	Flows from INPT pin	3n		3m	A
Specified VSET Voltage Range	2.7 V < V_{POS} < 6.5 V	0		V_{POS} − 1	V
	6.5 V < V_{POS} < 8 V	V_{POS} − 6.5		V_{POS} − 1	V
Incremental Gain from VSET to INPT	0.2 V < V_{SET} < 7.0 V	0.98	1	1.02	V/V
Incremental Input Resistance at VSET	V_{SET} = 4.0 V		>100		GΩ
Input Bias Current at VSET	V_{SET} = 4.0 V		<30		pA
SREF Voltage, Relative to V_{POS}	2.7 V < V_{POS} < 8 V	−1.04	−1.0	−0.97	V
OVERCURRENT PROTECTION					
INPT Current Limit	V_{INPT} drops to 0 V, R_{LIM} = 0 Ω		16		mA
	V_{INPT} drops to 0 V, R_{LIM} = 3 kΩ	6.4	8	9.6	mA
POWER SUPPLY	VPOS (Pin 6)				
Supply Voltage Range		2.7		8	V
Quiescent Current	I_{INPT} = 3 µA		1.8	2.2	mA
	I_{INPT} = 3 mA		8.3	10.2	mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	8 V
Input Current at INPT	20 mA
Internal Power Dissipation	500 mW
θ_{JA} (Soldered Exposed Paddle)	80°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

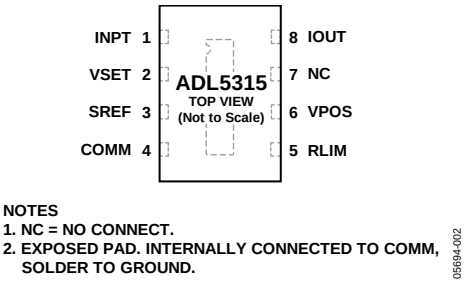


Figure 2. 8-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INPT	Input Current. Pin sources current only.
2	VSET	Sets Voltage at INPT (Gain = 1). Range 0 V to V_{POS} − 1.0 V for V_{POS} < 6.5 V. For V_{POS} ≥ 6.5 V range, V_{POS} − 6.5 V to V_{POS} − 1 V. Optional shielding of INPT trace.
3	SREF	Reference Voltage for VSET. Internally generated at V_{POS} − 1.0 V through 20 kΩ. Can be shorted to VSET for standard mirror operation.
4	COMM	Analog Ground.
5	RLIM	External Resistor to VPOS. Sets current limit at INPT from 1 mA to 16 mA. $I_{LIM} = 48\ V/(R_{LIM} + 3\ k\Omega)$.
6	VPOS	Positive Supply (2.7 V to 8.0 V).
7	N/C	Optional Shielding of IOUT Trace. No connection to die.
8	IOUT	Output Current. Mirrors current at INPT with a gain of 1.0. Sources current only.
	PADDLE	Exposed Pad. Internally connected to COMM, solder to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 5 V, V_{SET} = V_{SREF}, V_{OUT} = 0 V, T_A = 25°C, unless otherwise noted.

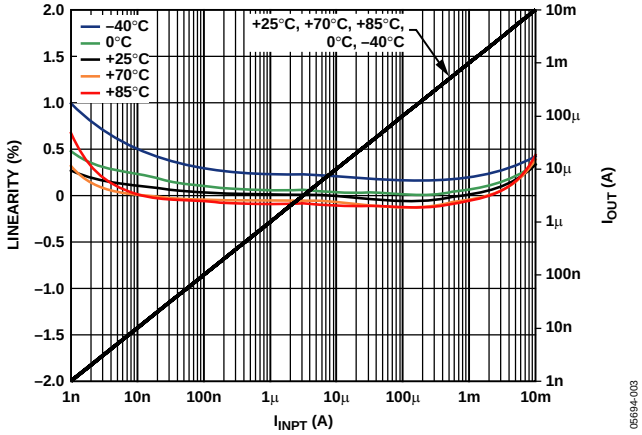


Figure 3. I_{OUT} Linearity vs. I_{INPT} for Multiple Temperatures, Normalized to 25°C and I_{INPT} = 3 µA

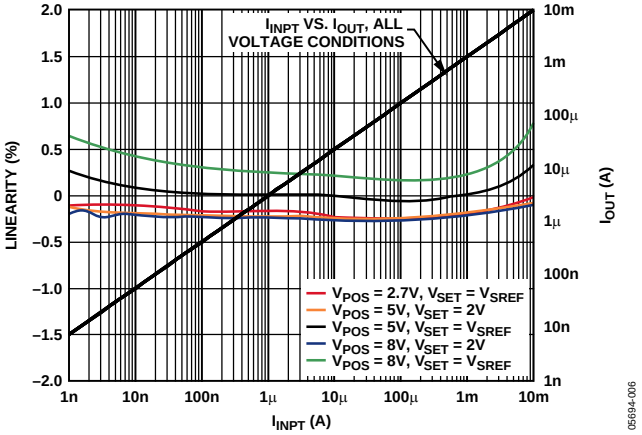


Figure 6. I_{OUT} Linearity vs. I_{INPT} for Multiple Supply Conditions, Normalized to V_{POS} = 5 V, V_{SET} = V_{SREF}, and I_{INPT} = 3 µA

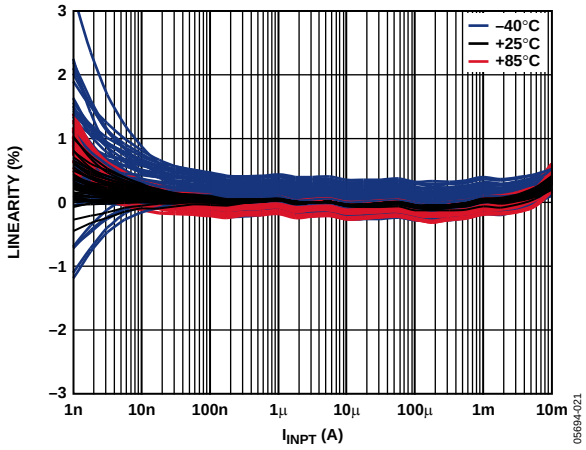


Figure 4. I_{OUT} Linearity vs. I_{INPT} for Multiple Temperatures and Devices Normalized to 25°C and I_{INPT} = 3 µA

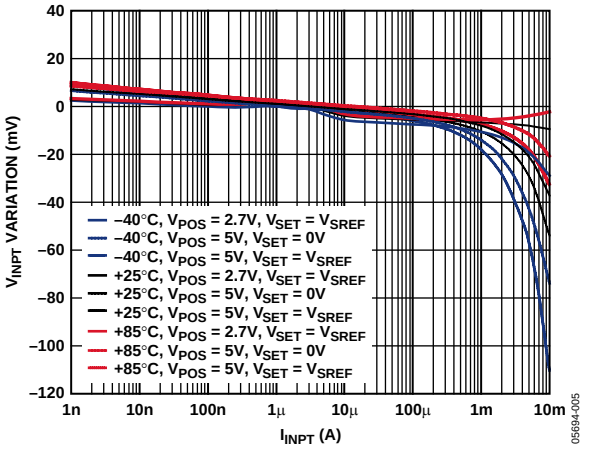


Figure 7. V_{INPT} Variation vs. I_{INPT} for Multiple Temperatures and Voltage, Normalized to V_{POS} = 5 V, V_{SET} = V_{SREF}, I_{INPT} = 3 µA and 25°C

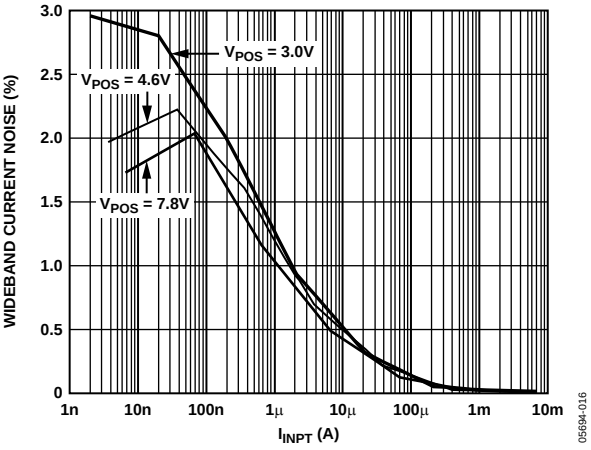


Figure 5. Output Wideband Current Noise as a Percentage of I_{OUT} vs. I_{INPT} for Multiple Values of V_{POS}, C_{SET} = 2.2 nF, BW = 10 MHz

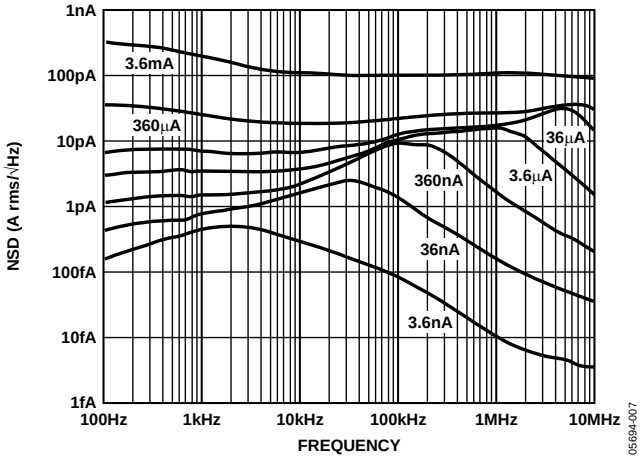


Figure 8. Output Current Noise Density vs. Frequency for Multiple Values of I_{INPT}, V_{POS} = 4.6 V, V_{SET} = V_{SREF}, C_{SET} = 2.2 nF

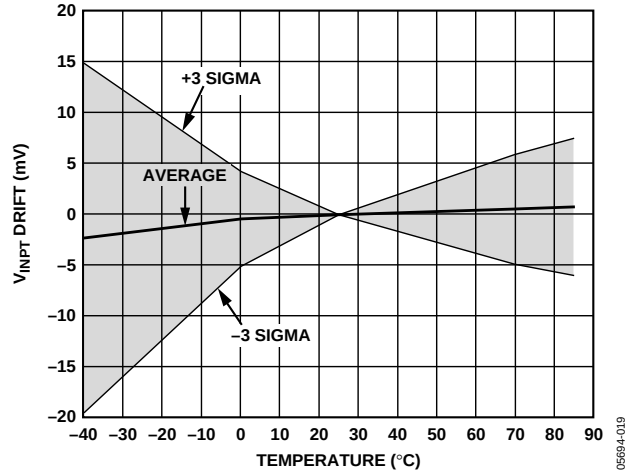


Figure 9. Temperature Drift of V_{INPT} with $V_{SET} = V_{SREF}$, 3-σ to Either Side of Mean

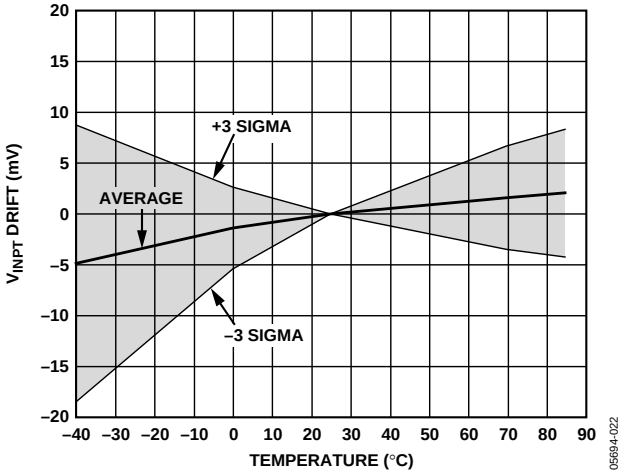


Figure 12. Temperature Drift of V_{INPT} with V_{SET} = 4 V (External Voltage Source), 3-σ to Either Side of Mean

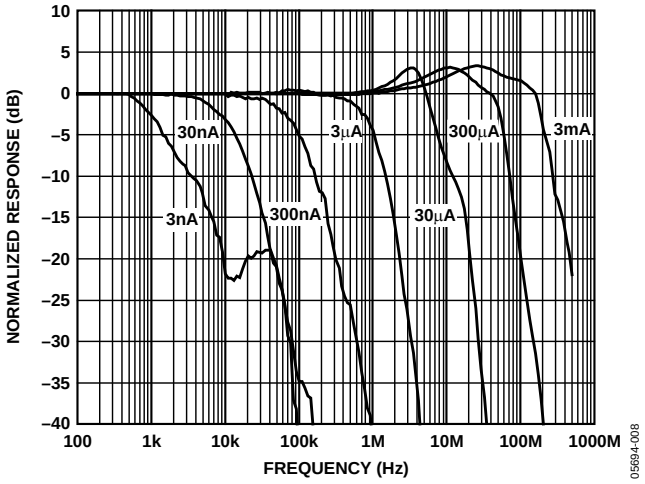


Figure 10. Small-Signal AC Response of I_{INPT} to I_{OUT} for I_{INPT} in Decades from 3 nA to 3 mA

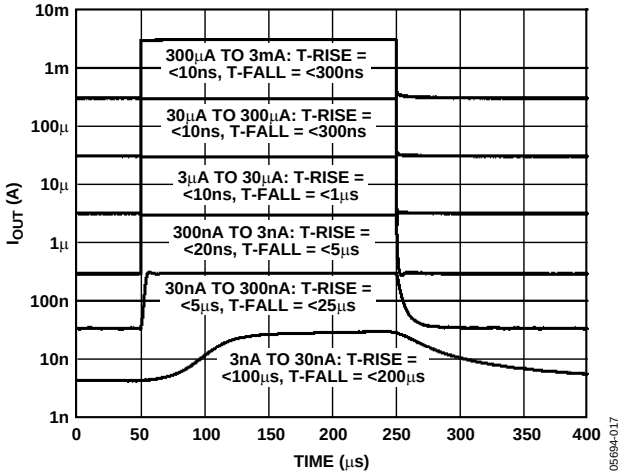


Figure 13. Pulse Response of I_{INPT} to I_{OUT} for I_{OUT} in Decades from 3 nA to 3 mA

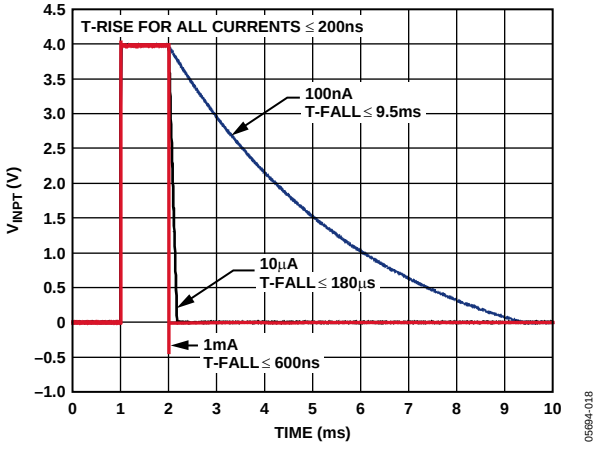


Figure 11. Pulse Response of V_{SET} to V_{INPT} (V_{SET} Pulsed from 0 V to 4 V) for Multiple Values of I_{INPT}

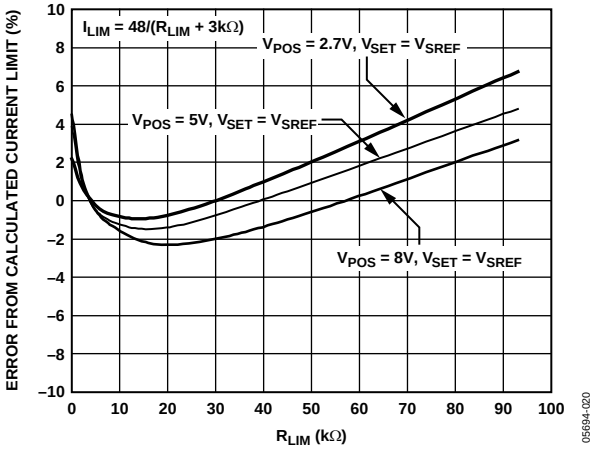


Figure 14. Current Limit Error in Percent vs. R_{LIM} for Multiple Voltages

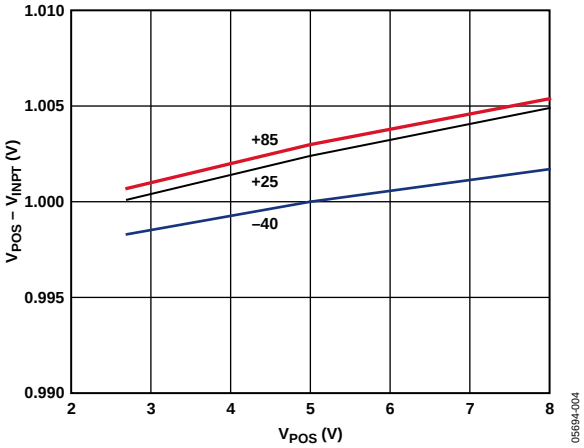


Figure 15. $V_{POS} - V_{INPT}$ vs. V_{POS} for Multiple Temperatures

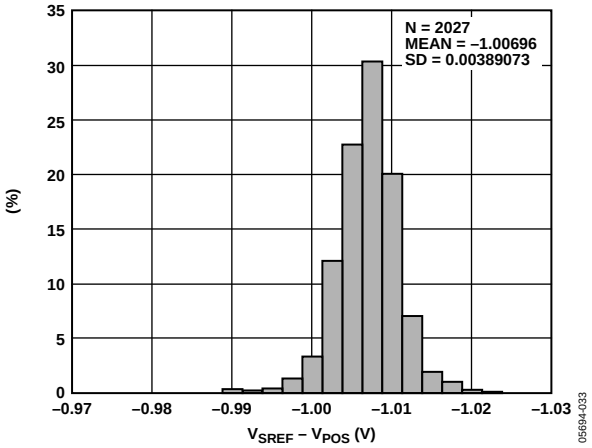


Figure 17. Distribution of $V_{SREF} - V_{POS}$ for $V_{POS} = 5$ V and $I_{INPT} = 3$ µA

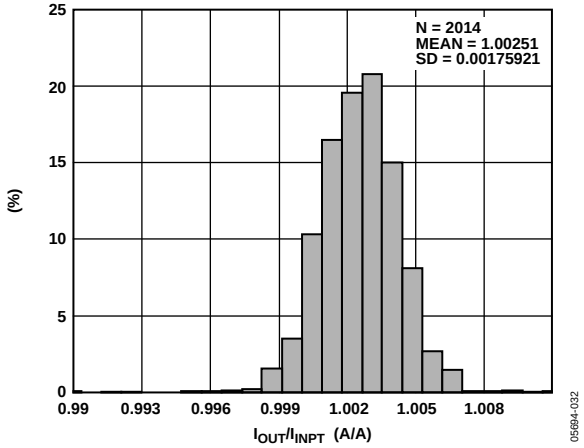


Figure 16. Distribution of I_{OUT}/I_{INPT} for $V_{POS} = 5$ V, $V_{SET} = 4$ V, and $I_{INPT} = 3$ µA

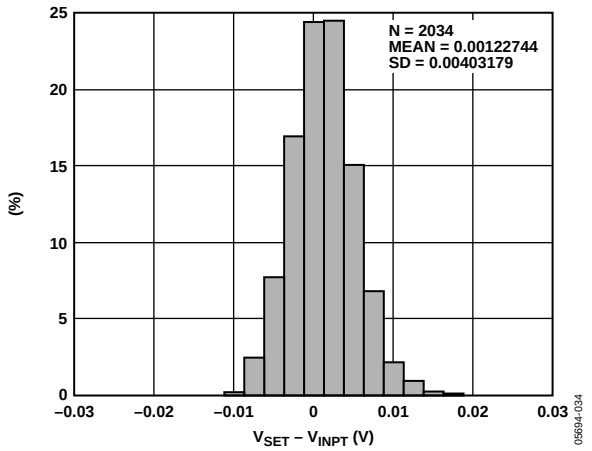


Figure 18. Distribution of $V_{SET} - V_{INPT}$ for $V_{POS} = 5$ V, $V_{SET} = 4$ V, and $I_{INPT} = 3$ µA

THEORY OF OPERATION

The ADL5315 addresses the need for precision high-side monitoring of photodiode current in fiber optic systems and is useful in many nonoptical applications as well. It is optimized for use with ADI's family of translinear logarithmic amplifiers, which take advantage of the wide input current range of the ADL5315. This arrangement allows the anode of the photodiode to connect directly to a transimpedance amplifier for the extraction of the data stream without the need for a separate optical power monitoring tap. Figure 19 shows the basic connections for the ADL5315.

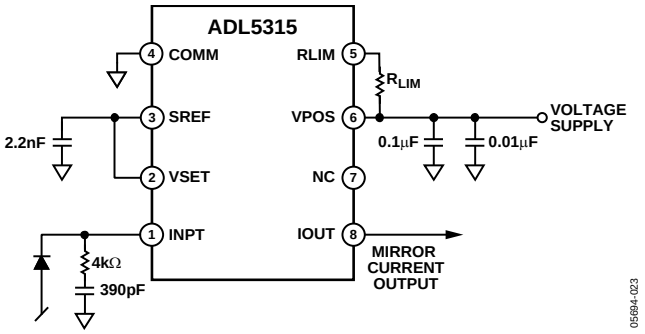


Figure 19. Basic Connections

At the heart of the ADL5315 is a precision 1:1 current mirror with a voltage following characteristic that provides an adjustable bias voltage at the mirror input. This architecture uses a JFET input amplifier to drive the bipolar mirror and maintain stable V_{INPT} voltage, while offering very low leakage current at the INPT pin. The current sourced by the low impedance INPT pin is mirrored and sourced by the high impedance IOUT pin.

BIAS CONTROL INTERFACE

The voltage at the INPT pin, V_{INPT}, is forced to be equal to the voltage applied to VSET by the mirror-biasing loop. The V_{SET} voltage range extends down to ground, allowing the ADL5315 to be used as a voltage-to-current converter with a single resistor from INPT to ground. This capability allows dark current to be minimized in PIN photodiode systems by maintaining a small voltage bias. The VSET control also allows V_{INPT} to be set approximately equal to the load voltage at IOUT. Balancing the mirror voltages in this way provides inherently superior linearity over the widest current range independent of the supply voltage. Only leakage currents from the JFET op amp and ESD devices remain as significant sources of nonlinearity at very low currents. The voltage at VSET can also be used to shield the highly sensitive INPT pin and its board trace from leakage currents, because the two pins operate at approximately the same potential. Care must be taken to provide a low noise V_{SET} signal, since voltage noise at VSET also appears at INPT and is transformed by the input compensation network into current noise.

The ADL5315 provides a setpoint reference pin, SREF, which can be connected to VSET for standard 2-port mirror operation. V_{SREF} is maintained 1.0 V below V_{POS} over temperature and is independent of input current. When using SREF to set the input voltage, a capacitor should be placed between SREF and ground to filter noise from SREF as well as improve power supply rejection over frequency. A value of 2.2 nF, for example, combined with the 20 kΩ output resistance at SREF, creates a pole at approximately 3 kHz.

The voltage at the SREF pin can be lowered to a desired fixed value with the use of a single external resistor from SREF to ground. Mismatch between on-chip and external resistors limits the accuracy of the resultant voltage. In addition, internal clamping to protect the precision bias limits the range. Figure 20 shows an equivalent circuit model of the SREF biasing. The Schottky diode clamp protects the 50 µA current source when SREF is pulled to ground. When V_{SREF} is 1.2 V or higher, the 50 µA current flows to the SREF pin. The current is shunted away and does not appear at the SREF pin for $V_{SREF} < 0.6$ V. The transition region is between 0.6 V and 1.2 V with a large uncertainty in the pull-down current. It is recommended that a 2-resistor divider from VPOS (with no connection to SREF) or another external bias be used to bias VREF in this transition region.

Equations for the SREF voltage with an external pull-down R_{EXT} follow:

$$V_{SREF} = \frac{R_{EXT}}{R_{EXT} + 20\,\text{k}\Omega}\left(V_{POS} - 1.0\,\text{V}\right), \quad V_{SREF} \geq 1.2\,\text{V}$$

$$V_{SREF} = \frac{R_{EXT}}{R_{EXT} + 20\,\text{k}\Omega} V_{POS}, \quad V_{SREF} \leq 0.6\,\text{V}$$

where the 20 kΩ is the process-dependent internal resistor.

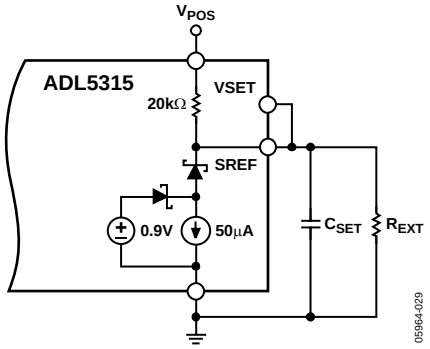


Figure 20. Model of SREF Bias Source with External Pull-Down

The VSET control is intended primarily to provide a dc bias voltage for the mirror input, but it is also well behaved in the presence of the V_{SET} transients. The rise time of V_{INPT} is largely independent of input current because the mirror is capable of sourcing large currents to pull up the INPT pin. The fall time, however, is inversely proportional to I_{INPT} because only I_{INPT} is available to discharge the input compensation capacitor and other parasitics (see Figure 11). The mirror output current can vary significantly from zero to several milliamps until V_{INPT} is fully settled.

NOISE PERFORMANCE

The noise performance for the ADL5315, defined as the rms noise current as a fraction of the output dc current, generally improves with increasing signal current. This partially results from the relationship between the quiescent collector current and the shot noise in the bipolar transistors. At lower signal current levels, the noise contribution from the JFET amplifier and other voltage noise sources appearing at INPT contribute significantly to the current noise. Filtering noise at VSET, whether provided by SREF or generated externally, as well as selecting optimal external compensation components on INPT, minimizes the amount of current noise at IOUT generated by the voltage noise at INPT.

MIRROR RESPONSE TIME

The response time of I_{OUT} to changes in I_{INPT} is fundamentally a function of input current, with small-signal bandwidth increasing roughly in proportion to I_{INPT} (see Figure 10). The value of the external compensating capacitor on INPT strongly affects the I_{OUT} response time (as well as the V_{SET} to V_{INPT} fall time, as noted in the Bias Control Interface section), although the value must be chosen to maintain stability and prevent noise peaking.

INPUT CURRENT LIMITING

The ADL5315 provides a resistor-programmable input current limit with a fixed maximum of 16 mA for the RLIM pin tied to VPOS. The fixed maximum provides input short-circuit protection to ground. The current limit is defined as the current that forces V_{INPT} to 0 V (when using a current source on the INPT pin). Resistor R_{LIM} between the VPOS and RLIM pins controls the current limit according to

$$I_{LIM} = \frac{48\text{ V}}{R_{LIM} + 3\text{ k}\Omega}$$

over an R_{LIM} range of 0 to 45 kΩ, corresponding to 16 mA down to 1 mA. Larger values of R_{LIM} can be used for currents below 1 mA (down to approximately 250 μA) with some degradation in accuracy. See Figure 14 for more performance detail.

APPLICATIONS

The ADL5315 is primarily designed for wide dynamic range applications, simplifying power monitoring designs where access is only permitted to the cathode of a PIN photodiode or receiver module. Figure 22 shows a typical application where the ADL5315 is used to provide an accurate bias to a PIN diode while simultaneously mirroring the diode current to be measured by a translinear logarithmic amplifier.

In this application, the ADL5315 sets the bias voltage on the PIN diode. This voltage is delivered at the INPT pin and is controlled by the voltage at the VSET pin. VSET is driven by the on-board reference V_{SREF}, which is equal to V_{POS} − 1 V.

The input current, I_{INPT}, is precisely mirrored at a ratio of 1:1 to the IOUT pin. This interface is optimized for use with any of ADI's translinear logarithmic amplifiers (for example, the AD8304 or AD8305) to offer a precise, wide dynamic range measurement of the optical power incident upon the PIN.

If a linear voltage output is preferred at IOUT, a single external resistor to ground is all that is necessary to perform the conversion.

AVERAGE POWER MONITORING

In applications where a modulated signal is incident upon the photodiode, the average power of the signal can be measured. Figure 21 shows the connections necessary for using the ADL5315 in such a measurement system.

The value of the capacitor to ground should be selected to eliminate errors due to modulation of the ADL5315 input current.

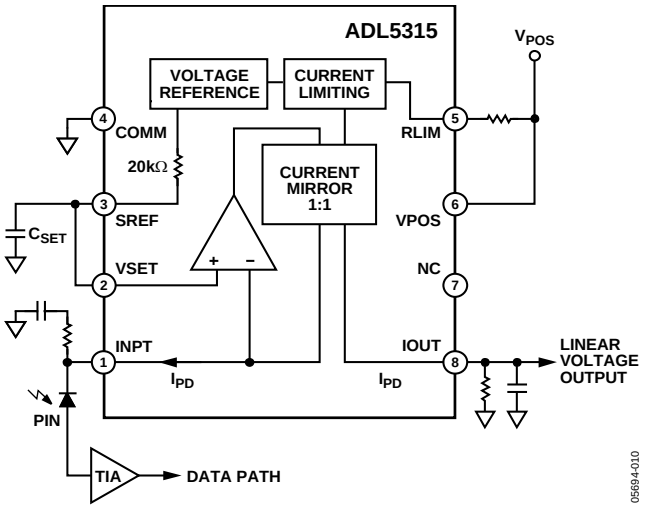


Figure 21. Average Power Monitoring Using the ADL5315

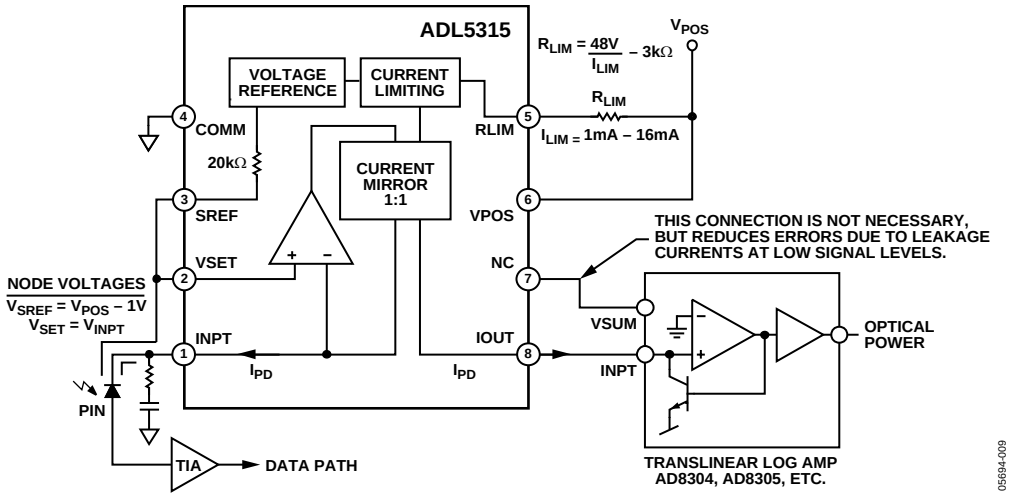


Figure 22. Typical Application Using the ADL5315

TRANSLINEAR LOG AMP INTERFACING

The mirror current output, IOUT, of the ADL5315 is designed to interface directly to an Analog Devices translinear logarithmic amplifier, such as the AD8304, AD8305, or ADL5306.

Figure 24 shows the basic connections necessary for interfacing the ADL5315 to the AD8305. In this configuration, the designer can use the full current mirror range of the ADL5315 for high accuracy power monitoring.

The measured rms noise voltage at the output of the AD8305 vs. the input current is shown in Figure 23, both for the AD8305 by itself and in cascade with the ADL5315. The relatively low noise produced by the ADL5315, combined with the additional noise filtering inherent in the frequency response characteristics of the AD8305, results in minimal degradation to the noise performance of the AD8305.

Careful consideration should be made to the layout of the circuit board in this configuration. Leakage current paths in the board itself could lead to measurement errors at the output of the translinear log amp, particularly when measuring the low end of the ADL5315's dynamic range. It is recommended that when designing such an interface that a guard potential be used to minimize this leakage. This can be done by connecting the translinear log amp's VSUM pin to the NC pin of the ADL5315, with the VSUM guard trace running on both sides of the IOUT trace. Additional details on using VSUM can be found in the AD8304 or AD8305 data sheets. The VSET pin of the ADL5315 can be used in a similar fashion to guard the INPT trace.

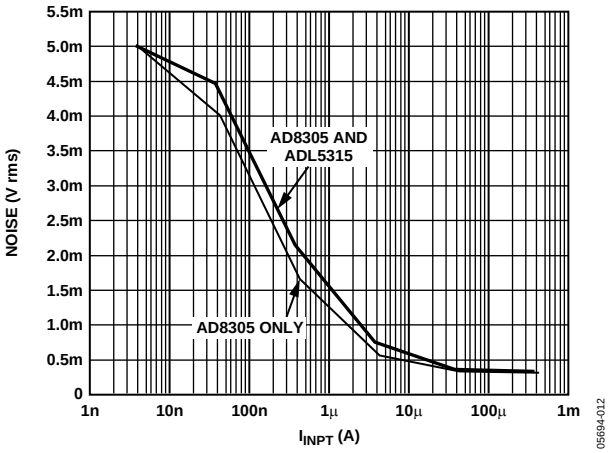


Figure 23. Measured RMS Noise of AD8305 vs. AD8305 Cascaded with ADL5315

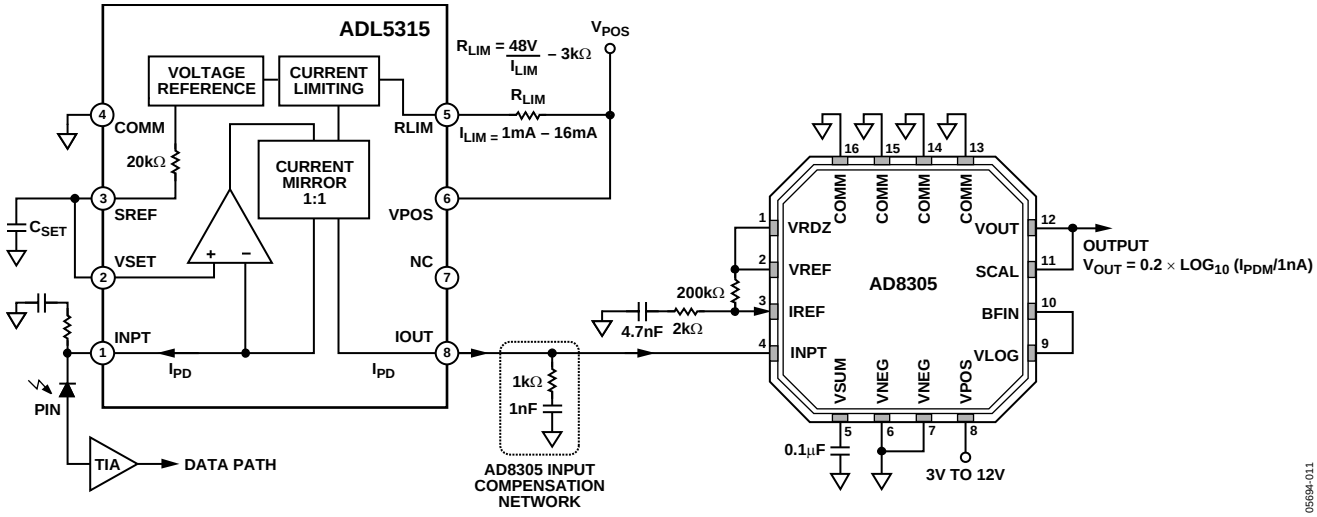


Figure 24. Interfacing the ADL5315 to the AD8305 for High Accuracy PIN Power Monitoring

EXTENDED OPERATING RANGE

The ADL5315 is specified over an input current range of 3 nA to 3 mA, but the device remains fully functional over the full eight decade range specified for ADI's flagship translinear logarithmic amplifier, the AD8304 (100 pA to 10 mA). Figure 25 and Figure 26 show the performance of the ADL5315 for this extended operating range vs. various temperature and supply conditions.

This extended dynamic range capability allows the ADL5315 to be used in optical power measurement systems, precision test equipment, or any other system that requires accurate, high dynamic range current monitoring.

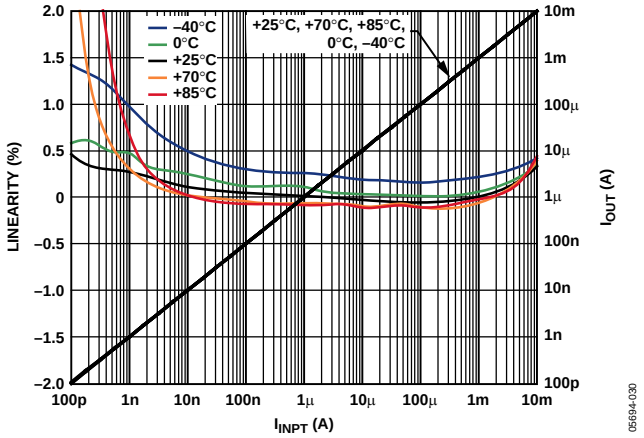


Figure 25. Extended Operating Range of 100 pA to 10 mA for Multiple Temperatures, Normalized to 25°C and I_{INPT} = 3 µA

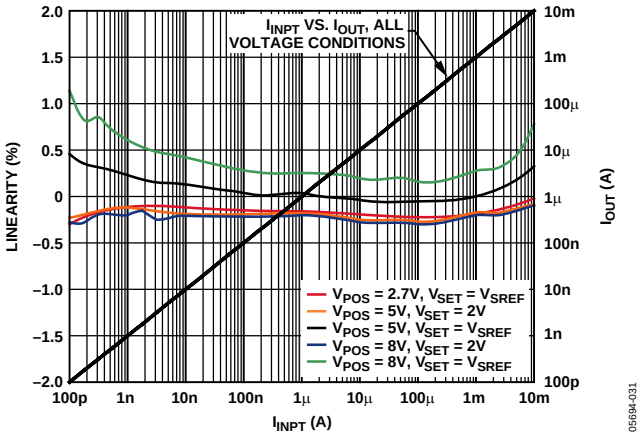


Figure 26. Extended Operating Range of 100 pA to 10 mA for Multiple Supply Conditions, Normalized to V_{POS} = 5 V, V_{SET} = V_{SREF} and I_{INPT} = 3 µA

USING RLIM AS A SECONDARY MONITOR

The RLIM pin can be used as a secondary linear output for monitoring input currents near the upper end of the ADL5315 current range. The RLIM pin sinks a current approximately equal to $I_{INPT}/40$. The voltage generated by this current through the series combination of an internal 3 kΩ resistor and the external R_{LIM} is compared to a 1.2 V threshold and fed back to the mirror bias to limit I_{INPT}.

Figure 27 shows the equivalent circuit and one method for using RLIM to form a V_{SET} bias proportional to I_{INPT}, also referred to as automatic photodiode biasing. This configuration is useful in PIN photodiode systems to compensate for photodiode equivalent series resistance (ESR) while maintaining low reverse bias at low signal levels to minimize dark current. Choosing R2 >> R_{LIM} minimizes impact on I_{LIM} and allows the resistor ratio, R2/R1, to be calculated based on maximum photodiode ESR using the following simplified equation.

$$\frac{R2}{R1} = \frac{40\ R_{PDmax}}{R_{LIM}},\ R2 >> R_{LIM},\ R1 = R3$$

where R_{PDmax} is the maximum ESR of the photodiode.

For zero bias at zero input current, the sum of R_{LIM} and R3 must equal R1. For positive bias at zero input current, the sum of R_{LIM} and R3 should be greater than R1. The ratio of V_{POS} to V_{SET} varies directly.

For example, choosing R_{LIM} = 1.82 kΩ (10 mA I_{LIM}), R2 = 100 kΩ, and R1 = 18.2 kΩ compensates for photodiode ESR up to 250 Ω.

A simple low voltage drop current mirror with a load resistor can replace the differential amplifier shown in Figure 27, although the resulting input current limit is less accurate and will vary with temperature.

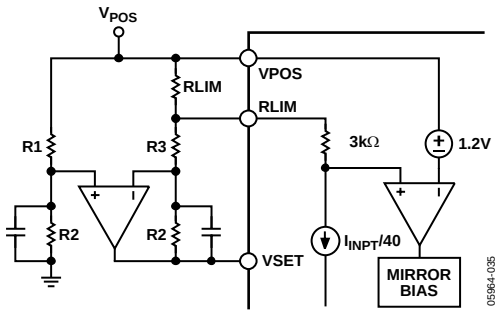


Figure 27. Providing Automatic Photodiode Voltage Biasing Using RLIM Pin

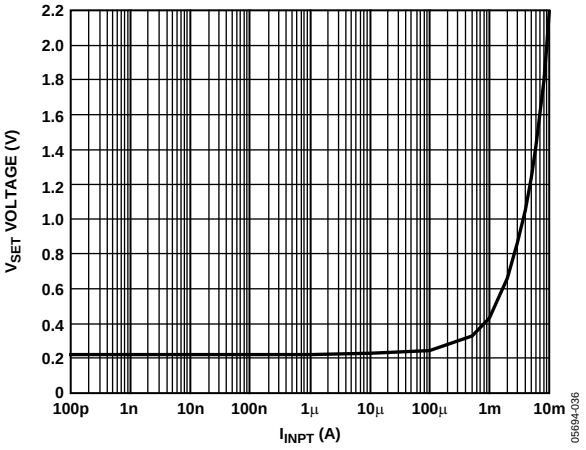


Figure 28. V_{SET} Voltage vs. I_{INPT} when RLIM Is Configured for Automatic Photodiode Biasing

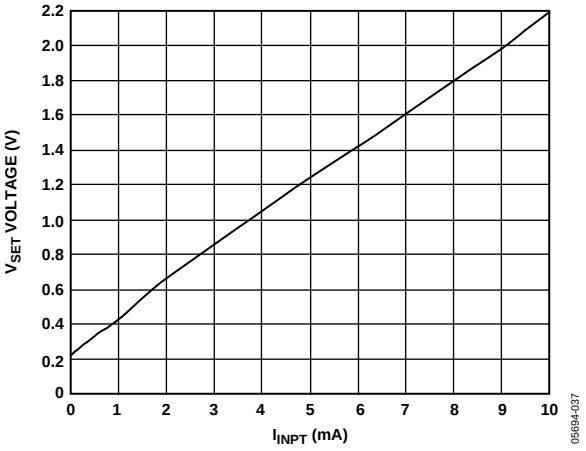


Figure 29. V_{SET} Voltage vs. I_{INPT} when RLIM Is Configured for Automatic Photodiode Biasing

Figure 28 and Figure 29 show the performance of the circuit in Figure 27. The reverse bias across the photodiode is held at a low value for small input currents to minimize dark current. The V_{SET} voltage increases in a linear manner at the higher input currents to maintain accurate photodiode responsivity. The minimum bias level for the configuration above is ~200 mV.

CHARACTERIZATION METHODS

During characterization, the ADL5315 was treated as a precision 1:1 current mirror. To make accurate measurements throughout the six-decade current range, calibrated Keithley 236 current sources were used to create and measure the test currents. Measurements at low currents are very susceptible to leakage to the ground plane. To minimize leakage on the characterization board, the VSET pin is connected to traces that buffer V_{INPT} from ground. These traces are connected to the triax guard connector to provide buffering along the cabling.

The primary characterization setup shown in Figure 30 is used to perform all static measurements, including mirror linearity between I_{INPT} and I_{OUT}, V_{INPT} variation vs. I_{INPT}, supply current, and I_{INPT} current limiting. Component selection of the characterization board is similar to that of the evaluation board, except that triax connectors are used instead of SMA. To measure pulse response, noise, and small signal bandwidth, more specialized test setups are used.

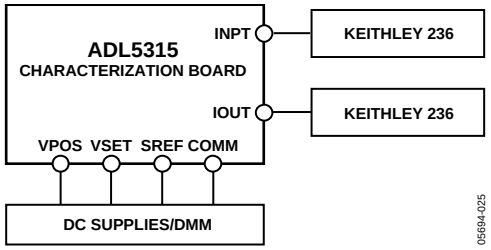


Figure 30. Primary Characterization Setup

The setup in Figure 31 is used to measure the output current noise of the ADL5315. Batteries are used in numerous places to minimize introduced noise and remove the uncertainty resulting from the use of multiple dc supplies. In application, properly bypassed dc supplies provide similar results. The load resistor is chosen for each current to maximize signal-to-noise ratio while maintaining measurement system bandwidth (when combined with the low capacitance JFET buffer). The custom LNA is used to overcome noise floor limitations in the HP89410A signal analyzer.

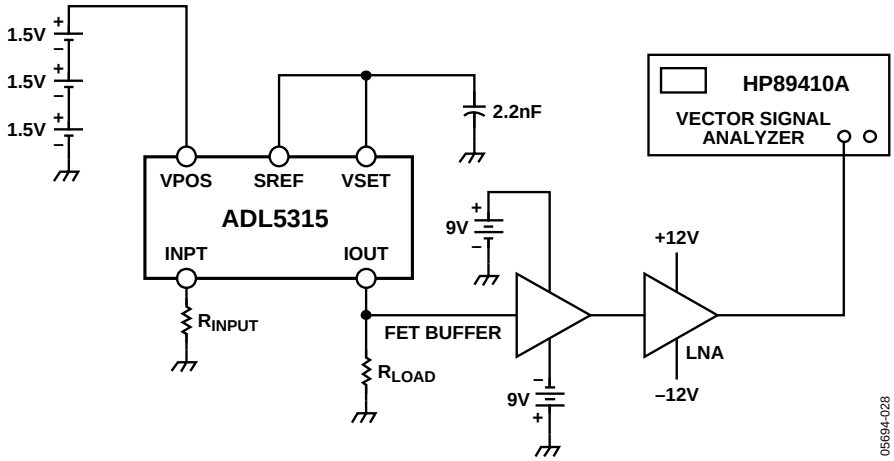


Figure 31. Configuration for Noise Spectral Density and Wideband Current Noise

Figure 32 shows the configuration used to measure the pulse response of I_{INPT} to I_{OUT}. To create the test current pulse, Q1 is used in a common base configuration with the Agilent 33250A pulse generator. The output of the 33250A is a negative biased square wave with an amplitude that results in a one decade current step at I_{OUT}.

R_C is chosen according to what current range is desired. For 30 µA and lower, the AD8067 FET input op amp is used in a transimpedance amplifier configuration to allow for viewing on the TDS5104 oscilloscope. For signals greater than 30 µA, the ADA4899-1 replaced the AD8067 to avoid limiting the bandwidth of the ADL5315.

The configuration in Figure 33 is used to measure V_{INPT} while V_{SET} is pulsed. Q1 and R_C are used to generate the operating current on the INPT pin. An Agilent 33250A pulse generator is used on the VSET pin to create a 0.0 V to 4.0 V square wave.

The setup in Figure 34 was used to measure the small signal ac response from I_{INPT} to I_{OUT}. The AD8138 differential amplifier was used to couple the ac and dc signals together. The ac signal was modulated to a depth of 5% of full scale over frequency. The voltage across R_F sets the dc operating point of I_{INPT}. The values of R_F are chosen to result in decade changes in I_{INPT}. The ADA4899-1 op amp is used as a transimpedance amplifier for all current conditions.

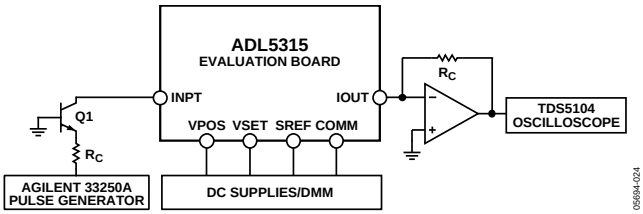


Figure 32. Configuration for Pulse Response of I_{INPT} to I_{OUT}

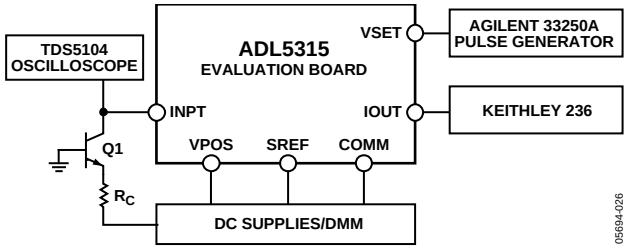


Figure 33. Configuration for Pulse Response from V_{SET} to V_{INPT}

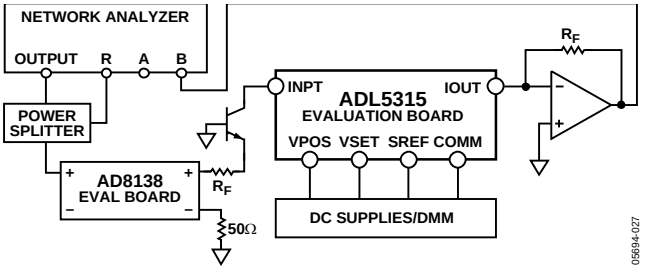


Figure 34. Configuration for Small-Signal AC Response

EVALUATION BOARD

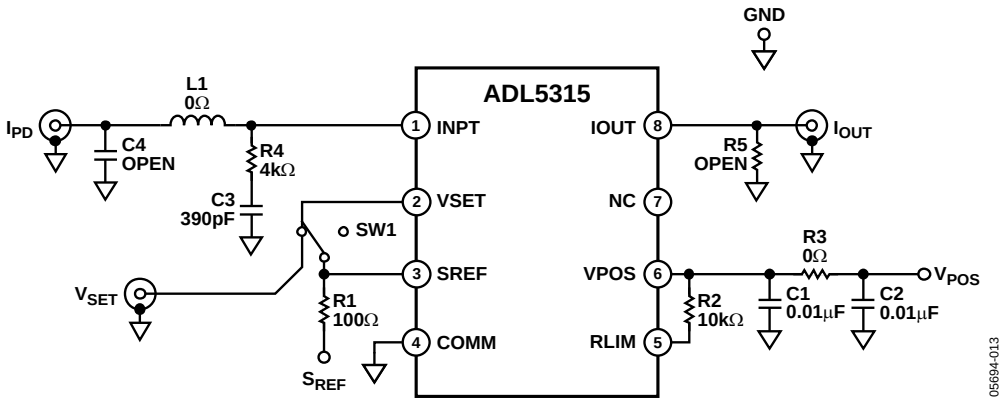


Figure 35. Evaluation Board Schematic (Rev. A)

Table 4. Evaluation Board (Rev. A) Configuration Options

Component	Function	Default Conditions
VPOS, GND	Supply and ground connections.	Not applicable
INPUT, L1, C4	Input Interface: The evaluation board is configured to accept an input current at the SMA connector labeled INPUT. Filtering of this current can be done using L1 and C4.	L1 = 0 Ω (size 0805) C4 = open (size 00603)
R4, C3	Input Compensation. Provides essential HF compensation at the INPT pin.	C3 = 390 pF (size 0805) R4 = 4.02 kΩ (size 0402)
SREF, VSET, SW1, R1, R6, R7	INPT Bias Voltage. The dc voltage applied to VSET determines the voltage at INPT, $V_{SET} = V_{INPT}$. Connecting SREF to VSET sets the bias at INPT to be 1 V below V_{POS}. Opening SW1 allows for VSET to be driven externally via the SMA connector.	SW1 = closed R1 = 100 Ω (size 0402) R6 = R7 = 0 Ω (size 0402)
IOUT, R5	Output/Mirror Current Interface: The output current at the SMA connector labeled IOUT is equal to the value at INPT. R5 allows a resistor to be installed for applications where a scaled voltage referenced to IPD is desirable instead of a current.	R5 = open (size 0603)
R2	Current Limiting. An external resistor to VPOS sets the current limit at INPT from 1 mA to 16 mA. $I_{LIM} = 48\ V/(R_{LIM} + 3\ k\Omega)$. The evaluation board is configured such that $I_{LIM} = 3.7$ mA.	R2 = 10 kΩ (size 0402)
C1, C2, R3	Supply Filtering/Decoupling.	C1 = 0.01 µF (size 0402) C2 = 0.1 µF (size 0603) R3 = 0 Ω (size 0805)

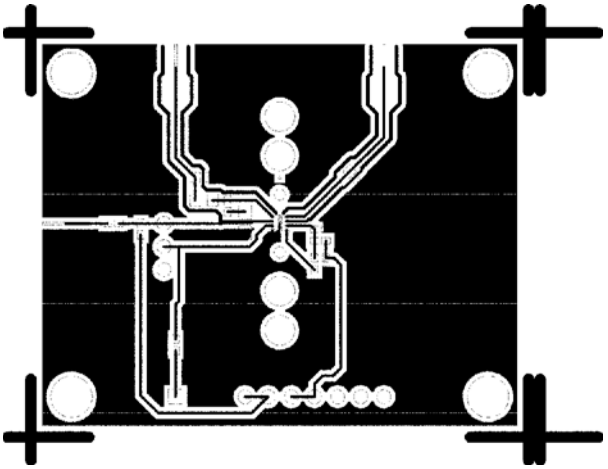


Figure 36. Component Side Layout

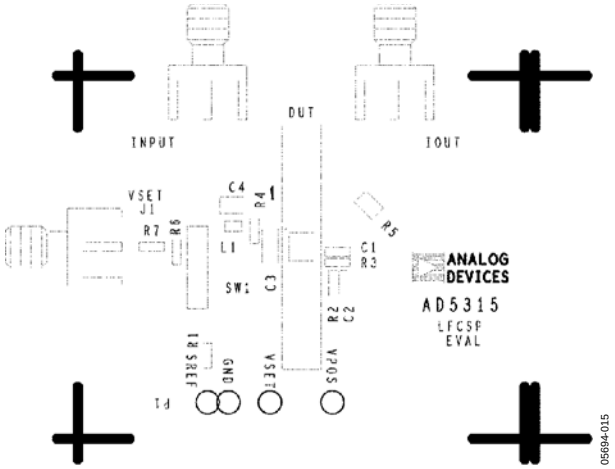


Figure 37. Component Side Silkscreen

OUTLINE DIMENSIONS

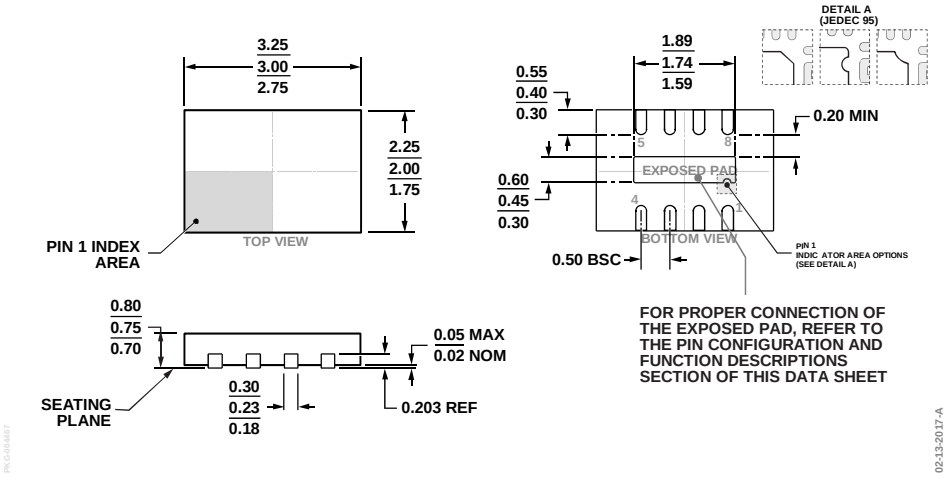


Figure 38. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 2 mm Body and 0.75 mm Package Height
(CP-8-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Branding
ADL5315ACPZ-R7	–40°C to +85°C	8-Lead LFCSP	CP-8-23	Q0
ADL5315ACPZ-WP	–40°C to +85°C	8-Lead LFCSP	CP-8-23	Q0
ADL5315-EVAL		Evaluation Board		

[1] Z = Pb-free part.
[2] WP = Waffle pack

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