Wide Dynamic Range, High Speed, Digitally Controlled VGA

Data Sheet

ADL5201

FEATURES

- –11.5 dB to +20 dB gain range
- 0.5 dB ± 0.1 dB step size
- 150 Ω differential input and output
- 7.5 dB noise figure at maximum gain
- OIP3 > 50 dBm at 200 MHz
- –3 dB upper frequency bandwidth of 700 MHz
- Multiple control interface options
  - Parallel 6-bit control interface (with latch)
  - Serial peripheral interface (SPI) (with fast attack)
  - Gain up/down mode
- Wide input dynamic range
- Low power mode option
- Power-down control
- Single 5 V supply operation
- 24-lead, 4 mm × 4 mm LFCSP package

APPLICATIONS

- Differential ADC drivers
- High IF sampling receivers
- High output power IF amplification
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

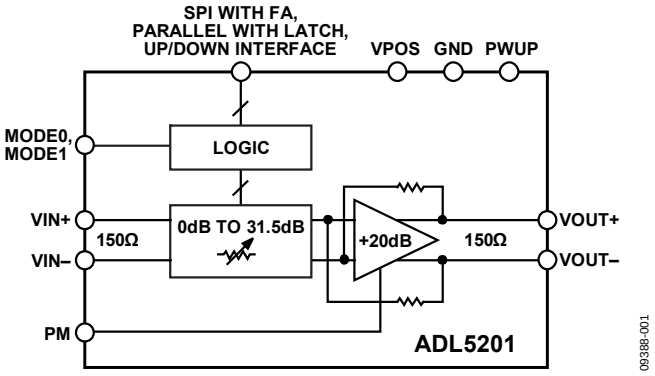


Figure 1.

GENERAL DESCRIPTION

The ADL5201 is a digitally controlled, variable gain, wide bandwidth amplifier that provides precise gain control, high IP3, and low noise figure. The excellent distortion performance and high signal bandwidth make the ADL5201 an excellent gain control device for a variety of receiver applications. The ADL5201 also incorporates a low power mode option that lowers the supply current.

For wide input dynamic range applications, the ADL5201 provides a broad 31.5 dB gain range with 0.5 dB resolution. The gain is adjustable through multiple gain control interface options: parallel, serial peripheral interface, and up/down.

Incorporating proprietary distortion cancellation techniques, the ADL5201 achieves an output IP3 of greater than 47 dBm at frequencies approaching 200 MHz for most gain settings.

The ADL5201 is powered on by applying the appropriate logic level to the PWUP pin. The quiescent current of the ADL5201 is typically 80 mA in low power mode. When configured in high performance mode for more demanding applications, the quiescent current is 110 mA. When powered down, the ADL5201 consumes less than 7 mA and offers excellent input-to-output isolation. The gain setting is preserved during power-down.

Fabricated on an Analog Devices, Inc., high speed SiGe process, the ADL5201 provides precise gain adjustment capabilities with good distortion performance and low phase error. The ADL5201 amplifier comes in a compact, thermally enhanced, 24-lead, 4 mm × 4 mm LFCSP package and operates over the temperature range of −40°C to +85°C.

Rev. C
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REVISION HISTORY

1/15—Rev. B to Rev. C

Changes to Table 1 ... 4
Change to Table 3 ... 6

9/13—Rev. A to Rev. B

Changed Logic Pins Absolute Maximum Rating from 3.6 V to −0.3 V to +3.6 V (not to exceed |VPOS − 0.5 V| at any time) ... 5

12/12—Rev. 0 to Rev. A

Changes to Layout Consideration Section ... 20
Updated Outline Dimensions ... 26

10/11—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, R_S = R_L = 150 Ω at 100 MHz, high performance mode, 2 V p-p differential output, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} < 2 V p-p (5.2 dBm)		700		MHz
Slew Rate			5.5		V/ns
Input Return Loss (S11)	100 MHz		−18.73		dB
Output Return Loss (S22)	100 MHz		−18.8		dB
INPUT STAGE	VIN+ and VIN− pins				
Maximum Input Swing (Differential)	Gain code = 111111		10.8		V p-p
Differential Input Resistance			150		Ω
Common-Mode Input Voltage			1.5		V
CMRR	Gain code = 000000		51.44		dB
GAIN					
Maximum Voltage Gain	Gain code = 000000		20		dB
Minimum Voltage Gain	Gain code = 111111		−11.5		dB
Gain Step Size			0.5		dB
Gain Flatness	30 MHz < f_C < 200 MHz		0.285		dB
Gain Temperature Sensitivity	Gain code = 000000		0.0089		dB/°C
Gain Step Response	For V_{IN} = 0.2 V, gain code = 111111 to 000000		15		ns
Gain Conformance Error	Over 10 dB gain range		±0.03		dB
Phase Conformance Error	Over 10 dB gain range		1.0		Degrees
OUTPUT STAGE	VOUT+ and VOUT− pins				
Output Voltage Swing	At P1dB, gain code = 000000		10		V p-p
Differential Output Resistance	Differential		150		Ω
NOISE/HARMONIC PERFORMANCE					
46 MHz	Gain code = 000000, high performance mode				
Second Harmonic	V_{OUT} = 2 V p-p		−86		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−104		dBc
Output IP3 (OIP3)	V_{OUT} = 2 V p-p composite		50		dBm
70 MHz	Gain code = 000000, high performance mode				
Second Harmonic	V_{OUT} = 2 V p-p		−91		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−103		dBc
Output IP3 (OIP3)	V_{OUT} = 2 V p-p composite		51		dBm
140 MHz	Gain code = 000000, high performance mode				
Noise Figure			7.5		dB
Second Harmonic	V_{OUT} = 2 V p-p		−89		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−97		dBc
Output IP3 (OIP3)	V_{OUT} = 2 V p-p composite		51		dBm
Output 1 dB Compression Point (OIP1dB)			19.8		dBm
300 MHz	Gain code = 000000, high performance mode				
Second Harmonic	V_{OUT} = 2 V p-p		−85		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−90		dBc
Output IP3 (OIP3)	V_{OUT} = 2 V p-p composite		50		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-UP INTERFACE	PWUP pin				
Power-Up Threshold	Minimum voltage to enable the device	1.4			V
	Maximum voltage to enable the device			3.3	V
PWUP Input Bias Current			1		µA
GAIN CONTROL INTERFACE					
V_{IH}	Minimum/maximum voltage for a logic high	1.4[1]		3.3	V
V_{IL}	Maximum voltage for a logic low			0.8	
Maximum Input Bias Current			1		µA
SPI TIMING	LATCH, SCLK, SDIO, data pins				
f_{SCLK}	$1/t_{SCLK}$		20		MHz
t_{DH}	Data hold time		5		ns
t_{DS}	Data setup time		5		ns
t_{PW}	SCLK high pulse width		5		ns
POWER INTERFACE					
Supply Voltage		4.5		5.5	V
Quiescent Current	High performance mode		110		mA
	85°C			120	mA
	Low power mode		80		mA
	85°C			95	mA
Power-Down Current	PWUP low		7		mA

[1] The minimum value for a logic high on the PM pin is 2.8 V.

TIMING DIAGRAMS

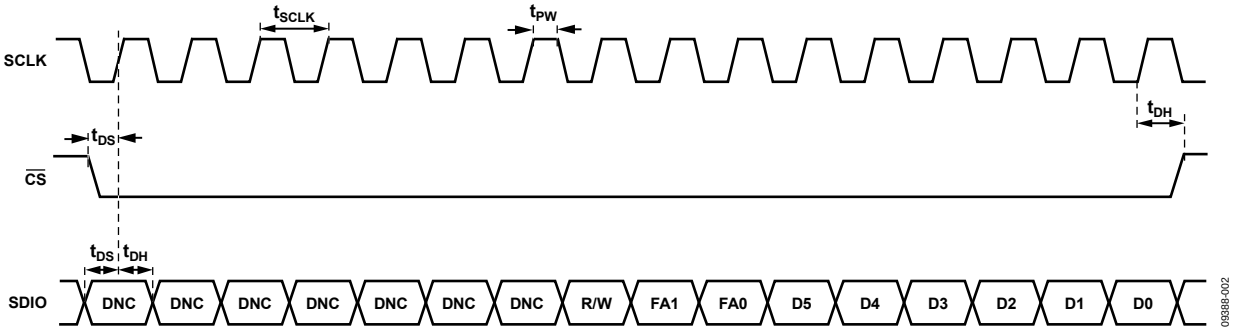


Figure 2. SPI Interface Read/Write Mode Timing Diagram

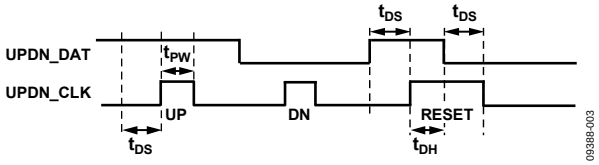


Figure 3. Up/Down Mode Timing Diagram

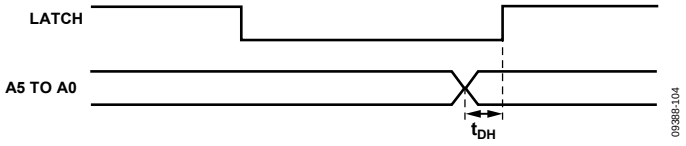


Figure 4. Parallel Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
PWUP, A0 to A5, MODE0, MODE1, PM, LATCH	−0.3 V to +3.6 V (not to exceed |VPOS − 0.5 V| at any time)
Input Voltage, VIN+ and VIN−	+3.6 V to −1.2 V
Internal Power Dissipation	676.5 mW
θ_{JA} (Exposed Paddle Soldered Down)	37.16°C/W
θ_{JC} (at Exposed Paddle)	2.29°C/W
Maximum Junction Temperature	140°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	240°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

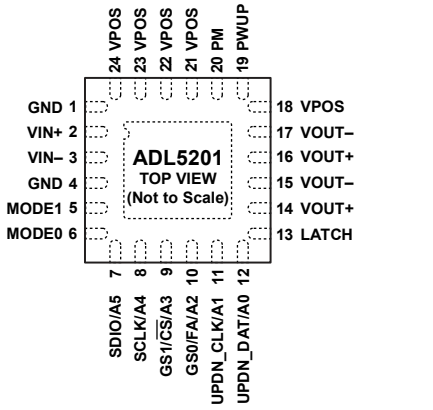


Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, EP	GND	Ground. The exposed paddle (EP) must be connected to a low impedance ground pad.
2	VIN+	Positive Input.
3	VIN−	Negative Input.
5	MODE1	MSB for Mode Control. With the MODE0 pin, selects parallel, SPI, or up/down interface mode.
6	MODE0	LSB for Mode Control. With the MODE1 pin, selects parallel, SPI, or up/down interface mode.
7	SDIO/A5	Serial Data Input/Output (SDIO). When $\overline{CS}$ is pulled low, SDIO is used for reading and writing to the SPI port. Bit 5 for Parallel Gain Control Interface (A5).
8	SCLK/A4	Serial Clock Input in SPI Mode (SCLK). Bit 4 for Parallel Gain Control Interface (A4).
9	GS1/$\overline{CS}$/A3	MSB for Gain Step Size Control in Up/Down Mode (GS1). SPI Interface Select ($\overline{CS}$). When serial mode is enabled, a logic low (0 V ≤ $\overline{CS}$ ≤ 0.8 V) enables the SPI interface. Bit 3 for Parallel Gain Control Interface (A3).
10	GS0/FA/A2	LSB for Gain Step Size Control in Up/Down Mode (GS0). Fast Attack (FA). In serial mode, a logic high (1.4 V ≤ FA ≤ 3.3 V) attenuates according to the FA setting in the SPI word. Bit 2 for Parallel Gain Control Interface (A2).
11	UPDN_CLK/A1	Clock Interface for Up/Down Function (UPDN_CLK). Bit 1 for Parallel Gain Control Interface (A1).
12	UPDN_DAT/A0	Data Pin for Up/Down Function (UPDN_DAT). Bit 0 for Parallel Gain Control Interface (A0).
13	LATCH	A logic low (0 V ≤ LATCH ≤ 0.8 V) allows gain changes. A logic high (1.4 V ≤ LATCH ≤ 3.3 V) disallows gain changes.
14, 16	VOUT+	Positive Output.
15, 17	VOUT−	Negative Output.
18, 21, 22, 23, 24	VPOS	Positive Power Supply.
19	PWUP	Power-Up Pin. A logic high (1.4 V ≤ PWUP ≤ 3.3 V) enables the part.
20	PM	Performance Mode. A logic low (0 V ≤ PM ≤ 0.8 V) enables high performance mode. A logic high (2.8 V ≤ PM ≤ 3.3 V) enables low power mode.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, R_S = R_L = 150 Ω at 200 MHz, high performance mode, 2 V p-p differential output, unless otherwise noted.

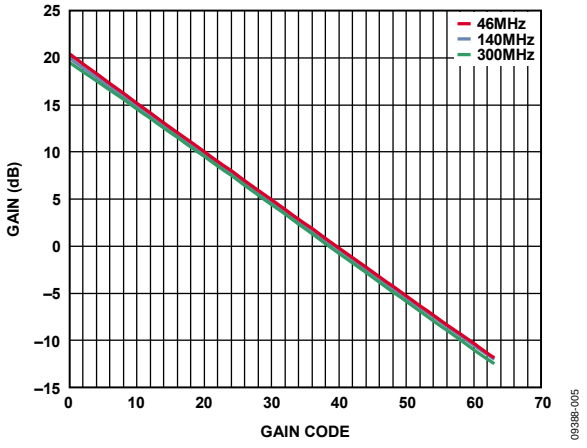


Figure 6. Gain vs. Gain Code at 46 MHz, 140 MHz, and 300 MHz

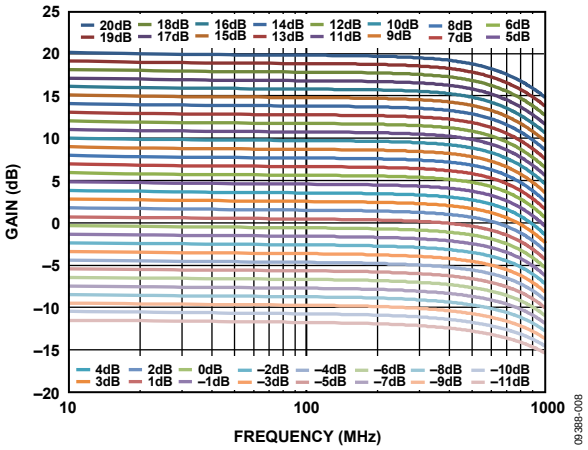


Figure 9. Gain vs. Frequency Response (Every 1 dB Step)

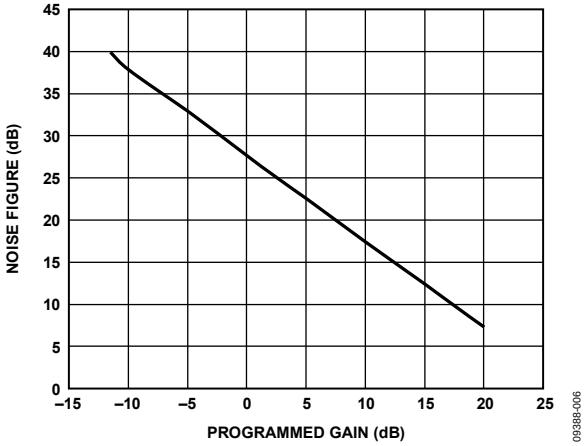


Figure 7. Noise Figure vs. Programmed Gain at 140 MHz

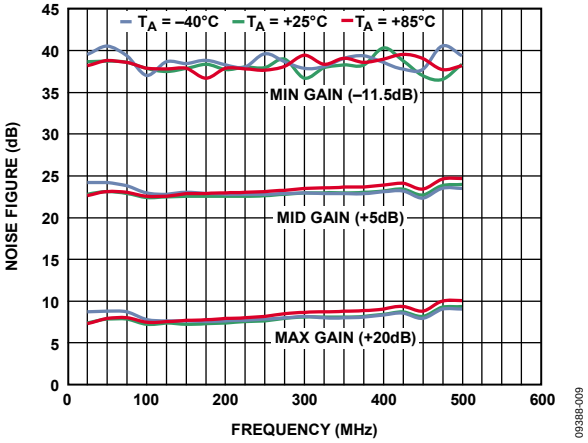


Figure 10. Noise Figure vs. Frequency at Max, Mid, and Min Gain Outputs

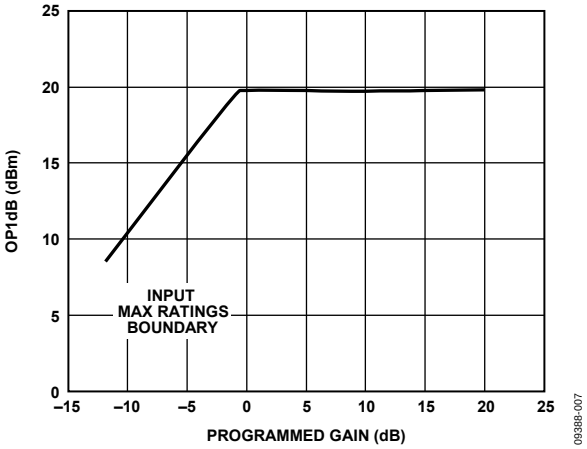


Figure 8. OP1dB vs. Programmed Gain at 140 MHz

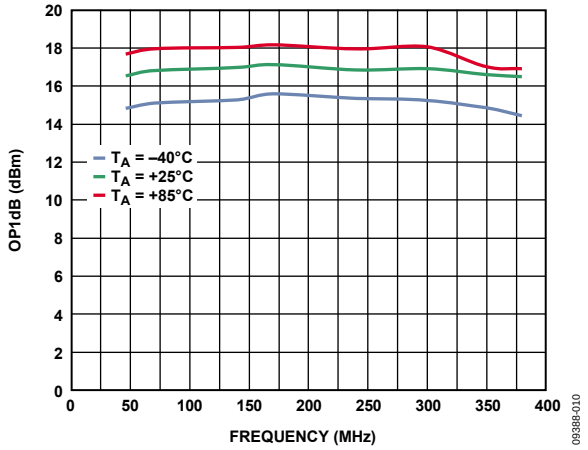


Figure 11. OP1dB vs. Frequency at Maximum Gain, Three Temperatures

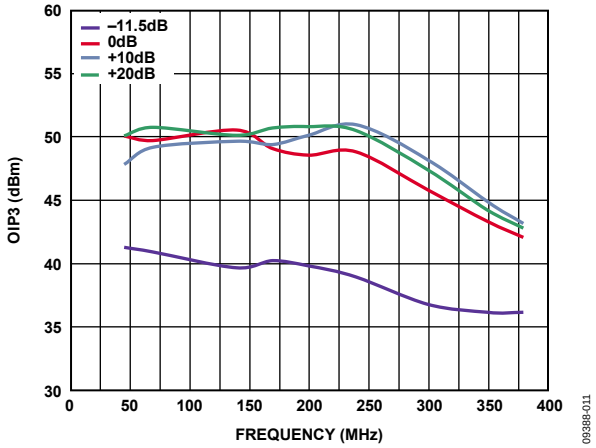


Figure 12. Output Third-Order Intercept vs. Frequency at Four Gain Codes

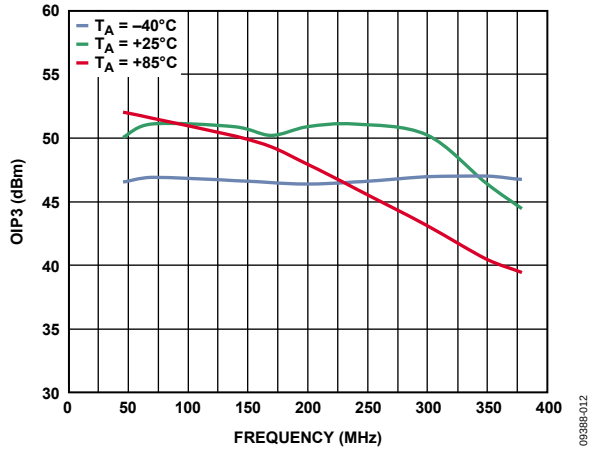


Figure 13. Output Third-Order Intercept vs. Frequency, Three Temperatures at 2 V p-p Composite

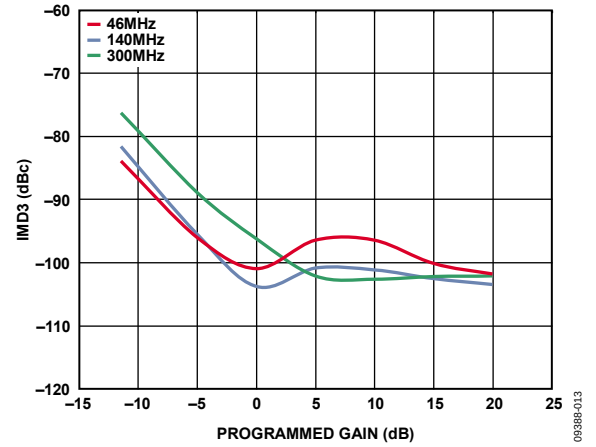


Figure 14. Two-Tone Output IMD3 vs. Programmed Gain at 46 MHz, 140 MHz, and 300 MHz

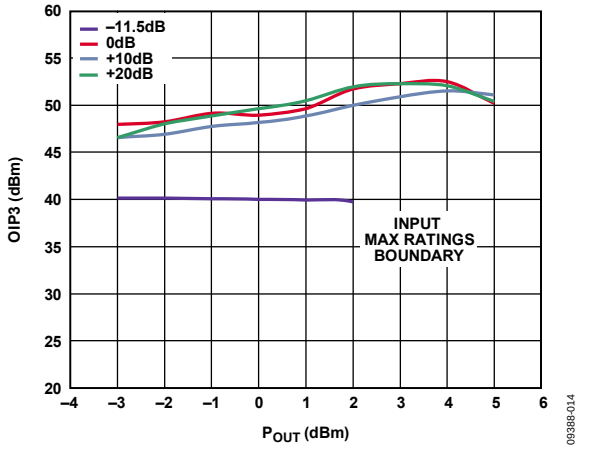


Figure 15. Output Third-Order Intercept vs. Power at Four Gain Codes, Frequency = 140 MHz at 2 V p-p Composite

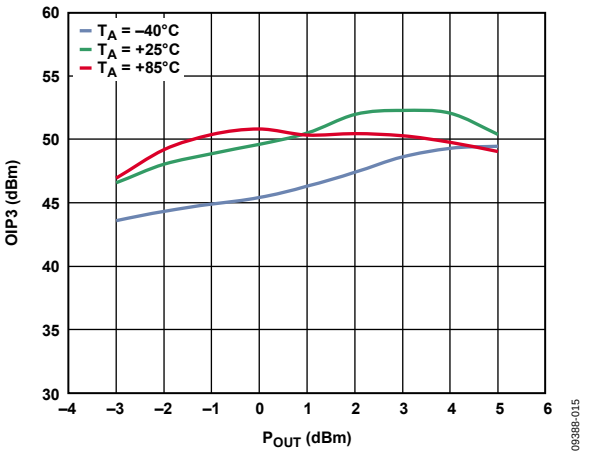


Figure 16. Output Third-Order Intercept vs. Power, Frequency = 140 MHz, Three Temperatures

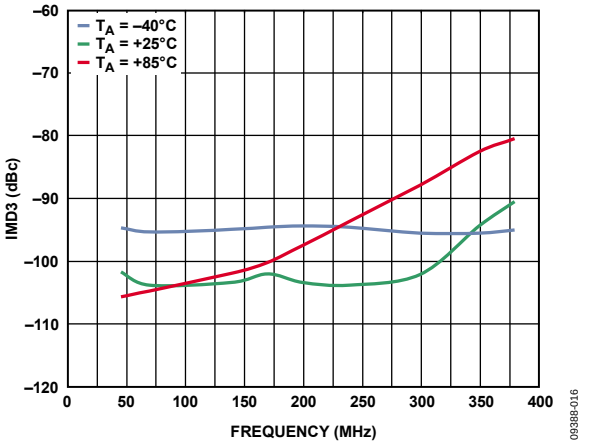


Figure 17. Two-Tone Output IMD3 vs. Frequency, Three Temperatures

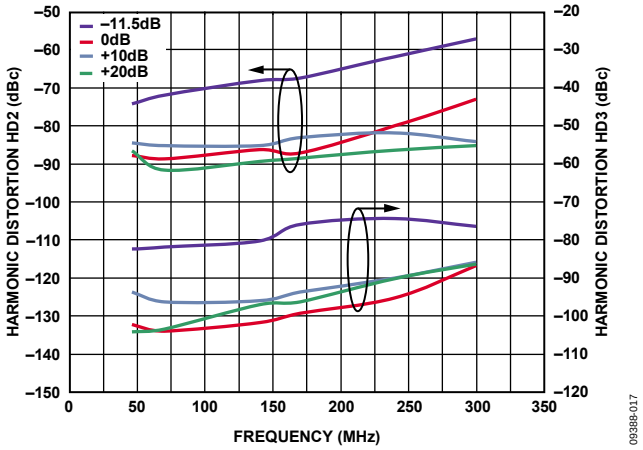


Figure 18. Harmonic Distortion vs. Frequency at Four Gain Codes

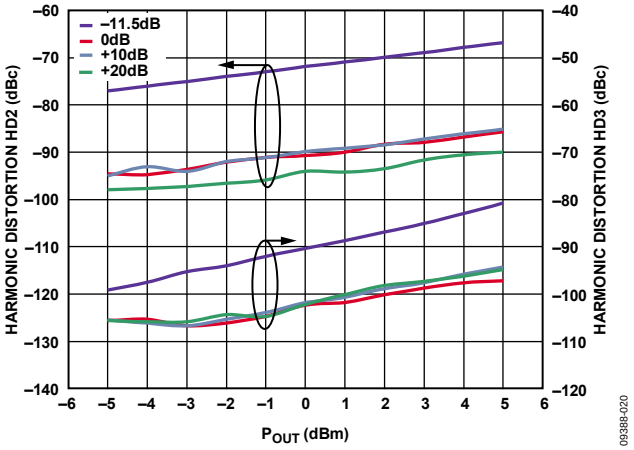


Figure 21. Harmonic Distortion vs. Power at Four Gain Codes, Frequency = 140 MHz

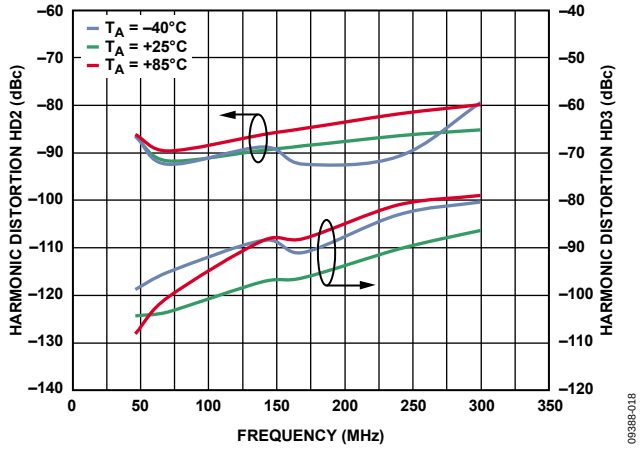


Figure 19. Harmonic Distortion vs. Frequency, Three Temperatures

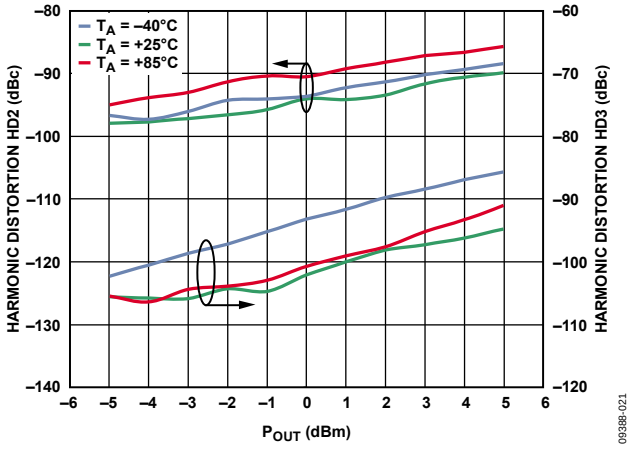


Figure 22. Harmonic Distortion vs. Power, Frequency = 140 MHz, Three Temperatures

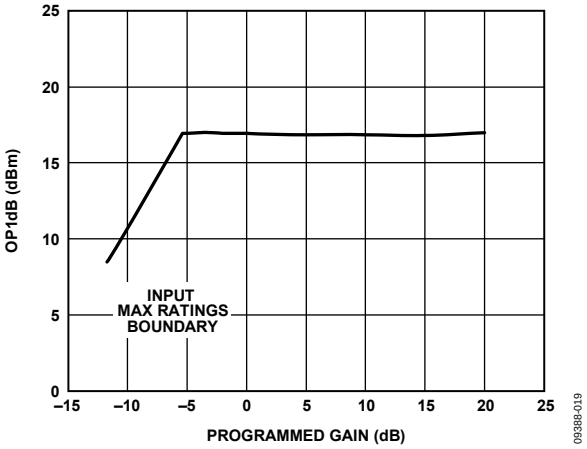


Figure 20. OP1dB vs. Programmed Gain at 140 MHz, Low Power Mode

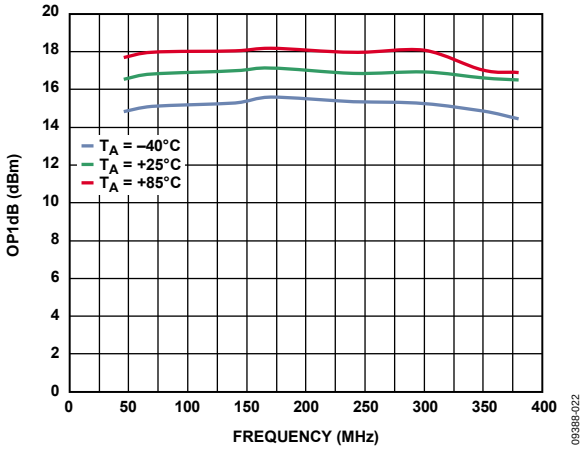


Figure 23. OP1dB vs. Frequency at Maximum Gain, Three Temperatures, Low Power Mode

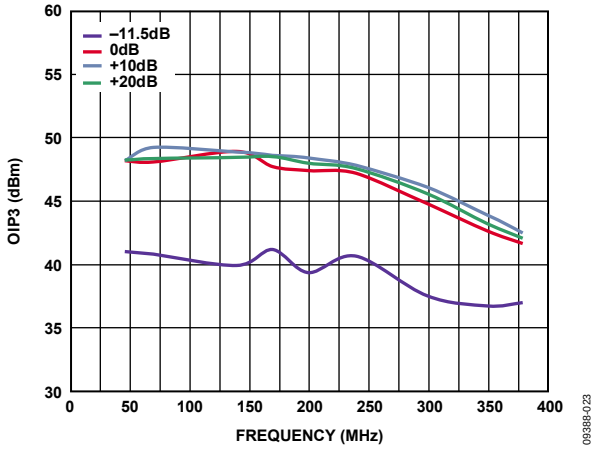


Figure 24. Output Third-Order Intercept vs. Frequency at Four Gain Codes, Low Power Mode at 2 V p-p Composite

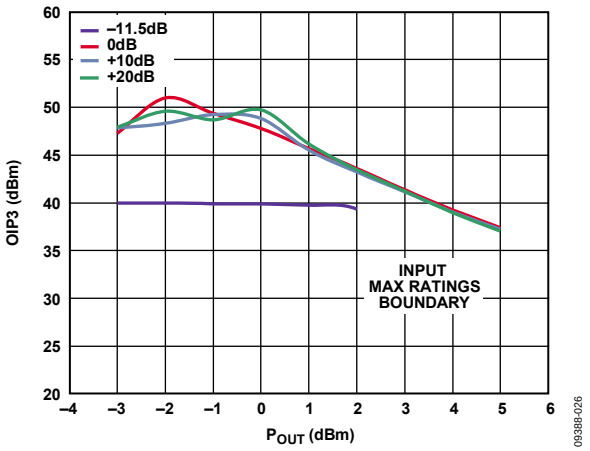


Figure 27. Output Third-Order Intercept vs. Power at Four Gain Codes, Frequency = 140 MHz, Low Power Mode

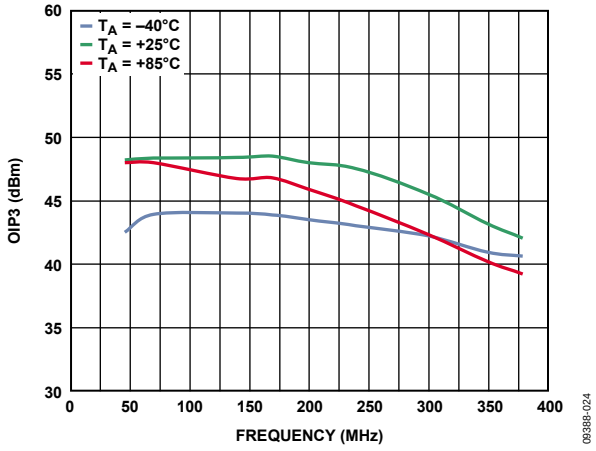


Figure 25. Output Third-Order Intercept vs. Frequency, Three Temperatures, Low Power Mode

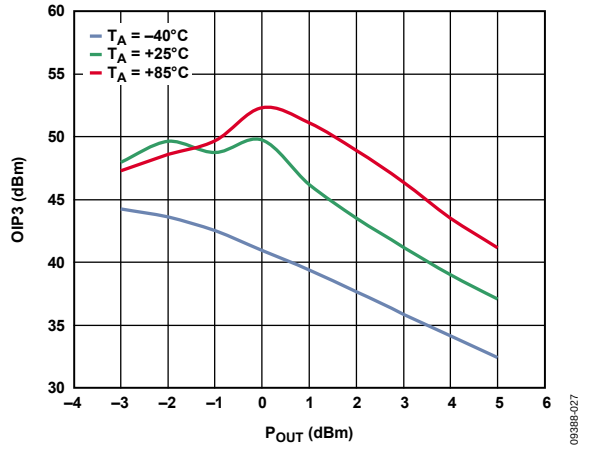


Figure 28. Output Third-Order Intercept vs. Power, Three Temperatures, Low Power Mode at 2 V p-p Composite

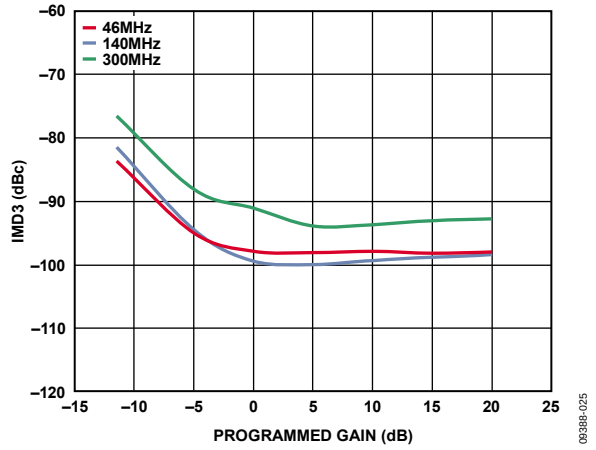


Figure 26. Two-Tone Output IMD3 vs. Programmed Gain at 46 MHz, 140 MHz, and 300 MHz; Low Power Mode

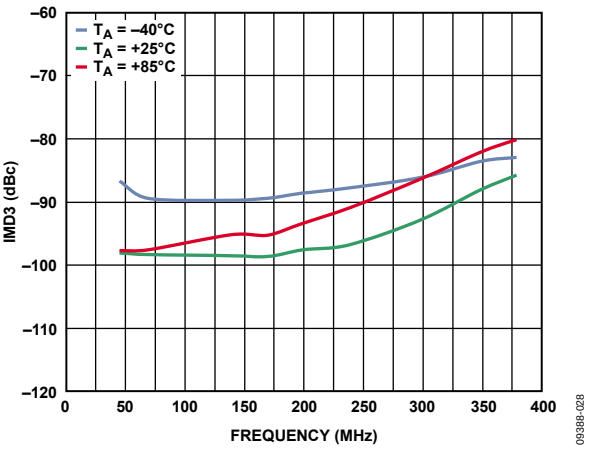


Figure 29. Two-Tone Output IMD3 vs. Frequency, Three Temperatures, Low Power Mode

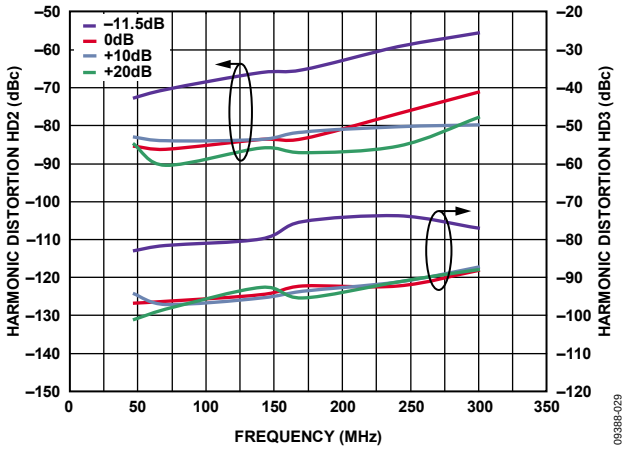


Figure 30. Harmonic Distortion vs. Frequency at Four Gain Codes, Low Power Mode

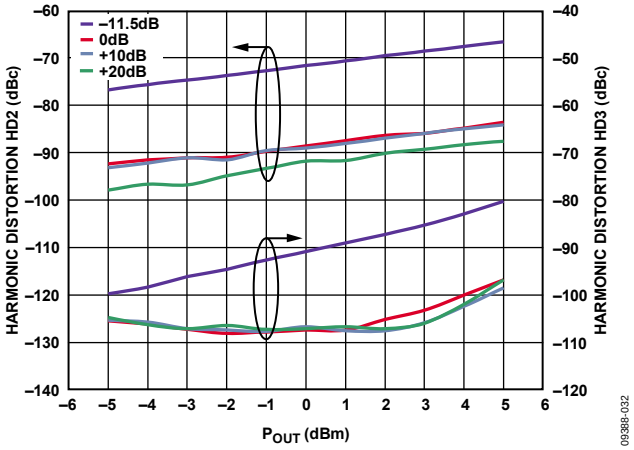


Figure 33. Harmonic Distortion vs. Power at Four Gain Codes, Frequency = 140 MHz, Low Power Mode

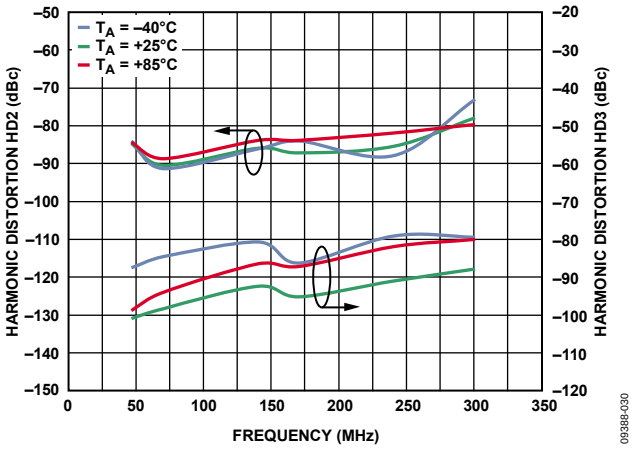


Figure 31. Harmonic Distortion vs. Frequency, Three Temperatures, Low Power Mode

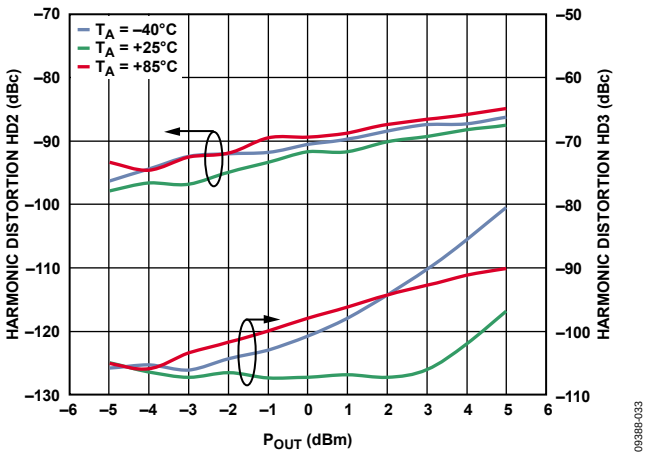


Figure 34. Harmonic Distortion vs. Power, Frequency = 140 MHz, Three Temperatures, Low Power Mode

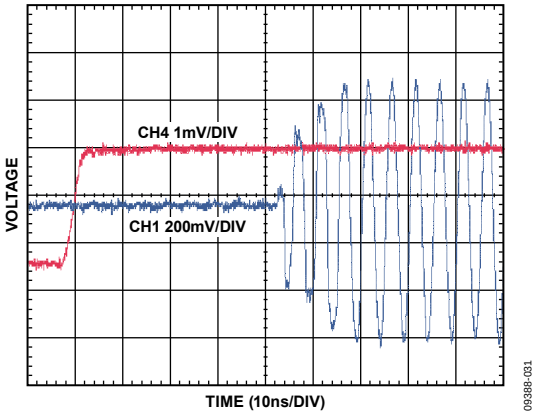


Figure 32. Enable Time Domain Response

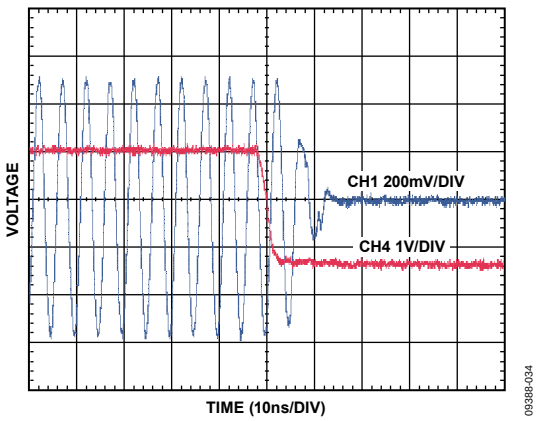


Figure 35. Disable Time Domain Response

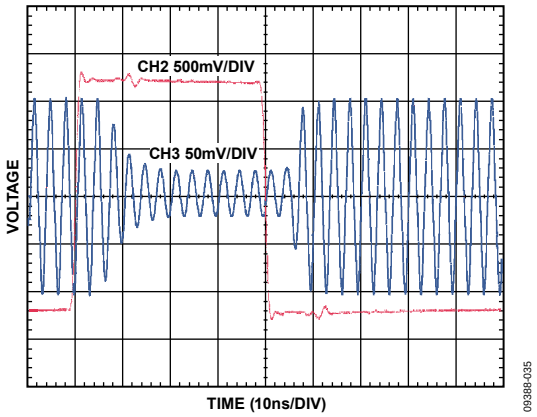


Figure 36. Gain Step Time Domain Response

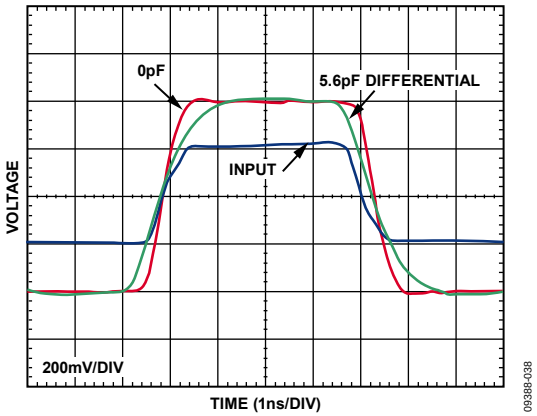


Figure 39. Large Signal Pulse Response, 0 pF and 5.6 pF, 2 V p-p Composite

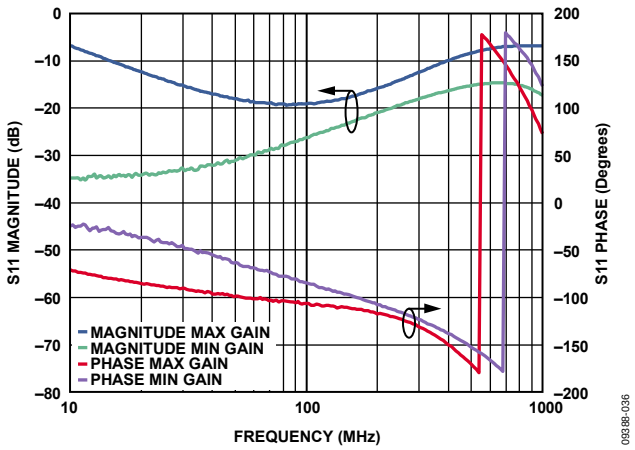


Figure 37. S11 Magnitude and Phase vs. Frequency

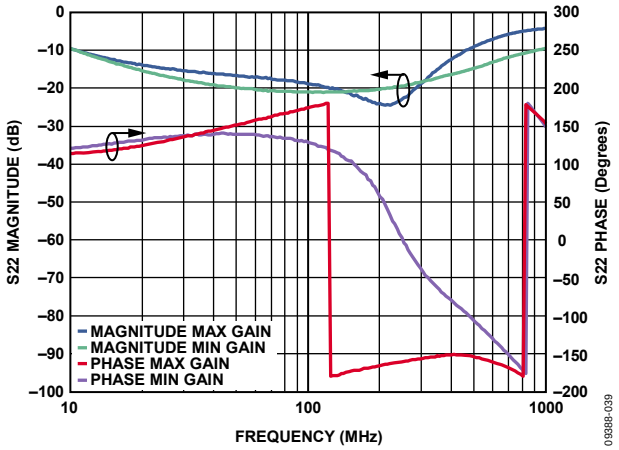


Figure 40. S22 Magnitude and Phase vs. Frequency

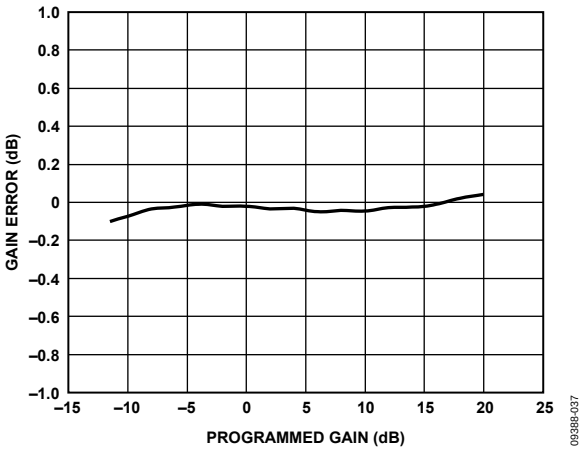


Figure 38. Gain Step Error, Frequency = 140 MHz

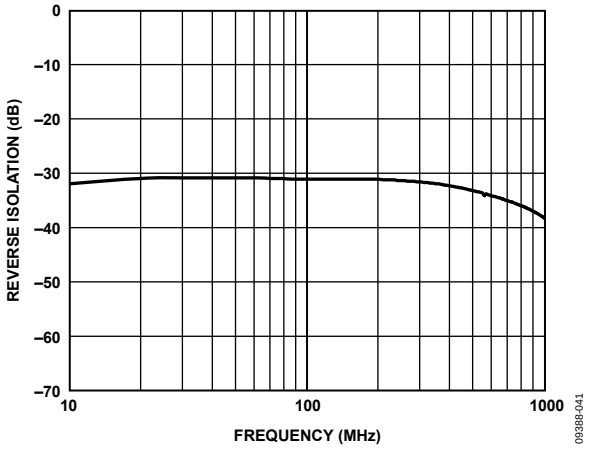


Figure 41. Reverse Isolation vs. Frequency

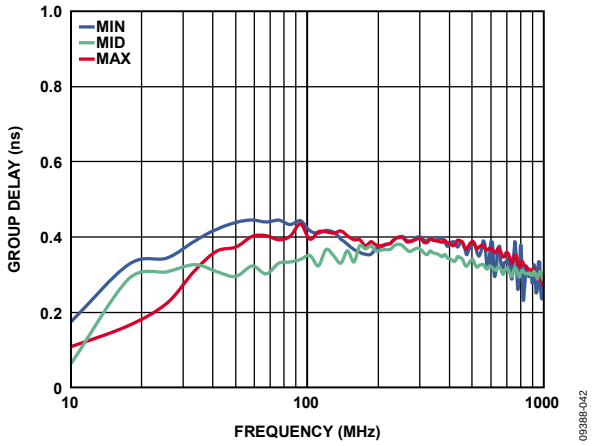


Figure 42. Group Delay vs. Frequency at Max, Mid, and Min Gain Outputs

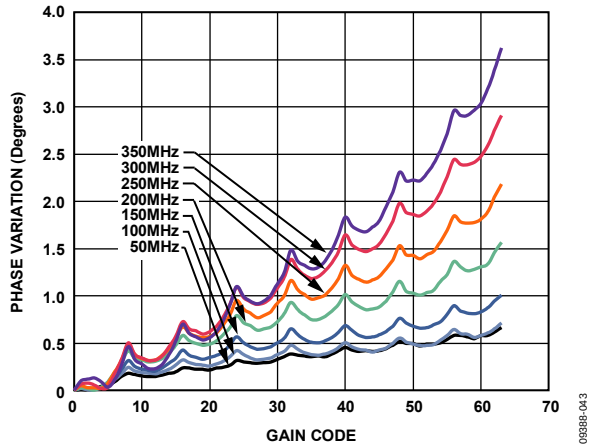


Figure 43. Phase Variation vs. Gain Code

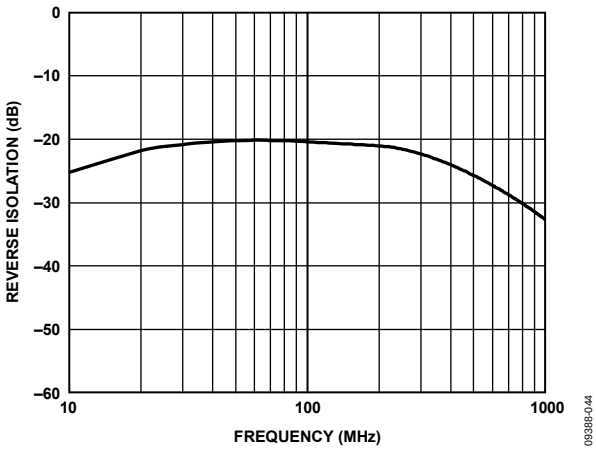


Figure 44. Disable-State Reverse Isolation vs. Frequency

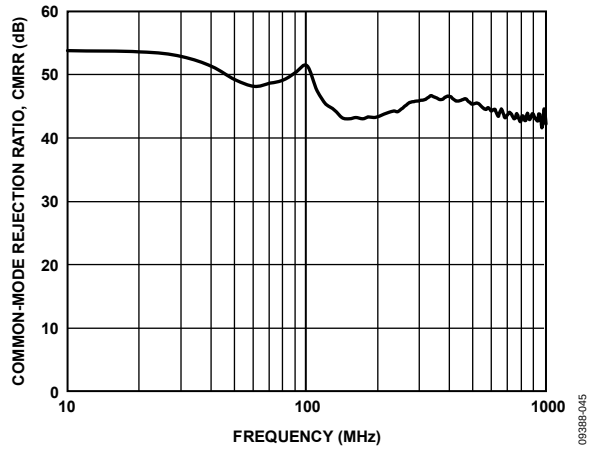


Figure 45. Common-Mode Rejection Ratio vs. Frequency

CHARACTERIZATION AND TEST CIRCUITS

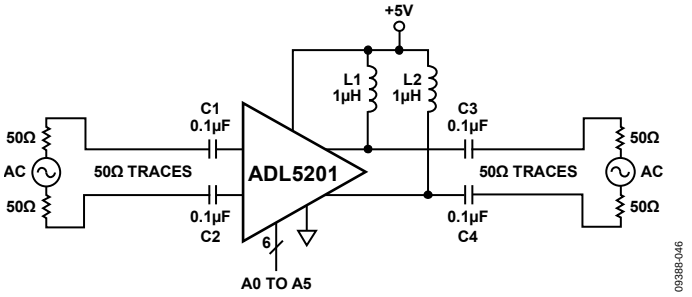


Figure 46. Test Circuit for S-Parameters on Dedicated 50 Ω Differential-to-Differential Board

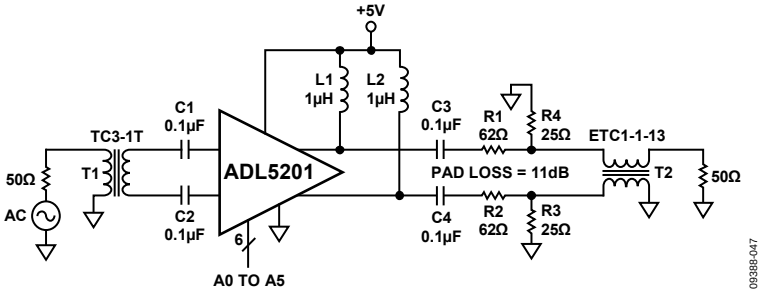


Figure 47. Test Circuit for Distortion, Gain, and Noise

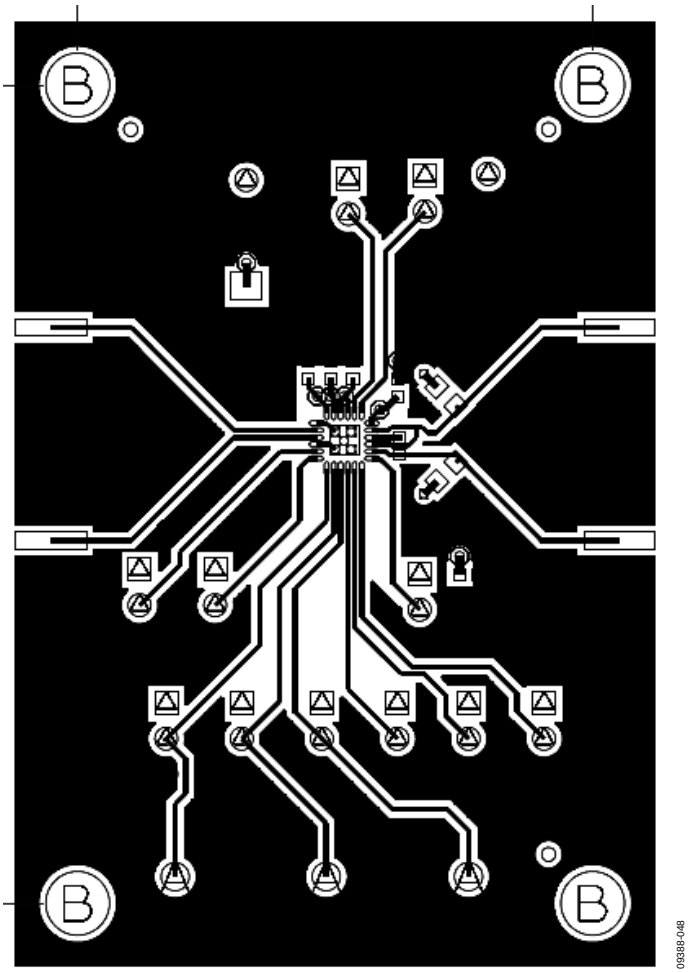


Figure 48. Differential-to-Differential Characterization Board

THEORY OF OPERATION

DIGITAL INTERFACE OVERVIEW

The ADL5201 DVGA has three digital gain control options: parallel control interface, serial peripheral interface, and gain up/down interface. The desired gain control option is selected via two control pins, MODE0 and MODE1 (see Table 4 for the truth table for the mode control pins). The gain code is in 6-bit binary format. A voltage from 1.4 V to 3.3 V is required for a logic high.

Two pins are common to all gain control options: PM and PWUP. PM allows the user to choose operation in low power mode or high performance mode. PWUP is the power-up pin. Physical pins are shared among the three interfaces, resulting in as many as three different functions per digital pin (see Table 3).

Table 4. Digital Control Interface Selection Truth Table

MODE1	MODE0	Interface
0	0	Parallel control
0	1	Serial peripheral (SPI)
1	0	Up/down
1	1	Up/down

PARALLEL DIGITAL INTERFACE

The parallel digital interface uses six binary bits (Bits[A5:A0]) and a latch pin (LATCH). The Latch pin controls whether the input data latch is transparent or latched. In transparent mode, the gain changes as the input gain control bits change. In latched mode, gain is determined by the latched gain setting and does not change with the input gain control bits.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI uses three pins: SDIO, SCLK, and $\overline{CS}$. The SPI data register consists of two bytes: six gain control bits, two attenuation step size address bits, one read/write bit, and seven don't care bits. SDIO is the serial data input and output pin. The SCLK pin is the serial clock, and $\overline{CS}$ is the channel select pin.

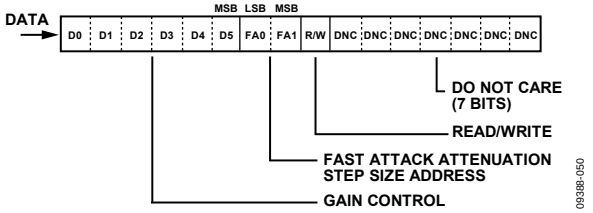


Figure 49. 16-Bit SPI Register

To write to the SPI register, $\overline{CS}$ must be pulled low and 16 clock pulses must be applied to SCLK. To read the SPI register value, the R/W bit must be set high, $\overline{CS}$ must be pulled low, and the part must be clocked. After the register is read out during the next 16 clock cycles, the SPI is automatically placed in write mode.

Fast Attack

The fast attack feature, accessible via the SPI, allows the gain to be reduced from its present gain setting by a predetermined step size. Four different attenuation step sizes are available. The truth table for fast attack is shown in Table 5.

Table 5. SPI 2-Bit Attenuation Step Size Truth Table

FA1	FA0	Step Size (dB)
0	0	2
0	1	4
1	0	8
1	1	16

SPI fast attack mode is controlled by the FA pin. A logic high on the FA pin results in an attenuation that is selected by Bits[FA1:FA0] in the SPI register.

UP/DOWN INTERFACE

The GS1 and GS0 pins control the up/down gain step function. Gain is increased by a clock pulse on the UPDN_CLK pin (rising and falling edges) when the UPDN_DAT pin is high. Gain is decreased by a clock pulse on the UPDN_CLK pin when the UPDN_DAT pin is low.

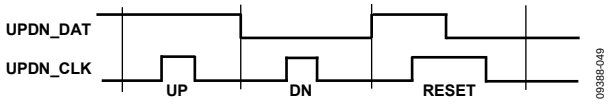


Figure 50. Up/Down Timing

Reset is detected by a rising edge latching data having one polarity, with the falling edge latching the opposite polarity. Reset results in a minimum binary gain code of 111111.

The truth table for the gain step function is shown in Table 6. The step size is selectable using the GS1 and GS0 pins. The gain is limited by the top and bottom of the control range.

Table 6. Gain Step Size Control Truth Table

GS1	GS0	Step Size (dB)
0	0	0.5
0	1	1
1	0	2
1	1	4

Truth Table

Table 7. Gain Code vs. Voltage Gain Lookup Table

6-Bit Binary Gain Code	Voltage Gain (dB)	6-Bit Binary Gain Code	Voltage Gain (dB)
000000	20	100000	4
000001	19.5	100001	3.5
000010	19	100010	3
000011	18.5	100011	2.5
000100	18	100100	2
000101	17.5	100101	1.5
000110	17	100110	1
000111	16.5	100111	0.5
001000	16	101000	0
001001	15.5	101001	−0.5
001010	15	101010	−1
001011	14.5	101011	−1.5
001100	14	101100	−2
001101	13.5	101101	−2.5
001110	13	101110	−3
001111	12.5	101111	−3.5
010000	12	110000	−4
010001	11.5	110001	−4.5
010010	11	110010	−5
010011	10.5	110011	−5.5
010100	10	110100	−6
010101	9.5	110101	−6.5
010110	9	110110	−7
010111	8.5	110111	−7.5
011000	8	111000	−8
011001	7.5	111001	−8.5
011010	7	111010	−9
011011	6.5	111011	−9.5
011100	6	111100	−10
011101	5.5	111101	−10.5
011110	5	111110	−11
011111	4.5	111111	−11.5

LOGIC TIMING

To write to the ADL5201, refer to the timing shown in Figure 51. The write mode uses a 16-bit serial word on the SDIO pin. The R/W bit of the word must be low to write Bits[D5:D0], which are the binary weighted codes for the attenuation level (0 = minimum attenuation, 63 = maximum attenuation). The FA0 and FA1 bits control the fast attack step size. The DNC bits are nonfunctional, do not care bits.

Reading the ADL5201 SPI register requires the following two steps:

1. Set the R/W bit high using a 16-bit word and the timing shown in Figure 51. All other bits are ignored when the R/W bit is high.
2. The SDIO is used as an output during the next sequence. The written pattern is serially clocked out on SDIO using 16 clocks and the timing shown in Figure 51. The R/W bit automatically returns low to the write state following the read sequence.

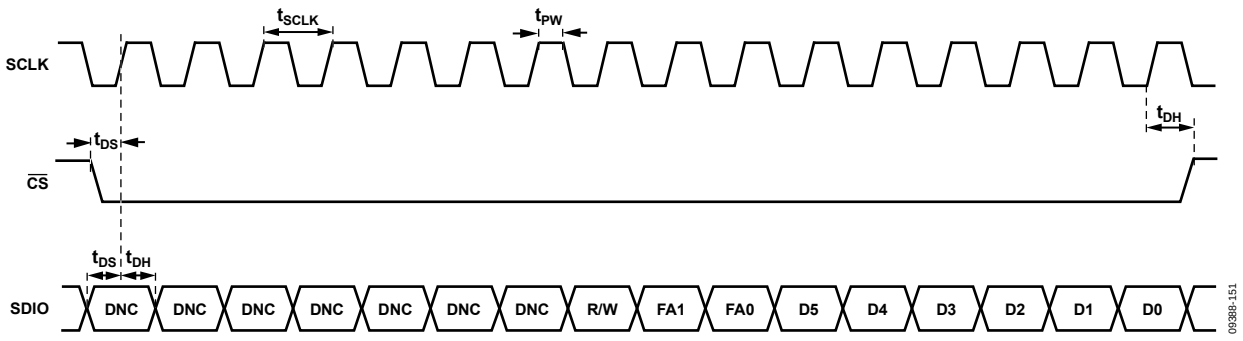


Figure 51. SPI Interface Read/Write Mode Timing Diagram

CIRCUIT DESCRIPTION

BASIC STRUCTURE

The ADL5201 is a differential variable gain amplifier (VGA) consisting of a 150 Ω digitally controlled passive attenuator followed by a highly linear transconductance amplifier with feedback.

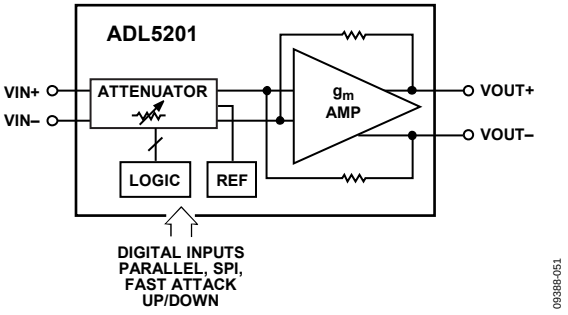


Figure 52. Simplified Schematic

INPUT SYSTEM

The dc voltage level at the input of the amplifier is set by an independent internal voltage reference circuit to approximately 1.6 V. The reference is not accessible and cannot be adjusted.

The amplifier can be powered down by pulling the PWUP pin low. In power-down mode, the total current is reduced to 7 mA (typical). The dc level at the input remains at approximately 1.6 V, regardless of the state of the PWUP pin.

OUTPUT AMPLIFIER

Gain of the output amplifier is set to be 22 dB when driving a 150 Ω load. The input and output resistance of this amplifier is set to 150 Ω in matched condition. If the load or the source resistance is not equal to 150 Ω, the following equations can be used to determine the resulting gain and input/output resistances.

$$Voltage\ Gain = A_V = 0.09 \times (2000)//R_L$$

$$R_{IN} = (2000 + R_L)/(1 + 0.09 \times R_L)$$

$$S21\ (Gain) = 2 \times R_{IN}/(R_{IN} + R_S) \times A_V$$

$$R_{OUT} = (2000 + R_S)/(1 + 0.09 \times R_S)$$

Note that the at maximum attenuation setting, R_S, as seen by the output amplifier, is the output resistance of the attenuator, which is 150 Ω. However, at the minimum attenuation setting, R_S is the source resistance that is connected to the input of the part.

The dc current to the outputs of each amplifier is supplied through two external chokes. The inductance of the chokes and the resistance of the load, in parallel with the output resistance of the device, add a low frequency pole to the response. The parasitic capacitance of the chokes adds to the output capacitance of the part. This total capacitance, in parallel with the load and output resistance, sets the high frequency pole of the device. Generally, the larger the inductance of the choke, the higher its parasitic capacitance. Therefore, this trade-off must be considered when the value and type of the choke are selected. For an operation frequency of 15 MHz to 700 MHz driving a 150 Ω load, 1 µH chokes with an SRF of 160 MHz or higher are recommended (such as the 0805LS-102XJBB from Coilcraft). If higher value chokes are used, a 4 MHz zero, due to the internal ac-coupled feedback, causes an increase in S21 of up to 6 dB at frequencies below 4 MHz.

The supply current of the amplifier consists of about 35 mA through the VPOS pin and 50 mA through the two chokes combined. The latter increases with temperature at approximately 2.5 mA per 10°C. The total choke current increases to 75 mA for high performance mode. The amplifier has two output pins for each polarity, and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. To minimize the parasitic capacitance, a good practice is to avoid any ground or power plane under this routing region and under the chokes.

GAIN CONTROL

The gain can be adjusted using the parallel control interface, the serial peripheral interface, or the gain up/down interface. In general, the gain step size is 0.5 dB, but larger sizes can be programmed using the various interfaces, as described in the Digital Interface Overview section. The amplifier has a maximum gain of +20 dB (Code 0) to −11.5 dB (Code 63).

The noise figure of the amplifier is approximately 7.5 dB at the maximum gain setting, and it increases as the gain is reduced. The increase in noise figure is equal to the reduction in gain. The linearity of the part, measured at the output, is first-order independent of the gain setting. From −4 dB to +20 dB gain, the OIP3 is approximately 50 dBm into a 150 Ω load at 200 MHz (0 dBm per tone). At gain settings below −4 dB, the OIP3 drops to approximately 40 dBm.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 53 shows the basic connections for operating the ADL5201. A voltage between 4.5 V and 5.5 V should be applied to the VPOS pins. Each supply pin should be decoupled with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF, placed as close as possible to the device.

The outputs of the ADL5201 must be pulled up to the positive supply with 1 µH RF chokes. The differential outputs are biased to the positive supply and require ac coupling capacitors, preferably 0.1 µF. Similarly, the input pins are at bias voltages of about 1.6 V above ground and should be ac-coupled, as well. The ac coupling capacitors and the RF chokes are the principle limitations for operation at low frequencies.

The digital pins (mode control pins, associated SPI and parallel gain control pins, PM, and PWUP) operate on a voltage of 3.3 V.

To enable the ADL5201, the PWUP pin must be pulled high (1.4 V ≤ PWUP ≤ 3.3 V). Taking PWUP low puts the ADL5201 in sleep mode, reducing current consumption to approximately 7 mA at ambient temperature.

ADC DRIVING

The ADL5201 is a highly linear, variable gain amplifier that is optimized for ADC interfacing. The output IMDs and noise floor remain constant throughout the 31.5 dB gain range. This is a valuable feature in a variable gain receiver, where it is desirable to maintain a constant instantaneous dynamic range as the receiver range is modified. The output noise is 15 nV/√Hz, which is compatible with 14- or 16-bit ADCs. The two-tone IMDs are usually greater than −100 dB for −1 dBm into 150 Ω or 2 V p-p output. The 150 Ω output impedance makes the task of designing a filter for the high input impedance ADCs more straightforward.

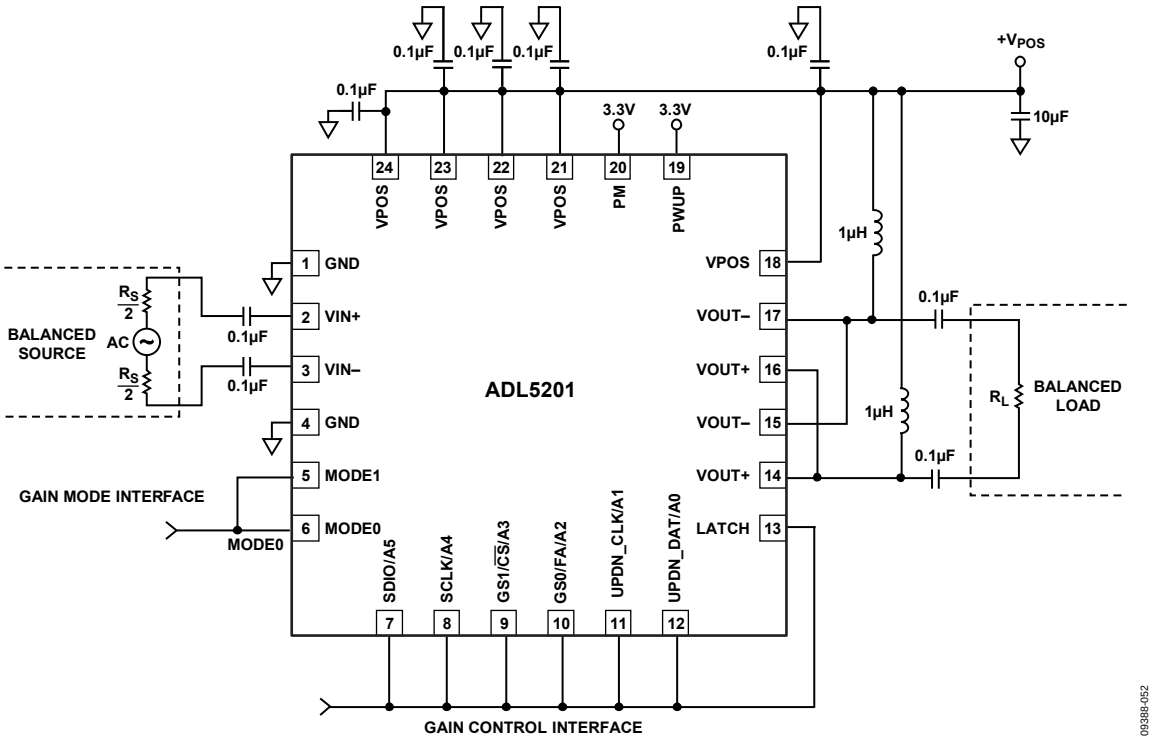


Figure 53. Basic Connections

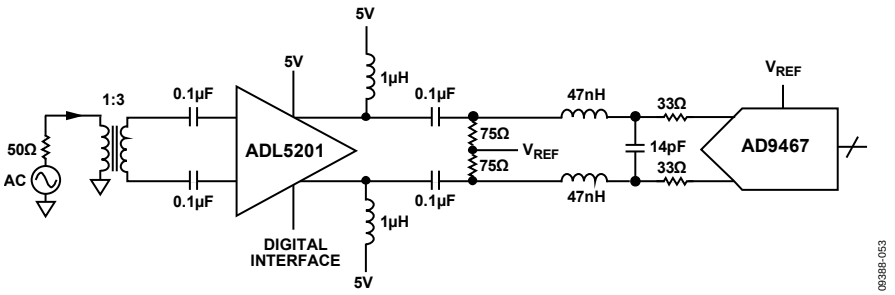


Figure 54. Wideband ADC Interfacing Example Featuring the ADL5201 and the AD9467

Figure 54 shows the ADL5201 driving a two-pole, 100 MHz, low-pass filter into the AD9467. The AD9467 is a 16-bit, 200 MSPS to 250 MSPS ADC with a buffered wideband input that presents a 530 Ω differential input impedance and requires a 2 V or 2.5 V input swing to reach full scale. For optimum performance, the ADL5201 should be driven differentially, using an impedance transformer or input balun.

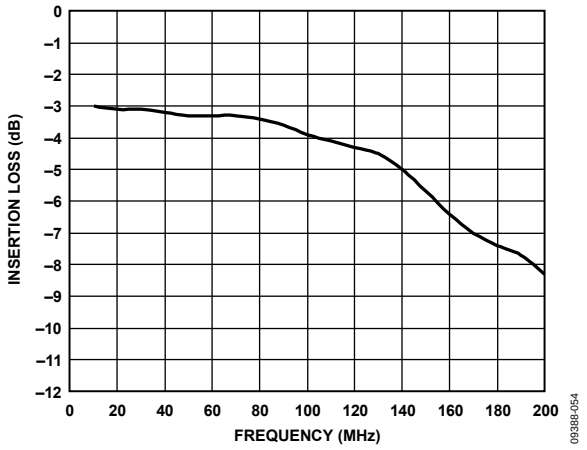


Figure 55. Measured Frequency Response of the Wideband ADC Interface Shown in Figure 54

Figure 54 uses a 1:3 impedance transformer to provide the 150 Ω input impedance of the ADL5201 with a matched input. The outputs of the ADL5201 are biased through the two 1 µH inductors, and the two 0.1 µF capacitors on the outputs decouple the 5 V inductor voltage from the input common-mode voltage of the AD9467. The two 75 Ω resistors provide the 150 Ω load to the ADL5201, whose gain is load dependent. The 47 nH inductors and 14 pF capacitor constitute the (100 MHz − 1 dB) low-pass filter. The two 33 Ω isolation resistors suppress any switching currents from the ADC input sample-and-hold circuitry. The circuit depicted in Figure 54 provides variable gain, isolation, filtering, and source matching for the AD9467. By using this circuit with the ADL5201 in a gain of 20 dB (maximum gain), an SNR of 68 dB and an SFDR performance of 88 dBc are achieved at 100 MHz, as shown in Figure 56.

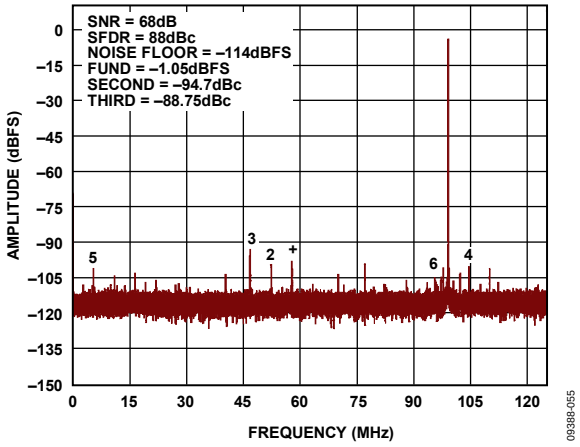


Figure 56. Measured Single-Tone Performance of the Circuit Shown in Figure 54 for a 100 MHz Input Signal

The two-tone 100 MHz IMDs of two 1 V p-p signals have an SFDR of greater than 91 dBc, as shown in Figure 57.

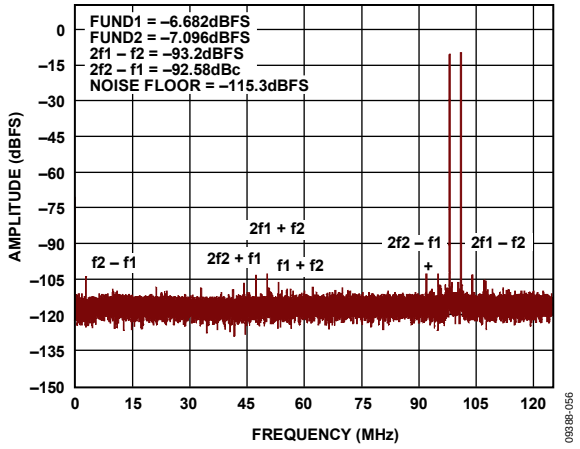


Figure 57. Measured Two-Tone Performance of the Circuit Shown in Figure 54 for a 100 MHz Input Signal

An alternative narrow-band approach is presented in Figure 58. By designing a narrow band-pass antialiasing filter between the ADL5201 and the target ADC, the output noise of the ADL5201 outside the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves by several decibels (dB) when a reasonable order antialiasing filter is included. In this example, a low loss 1:3 input transformer is used to match the 150 Ω balanced input of the ADL5201 to a 50 Ω unbalanced source, resulting in minimum insertion loss at the input.

Figure 58 shows the ADL5201 optimized for driving some of the popular unbuffered Analog Devices ADCs: the AD9246, AD9640, and AD6655. Table 8 includes antialiasing filter component recommendations for popular IF sampling center frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure that the ADC input looks like a real resistance at the target center frequency. In addition, the L6 inductor shorts the ADC inputs at dc, which introduces a zero into the transfer function. The ac coupling capacitors and the bias chokes introduce additional zeros into the transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 8 provides initial suggestions for prototyping purposes. Some empirical optimization may be needed to help compensate for actual PCB parasitics.

LAYOUT CONSIDERATIONS

The ADL5201 amplifier has two output pins for each polarity, and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. To minimize the parasitic capacitance, a good practice is to avoid any ground or power planes under this routing region and under the chokes.

If the common-mode load capacitance including the capacitance of the trace is > 2 pF, use parasitic suppressing resistors at the device output pins. The resistors should be placed in the output traces just after the crossover connections. Use 5 Ω series resistors (Size 0402) to adequately de-Q the output system without a significant decrease in gain.

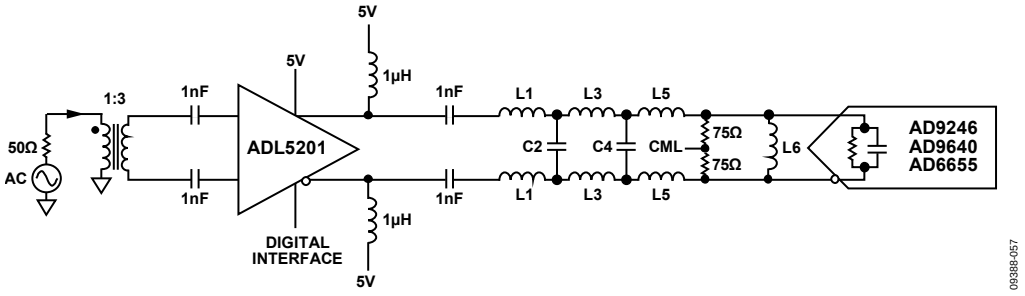


Figure 58. Narrow-Band IF Sampling Solution for Unbuffered ADC Applications

Table 8. Interface Filter Recommendations for Various IF Sampling Center Frequencies

Center Frequency (MHz)	1 dB Bandwidth (MHz)	L1 (nH)	C2 (pF)	L3 (nH)	C4 (pF)	L5 (nH)	L6 (nH)
96	27	68	15	220	15	68	150
140	31	47	11	150	11	47	82
170	25	39	10	120	10	47	51
211	40	30	7	100	7.5	30	43

EVALUATION BOARD

The ADL5201 evaluation board is available with software to program the variable gain control. It is a 4-layer board with a split ground plane for analog and digital sections. Special care is taken to place the power decoupling capacitors close to the device pins. The board is designed for easy single-ended (through a Mini-Circuits TC3-1T+ RF transformer) or differential configuration for each channel.

EVALUATION BOARD CONTROL SOFTWARE

The ADL5201 evaluation board is configured with a USB-friendly interface to program the gain of the ADL5201. The software graphical user interface (see Figure 59) lets users select a particular gain mode and gain level to write to the device. The GUI also allows users to read back data from the SDIO pin, showing the currently programmed gain setting. The software setup files can be downloaded from the ADL5201 product page at www.analog.com.

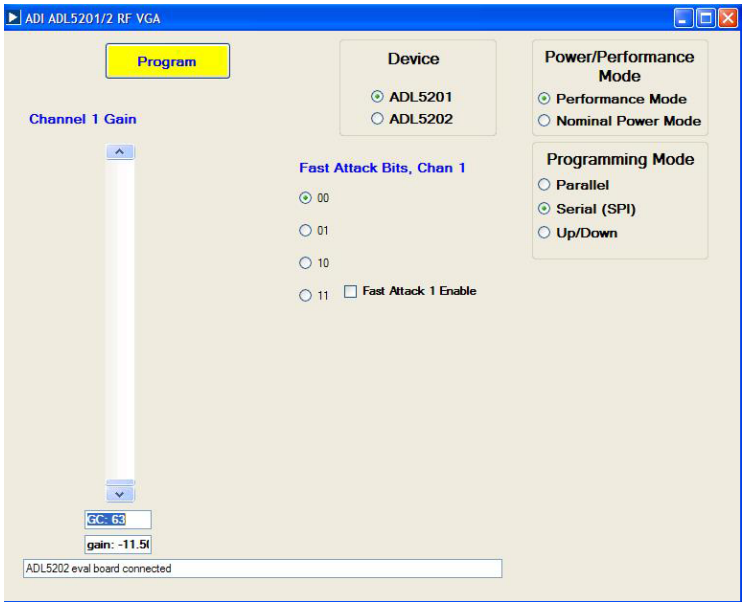


Figure 59. Evaluation Board Control Software

SCHEMATICS AND ARTWORK

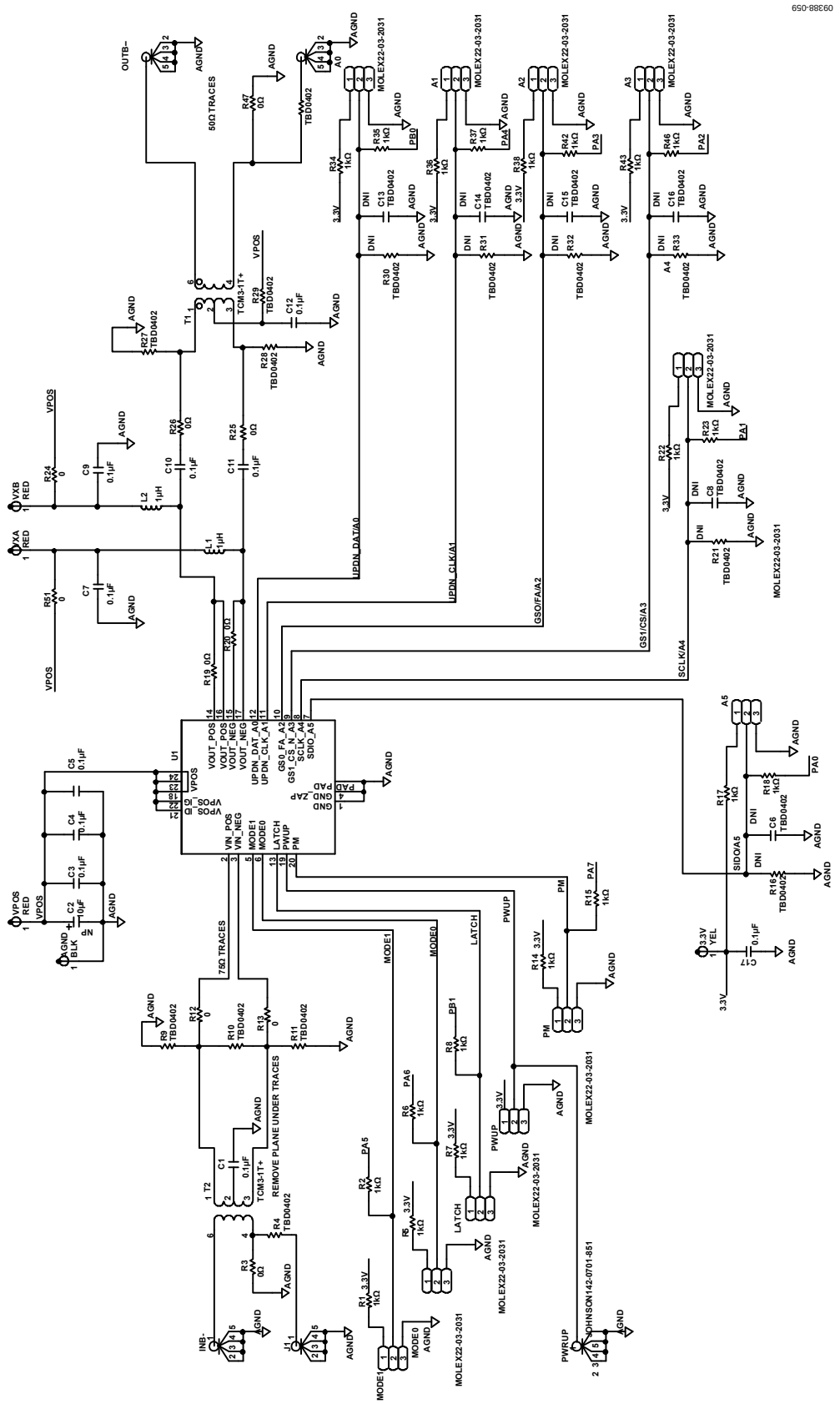


Figure 60. Evaluation Board Schematic

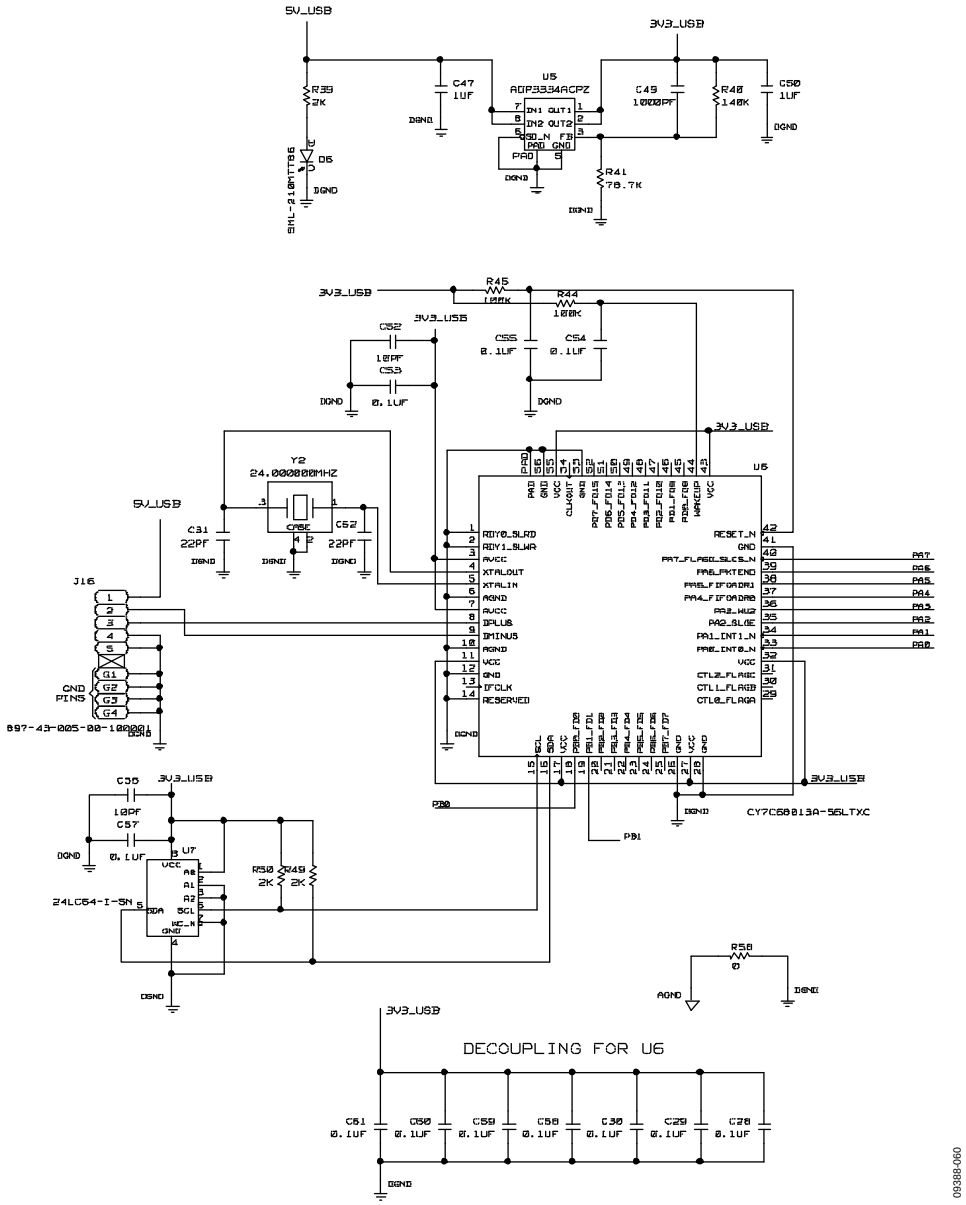


Figure 61. Logic Schematic

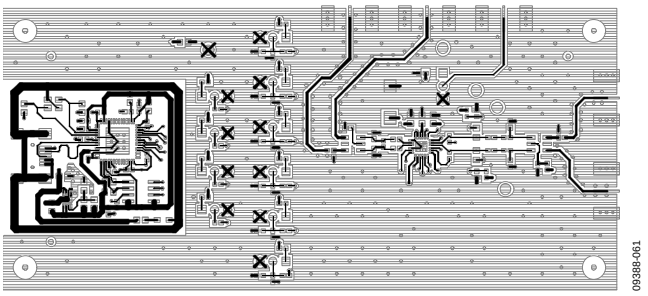


Figure 62. Top Layer

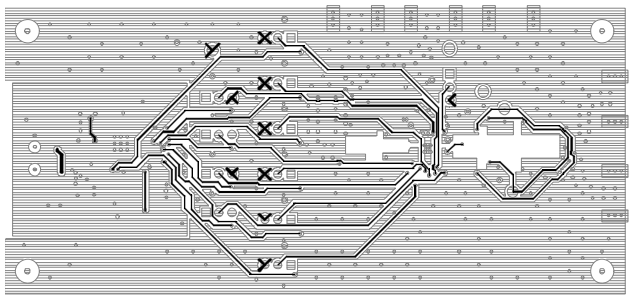


Figure 63. Bottom Layer

EVALUATION BOARD CONFIGURATION OPTIONS

Configuration Options for the Main Section

Table 9. Bill of Materials for Main Section

Components	Function	Default Conditions
C2 to C5, C7, C9, C17	Power supply decoupling. Nominal supply decoupling consists of a 0.1 µF capacitor to ground.	C2 = 10 µF (Size C7343) C3 to C5, C7, C9, C17 = 0.1 µF (Size 0603)
U1	Device under test.	Installed
INB– T2 J1 C1 R3, R4, R9 to R13	Input interface. INB– is the RF input. T2 is a 3:1 impedance ratio balun used to transform a single ended 50 Ω signal into a 150 Ω balanced differential signal. The input can be configured for a differential by removing R3 and installing a 0 Ω jumper at R4. C1 provides dc blocking. R12 and R13 are placeholders and can be replaced with blocking capacitors when driving the ADL5201 from a fully differential source. R3 grounds one side of the differential drive interface for single-ended applications. R9, R10, and R11 are provided for generic placement of matching components.	T2 = TC3-1T+ (Mini-Circuits) C1 = 0.1 µF (Size 0402) R3, R12, R13 = 0 Ω (Size 0402) R4, R9 to R11 = open INB– (SMA connector) installed J1 (SMA connector) installed
T1 C10 to C12 L1, L2 R19, R20, R24 to R28, R47, R48, R51 OUTB+, OUTB–	Output interface. T1 is a 3:1 impedance ratio balun used to transform a 150 Ω balanced differential signal to a 50 Ω singled-end signal. C10 and C11 are dc blocks. L1 and L2 provide dc bias to the open-collector output. R24 to R28 are provided for the generic placement of matching components. R47 grounds one side of the differential output interface for single-ended applications.	T1 = TC3-1T+ (Mini-Circuits) C10 to C12 = 0.1 µF (Size 0402) R19, R20, R24 to R26, R47, R51 = 0 Ω (Size 0402) R27, R28, R48 = open L1, L2 = 1 µH (Size 0805) OUTB+ (SMA connector) installed OUTB– (SMA connector) installed
PWUP, PWRUP	Power-up interface. The ADL5201 is powered up by applying a logic high (1.4 V ≤ PWUPA/B ≤ 3.3 V) to PWUP from an external source or by installing a shunt between Pin 1 and Pin 2 of the 3-pin header, PWUP.	PWUP (3-pin header) installed PWRUP (SMA connector) installed
A0 to A5 LATCH PM MODE0, MODE1 R1, R2, R5 to R8, R14 to R18, R21 to R23, R30 to R38, R42, R43, R46 C6, C8, C13 to C16	Gain control interface. All of the gain control functions are fully controlled via the USB microcontroller using the supplied software. Three-pin headers allow for manual operation of the gain control, if desired. R1, R2, R5 to R8, R14, R15, R17, R18, R22, R23, R34 to R38, R42, R43, and R46 isolate the digital control pins from the microcontroller and provide current limiting. The R16, R21, and R30 to R33 resistors and the C6, C8, and C13 to C16 capacitors allow for the generic placement of filter components.	A0 to A5 (3-pin header) installed LATCH (3-pin header) installed MODE0 (3-pin header) installed MODE1 (3-pin header) installed PM (3-pin header) installed R1, R2, R5 to R8, R14, R15, R17, R18, R22, R23, R34 to R38, R42, R43, R46 = 1 kΩ (Size 0402) R16, R21, R30 to R33 = open C6, C8, C13 to C16 = open

Configuration Options for the USB Section

Table 10. Bill of Materials for USB Section

Components	Default Conditions
C31, C62	22 pF (Size 0603)
C49	1000 pF (Size 0603)
C28 to C30, C53 to C55, C57 to C61	0.1 µF (Size 0402)
C47, C50	1 µF (Size 0402)
C52, C56	10 pF (Size 0402)
D6	Green LED (Panasonic LNJ308G8TRA)
J16	USB SMT connector (Hirose Electric UX60A-MB-5ST 240-0003-4)
R39, R49, R50	2 kΩ (Size 0603)
R41	78.7 kΩ (Size 0603)
R40	140 kΩ (Size 0603)
R44, R45	100 kΩ (Size 0603)
R58	0 Ω (Size 0603)
U6	USB microcontroller (Cypress CY7C68013A-56LFXC)
U7	64 kbit EEPROM (Microchip 24LC64-I/SN)
U5	Low dropout regulator (Analog Devices ADP3334ACPZ)
Y2	24 MHz crystal oscillator (AEL Crystals X24M000000S244)

OUTLINE DIMENSIONS

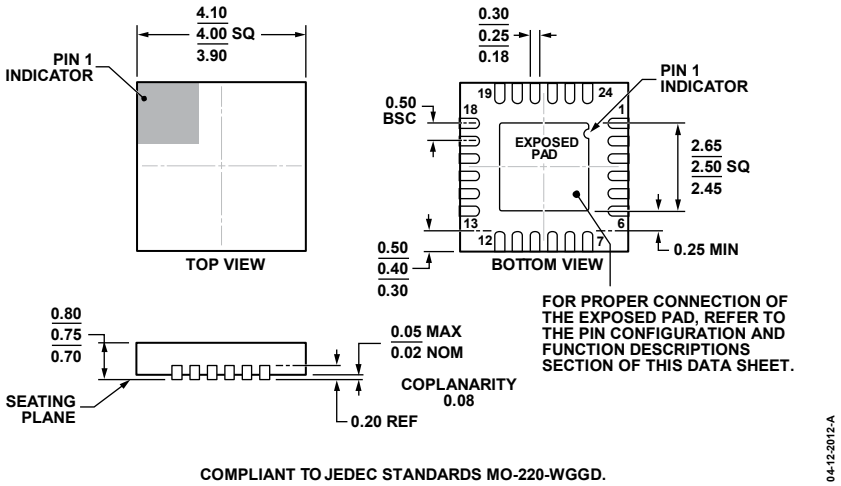


Figure 64. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5201ACPZ-R7	−40°C to +85°C	24 Lead LFCSP_WQ, 7″ Tape and Reel	CP-24-7
ADL5201-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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