±450°/Sec Precision Angular Rate Sensor

Data Sheet

ADIS16136

FEATURES

- Digital gyroscope system, ±450°/sec measurement range
- In-run bias stability, 4°/hour
- Autonomous operation and data collection
  - No external configuration commands required
  - Start-up time: 180 ms; sleep mode recovery: 2.5 ms
- Factory calibrated sensitivity and bias
- Calibration temperature range: −40°C to +70°C
- SPI-compatible serial interface
- Wide bandwidth: 380 Hz
- Embedded temperature sensor
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Digital filters: Bartlett FIR, average/decimation
  - Internal sample rate: up to 2048 SPS
  - Digital I/O: data ready, alarm indicator, general-purpose
  - Alarms for condition monitoring
  - Sleep mode for power management
  - Enable external sample clock input: up to 2048 Hz
- Single-supply operation: 4.75 V to 5.25 V
- 2000 *g* shock survivability
- Operating temperature range: −40°C to +85°C

APPLICATIONS

- Precision instrumentation
- Platform stabilization and control
- Industrial vehicle navigation
- Downhole instrumentation
- Robotics

GENERAL DESCRIPTION

The ADIS16136 *i*Sensor® is a high performance, digital gyroscope sensing system that operates autonomously and requires no user configuration to produce accurate rate sensing data. It provides performance advantages with its low noise density, wide bandwidth, and excellent in-run bias stability, which enable applications such as platform control, navigation, robotics, and medical instrumentation.

This sensor system combines industry leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes the entire sensor signal chain for sensitivity and bias over a temperature range of −40°C to +70°C. As a result, each ADIS16136 has its own unique correction formulas to produce accurate measurements upon installation. For some systems, the factory calibration eliminates the need for system level calibration and greatly simplifies it for others.

The ADIS16136 provides data at rates of up to 2048 SPS and offers an averaging/decimation filter structure for optimizing noise/bandwidth trade-offs. The serial peripheral interface (SPI) and user register structure provide easy access to configuration controls and calibrated sensor data for embedded processor platforms.

The 36 mm × 44 mm × 14 mm package provides four holes for simple mechanical attachment, using M2 (or 2-56 standard size) machine screws along with a standard 24-pin, dual row, 1 mm pitch connector that supports electrical attachment to a printed circuit board (PCB) or cable system.

FUNCTIONAL BLOCK DIAGRAM

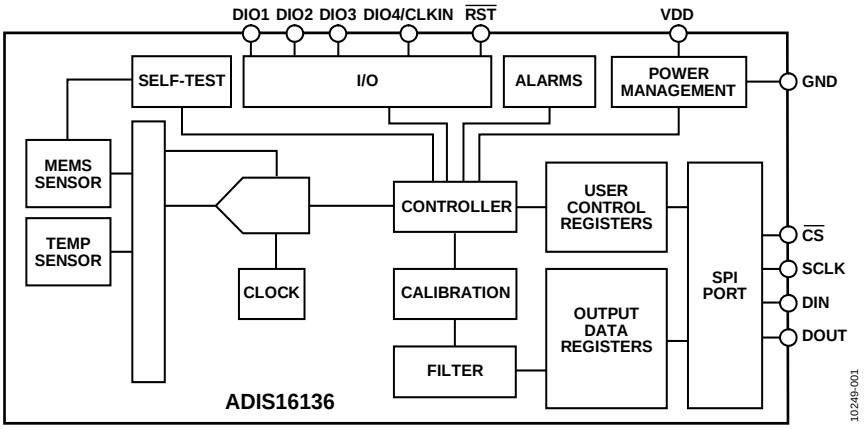

Figure 1.

Rev. A

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Timing Specifications ... 4
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Theory of Operation ... 8
Reading Sensor Data ... 8
Output Data Registers ... 9
Device Configuration ... 9
User Registers ... 10
Digital Processing Configuration ... 11
Internal Sample Rate ... 11
Input Clock Configuration ... 11
Digital Filtering ... 11
Averaging/Decimation Filter ... 12
Calibration ... 13
Automatic Bias Correction (Autonull) ... 13
Manual Bias Correction ... 13
Alarms ... 14
Static Alarm Use ... 14
Dynamic Alarm Use ... 14
Alarm Reporting ... 14
System Controls ... 15
Global Commands ... 15
Memory Management ... 15
General-Purpose Input/Output ... 15
Self Test ... 16
Power Management ... 16
Status ... 16
Product Identification ... 17
Applications Information ... 18
Power Supply Considerations ... 18
Prototype Interface Board ... 18
Installation Tips ... 19
Packaging and Ordering Information ... 20
Outline Dimensions ... 20
Ordering Guide ... 20

REVISION HISTORY

11/11—Rev. 0 to Rev. A

Changes to Functional Times Parameters, Table 1 ... 3

10/11—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, VDD = 5.0 V, angular rate = 0°/sec, dynamic range = ±450°/sec, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±450		±480	°/sec
Initial Sensitivity	GYRO_OUT, GYRO_OUT2 (24 bits)		7.139×10^{-5}		°/sec/LSB
Initial Sensitivity Tolerance				±1	%
Sensitivity Temperature Coefficient	−40°C ≤ T_A ≤ +70°C, 1 σ		±35		ppm/°C
Nonlinearity	Best fit straight line, ±400°/sec		±0.05		% of FS
Initial Bias Error	1 σ		±0.15		°/sec
Bias Temperature Coefficient	−40°C ≤ T_A ≤ +70°C, 1 σ		±0.00125		°/sec/°C
In-Run Bias Stability	25°C, SMPL_PRD = 0x000F		4		°/hr
Angular Random Walk	1 σ, 25°C		0.167		°/√hr
Linear Acceleration Effect on Bias	1 σ		0.017		°/sec/*g*
Bias Voltage Sensitivity	VDD = 4.75 V to 5.25 V, 1 σ		±0.08		°/sec/V
Misalignment	Axis-to-frame (package)		±1.0		Degrees
Output Noise	No filtering		0.11		°/sec rms
Rate Noise Density	f = 25 Hz, no filtering		0.00357		°/sec/√Hz rms
3 dB Bandwidth			380		Hz
Sensor Resonant Frequency		15.5	17.5	20	kHz
LOGIC INPUTS[1]					
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
Logic 1 Input Current, I_{IH}	V_{IH} = 3.3 V		±0.2	±1	µA
Logic 0 Input Current, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$			40	60	µA
$\overline{RST}$ Pin			80		µA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[1]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
FLASH MEMORY	Endurance[2]	10,000			Cycles
Data Retention[2]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[3]	Time until data is available				
Power-On Start-Up Time			245		ms
Reset Recovery Time			128		ms
Sleep Mode Recovery Time			2.5		ms
Flash Memory Update			72		ms
Flash Memory Self Test			21		ms
Automatic Sensor Self Test Time	SMPL_PRD ≠ 0x0000		110		ms
CONVERSION RATE		680[4]		2048	kSPS
Clock Accuracy	SMPL_PRD = 0x000F			±3	%
Sync Input Clock	SMPL_PRD = 0x0000	680[4]		2048	kHz
POWER SUPPLY	Operating voltage range, VDD	4.75	5.0	5.25	V
Power Supply Current	SMPL_PRD = 0x001F		120		mA
	Sleep mode		1.4		mA

[1] The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.
[2] JEDEC Standard 22, Method A117. Endurance measured at −40°C, +25°C, +85°C, and +125°C.
[3] These times do not include thermal settling and internal filter response times, which may affect overall accuracy.
[4] The sync input clock and internal sampling clock function below the specified minimum value, at reduced performance levels.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = 5 V, unless otherwise noted.

Table 2.

		Normal Mode			
Parameter	**Description**	**Min[1]**	**Typ**	**Max**	**Unit**
f_{SCLK}	Serial clock	0.01		2.5	MHz
t_{STALL}	Stall period between data, see Figure 3	15			µs
$t_{READRATE}$	Read rate	25			µs
$t_{\overline{CS}}$	Chip select to clock edge	48.8			ns
t_{DAV}	DOUT valid after SCLK edge			25	ns
t_{DSU}	DIN setup time before SCLK rising edge	24.4			ns
t_{DHD}	DIN hold time after SCLK rising edge	48.8			ns
t_{SCLKR}, t_{SCLKF}	SCLK rise and fall times		5	12.5	ns
t_{DR}, t_{DF}	DOUT rise and fall times		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns
t_1	Input sync positive pulse width	5			µs
t_2	Input sync to data ready output		300		µs
t_3	Input sync period	488			µs
t_x	Input sync low time	100			µs

[1] Guaranteed by design and characterization but not tested in production.

Timing Diagrams

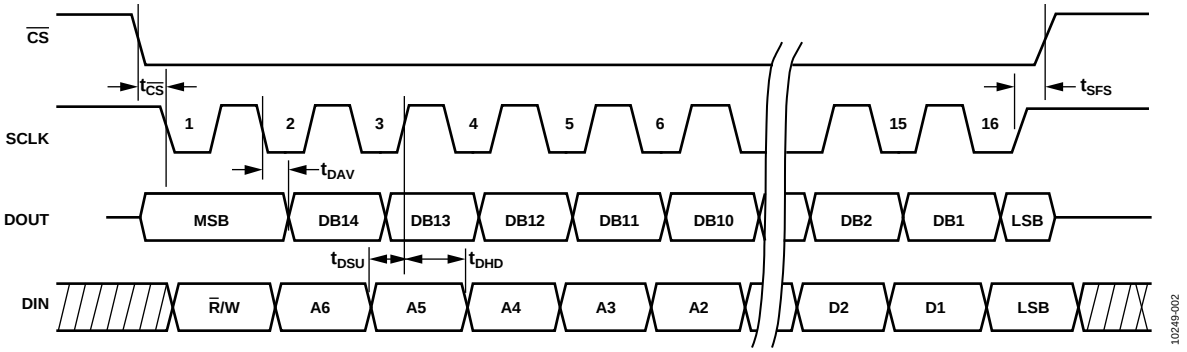

Figure 2. SPI Timing and Sequence

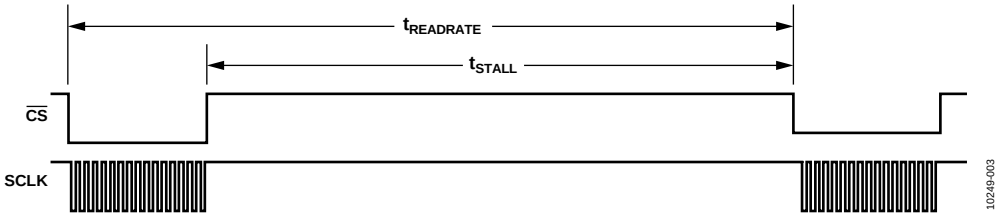

Figure 3. Stall Time and Data Rate

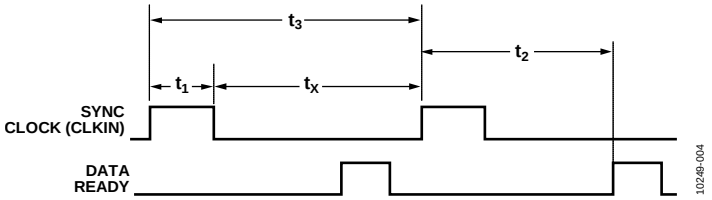

Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +6.0 V
Digital Input Voltage to GND	−0.3 V to +5.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C[1, 2]

[1] Extended exposure to temperatures outside the specified temperature range of −40°C to +105°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the devices within the specified operating range of −40°C to +105°C.
[2] Although the device is capable of withstanding short term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
24-Lead Module with Connector Interface	15.7	1.48	25 g

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

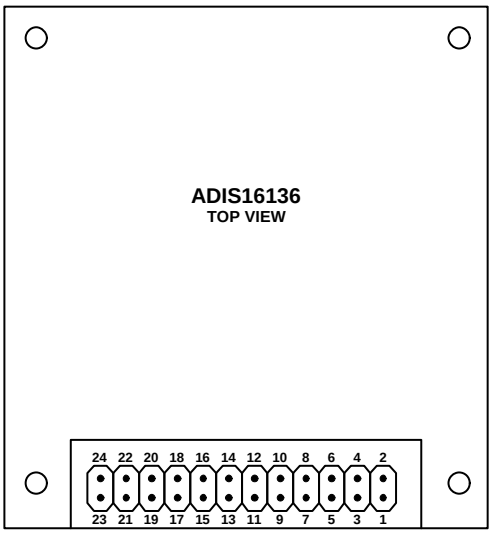

Figure 5. Mating Connector Pin Assignments

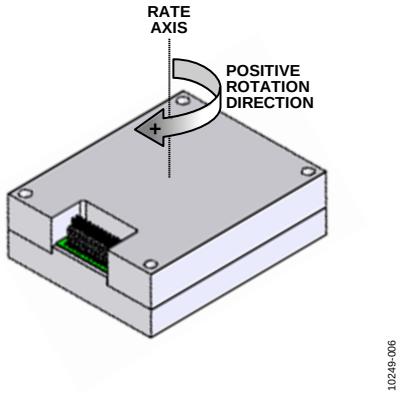

Figure 6. Axial Orientation (Bottom Side Facing Up)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DIO3	I/O	Configurable Digital Input/Output.
2	DIO4/CLKIN	I	Configurable Digital Input/Output/Clock Input (SMPL_PRD = 0x0000).
3	SCLK	I	SPI Serial Clock.
4	DOUT	O	SPI Data Output. Clocks output on SCLK falling edge.
5	DIN	I	SPI Data Input. Clocks input on SCLK rising edge.
6	$\overline{CS}$	I	SPI Chip Select.
7	DIO1	I/O	Configurable Digital Input/Output.
8	$\overline{RST}$	I	Reset.
9	DIO2	I/O	Configurable Digital Input/Output.
10, 11, 12	VDD	S	Power Supply.
13, 14, 15	GND	S	Power Ground.
16 to 24	DNC	N/A	Do Not Connect. Do not connect to these pins.

[1] I/O is input/output, I is input, O is output, S is supply, N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

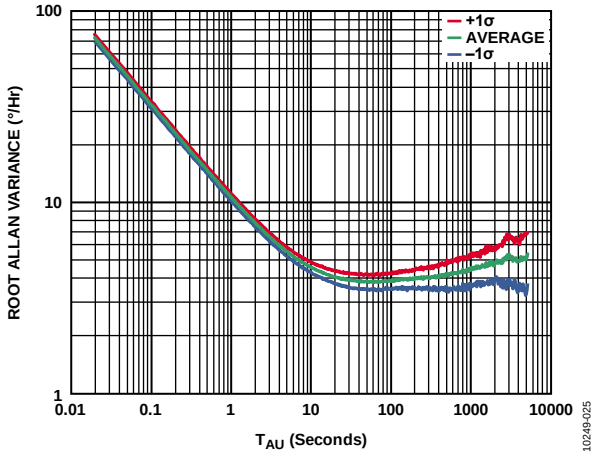

Figure 7. Root Allan Variance, 5 V, 25°C, 1024 SPS

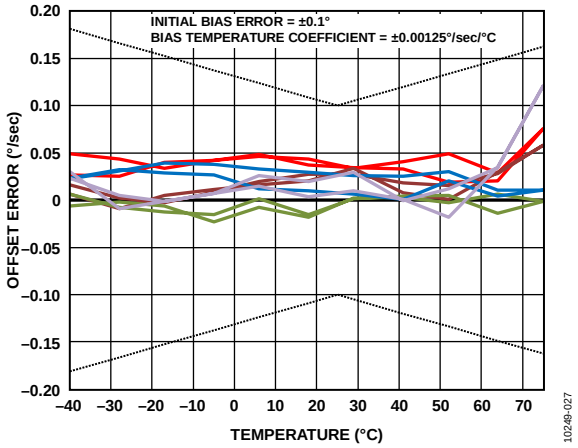

Figure 9. Offset (Bias) Error vs. Temperature, –40°C to +75°C to –40°C

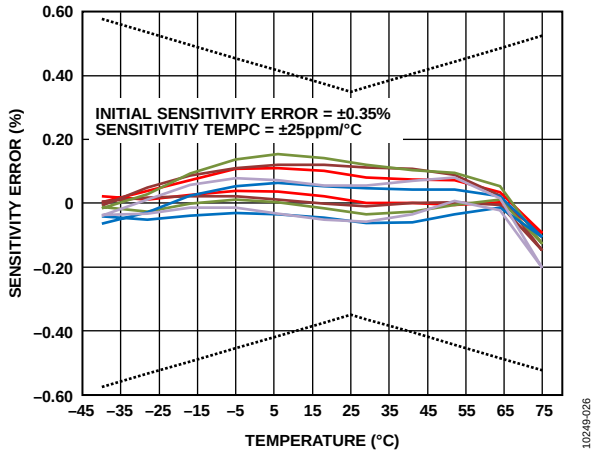

Figure 8. Sensitivity Error vs. Temperature, –40°C to +75°C to –40°C

THEORY OF OPERATION

The ADIS16136 is an autonomous system that requires no user initialization. As soon as it has a valid power supply, it initializes and starts sampling, processing, and loading sensor data into the output registers. After each sample cycle concludes, DIO1 pulses high. The SPI interface enables simple integration with many embedded processor platforms, as shown in Figure 10 (electrical connection) and Table 6 (processor pin names and functions).

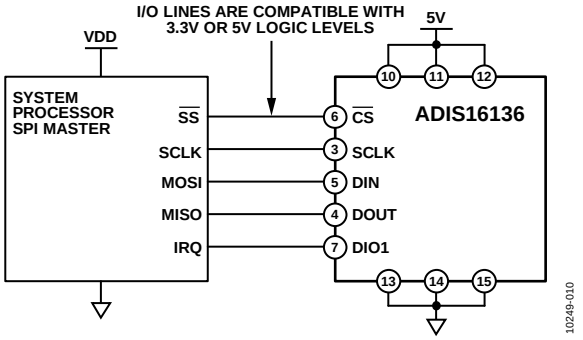

Figure 10. Electrical Connection Diagram

Table 6. Generic Master Processor Pin Names and Functions

Pin Name	Function
$\overline{SS}$	Slave select
IRQ	Interrupt request
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

The ADIS16136 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 13. Table 7 provides a list of the most common settings that require attention to initialize a processor serial port for the ADIS16136 SPI interface.

Table 7. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16136 operates as a slave
SCLK Rate ≤ 2 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence
16-Bit Mode	Shift register/data length

READING SENSOR DATA

A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 13. Then, the register contents follow on DOUT during the second sequence. Figure 11 includes three single register reads in succession. In this example, the process starts with Pin 5, DIN = 0x0600, to request the contents of the GYRO_OUT register and follows with 0x0400 to request the contents of the GYRO_OUT2 register and with 0x0200 to request the contents of the TEMP_OUT register. Full duplex operation enables processors to use the same 16-bit SPI cycle to read data from DOUT while requesting the next set of data on the DIN pin. Figure 12 provides an example of the four SPI signals when reading GYRO_OUT in a repeating pattern.

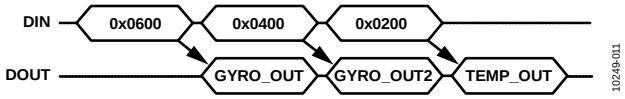

Figure 11. SPI Read Example

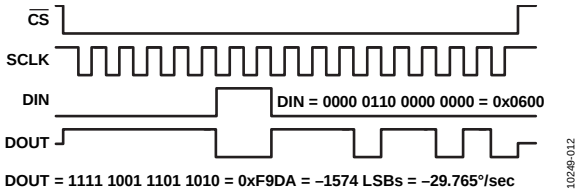

Figure 12. SPI Read Example, Second 16-Bit Sequence

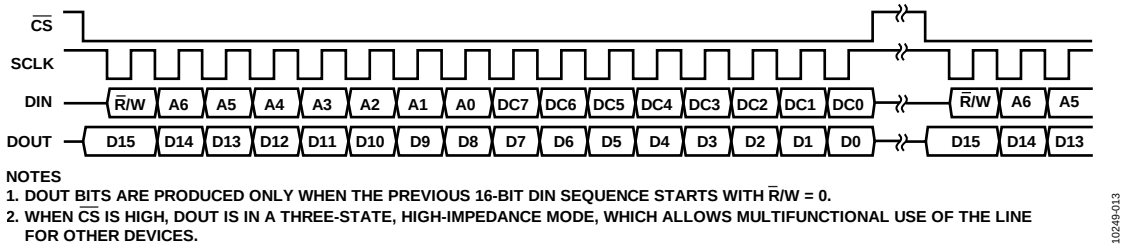

Figure 13. SPI Communication Bit Sequence

OUTPUT DATA REGISTERS

Table 8. Output Data Register Formats

Register	Address	Measurement
TEMP_OUT	0x02	Internal temperature
GYRO_OUT2	0x04	Gyroscope, lower 16 bits
GYRO_OUT	0x06	Gyroscope, upper 16 bits

Rotation Rate (Gyroscope)

GYRO_OUT is the primary register for gyroscope output data and uses 16-bit twos complement format for its data. Table 9 provides the numerical format, and Table 10 provides several examples for converting digital data into °/sec.

Table 9. GYRO_OUT Bit Descriptions

Bits	Description
[15:0]	Gyroscope data; twos complement, 0.018275°/sec per LSB, 0°/sec = 0x0000

Table 10. GYRO_OUT, Twos Complement Format

Rotation Rate	Decimal	Hex	Binary
+450°/sec	+24,623	0x602F	0110 0000 0010 1111
+0.03655°/sec	+2	0x0002	0000 0000 0000 0010
+0.018275°/sec	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
−0.018275°/sec	−1	0xFFFF	1111 1111 1111 1111
−0.03655°/sec	−2	0xFFFE	1111 1111 1111 1110
−450°/sec	−24,623	0x9FD1	1001 1111 1101 0001

The GYRO_OUT2 register (see Table 11) captures the bit growth associated with the decimation and FIR filters that are shown in Figure 18 using a MSB justified format. The bit growth starts with the MSB (GYRO_OUT2[15]), is equal to the decimation rate setting in DEC_RATE[4:0] (see Table 18), and grows in the LSB direction as the decimation rate increases. See Figure 14 for more details.

Table 11. GYRO_OUT2 Bit Descriptions

Bits	Description
[15:0]	Rotation rate data; resolution enhancement bits

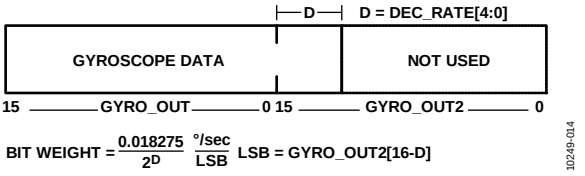

Figure 14. Gyroscope Output Format, DEC_RATE[4:0] > 0

Internal Temperature

The TEMP_OUT register (see Table 12) provides an internal temperature measurement that can be useful for observing relative temperature changes in the environment. Table 13 provides several coding examples for converting the 16-bit twos complement number into units for temperature (°C).

Table 12. TEMP_OUT Bit Descriptions

Bits	Description
[15:0]	Temperature data; twos complement, 0.010697°C per LSB, 0°C = 0x0000

Table 13. Temperature, Twos Complement Format

Temperature	Decimal	Hex	Binary
+85°C	+7946	0x1F0A	0001 1111 0000 1010
+0.021394°C	+2	0x0002	0000 0000 0000 0010
+0.010697°C	+1	0x0001	0000 0000 0000 0001
0°C	0	0x0000	0000 0000 0000 0000
−0.010697 °C	−1	0xFFFF	1111 1111 1111 1111
−0.021394°C	−2	0xFFFE	1111 1111 1111 1110
−40°C	−3739	0xF165	1111 0001 0110 0101

DEVICE CONFIGURATION

The control registers listed in Table 14 provide a variety of user configuration options. The SPI provides access to these registers, one byte at a time, using the bit assignments shown in Figure 13. Each register has 16 bits, wherein Bits[7:0] represent the lower address and Bits[15:8] represent the upper address.

Figure 15 provides an example of writing 0x03 to Address 0x22 (DEC_RATE[7:0]), using Pin 5, DIN = 0xA203. This example reduces the sample rate by a factor of 8 (see Table 16).

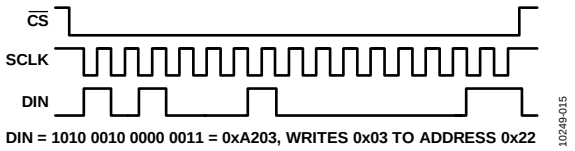

Figure 15. SPI Sequence for Setting the Decimate Rate to 8 (DIN = 0xA203)

Dual Memory Structure

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, set GLOB_CMD[3] = 1 (DIN = 0xA808) to backup these settings in the nonvolatile flash memory. The flash back up process requires a valid power supply level for the entire 72 ms process time. Table 14 provides a user register memory map that includes a column of flash backup information. A "yes" in this column indicates that a register has a mirror location in flash and, when backed up properly, automatically restores itself during startup or after a reset. Figure 16 provides a diagram of the dual memory structure that is used to manage operation and store critical user settings.

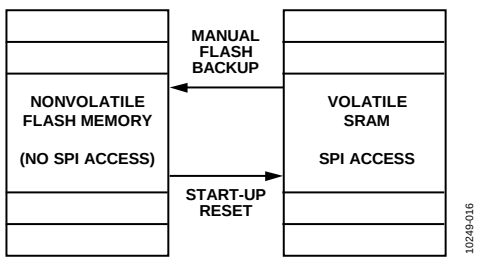

Figure 16. SRAM and Flash Memory Diagram

USER REGISTERS

Table 14. User Register Memory Map

Name	R/W	Flash Backup	Address[1]	Default	Register Description	Bit Descriptions
FLASH_CNT	R	Yes	0x00	N/A[2]	Flash memory write count	Table 30
TEMP_OUT	R	No	0x02	N/A[2]	Output, temperature (internal)	Table 12
GYRO_OUT2	R	No	0x04	N/A[2]	Output, gyroscope, lower 16 bits	Table 11
GYRO_OUT	R	No	0x06	N/A[2]	Output, gyroscope, upper 16 bits	Table 9
GYRO_OFF2	R/W	Yes	0x08	0x0000	Gyroscope bias correction, lower 16 bits	Table 21
GYRO_OFF	R/W	Yes	0x0A	0x0000	Gyroscope bias correction, upper 16 bits	Table 20
Reserved	N/A[2]	N/A[2]	0x0C to 0x0F	N/A[2]	Reserved	
ALM_MAG1	R/W	Yes	0x10	0x0000	Alarm 1 trigger setting	Table 23
ALM_MAG2	R/W	Yes	0x12	0x0000	Alarm 2 trigger setting	Table 24
ALM_SMPL1	R/W	Yes	0x14	0x0000	Alarm 1 sample period	Table 25
ALM_SMPL2	R/W	Yes	0x16	0x0000	Alarm 2 sample period	Table 25
ALM_CTRL	R/W	Yes	0x18	0x0000	Alarm configuration	Table 26
GPIO_CTRL	R/W	Yes	0x1A	0x0000	Auxiliary digital input/output control	Table 32
MSC_CTRL	R/W	Yes	0x1C	0x0006	Miscellaneous control: data ready, self test	Table 31
SMPL_PRD	R/W	Yes	0x1E	0x001F	Internal sample period (rate) control	Table 16
AVG_CNT	R/W	Yes	0x20	0x0000	Digital filter control	Table 17
DEC_RATE	R/W	Yes	0x22	0x0000	Decimation rate setting	Table 18
SLP_CTRL	W	Yes	0x24	0x0000	Sleep mode control	Table 33
DIAG_STAT	R	No	0x26	0x0000	System status	Table 34
GLOB_CMD	W	No	0x28	0x0000	System command	Table 29
Reserved	N/A[2]	N/A[2]	0x2A to 0x31	N/A[2]	Reserved	
LOT_ID1	R	Yes	0x32	N/A[2]	Lot Identification Code 1	Table 36
LOT_ID2	R	Yes	0x34	N/A[2]	Lot Identification Code 2	Table 36
LOT_ID3	R	Yes	0x36	N/A[2]	Lot Identification Code 3	Table 36
PROD_ID	R	Yes	0x38	0x3F08	Product ID, binary number for 16,136	Table 35
SERIAL_NUM	R	Yes	0x3A	N/A[2]	Serial number	Table 37

[1] Each register contains two bytes. The address column in this table only offers the address of the lower byte. Add 1 to it to calculate the address of the upper byte.
[2] N/A means not applicable.

DIGITAL PROCESSING CONFIGURATION

Figure 18 provides a block diagram for the sampling and digital filter stages inside the ADIS16136. Table 15 provides a summary of registers for sample rate and filter control.

Table 15. Digital Processing Registers

Register Name	Address	Description
SMPL_PRD	0x1E	Sample rate control
AVG_CNT	0x20	Digital filtering and range control
DEC_RATE	0x22	Decimation rate setting

INTERNAL SAMPLE RATE

The SMPL_PRD register in Table 16 provides a programmable control for the internal sample rate. Use the following formula to calculate the decimal number for the code to write into this register:

$$SMPL_PRD = \frac{32{,}768}{(f_S)} - 1;\ f_S \le 2048\ \text{SPS}$$

The factory default setting for SMPL_PRD sets the internal sample rate to a rate of 1024 SPS; the minimum setting for the SMPL_PRD register is 0x000F, which results in an internal sample rate of 2048 SPS.

Table 16. SMPL_PRD Bit Descriptions

Bits	Description (Default = 0x001F)
[15:0]	Clock setting bits; sets f_S in Figure 18

INPUT CLOCK CONFIGURATION

Set SMPL_PRD = 0x0000 (DIN = 0x9F00, then DIN = 0x9E00) to disable the internal clock and enable DIO4/CLKIN as a clock input pin.

DIGITAL FILTERING

The AVG_CNT register (see Table 17) provides user controls for the low-pass filter. This filter contains two cascaded averaging filters that provide a Bartlett window FIR filter response (see Figure 18). For example, set AVG_CNT[7:0] = 0x04 (DIN = 0xA004) to set each stage to 16 taps. When used with the default sample rate of 1024 SPS, this establishes a −3 dB bandwidth of approximately 24 Hz for this filter.

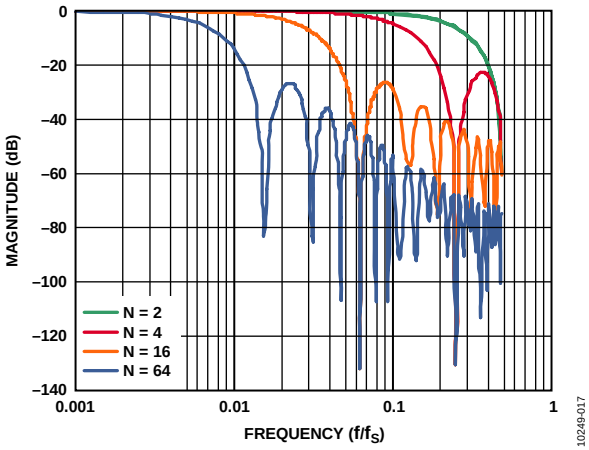

Figure 17. Bartlett Window FIR Filter Frequency Response

Table 17. AVG_CNT Bit Descriptions

Bits	Description (Default = 0x0000)
[15:3]	Don't care
[2:0]	Binary; B variable in Figure 18; maximum = 110 (6)

AVERAGING/DECIMATION FILTER

The DEC_RATE register (see Table 18) provides user control for the final filter stage (see Figure 18), which averages and decimates the output data. For systems that value lower sample rates, this filter stage provides an opportunity to lower the sample rate while maintaining optimal bias stability performance. The −3 dB bandwidth of this filter stage is approximately one half the output data rate. For example, set DEC_RATE[7:0] = 0x04 (DIN = 0xA204) to reduce the sample rate by a factor of 16.

When the factory default 1024 SPS sample rate is used, this decimation setting reduces the output data rate to 64 SPS and the sensor bandwidth to approximately 32 Hz.

Table 18. DEC_RATE Bit Descriptions

Bits	Description (Default = 0x0000)
[15:5]	Don't care
[4:0]	Binary; D variable in Figure 18; maximum = 10000 (16)

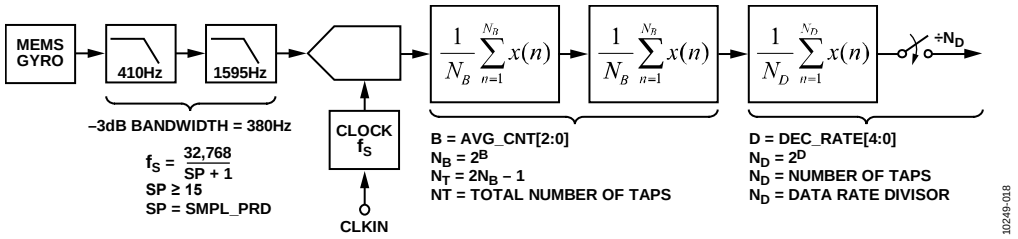

Figure 18. Sampling and Frequency Response Block Diagram

CALIBRATION

The ADIS16136 factory calibration produces correction formulas for the gyroscope and programs them into the flash memory. Table 19 contains a list of user control registers that provide an opportunity for user optimization after installation. Figure 19 illustrates the summing function of the sensor's offset correction register.

Table 19. Registers for User Calibration

Register	Address	Description
GYRO_OFF2	0x08	Gyroscope bias
GYRO_OFF	0x0A	Gyroscope bias
GLOB_CMD	0x28	Bias correction command

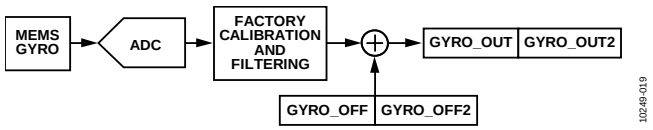

Figure 19. Gyroscope Bias Calibration User Controls

The factory calibration addresses initial and temperature dependent bias errors in the gyroscopes, but some environmental conditions, such as temperature cycling and mechanical stress on the package, can cause bias shifts in MEMS gyroscope structures. For systems that value absolute bias accuracy, there are two options for optimizing absolute bias accuracy: autonull and manual correction.

AUTOMATIC BIAS CORRECTION (AUTONULL)

Set GLOB_CMD[0] = 1 (DIN = 0xA801) to start the automatic bias correction (ABC) function, which uses the following internal sequence to calibrate each gyroscope for bias error:

1. Wait for a complete output data cycle to complete, which includes the entire average and decimation time in DEC_RATE.
2. Read the output registers of the gyroscope.
3. Multiply the measurement by −1 to change its polarity.
4. Write the final value into the offset registers.
5. Update the flash memory.

The Allan variance curve shown in Figure 7 provides a trade-off between bias accuracy and averaging time. The DEC_RATE register provides a user control for averaging time when using the ABC function. Set DEC_RATE[7:0] = 0x10 (DIN = 0xA210), which sets the decimation rate to 65,536 (2^{16}) and provides an averaging time of 64 seconds (65,536 ÷ 1024 SPS) for this function. Next, set GLOB_CMD[0] = 1 (DIN = 0xA801), and keep the platform stable for at least 65 seconds while the gyroscope bias data accumulates.

After this completes, the ADIS16136 automatically updates the flash memory. When the ABC function starts, the SPI is not active. The only way to interrupt the ABC function is to remove power or initiate a hardware reset using the $\overline{\text{RST}}$ pin. When using DEC_RATE = 0x0010, the 1 σ accuracy for this correction is approximately 0.001°/sec for the gyroscope correction factor. See Table 29 for more information on GLOB_CMD.

MANUAL BIAS CORRECTION

The GYRO_OFF and GYRO_OFF2 registers (see Table 20 and Table 21) provide a bias adjustment function for the output of each sensor. GYRO_OFF has the same format as GYRO_OUT, and GYRO_OFF2 has the same format as GYRO_OUT2.

Table 20. GYRO_OFF Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Gyroscope offset correction; twos complement, 0.018275°/sec per LSB

Table 21. GYRO_OFF2 Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Gyroscope offset correction, finer resolution; uses same format as GYRO_OUT2 (see Table 11)

Restoring Factory Calibration

Set GLOB_CMD[1] = 1 (DIN = 0xA802) to execute the factory calibration restore function. This function resets each user calibration register to 0x0000, resets all sensor data to 0, and automatically updates the flash memory within 72 ms. See Table 29 for more information on GLOB_CMD.

ALARMS

The alarm function provides monitoring for two independent conditions. Table 22 contains a list of registers that provide configuration and control inputs for the alarm function.

Table 22. Registers for Alarm Configuration

Register	Address	Description
ALM_MAG1	0x10	Alarm 1, trigger setting
ALM_MAG2	0x12	Alarm 2, trigger setting
ALM_SMPL1	0x14	Alarm 1, sample period
ALM_SMPL2	0x16	Alarm 2, sample period
ALM_CTRL	0x18	Alarm configuration

The ALM_CTRL register (see Table 26) provides data source selection (Bits[15:8]), static/dynamic setting for each alarm (Bits[7:6]), trigger polarity (Bits[5:4]), data source filtering (Bit 3), and an alarm indicator signal (Bits[2:0]).

STATIC ALARM USE

The static alarms setting compares the data source selection (ALM_CTRL[15:8]) with the values in the ALM_MAGx registers in Table 23 and Table 24. The data format in these registers matches the format of the data selection in ALM_CTRL[15:8]. ALM_CTRL[5:4] provide polarity settings. See Table 27 for a static alarm configuration example.

Table 23. ALM_MAG1 Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches format of the ALM_CTRL[11:8] selection

Table 24. ALM_MAG2 Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches for format of the ALM_CTRL[15:12] selection

DYNAMIC ALARM USE

The dynamic alarm setting monitors the data selection for a rate-of-change comparison. The rate of change is represented by the magnitude in the ALM_MAGx registers over the time represented by the number of samples in the ALM_SMPLx register (see Table 25). See Table 27 for a dynamic alarm configuration example.

Table 25. ALM_SMPL1, ALM_SMPL2 Bit Descriptions

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Binary, number of samples (both 0x00 and 0x01 = 1)

ALARM REPORTING

DIAG_STAT[9:8] provide error flags that indicate an alarm condition. ALM_CTRL[2:0] provide controls for a hardware indicator using DIO1 or DIO2.

Table 26. ALM_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Alarm 2 source selection 0000 = disable 0001 = GYRO_OUT (does not include GYRO_OUT2) 0010 = TEMP_OUT 0011 = DIAG_STAT
[11:8]	Alarm 1 source selection (same as Alarm 2)
7	Rate-of-change enable for Alarm 2 (1 = rate of change, 0 = static level)
6	Rate-of-change enable for Alarm 1 (1 = rate of change, 0 = static level)
5	Comparison polarity for Alarm 2 (1 specifies >ALM_MAG2, 0 specifies <ALM_MAG2)
4	Comparison polarity for Alarm 1 (1 specifies >ALM_MAG1, 0 specifies <ALM_MAG1)
3	Comparison data filter setting[1] (1 = Bartlett filter, 0 = no filtering)
2	Alarm output enable (1 = enabled, 0 = disabled)
1	Alarm output polarity (1 = active high, 0 = active low)
0	Alarm output line select (1 = DIO2, 0 = DIO1)

[1] Filtering applies to GYRO_OUT only.

Alarm Example

Table 27 offers an example that configures Alarm 1 to trigger when filtered GYRO_OUT data drops below 50°/sec and Alarm 2 to trigger when filtered GYRO_OUT data changes by more than 50°/sec over a 100 ms period, or 500°/sec^2. The filter setting helps reduce false triggers from noise and refine the accuracy of the trigger points. The ALM_SMPL2 setting of 102 samples provides a comparison period that is 99.6 ms for an internal sample rate of 1024 SPS. There is no need to program ALM_SMPL1 because Alarm 1 is a static alarm in this example.

Table 27. Alarm Configuration Example 1

DIN	Description
0x9911, 0x98AF	ALM_CTRL = 0x11AF Alarm 2: dynamic; ΔGYRO_OUT (Δtime, ALM_ SMPL2) > ALM_MAG2 Alarm 1: static; GYRO_OUT < ALM_MAG1 use filtered data source for comparison DIO2 output indicator, positive polarity
0x930A, 0x92AF	ALM_MAG2 = 0x0AAF, (+50°/sec)
0x910A, 0x90AF	ALM_MAG1 = 0x0AAF, (+50°/sec)
0x9666	ALM_SMPL2[7:0] = 0x66, (102 samples)

SYSTEM CONTROLS

The ADIS16136 provides a number of system level controls for managing its operation using the registers listed in Table 28.

Table 28. System Tool Registers

Register Name	Address	Description
GPIO_CTRL	0x1A	General-purpose I/O control
MSC_CTRL	0x1C	Self test, calibration, data ready
SLP_CTRL	0x24	Sleep mode control
DIAG_STAT	0x26	Error flags
GLOB_CMD	0x28	Single command functions
LOT_ID1	0x32	Lot Identification Code 1
LOT_ID2	0x34	Lot Identification Code 2
LOT_ID3	0x36	Lot Identification Code 3
PROD_ID	0x38	Product identification
SERIAL_NUM	0x3A	Serial number

GLOBAL COMMANDS

The GLOB_CMD register (see Table 29) provides trigger bits for several operations. Write 1 to the appropriate bit in GLOB_CMD to start a function. After the function completes, the bit restores to 0.

Software Reset

Set GLOB_CMD[7] = 1 (DIN = 0xA880) to reset the operation, which removes all data, initializes all registers from their flash settings, and starts data collection. This function provides a firmware alternative to the $\overline{\text{RST}}$ line (see Table 5, Pin 8).

Table 29. GLOB_CMD Bit Descriptions

Bits	Description (Default = 0x0000)	Execution Time[1]
[15:8]	Not used	N/A
7	Software reset	70 ms
[6:4]	Not used	N/A
3	Flash update	70 ms
2	Not used	N/A
1	Factory calibration restore	71 ms
0	Automatic bias correction	N/A[2]

[1] N/A in this column means not applicable.

[2] Execution time is based on SMPL_PRD and DEC_RATE settings. This starts at the next data ready pulse, restarts the decimation cycle, and then writes to the flash (70 ms) after completing a decimation cycle. With respect to Figure 18, the decimation cycle time = $N_D \div f_S$.

MEMORY MANAGEMENT

The data retention of the flash memory depends on the temperature, as shown in Figure 20. The FLASH_CNT register (see Table 30) provides a 16-bit counter that helps track the number of write cycles to the nonvolatile flash memory, which helps the user manage against the endurance rating. The flash updates every time any of the following bits are set to 1: GLOB_CMD[3], GLOB_CMD[1], and GLOB_ CMD[0].

Table 30. FLASH_CNT Bit Descriptions

Bits	Description)
[15:0]	Binary counter; number of flash updates

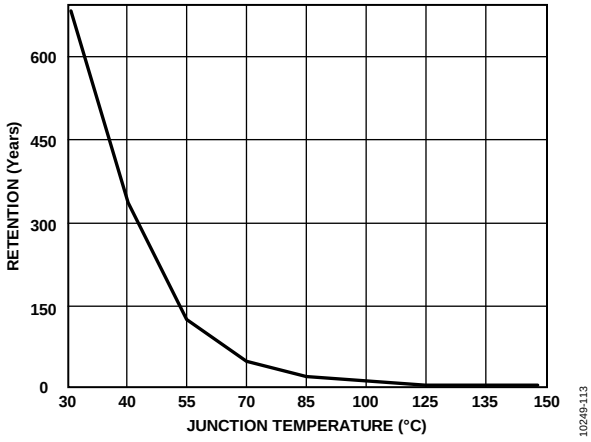

Figure 20. Flash Memory Retention

Checksum Test

Set MSC_CTRL[11] = 1 (DIN = 0x9D08) to perform a checksum verification of the internal program memory. This takes a summation of the internal program memory and compares it with the original summation value for the same locations (from factory configuration). Check the results in the DIAG_STAT register (see Table 34). DIAG_STAT[6] = 0 if the sum matches the correct value and 1 if it does not. Make sure that the power supply is within specification for the entire 21 ms that this function takes to complete.

GENERAL-PURPOSE INPUT/OUTPUT

There are four general-purpose I/O lines, DIO1, DIO2, DIO3, and DIO4/CLKIN that provide a number of useful functions. The MSC_CTRL[2:0] bits (see Table 31) control the data ready configuration and have the highest priority for setting either DIO1 or DIO2 (but not both). The ALM_CTRL[2:0] control bits (see Table 26) provide the alarm indicator configuration control and have the second highest priority for DIO1 or DIO2. When DIO1 and DIO2 are not in use as either data ready or alarm indicator signals, the GPIO_CTRL register (see Table 32) provides the control and data bits for them, together with the DIO3 and DIO4 lines.

Data Ready Input/Output Indicator

The factory default setting for MSC_CTRL[2:0] is 110, which configures DIO1 as a positive data ready indicator signal. A common option for this function is MSC_CTRL[2:0] = 100 (DIN = 0x9C04), which changes data ready to a negative polarity for processors that provide only negative triggered interrupt pins. The pulse width is between 100 µs and 200 µs over all conditions.

Example Input/Output Configuration

For example, set GPIO_CTRL[7:0] = 0x02 (DIN = 0x9A02) to set DIO1 as an input and DIO2 as an output. Then, set GPIO_CTRL[15:8] = 0x02 (DIN = 0x9B02) to set DIO2 in a high output state. Monitor DIO1 by reading GPIO_CTRL[8] (DIN = 0x1B00).

Table 31. MSC_CTRL Bit Descriptions

Bits	Description (Default = 0x0006)
[15:12]	Not used
11	Memory test (cleared upon completion) (1 = enabled, 0 = disabled)
10	Automatic self test (cleared upon completion) (1 = enabled, 0 = disabled)
9	Manual self test (1 = enabled, 0 = disabled)
8	Not used
7	Disable sensor compensation (1 = disable compensation, 0 = enable compensation)
[6:3]	Not used
2	Data ready enable (1 = enabled, 0 = disabled)
1	Data ready polarity (1 = active high, 0 = active low)
0	Data ready line select (1 = DIO2, 0 = DIO1)

Table 32. GPIO_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Don't care
11	General-Purpose I/O Line 4 (DIO4) data level
10	General-Purpose I/O Line 3 (DIO3) data level
9	General-Purpose I/O Line 2 (DIO2) data level
8	General-Purpose I/O Line 1 (DIO1) data level
[7:4]	Don't care
3	General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input)
2	General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input)
1	General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input)
0	General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input)

SELF TEST

The MSC_CTRL bits (see Table 31) provide a self test function that helps verify the mechanical integrity of the MEMS and signal processing circuit. When enabled, the self test applies an electrostatic force to the internal sensor element, which causes it to move in a manner that simulates its response to actual rotation. There are two self test options in the MSC_CTRL register: automatic and manual. Set MSC_CTRL[10] = 1 (DIN = 0x9D04) to run the automatic self test routine, which reports a pass/fail result in DIAG_STAT[5]. MSC_CTRL[10] resets itself to 0 after completing this routine. This process takes approximately 45 ms. Set MSC_CTRL[9] = 1 (DIN = 9D02) to manually activate the self test function, and set MSC_CTRL[9] = 0 (DIN = 9D00) to manually deactivate the self test function. Measure the output bias for each condition, calculate the difference between them, and compare it to the expected self test response shown in Table 1.

POWER MANAGEMENT

The SLP_CTRL register (see Table 33) provides two different sleep modes for system level management: normal and timed. Set SLP_CTRL[7:0] = 0xFF (DIN = 0xA4FF) to start normal sleep mode. To awaken the device from sleep mode, use one of the following options to restore normal operation: assert $\overline{CS}$ from high to low, pulse $\overline{RST}$ low, then high again, or cycle the power. Use SLP_CTRL[7:0] to put the device into sleep mode for a specified period. For example, SLP_CTRL[7:0] = 0x64 (DIN = 0xA464) puts the ADIS16136 to sleep for 50 sec.

Table 33. SLP_CTRL Bit Descriptions

Bits	Description
[15:8]	Not used
[7:0]	0xFF: normal sleep mode 0x00 to 0xFE: programmable sleep time bits; 0.5 sec/LSB

STATUS

The DIAG_STAT register (see Table 34) provides error flags for a number of functions. Each flag uses a 1 to indicate an error condition and a 0 to indicate a normal condition. Reading this register provides access to the status of each flag and resets all of the bits to 0 for monitoring future operation. If the error condition remains, the error flag returns to 1 at the conclusion of the next sample cycle. The SPI communication error flag in DIAG_STAT[3] indicates that the number of SCLKs in a SPI sequence did not equal a multiple of 16 SCLKs.

Table 34. DIAG_STAT Bit Descriptions

Bits	Description (Default = 0x0000)
[15:10]	Not used
9	Alarm 2 status (1 = active, 0 = inactive)
8	Alarm 1 status (1 = active, 0 = inactive)
7	Not used
6	Flash test, checksum flag (1 = fail, 0 = pass)
5	Self test diagnostic error flag (1 = fail, 0 = pass)
4	Sensor over range (1 = over range, 0 = normal)
3	SPI communication failure (1 = fail, 0 = pass)
2	Flash update failure (1 = fail, 0 = pass)
[1:0]	Not used

PRODUCT IDENTIFICATION

The PROD_ID register (see Table 35) contains 0x3F08, which is the hexadecimal equivalent of 16,136. The LOT_ID1, LOT_ID2, and LOT_ID3 registers (see Table 36) provide manufacturing lot information. The SERIAL_NUM register (see Table 37) contains a binary number that represents the serial number on the device label and is lot specific.

Table 35. PROD_ID Bit Descriptions

Bits	Description
[15:0]	Product identification = 0x3F08 (16,136)

Table 36. LOT_ID1, LOT_ID2, LOT_ID3 Bit Descriptions

Bits	Description
[15:0]	Lot identification, binary code

Table 37. SERIAL_NUM Bit Descriptions

Bits	Description
[15:14]	Not used
[13:0]	Serial number, 1 to 9999 (0x270F)

APPLICATIONS INFORMATION

POWER SUPPLY CONSIDERATIONS

The ADIS16136 includes 12 µF of capacitance across the VDD and GND pins. This capacitance presents low input impedance for power supplies that have fast rise times. The internal power regulator waits for a valid input supply voltage, and then goes through a start-up process that draws an elevated current (~400 mA) for approximately 1.5 ms. This transient current occurs approximately 125 ms after VDD reaches a valid level. This regulation circuit also provides a constant power load, which results in a load that has a negative dynamic resistance. Figure 21 provides a graphical relationship between the supply current and voltage for systems that need to account for this type of load when designing supply feedback loops.

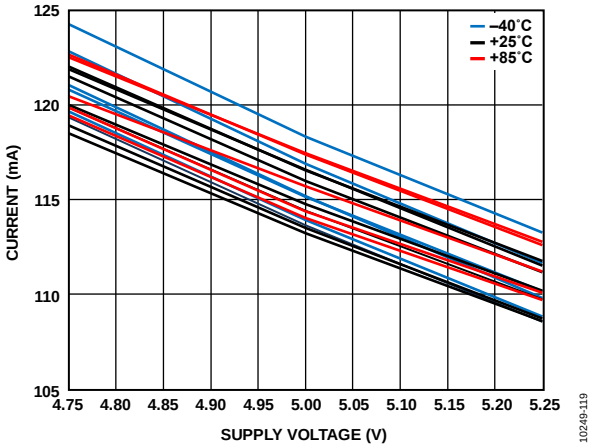

Figure 21. Supply Current vs Supply Voltage

PROTOTYPE INTERFACE BOARD

The ADIS16136/PCBZ includes one ADIS16136AMLZ, one interface PCB, and four M2 × 18 machine screws. The interface PCB provides larger connectors than the ADIS16136AMLZ for simpler prototyping, four tapped M2 holes for attachment of the ADIS16136AMLZ, and four holes (machine screw size M2.5 or No. 4) for mounting the ADIS16136AMLZ to a solid structure. J1 and J2 are dual row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon crimp connector) and 3M Part Number 3625/12 (ribbon cable).

Figure 22 provides the top level view of the interface board. Install the ADIS16136AMLZ onto this board using the silk pattern as an orientation guide. Figure 23 provides the pin assignments for J1 and J2. The pin descriptions match those listed in Table 5. The ADIS16136 does not require external capacitors for normal operation; therefore, the interface printed circuit board (PCB) does not use the C1 and C2 pads.

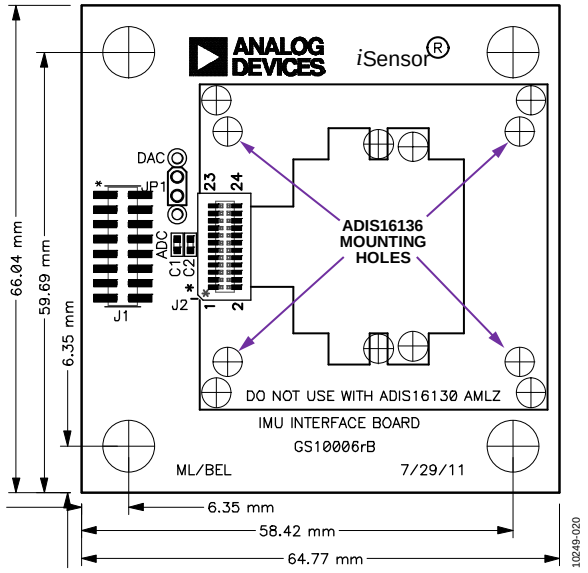

Figure 22. Physical Diagram for the ADIS16136/PCBZ

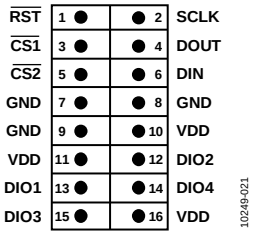

Figure 23. J1 Pin Assignments

INSTALLATION TIPS

Figure 24 and Figure 25 provide the mechanical design information used for the ADIS16136/PCBZ. Use these figures when implementing a connector-down approach, where the mating connector and the ADIS16136AMLZ are on the same surface. When designing a connector-up system, use the mounting holes shown in Figure 24 as a guide in designing the bulkhead mounting system, and use Figure 25 as a guide in developing the mating connector interface on a flexible circuit or other connector system. The mating connector pattern in Figure 25 assumes the use of the Samtec CLM-112-02 series of connectors.

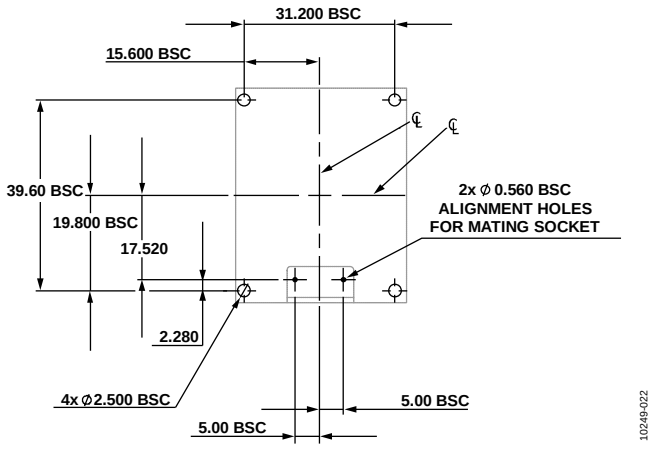

Figure 24. Suggested Mounting Hole Locations, Connector Down

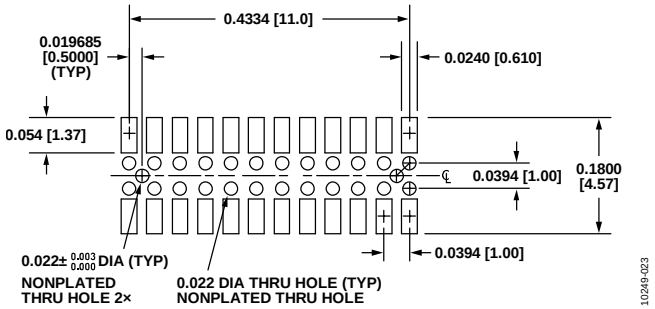

Figure 25. Suggested Layout and Mechanical Design for the Mating Connector

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

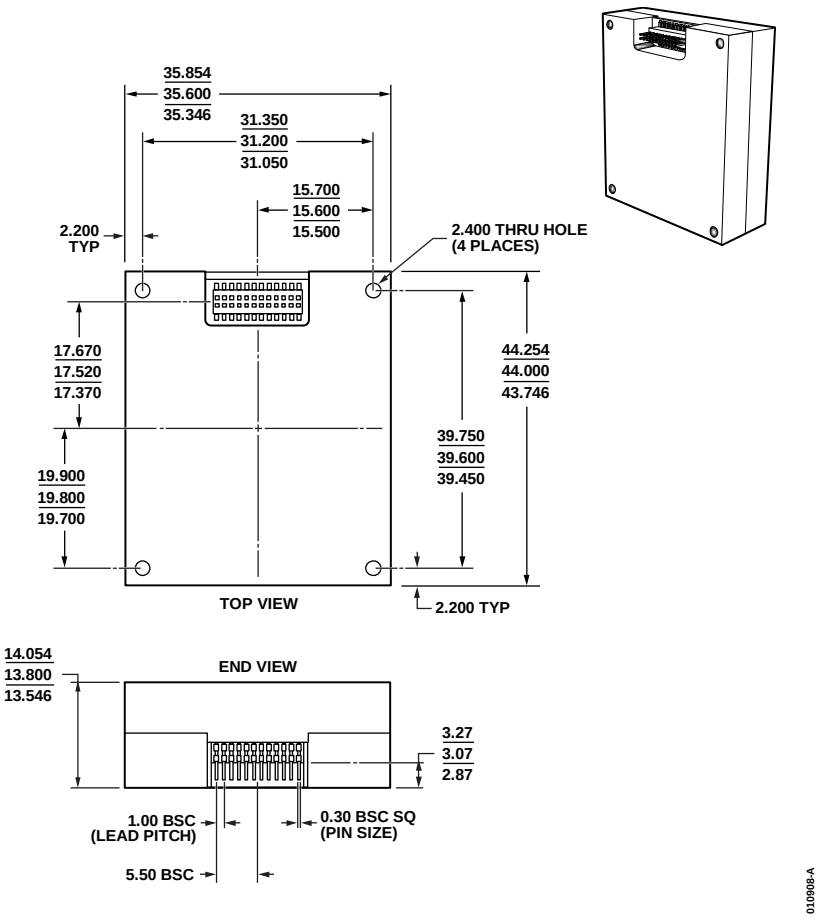

Figure 26. 24-Lead Module with Connector Interface
(ML-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADIS16136AMLZ	−40°C to +85°C	24-Lead Module with Connector Interface	ML-24-3
ADIS16136/PCBZ		Interface PCB	

[1] Z = RoHS Compliant Part.
[2] ADIS16136/PCBZ includes one ADIS16136AMLZ and one interface PCB. For more information about the interface PCB, see Figure 22.

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