

FEATURES

1.8 V to 5.5 V operation
Ultralow on resistance
 0.28 Ω typical at 5 V supply
 0.41 Ω maximum at 5 V supply
Excellent audio performance, ultralow distortion
 0.1 Ω typical
 0.15 Ω maximum R_{ON} flatness
High current carrying capability
 400 mA continuous
 600 mA peak current at 5 V supply
Rail-to-rail switching operation
Typical power consumption ($<0.1 \mu W$)

APPLICATIONS

Cellular phones
 PDAs
 MP3 players
 Power routing
 Battery-powered systems
 PCMCIA cards
 Modems
 Audio and video signal routing
 Communications systems

GENERAL DESCRIPTION

The **ADG884** is a low voltage CMOS device containing two independently selectable single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of 0.41 Ω over the full temperature range, making the part an ideal solution for applications that require minimal distortion through the switch. The **ADG884** also has the capability of carrying large amounts of current, typically 600 mA at 5 V operation.

The **ADG884** is available in a 10-ball, 2 mm $\times$ 1.5 mm WLCSP package, a 10-lead LFCSP_WD package, and a 10-lead MSOP package. These tiny packages make the **ADG884** the ideal solution for space-constrained applications.

When on, each switch conducts equally well in both directions and has an input signal range that extends to the supplies. The **ADG884** exhibits break-before-make switching action.

FUNCTIONAL BLOCK DIAGRAM

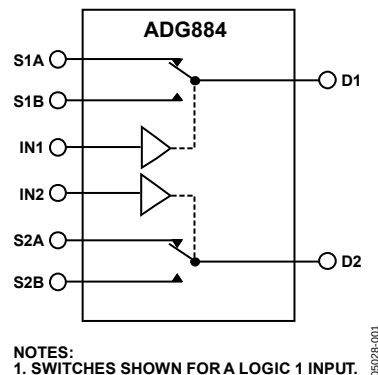


Figure 1.

PRODUCT HIGHLIGHTS

1. Single 1.8 V to 5.5 V operation.
2. High current handling capability (400 mA continuous current).
3. 1.8 V logic compatible.
4. Low THD + N (0.01% typical).
5. Tiny 2 mm $\times$ 1.5 mm WLCSP, 3 mm $\times$ 3 mm 10-lead LFCSP_WD, and 10-lead MSOP packages.

Rev. D

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TABLE OF CONTENTS

Features	1	ESD Caution.....	6
Applications.....	1	Pin Configurations and Function Descriptions	7
Functional Block Diagram	1	Typical Performance Characteristics	8
General Description	1	Test Circuits.....	11
Product Highlights	1	Terminology	13
Revision History	2	Outline Dimensions	14
Specifications.....	3	Ordering Guide	15
Absolute Maximum Ratings.....	6		

REVISION HISTORY

4/12—Rev. C to Rev. D

Added Exposed Pad Notation to Figure 2 and Table 5.....	7
Changes to Figure 3 and Table 6.....	7

6/08—Rev. B to Rev. C

Changes to Temperature Range.....	Universal
Changes to Product Highlights.....	1
Changes to Table 4.....	6
Updated Outline Dimensions	14
Changes to the Ordering Guide.....	15

7/06—Rev. A to Rev. B

Changes to Features Section.....	1
Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Table 3.....	5
Changes to Table 4.....	6
Changes to the Ordering Guide.....	15

6/05—Rev. 0 to Rev. A

Updated Outline Dimensions	14
Changes to Ordering Guide	15

10/04—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.28		Ω typ	$V_{DD} = 4.5\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$
	0.37	0.41	Ω max	See Figure 18
On-Resistance Match Between Channels, ΔR_{ON}	0.01		Ω typ	$V_{DD} = 4.5\text{ V}$, $V_S = 2\text{ V}$, $I_S = 100\text{ mA}$
	0.035	0.05	Ω max	
On-Resistance Flatness, R_{FLAT} (On)	0.1		Ω typ	$V_{DD} = 4.5\text{ V}$, $V_S = 0\text{ V}$ to V_{DD}
	0.13	0.15	Ω max	$I_S = 100\text{ mA}$
LEAKAGE CURRENTS				$V_{DD} = 5.5\text{ V}$
Source Off Leakage, I_S (Off)	± 0.2		nA typ	$V_S = 0.6\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/0.6\text{ V}$; see Figure 19
Channel On Leakage, I_D , I_S (On)	± 0.2		nA typ	$V_S = V_D = 0.6\text{ V}$ or 4.5 V ; see Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	42		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	50	53	ns max	$V_S = 3\text{ V}/0\text{ V}$; see Figure 21
t_{OFF}	15		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	20	21	ns max	$V_S = 3\text{ V}$; see Figure 21
Break-Before-Make Time Delay, t_{BBM}	16		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
		10	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$; see Figure 22
Charge Injection	125		pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 23
Off Isolation	−60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 24
Channel-to-Channel Crosstalk	−120		dB typ	S1A to S2A/S1B to S2B, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
	−60		dB typ	S1A to S1B/S2A to S2B, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 25
Total Harmonic Distortion, THD + N	0.017		% typ	$R_L = 32\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 3.5\text{ V p-p}$
Insertion Loss	−0.03		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
−3 dB Bandwidth	18		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
C_S (Off)	103		pF typ	
C_D , C_S (On)	295		pF typ	
POWER REQUIREMENTS				$V_{DD} = 5.5\text{ V}$
I_{DD}	0.003		μA typ	Digital inputs = 0 V or 5.5 V
		1	μA max	

¹ Guaranteed by design, not production tested.

$V_{DD} = 3.4 \text{ V}$ to 4.2 V ; $GND = 0 \text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analogue Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.33 0.4	0.47	Ω typ Ω max	$V_{DD} = 3.4 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 100 \text{ mA}$ See Figure 18
On-Resistance Match Between Channels, ΔR_{ON}	0.013		Ω typ	$V_{DD} = 3.4 \text{ V}$, $V_S = 2 \text{ V}$, $I_S = 100 \text{ mA}$
On-Resistance Flatness, R_{FLAT} (On)	0.042 0.13 0.155	0.065 0.175	Ω max Ω typ Ω max	$V_{DD} = 3.4 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} $I_S = 100 \text{ mA}$
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.2		nA typ	$V_{DD} = 4.2 \text{ V}$ $V_S = 0.6 \text{ V}/3.9 \text{ V}$, $V_D = 3.9 \text{ V}/0.6 \text{ V}$; see Figure 19
Channel On Leakage, I_D , I_S (On)	± 0.2		nA typ	$V_S = V_D = 0.6 \text{ V}$ or 3.9 V ; see Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005	± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	42 50	54	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}/0 \text{ V}$; see Figure 21
t_{OFF}	15 21	24	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}$; see Figure 21
Break-Before-Make Time Delay, t_{BBM}	17	10	ns typ ns min	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_{S1} = V_{S2} = 1.5 \text{ V}$; see Figure 22
Charge Injection	100		pC typ	$V_S = 1.5 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 23
Off Isolation	−60		dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 24
Channel-to-Channel Crosstalk	−120		dB typ	S1A to S2A/S1B to S2B, $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 27
	−60		dB typ	S1A to S1B/S2A to S2B, $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 25
Total Harmonic Distortion, THD + N	0.01		% typ	$R_L = 32 \Omega$, $f = 20 \text{ Hz}$ to 20 kHz , $V_S = 2 \text{ V}$ p-p
Insertion Loss	−0.03		dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 26
−3 dB Bandwidth	18		MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 26
C_S (Off)	110		pF typ	
C_D , C_S (On)	300		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.003	1	μA typ μA max	$V_{DD} = 4.2 \text{ V}$ Digital inputs = 0 V or 4.2 V

¹ Guaranteed by design, not production tested.

$V_{DD} = 2.7\text{ V}$ to 3.6 V , $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.4		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V}$ to V_{DD}
	0.51	0.61	Ω max	$I_S = 100\text{ mA}$; see Figure 18
On-Resistance Match Between Channels, ΔR_{ON}	0.02		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0.6\text{ V}$
On-Resistance Flatness, R_{FLAT} (On)	0.07	0.1	Ω max	$I_S = 100\text{ mA}$
	0.18		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V}$ to V_{DD}
		0.25	Ω max	$I_S = 100\text{ mA}$
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.2		nA typ	$V_{DD} = 3.6\text{ V}$
Channel On Leakage, I_D , I_S (On)	± 0.2		nA typ	$V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$; see Figure 19
				$V_S = V_D = 0.6\text{ V}$ or 3.3 V ; see Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.3	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	42		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	56	62	ns max	$V_S = 1.5\text{ V}/0\text{ V}$; see Figure 21
t_{OFF}	14		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	19	21	ns max	$V_S = 1.5\text{ V}$; see Figure 21
Break-Before-Make Time Delay, t_{BBM}	24		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
		10	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$; see Figure 22
Charge Injection	85		pC typ	$V_S = 1.25\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 23
Off Isolation	−60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 24
Channel-to-Channel Crosstalk	−120		dB typ	$S1A$ to $S2A/S1B$ to $S2B$, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
	−60		dB typ	$S1A$ to $S1B/S2A$ to $S2B$, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 25
Total Harmonic Distortion, THD + N	0.03		% typ	$R_L = 32\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 1.5\text{ V p-p}$
Insertion Loss	−0.03		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
−3 dB Bandwidth	18		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
C_S (Off)	110		pF typ	
C_D , C_S (On)	300		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.003		μA typ	$V_{DD} = 3.6\text{ V}$
		1	μA max	Digital inputs = 0 V or 3.6 V

¹ Guaranteed by design, not production tested.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	–0.3 V to +6 V
Analog Inputs, ¹ Digital Inputs	–0.3 V to $V_{DD} + 0.3$ V or 30 mA (whichever occurs first)
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	400 mA
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
10-Lead MSOP, Thermal Impedance	
θ_{JA}	206°C/W
θ_{JC}	44°C/W
10-Ball WLCSP (4-Layer Board), Thermal Impedance	
θ_{JA}	120°C/W
10-Lead LFCSP_WD (4-Layer Board), Thermal Impedance	
θ_{JA}	76°C/W
θ_{JC}	13.5°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+ 0 or –5)°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at IN, S, or D pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

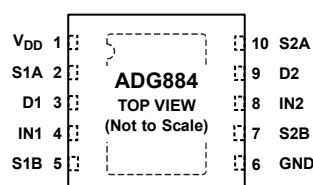
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

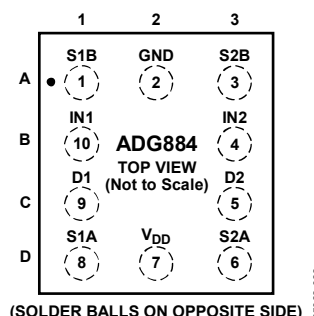


NOTES

1. THE LFCSP_WD PACKAGE HAS AN EXPOSED PAD THAT SHOULD BE TIED TO GROUND.

05028-002

Figure 2. LFCSP_WD and MSOP Pin Configuration



(SOLDER BALLS ON OPPOSITE SIDE)

05028-028

Figure 3. WLCSP Pin Configuration

Table 5. LFCSP_WD and MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD}	Most Positive Power Supply Potential.
2	S1A	Source Terminal. Can be an input or output.
3	D1	Drain Terminal. Can be an input or output.
4	IN1	Logic Control Input.
5	S1B	Source Terminal. Can be an input or output.
6	GND	Ground (0 V) Reference.
7	S2B	Source Terminal. Can be an input or output.
8	IN2	Logic Control Input.
9	D2	Drain Terminal. Can be an input or output.
10	S2A	Source Terminal. Can be an input or output.
	EPAD	The LFCSP_WD package has an exposed pad that should be tied to ground.

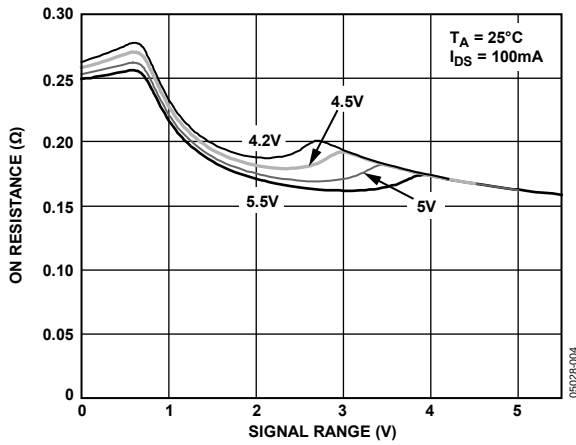
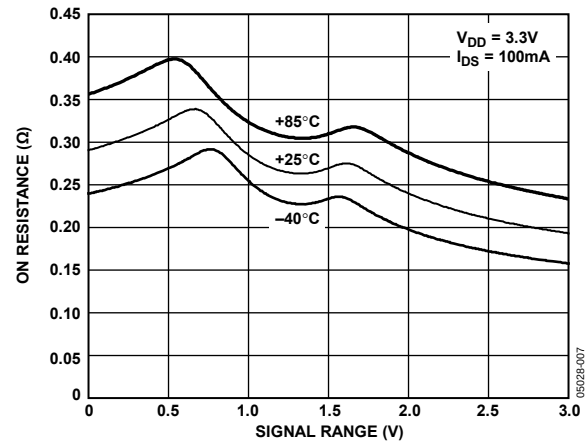
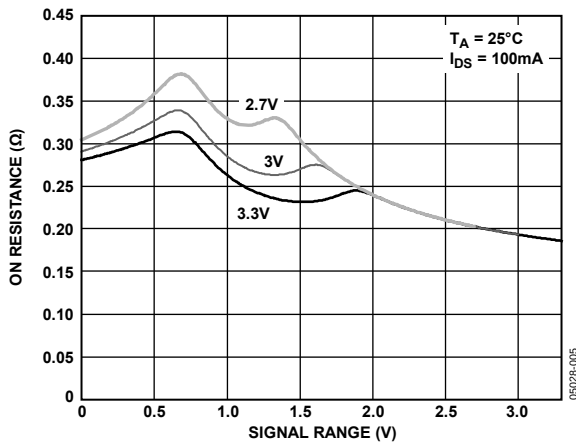
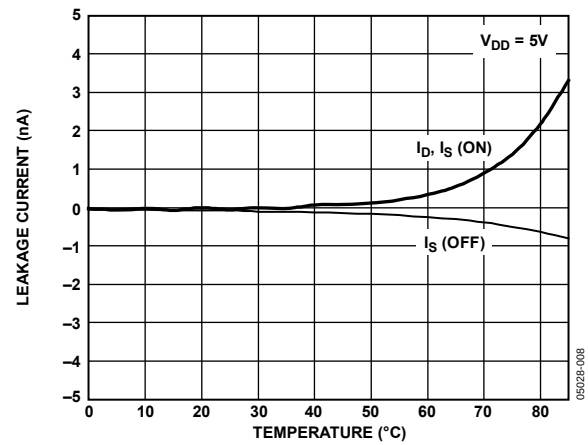
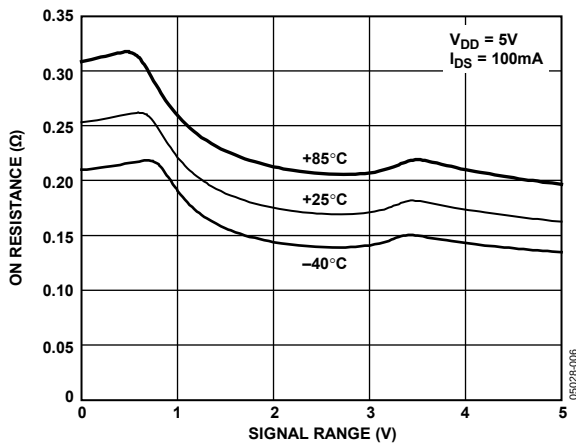
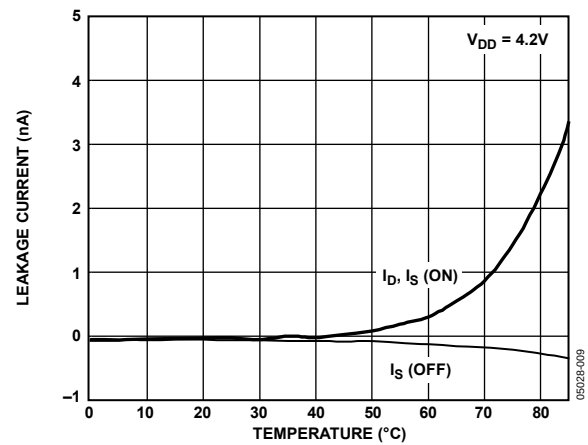
Table 6. WLCSP Package Pin Function Description

WLCSP Package		Mnemonic	Description
Ball Number	Location		
1	A1	S1B	Source Terminal. Can be an input or output.
2	A2	GND	Ground (0 V) Reference.
3	A3	S2B	Source Terminal. Can be an input or output.
4	B3	IN2	Logic Control Input.
5	C3	D2	Drain Terminal. Can be an input or output.
6	D3	S2A	Source Terminal. Can be an input or output.
7	D2	V _{DD}	Most Positive Power Supply Potential.
8	D1	S1A	Source Terminal. Can be an input or output.
9	C1	D1	Drain Terminal. Can be an input or output.
10	B1	IN1	Logic Control Input.

Table 7. ADG884 Truth Table

Logic (IN1/IN2)	Switch 1A/Switch 2A	Switch 1B/Switch 2B
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. On Resistance vs. V_D (V_S), $V_{DD} = 4.2$ V to 5.5 VFigure 7. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3.3$ VFigure 5. On Resistance vs. V_D (V_S), $V_{DD} = 2.7$ V to 3.3 VFigure 8. Leakage Current vs. Temperature, $V_{DD} = 5$ VFigure 6. On Resistance vs. V_D (V_S) for Different Temperature, $V_{DD} = 5$ VFigure 9. Leakage Current vs. Temperature, $V_{DD} = 4.2$ V

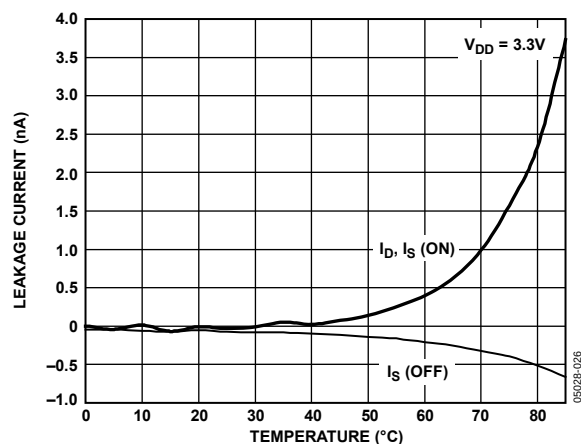
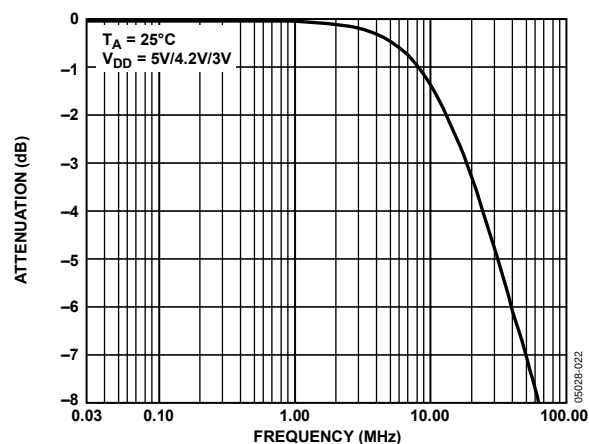
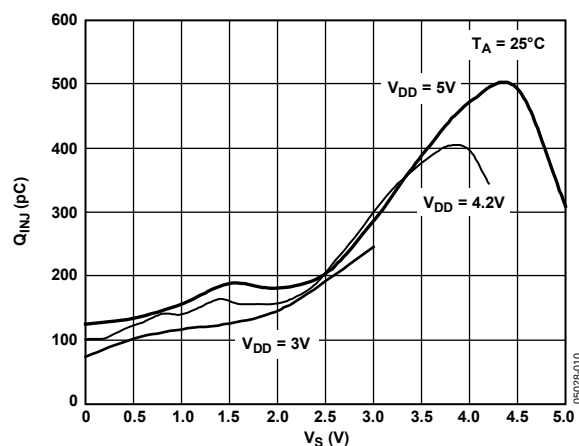
Figure 10. Leakage Current vs. Temperature, $V_{DD} = 3.3V$ Figure 13. Bandwidth, $V_{DD} = 5V/4.2V/3V$ 

Figure 11. Charge Injection vs. Source Voltage

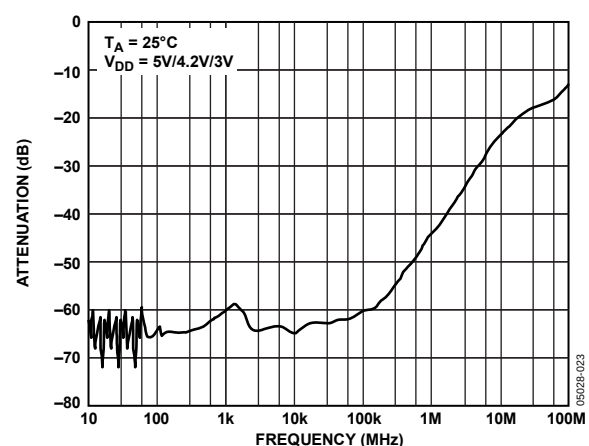


Figure 14. Off Isolation vs. Frequency

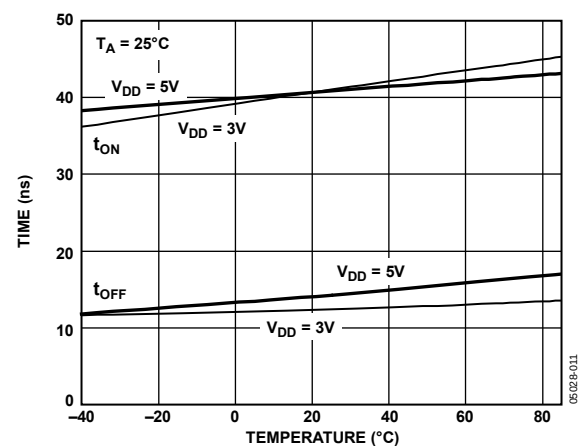
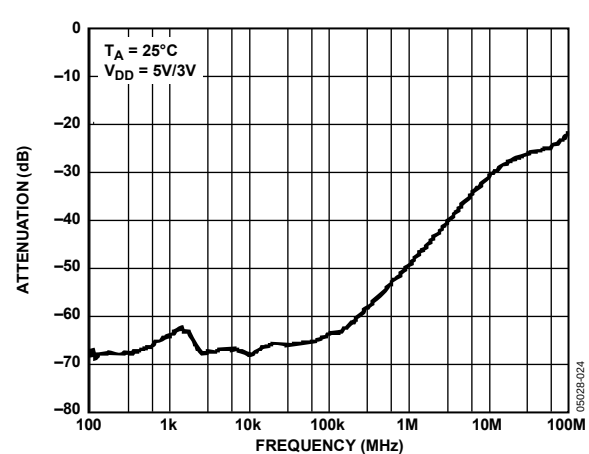
Figure 12. t_{ON}/t_{OFF} Times vs. Temperature

Figure 15. Crosstalk vs. Frequency

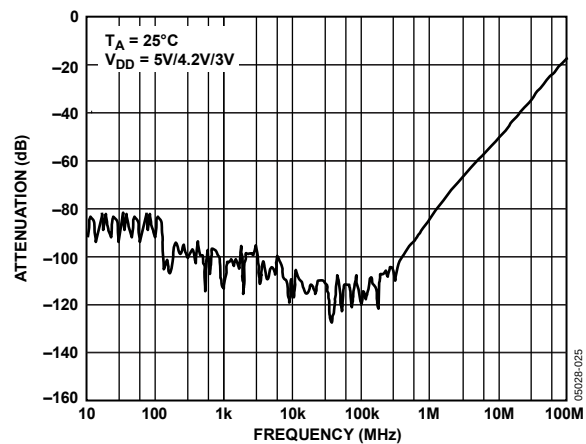


Figure 16. AC PSRR

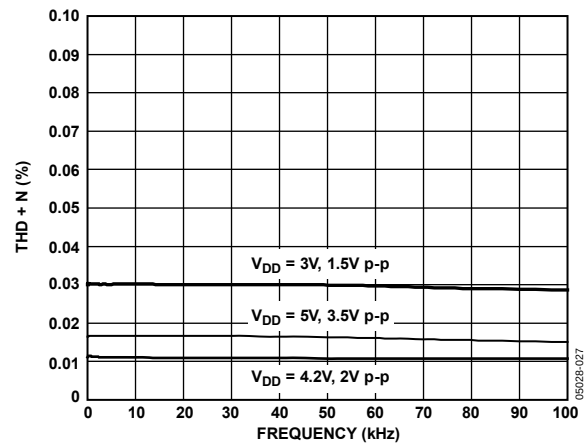


Figure 17. THD + N

TEST CIRCUITS

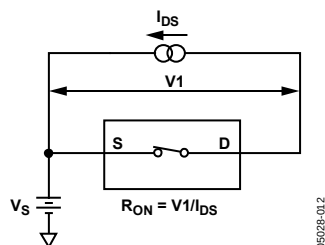


Figure 18. On Resistance

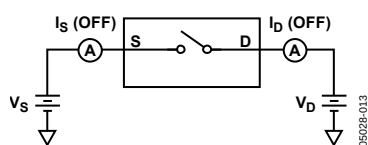


Figure 19. Off Leakage

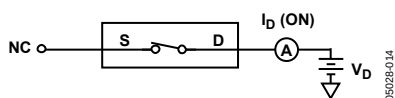
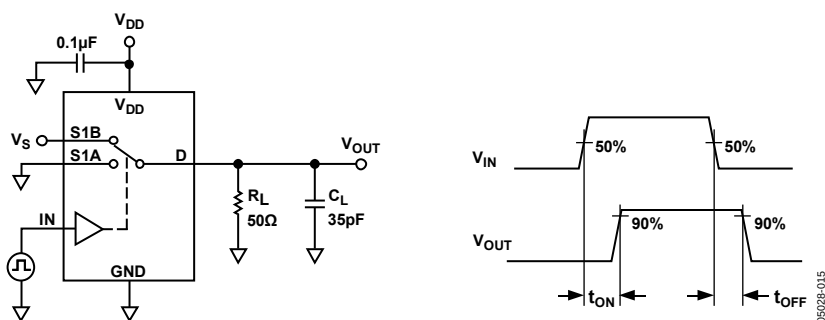
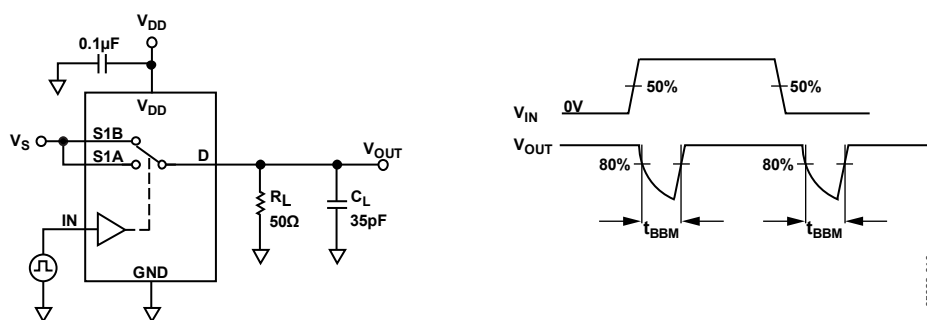


Figure 20. On Leakage

Figure 21. Switching Times, t_{ON} , t_{OFF} Figure 22. Break-Before-Make Time Delay, t_{BBM}

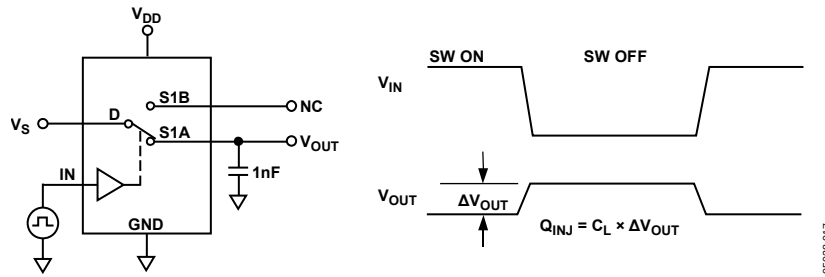


Figure 23. Charge Injection

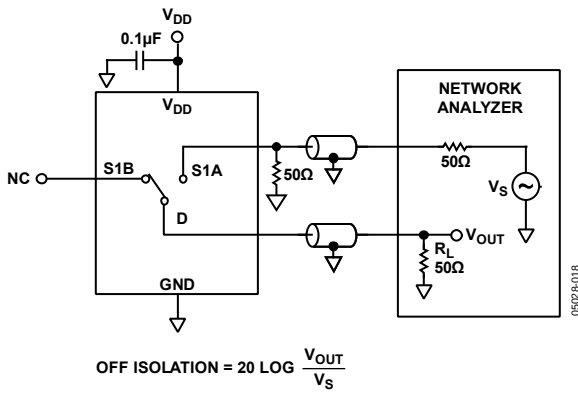


Figure 24. Off Isolation

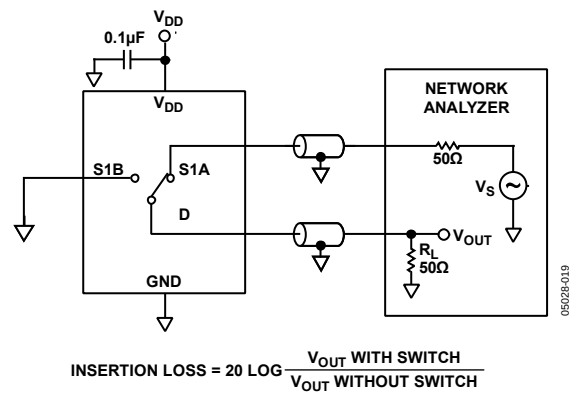


Figure 26. Bandwidth

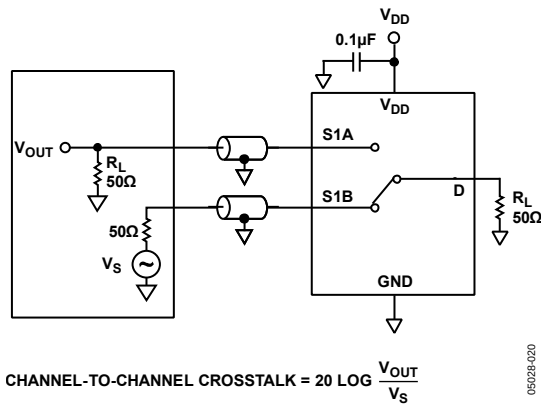


Figure 25. Channel-to-Channel Crosstalk (S1A to S1B)

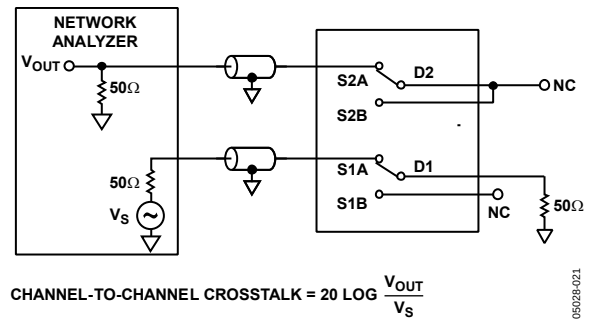


Figure 27. Channel-to-Channel Crosstalk (S1A to S2A)

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT} (On)

The difference between the maximum and minimum values of on resistance as measured on the switch.

ΔR_{ON}

On resistance match between any two channels.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance. Measured with reference to ground.

C_D (Off)

Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation

Measure of unwanted signal coupling through an off switch.

Crosstalk

Measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

–3 dB Bandwidth

Frequency at which the output is attenuated by 3 dB.

On Response

Frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

OUTLINE DIMENSIONS

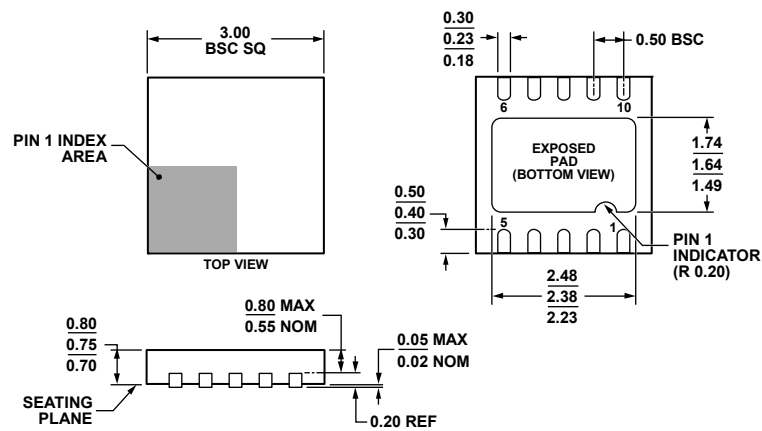
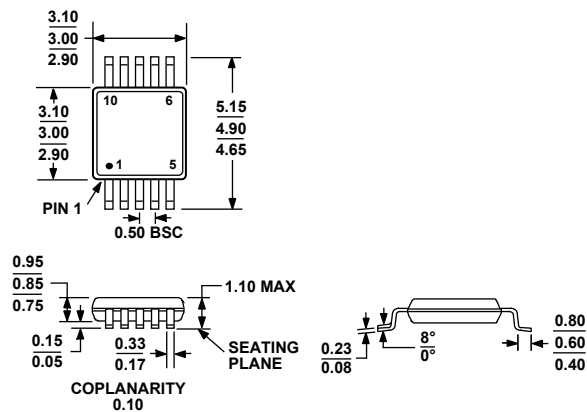


Figure 28. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm x 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 29. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)

Dimensions shown in millimeters

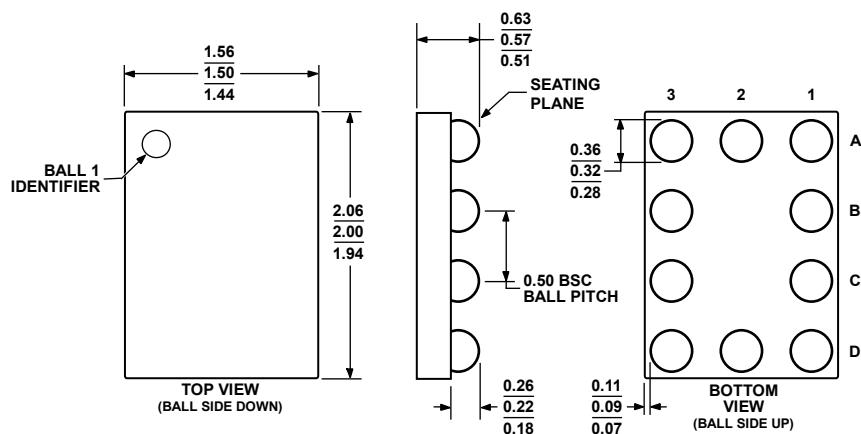


Figure 30. 10-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-10)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding ²
ADG884BRMZ	–40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S9C
ADG884BRMZ-REEL	–40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S9C
ADG884BRMZ-REEL7	–40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S9C
ADG884BCPZ-REEL	–40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	S9C
ADG884BCPZ-REEL7	–40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	S9C
ADG884BCBZ-REEL	–40°C to +85°C	10-Ball Wafer Level Chip Scale Package [WLCSP]	CB-10	S9C
ADG884BCBZ-REEL7	–40°C to +85°C	10-Ball Wafer Level Chip Scale Package [WLCSP]	CB-10	S9C
EVAL-ADG884EBZ		Evaluation Board		

¹ Z = RoHS Compliant Part.

² Branding on this package is limited to three characters due to space constraints.

NOTES