# 0.5 Ω CMOS 1.65 V TO 3.6 V 4-Channel Multiplexer

Data Sheet **ADG804**

## FEATURES

**0.5 Ω typical on resistance**
**0.8 Ω maximum on resistance at 125°C**
**1.65 V to 3.6 V operation**
**Automotive temperature range: –40°C to +125°C**
**High current carrying capability: 300 mA continuous**
**Rail-to-rail switching operation**
**Fast switching times <25 ns**
**Typical power consumption (<0.1 µW)**

## APPLICATIONS

**MP3 players**
**Power routing**
**Battery-powered systems**
**PCMCIA cards**
**Cellular phones**
**Modems**
**Audio and video signal routing**
**Communication systems**

## GENERAL DESCRIPTION

The ADG804 is a low voltage 4-channel CMOS multiplexer comprising four single channels. This device offers ultralow on resistance of less than 0.8 Ω over the full temperature range. The digital inputs can handle 1.8 V logic with a 2.7 V to 3.6 V supply.

The ADG804 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. A Logic 0 on the EN pin disables the device. The ADG804 has break-before-make switching.

The ADG804 is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation. It is available in a 10-lead MSOP package.

## FUNCTIONAL BLOCK DIAGRAM

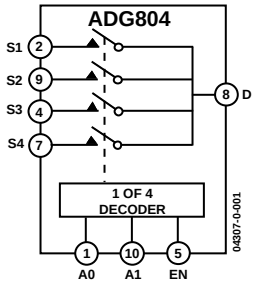



*Figure 1.*

## PRODUCT HIGHLIGHTS

1. <0.8 Ω over full temperature range of –40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Operational with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low THD + N (0.02% typ).
6. Small 10-lead MSOP package.

**Rev. A**
**Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.**

**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** **© 2004–2011 Analog Devices, Inc. All rights reserved.**

# TABLE OF CONTENTS

Revision History ..... 2
Specifications ..... 3
Absolute Maximum Ratings ..... 6
ESD Caution ..... 6
Pin Configuration ..... 7
Typical Performance Characteristics ..... 8
Test Circuits ..... 11
Outline Dimensions ..... 13
Ordering Guide ..... 13

## REVISION HISTORY

**9/11—Rev. 0 to Rev. A**

Changes to Maximum Leakage Currents Parameter and Conditions, Table 1 ..... 3
Changes to Maximum Leakage Currents Parameter and Conditions, Table 2 ..... 4
Changes to Maximum Leakage Currents Parameter and Conditions, Table 3 ..... 5
Added Lead Temperature Parameter ..... 6
Updated Outline Dimensions ..... 13
Changes to Ordering Guide ..... 13

**4/04—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.[1]

**Table 1.**

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 0.5 | | | Ω typ | $V_{DD}$ = 2.7 V; $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA; Figure 18 |
| | 0.65 | 0.75 | 0.8 | Ω max | |
| On Resistance Match between | 0.04 | | | Ω typ | $V_{DD}$ = 2.7 V; $V_S$ = 0.65 V, $I_S$ = 10 mA |
| Channels ($\Delta R_{ON}$) | | 0.075 | 0.08 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.1 | | | Ω typ | $V_{DD}$ = 2.7 V; $V_S$ = 0 V to $V_{DD}$, |
| | | 0.15 | 0.16 | Ω max | $I_S$ = 10 mA |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 3.6 V |
| Source Off Leakage $I_S$ (OFF) | ±0.1 | | | nA typ | $V_S$ = 1 V/2.6 V; $V_D$ = 2.6 V/1 V; Figure 19 |
| | ±2 | | | nA max | |
| Drain Off Leakage $I_D$ (OFF) | ±0.1 | | | nA typ | $V_S$ = 1 V/2.6 V; $V_D$ = 2.6 V/1 V; Figure 19 |
| | ±2 | | | nA max | |
| Channel On Leakage $I_D$, $I_S$ (ON) | ±0.1 | | | nA typ | $V_S$ = $V_D$ = 1 V or 2.6 V; Figure 20 |
| | ±2 | | | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 2 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V max | |
| Input Current $I_{INL}$ or $I_{INH}$ | 0.005 | | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | | ±0.1 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 4 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | | |
| $t_{TRANSISTION}$ | 24 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 30 | 32 | 35 | ns max | $V_S$ = 1.5 V/0 V; Figure 21 |
| $t_{ON}$ ENABLE | 23 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 29 | 30 | 31 | ns max | $V_S$ = 1.5 V/0 V; Figure 23 |
| $t_{OFF}$ ENABLE | 5 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 6 | 7 | 8 | ns max | $V_S$ = 1.5 V; Figure 23 |
| Break-Before-Make Time Delay ($t_{BBM}$) | 20 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | | | 5 | ns min | $V_{S1}$ = $V_{S2}$ = 1.5 V; Figure 22 |
| Charge Injection | 28 | | | pC typ | $V_S$ = 1.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Figure 24 |
| Off Isolation | −67 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF,f = 100 kHz; Figure 25 |
| Channel-to-Channel Crosstalk | −75 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz; Figure 27 |
| Total Harmonic Distortion (THD+N) | 0.02 | | | % | $R_L$ = 32 Ω, f = 20 Hz to 20 kHz, $V_S$ = 2 V p-p |
| Insertion Loss | 0.06 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz |
| −3 dB Bandwidth | 33 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 26 |
| $C_S$ (OFF) | 24 | | | pF typ | |
| $C_D$ (OFF) | 105 | | | pF typ | |
| $C_D$, $C_S$ (ON) | 125 | | | pF typ | |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 3.6 V |
| $I_{DD}$ | 0.003 | | | μA typ | Digital inputs = 0 V or 3.6 V |
| | | 1.0 | 4 | μA max | |

[1] Temperature range, Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

$V_{DD}$ = 2.5 V ± 0.2 V, GND = 0 V, unless otherwise noted.[1]

**Table 2.**

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 0.65 | | | Ω typ | $V_{DD}$ = 2.3 V; $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA; Figure 18 |
| | 0.77 | 0.8 | 0.88 | Ω max | |
| On Resistance Match between | 0.4 | | | Ω typ | $V_{DD}$ = 2.3 V; $V_S$ = 0.7 V; $I_S$ = 10 mA |
| Channels ($\Delta R_{ON}$) | | 0.08 | 0.085 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.16 | | | Ω typ | $V_{DD}$ = 2.3 V; $V_S$ = 0 V to $V_{DD}$; $I_S$ = 10 mA |
| | | 0.23 | 0.24 | Ω max | |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 2.7 V |
| Source Off Leakage $I_S$ (OFF) | ±0.1 | | | nA typ | $V_S$ = 1 V/2 V, $V_D$ = 2 V/1 V; Figure 19 |
| | ±2 | | | nA max | |
| Drain Off Leakage $I_D$ (OFF) | ±0.1 | | | nA typ | $V_S$ = 1/2 V, $V_D$ = 2/1 V; Figure 19 |
| | ±2 | | | nA max | |
| Channel On Leakage $I_D$, $I_S$ (ON) | ±0.1 | | | nA typ | $V_S$ = $V_D$ = 1 V or 2 V; Figure 20 |
| | ±2 | | | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 1.7 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.7 | V max | |
| Input Current $I_{INL}$ or $I_{INH}$ | 0.005 | | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | | ±0.1 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 4 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | | |
| $T_{TRANSITION}$ | 25 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 31 | 33 | 35 | ns max | $V_S$ = 1.5 V/0 V; Figure 21 |
| $t_{ON}$ ENABLE | 25 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 30 | 32 | 34 | ns max | $V_S$ = 1.5 V/0 V; Figure 22 |
| $t_{OFF}$ ENABLE | 5 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 7 | 8 | 9 | ns max | $V_S$ = 1.5 V; Figure 22 |
| Break-Before-Make Time Delay ($t_{BBM}$) | 20 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | | | 5 | ns min | $V_{S1}$ = $V_{S2}$ = 1.5 V; Figure 22 |
| Charge Injection | 20 | | | pC typ | $V_S$ = 1.25 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Figure 24 |
| Off Isolation | −67 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz; Figure 25 |
| Channel-to-Channel Crosstalk | −75 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz; Figure 27 |
| Total Harmonic Distortion (THD + N) | 0.022 | | | % | $R_L$ = 32 Ω, f = 20 Hz to 20 kHz, $V_S$ = 1.5 V p-p |
| Insertion Loss | −0.06 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz |
| −3 dB Bandwidth | 33 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 26 |
| $C_S$ (OFF) | 25 | | | pF typ | |
| $C_D$ (OFF) | 110 | | | pF typ | |
| $C_D$, $C_S$ (ON) | 128 | | | pF typ | |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 2.7 V |
| $I_{DD}$ | 0.003 | | | μA typ | Digital inputs = 0 V or 2.7 V |
| | | 1 | 4 | μA max | |

[1] Temperature range, Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

$V_{DD}$ = 1.65 V ± 1.95 V, GND = 0 V, unless otherwise noted.[1]

**Table 3.**

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 1 | | | Ω typ | $V_{DD}$ = 1.8 V; $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| | 1.4 | 2.2 | 2.2 | Ω max | |
| | 2.2 | 4 | 4 | Ω max | $V_{DD}$ = 1.65 V, $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA; Figure 18 |
| On Resistance Match between Channels ($\Delta R_{ON}$) | 0.1 | | | Ω typ | $V_{DD}$ = 1.65 V, $V_S$ = 0.7 V, $I_S$ = 10 mA |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 1.95 V |
| Source Off Leakage $I_S$ (OFF) | ±0.1 | | | nA typ | $V_S$ = 0.6 V/1.35 V, $V_D$ = 1.35 V/0.6 V; |
| | ±2 | | | nA max | Figure 19 |
| Drain Off Leakage $I_D$ (OFF) | ±0.1 | | | nA typ | $V_S$ = 0.6/1.35 V, $V_D$ = 1.35/0.6 V; |
| | ±2 | | | nA max | Figure 19 |
| Channel On Leakage $I_D$, $I_S$ (ON) | ±0.1 | | | nA typ | $V_S$ = $V_D$ = 0.6 V or 1.35 V; Figure 20 |
| | ±2 | | | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 0.65 $V_{DD}$ | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.35 $V_{DD}$ | V max | |
| Input Current $I_{INL}$ or $I_{INH}$ | 0.005 | | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | | ±0.1 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 4 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | | |
| $t_{TRANSISTION}$ | 32 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 40 | 42 | 44 | ns max | $V_S$ = 1.5 V/0 V; Figure 21 |
| $t_{ON}$ ENABLE | 34 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 39 | 40 | 41 | ns max | $V_S$ = 1.5 Ω/0 V; Figure 22 |
| $t_{OFF}$ ENABLE | 8 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | 10 | 11 | 13 | ns max | $V_S$ = 1.5 V; Figure 22 |
| Break-Before-Make Time Delay ($t_{BBM}$) | 22 | | | ns typ | $R_L$ = 50 Ω, $C_L$ = 35 pF |
| | | | 5 | ns min | $V_{S1}$ = $V_{S2}$ = 1 V; Figure 22 |
| Charge Injection | 12 | | | pC typ | $V_S$ = 1 V, $R_S$ = 0 V, $C_L$ = 1 nF; Figure 24 |
| Off Isolation | −67 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz; Figure 25 |
| Channel-to-Channel Crosstalk | −75 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz, Figure 27 |
| Total Harmonic Distortion (THD + N)) | 0.14 | | | % | $R_L$ = 32 Ω, f = 20 Hz to 20 kHz, $V_S$ = 1.2 V p-p |
| Insertion Loss | 0.08 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz |
| −3 dB Bandwidth | 30 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 26 |
| $C_S$ (OFF) | 26 | | | pF typ | |
| $C_D$ (OFF) | 115 | | | pF typ | |
| $C_D$, $C_S$ (ON) | 130 | | | pF typ | |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 1.95 V |
| $I_{DD}$ | 0.003 | | | μA typ | Digital inputs = 0 V or 1.95 V |
| | | 1.0 | 4 | μA max | |

[1] Temperature range, Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +4.6 V |
| Analog Inputs[1] | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Inputs[1] | −0.3 V to +4.6 V or 10 mA, whichever occurs first |
| Peak Current, S or D | (Pulsed at 1 ms, 10% Duty Cycle Max) |
| 3.3 V Operation | 500 mA |
| 2.5 V Operation | 460 mA |
| 1.8 V Operation | 420 mA |
| Continuous Current, S or D | |
| 3.3 V Operation | 300 mA |
| 2.5 V Operation | 275 mA |
| 1.8 V Operation | 250 mA |
| Operating Temperature Range | |
| Automotive (Y Version) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| MSOP Package | |
| $\theta_{JA}$ Thermal Impedance | 206°C/W |
| $\theta_{JC}$ Thermal Impedance | 44°C/W |
| Lead Temperature, Soldering | As per JEDEC J-STD-020 |

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

**Table 5. ADG804 Truth Table**

| A1 | A0 | EN | ON Switch |
|---|---|---|---|
| x | x | 0 | None |
| 0 | 0 | 1 | S1 |
| 0 | 1 | 1 | S2 |
| 1 | 0 | 1 | S3 |
| 1 | 1 | 1 | S4 |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION

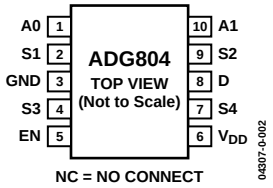



*Figure 2. 10-Lead MSOP (RM-10)*

**Table 6. Terminology**

| | |
|---|---|
| $V_{DD}$ | Most positive power supply potential. |
| $I_{DD}$ | Positive supply current. |
| GND | Ground (0 V) reference. |
| S | Source terminal. May be an input or an output. |
| D | Drain terminal. May be an input or an output. |
| EN | Active high logic control input. |
| A0, A1 | Logic control inputs. Used to select which source terminal, S1 to S4, is connected to the drain, D. |
| $V_D$, $V_S$ | Analog voltage on terminals D, S. |
| $R_{ON}$ | Ohmic resistance between D and S. |
| $R_{FLAT (ON)}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| $\Delta R_{ON}$ | On resistance match between any two channels. |
| $I_S$ (OFF) | Source leakage current with the switch off. |
| $I_D$ (OFF) | Drain leakage current with the switch off. |
| $I_D$, $I_S$ (ON) | Channel leakage current with the switch on. |
| $V_{INL}$ | Maximum input voltage for Logic 0. |
| $V_{INH}$ | Minimum input voltage for Logic 1. |
| $I_{INL}$ ($I_{INH}$) | Input current of the digital input. |
| $C_S$ (OFF) | Off switch source capacitance. Measured with reference to ground. |
| $C_D$ (OFF) | Off switch drain capacitance. Measured with reference to ground. |
| $C_D$, $C_S$ (ON) | On switch capacitance. Measured with reference to ground. |
| $C_{IN}$ | Digital input capacitance. |
| $t_{ON}$ (EN) | Delay time between the 50% and the 90% points of the digital input and switch on condition. |
| $t_{OFF}$ (EN) | Delay time between the 50% and the 90% points of the digital input and switch off condition. |
| $t_{TRANSITION}$ | Delay time between the 50% and the 90% points of the digital input and switch on condition when switching from one address state to the other. |
| $t_{BBM}$ | On or off time measured between the 80% points of both switches when switching from one to another. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching. |
| Off Isolation | A measure of unwanted signal coupling through an off switch. |
| Crosstalk | A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance. |
| −3 dB Bandwidth | The frequency at which the output is attenuated by 3 dB. |
| On Response | The frequency response of the on switch. |
| Insertion Loss | The loss due to the on resistance of the switch. |
| THD + N | The ratio of the harmonic amplitudes plus noise of a signal to the fundamental. |

# TYPICAL PERFORMANCE CHARACTERISTICS

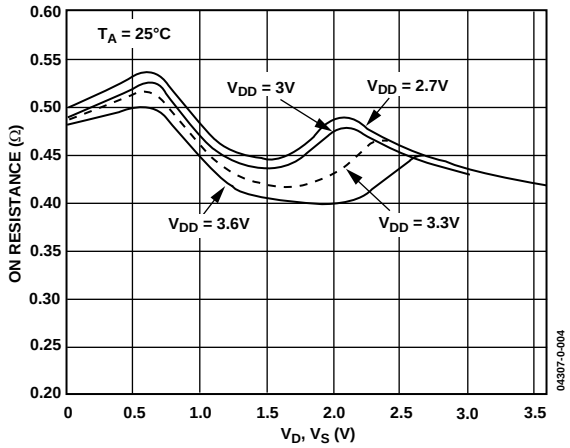



*Figure 3. On Resistance vs. $V_D$ ($V_S$) $V_{DD}$ = 2.7 V to 3.6 V*

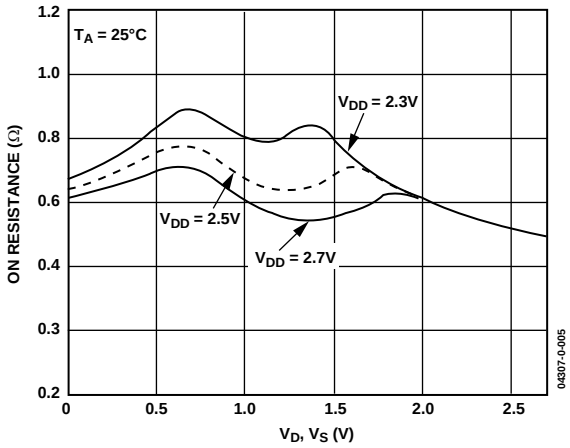



*Figure 4. On Resistance vs. $V_D$ ($V_S$) $V_{DD}$ = 2.5 V ± 0.2 V*

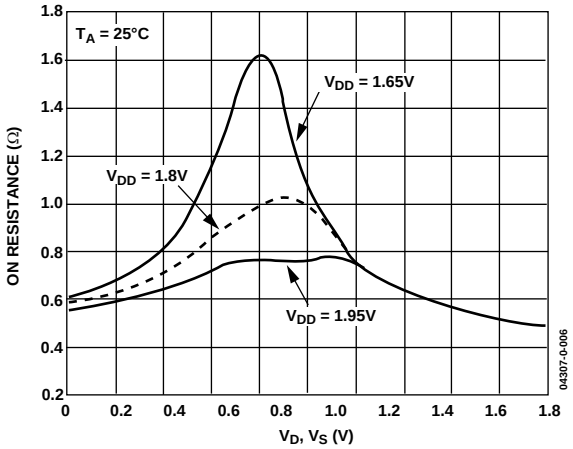



*Figure 5. On Resistance vs. $V_D$ ($V_S$) $V_{DD}$ = 1.8 ± 0.15 V*

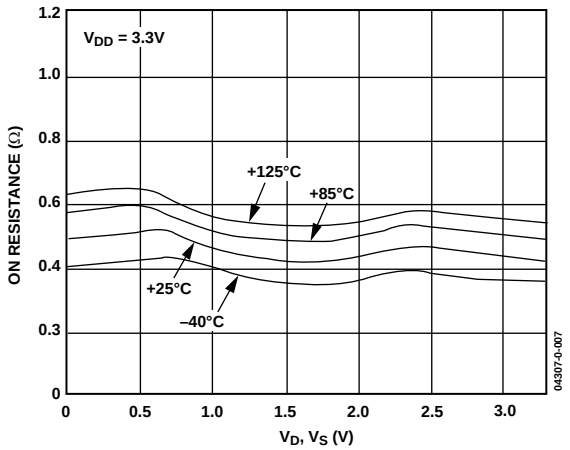



*Figure 6. On Resistance vs. $V_D$ ($V_S$) for Different Temperature, $V_{DD}$ = 3.3 V*

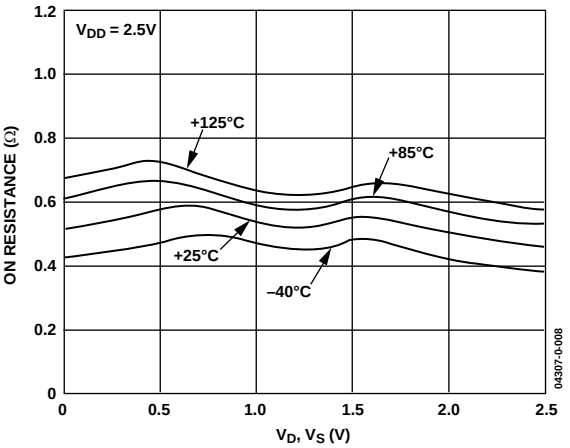



*Figure 7. On Resistance vs. $V_D$ ($V_S$) for Different Temperature, $V_{DD}$ = 2.5 V*

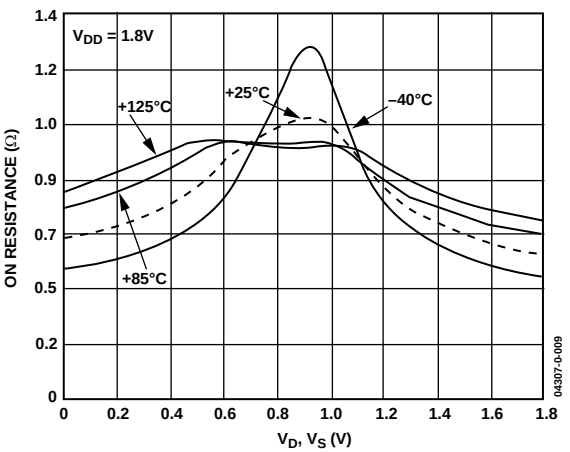



*Figure 8. On Resistance vs. $V_D$ ($V_S$) for Different Temperature, $V_{DD}$ = 1.8 V*

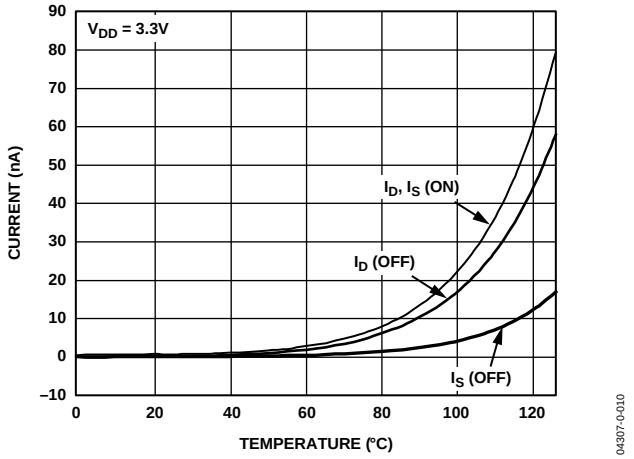



Figure 9. Leakage Current vs. Temperature, $V_{DD}$ = 3.3 V

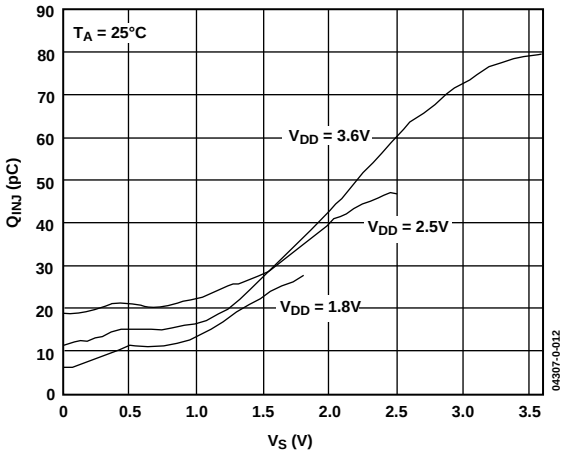



Figure 12. Charge Injection vs. Source Voltage, $V_{DD}$ = 1.8 V

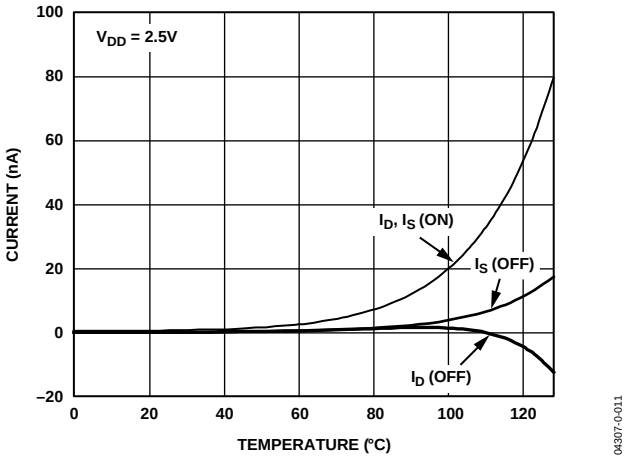



Figure 10. Leakage Current vs. Temperature, $V_{DD}$ = 2.5 V

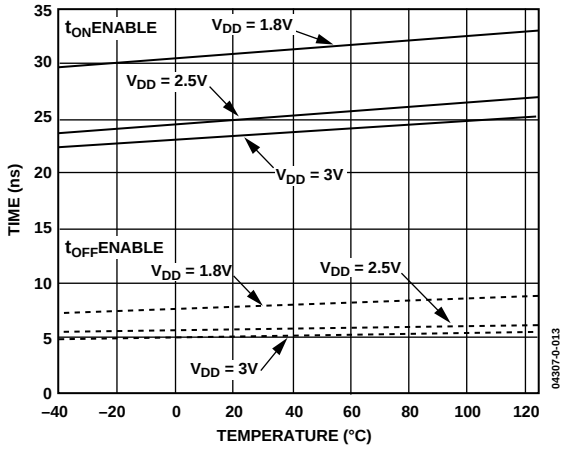



Figure 13. $t_{ON}/t_{OFF}$ Times vs. Temperature

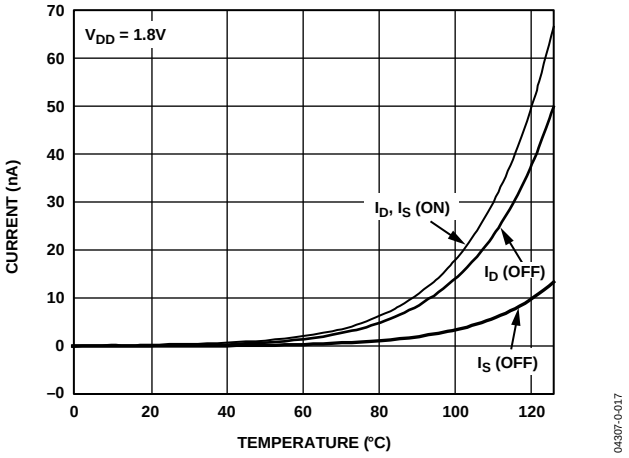



Figure 11. Leakage Current vs. Temperature, $V_{DD}$ = 1.8 V

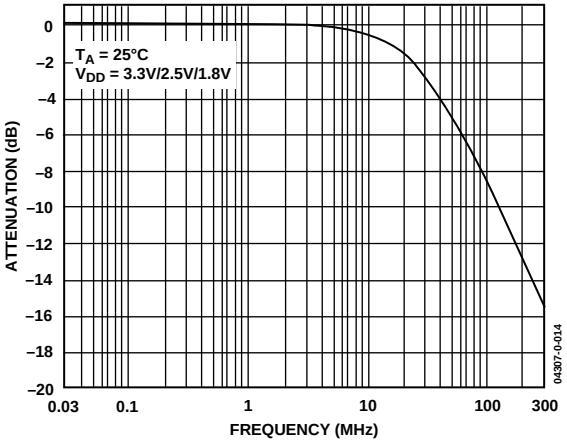



Figure 14. Bandwidth

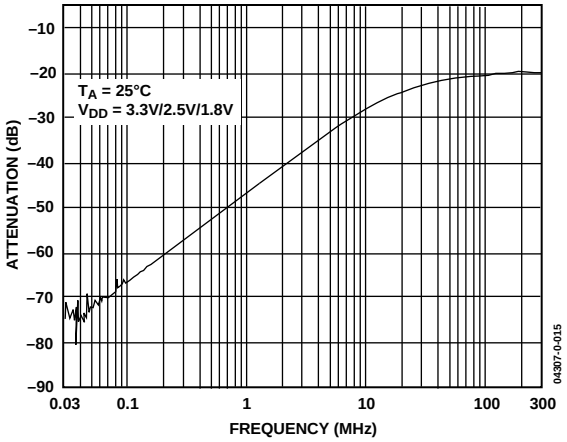



*Figure 15. Off Isolation vs. Frequency*

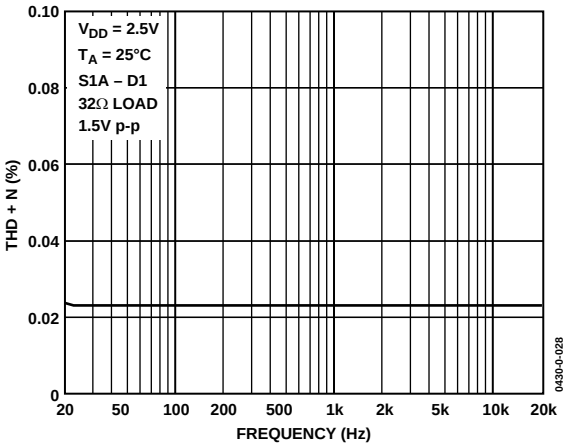



*Figure 17. Total Harmonic Distortion + Noise*

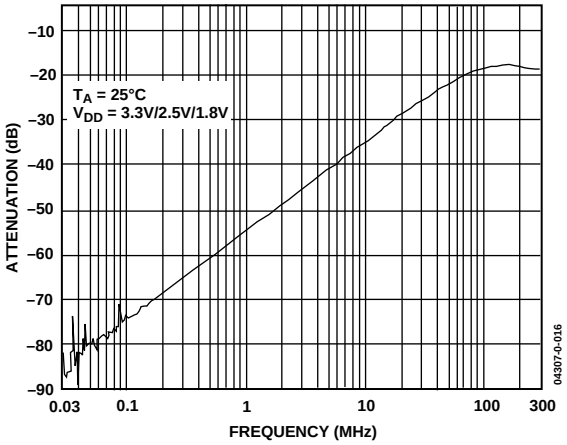



*Figure 16. Crosstalk vs. Frequency*

# TEST CIRCUITS

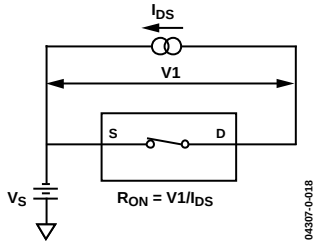



Figure 18. On Resistance

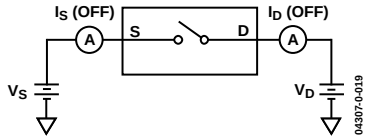



Figure 19. Off Leakage

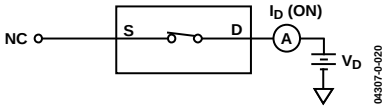



Figure 20. On Leakage

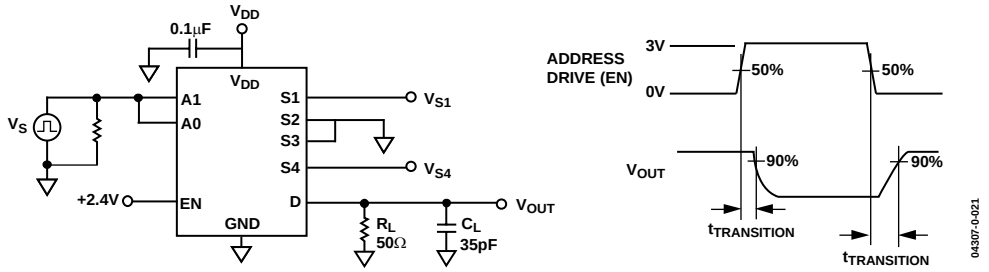



Figure 21. Switching Time of Multiplexer, $t_{TRANSITION}$

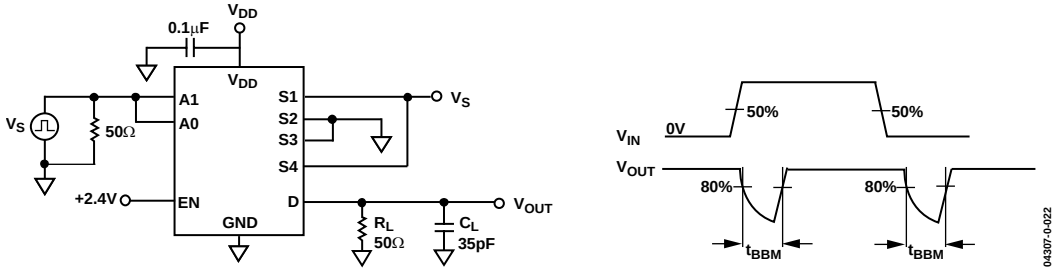



Figure 22. Break-Before-Make Time Delay, $t_{BBM}$

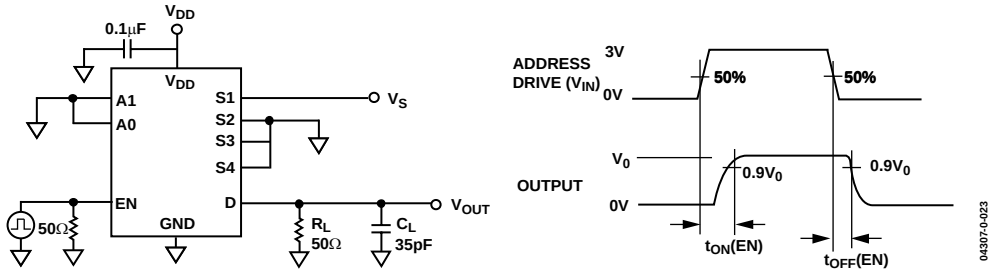



Figure 23. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

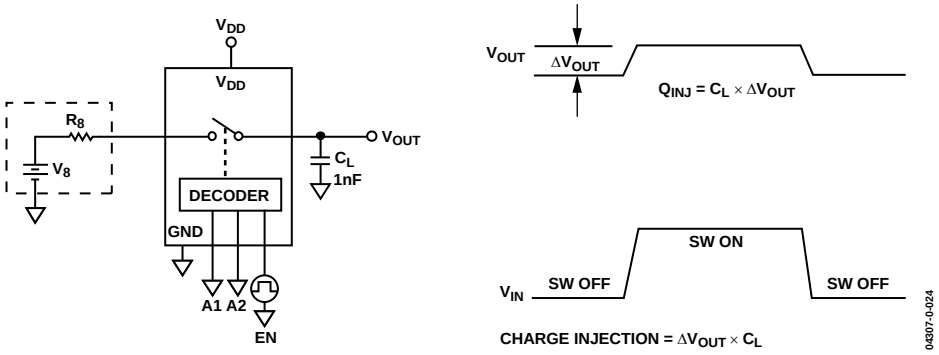



*Figure 24. Charge Injection*

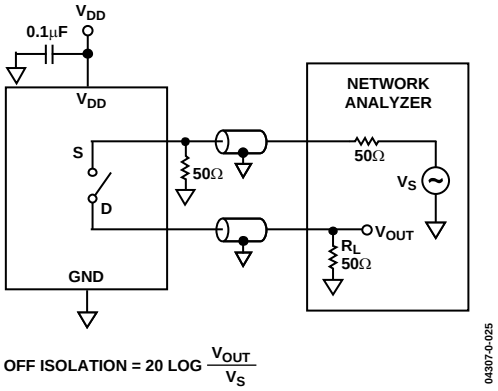



*Figure 25. Off Isolation*

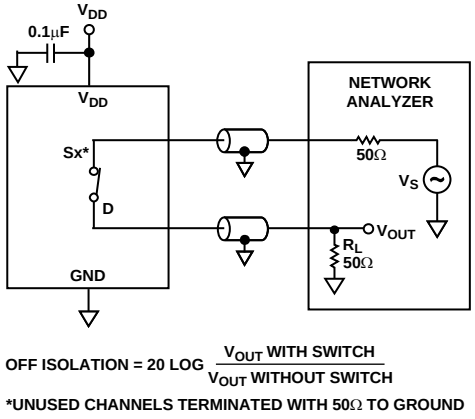



*Figure 26. Bandwidth*

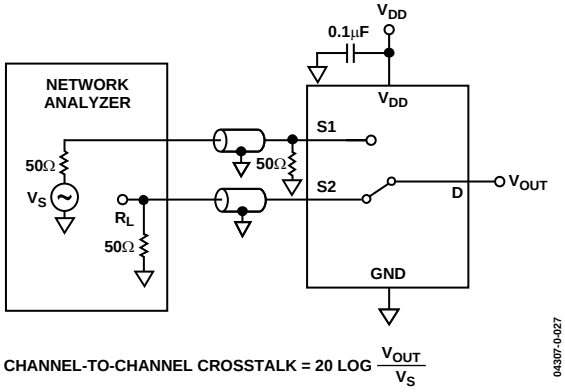



*Figure 27. Channel-to-Channel Crosstalk*

# OUTLINE DIMENSIONS

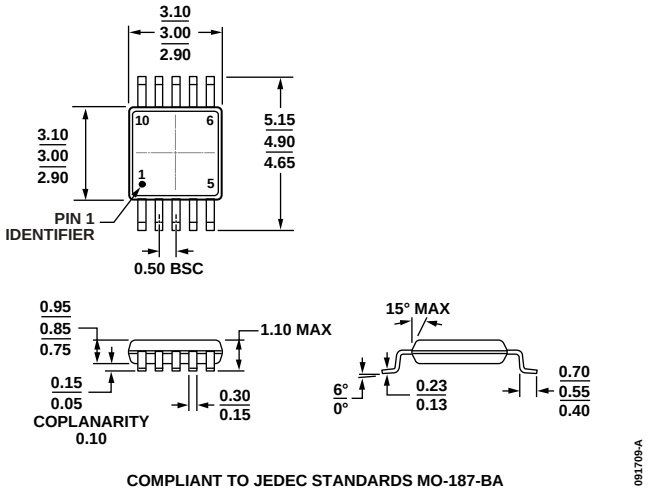



*Figure 28. 10-Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Branding[2, 3] |
|---|---|---|---|---|
| ADG804YRM | –40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S1A |
| ADG804YRMZ | –40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S0N# |
| ADG804YRMZ-REEL | –40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S0N# |
| ADG804YRMZ-REEL7 | –40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S0N# |

[1] Z= RoHS compliant part.
[2] Branding on this package is limited to three characters due to space constraints.
[3] # denotes lead-free product may be top or bottom marked

## NOTES

## NOTES

## NOTES

© 2004–2011 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D04307–0–9/11(A)