

FEATURES

- 0.4 Ω maximum on resistance at 125°C
- 0.08 Ω maximum on resistance flatness at 125°C
- 1.8 V to 5.5 V single supply
- Automotive temperature range from –40°C to +125°C
- 400 mA current-carrying capability
- Tiny 6-lead SOT-23 and 8-lead MSOP packages
- 35 ns switching times
- Low power consumption
- TTL-/CMOS-compatible inputs
- Pin compatible with [ADG701/ADG702](#)

APPLICATIONS

- Power routing
- Cellular phones
- Modems
- PCMCIA cards
- Hard drives
- Data acquisition systems
- Communications systems
- Relay replacement
- Battery-powered systems

GENERAL DESCRIPTION

The [ADG801](#) and [ADG802](#) are monolithic CMOS, single-pole, single throw (SPST) switches with on resistance of less than 0.4 Ω . These switches are designed using an advanced submicron process that provides extremely low on resistance, high switching speed, and low leakage currents.

The low on resistance of <0.4 Ω makes these parts ideal for applications where low on resistance switching is critical.

The [ADG801](#) switch is normally open (NO), while the [ADG802](#) is normally closed (NC). Each switch conducts equally well in both directions when on.

FUNCTIONAL BLOCK DIAGRAM

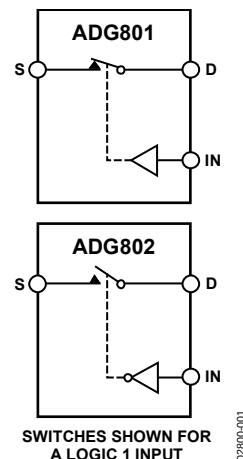


Figure 1.

PRODUCT HIGHLIGHTS

1. Low on resistance (0.25 Ω typical).
2. 1.8 V to 5.5 V single-supply operation.
3. Tiny 6-lead SOT-23 and 8-lead MSOP packages.
4. 400 mA current-carrying capability.
5. Automotive temperature range from –40°C to +125°C.
6. Pin compatible with [ADG701](#) ([ADG801](#)) and [ADG702](#) ([ADG802](#)).

Rev. B

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REVISION HISTORY

1/12—Rev. A to Rev. B

Deleted 6-Ball WLCSP Package.....	Universal
Added Table Title to Table 3; Renumbered Sequentially	5
Deleted Figure 4; Renumbered Sequentially.....	6
Changes to Table 5.....	6
Moved Terminology Section	9
Updated Outline Dimensions	12
Deleted Figure 23.....	13
Changes to Ordering Guide	13

3/07—Rev. 0 to Rev. A

Updated Format.....	Universal
Added 6-Ball WLCSP Package (Text and Figures)	Universal
Replaced Typical Performance Characteristics Section	8
Updated Outline Dimensions	12
Changes to Ordering Guide	14

5/02—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted. The automotive temperature range is -40°C to $+125^{\circ}\text{C}$.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.25 0.3	0.35	0.4	Ω typ Ω max	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$; see Figure 13 $V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$; see Figure 13
On Resistance Flatness ($R_{FLAT(ON)}$)	0.05	0.07	0.08	Ω typ Ω max	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01 ± 0.25	± 3	± 30	nA typ nA max	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V/1 V}$, $V_D = 1\text{ V/4.5 V}$; see Figure 14 $V_S = 4.5\text{ V/1 V}$, $V_D = 1\text{ V/4.5 V}$; see Figure 14
Drain Off Leakage, I_D (Off)	± 0.01 ± 0.25	± 3	± 30	nA typ nA max	$V_S = 4.5\text{ V/1 V}$, $V_D = 1\text{ V/4.5 V}$; see Figure 14 $V_S = 4.5\text{ V/1 V}$, $V_D = 1\text{ V/4.5 V}$; see Figure 14
Channel On Leakage, I_D , I_S (On)	± 0.01 ± 0.25	± 3	± 30	nA typ nA max	$V_S = V_D = 1\text{ V}$, or 4.5 V ; see Figure 15 $V_S = V_D = 1\text{ V}$, or 4.5 V ; see Figure 15
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	35 45	50	55	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 16
t_{OFF}	9 15	18	21	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 16
Charge Injection	50			pC typ	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$; $C_L = 1\text{ nF}$; see Figure 17
Off Isolation	-61			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; $f = 100\text{ kHz}$; see Figure 18
Bandwidth -3 dB	12			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 19
C_S (Off)	180			pF typ	$f = 1\text{ MHz}$
C_D (Off)	180			pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	420			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001	1.0	2.0	μA typ μA max	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5.5 V

¹ On resistance parameters tested with $I_S = 10\text{ mA}$.

² Guaranteed by design, not subject to production test.

$V_{DD} = 2.7\text{ V}$ to 3.6 V , $GND = 0\text{ V}$, unless otherwise noted. The automotive temperature range is -40°C to $+125^{\circ}\text{C}$.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.4			Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$; see Figure 13
	0.6	0.65	0.7	Ω max	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$; see Figure 13
On Resistance Flatness ($R_{FLAT(ON)}$)	0.1	0.1	0.1	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01			nA typ	$V_{DD} = 3.6\text{ V}$
	± 0.25	± 3	± 30	nA max	$V_S = 3.3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3.3\text{ V}$; see Figure 14
Drain Off Leakage, I_D (Off)	± 0.01			nA typ	$V_S = 3.3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3.3\text{ V}$; see Figure 14
	± 0.25	± 3	± 30	nA max	$V_S = 3.3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3.3\text{ V}$; see Figure 14
Channel On Leakage, I_D , I_S (On)	± 0.01			nA typ	$V_S = V_D = 1\text{ V}$, or 3.3 V ; see Figure 15
	± 0.25	± 3	± 30	nA max	$V_S = V_D = 1\text{ V}$, or 3.3 V ; see Figure 15
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	40			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	55	60	65	ns max	$V_S = 1.5\text{ V}$; see Figure 16
t_{OFF}	9			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	15	18	21	ns max	$V_S = 1.5\text{ V}$; see Figure 16
Charge Injection	10			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 17
Off Isolation	−61			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 18
Bandwidth −3 dB	12			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 19
C_S (Off)	180			pF typ	$f = 1\text{ MHz}$
C_D (Off)	180			pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	420			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 3.6\text{ V}$
		1.0	2.0	μA max	Digital inputs = 0 V or 3.6 V

¹ On resistance parameters tested with $I_S = 10\text{ mA}$.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Inputs ¹	−0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs ¹	−0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, Pin S or Pin D	400 mA
Peak Current, Pin S or Pin D	800 mA, pulsed at 1 ms, 10% duty cycle max
Operating Temperature Range Automotive	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_{JMAX})	150°C
Package Power Dissipation MSOP	$(T_{JMAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
SOT-23 (4-Layer Board)	
θ_{JA} Thermal Impedance	119°C/W
θ_{JC} Thermal Impedance	91.99°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at Pin IN, Pin S, or Pin D are clamped by internal diodes. Current should be limited to the maximum ratings provided.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Truth Table

ADG801 (Pin IN)	ADG802 (Pin IN)	Switch Condition
0	1	Off
1	0	On

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

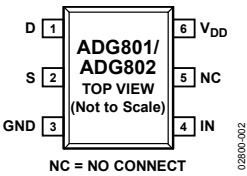


Figure 2. 6-Lead SOT-23 (RJ-6)

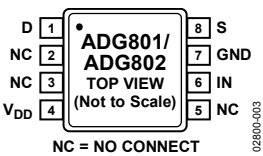


Figure 3. 8-Lead MSOP (RM-8)

Table 5. Pin Function Descriptions

Pin Number		Mnemonic	Description
SOT-23	MSOP		
1	1	D	Drain Terminal. Can be an input or an output.
2	8	S	Source Terminal. Can be an input or an output.
3	7	GND	Ground (0 V) Reference.
4	6	IN	Logic Control Input.
5	2, 3, 5	NC	No Connect. Do not connect to this pin.
6	4	V _{DD}	Most Positive Power Supply Potential.

TYPICAL PERFORMANCE CHARACTERISTICS

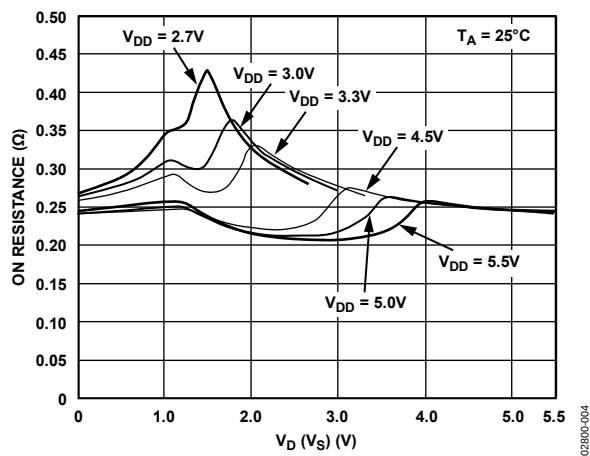
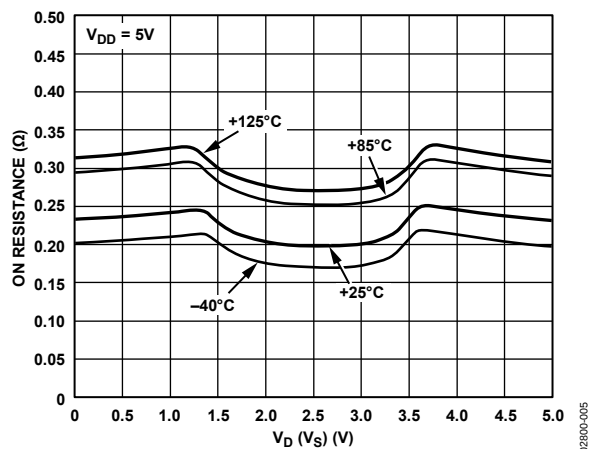
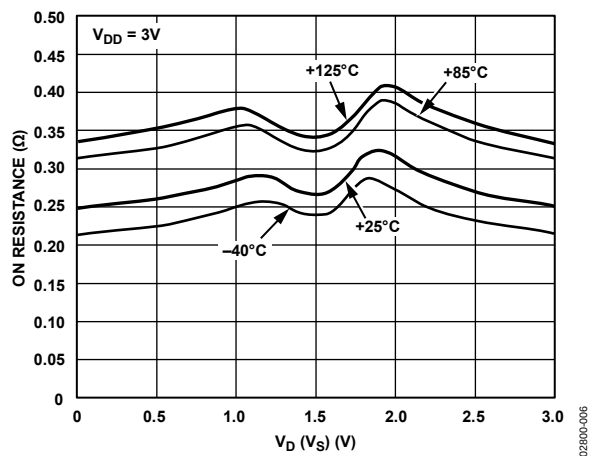
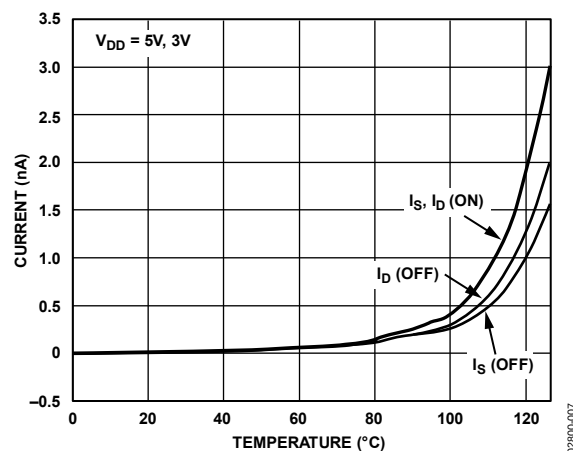
Figure 4. On Resistance vs. V_D (V_S)Figure 5. On Resistance vs. V_D (V_S) for Different TemperaturesFigure 6. On Resistance vs. V_D (V_S) for Different Temperatures

Figure 7. Leakage Current vs. Temperature

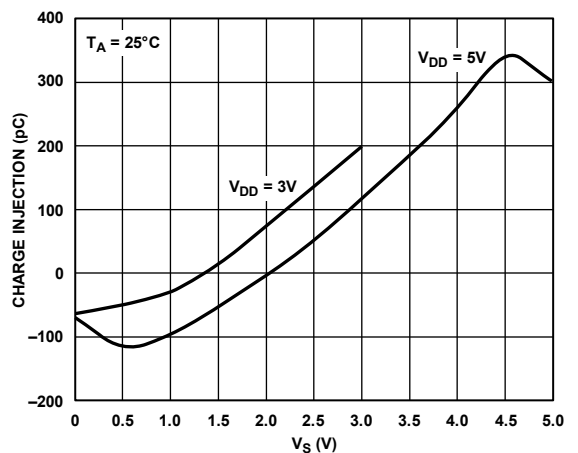
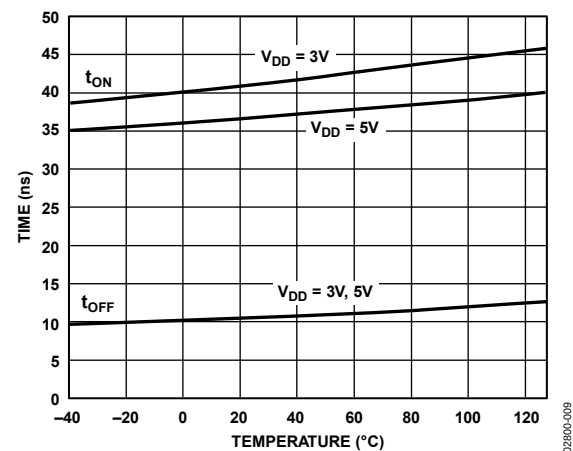


Figure 8. Charge Injection vs. Source Voltage

Figure 9. t_{ON}/t_{OFF} Times vs. Temperature

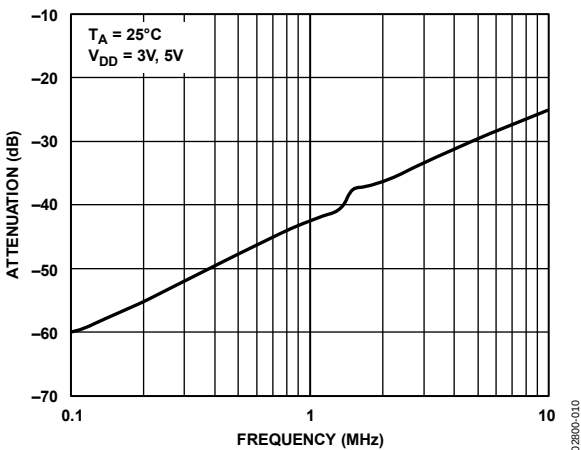


Figure 10. Off Isolation vs. Frequency

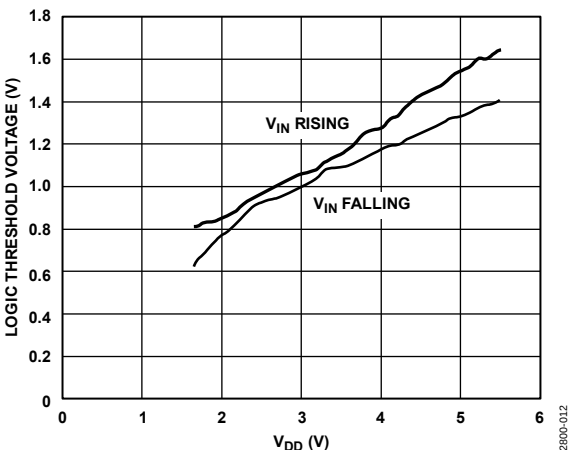


Figure 12. Logic Threshold Voltage vs. Supply Voltage

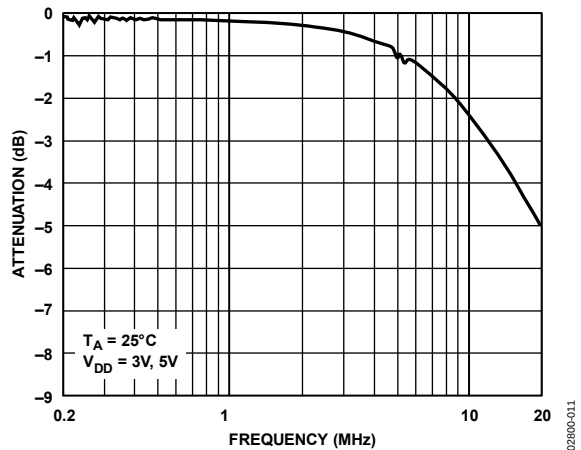


Figure 11. On Response vs. Frequency

TERMINOLOGY

V_{DD}

The most positive power supply potential.

I_{DD}

Positive supply current.

GND

Ground (0 V) reference.

S

The source terminal can be an input or an output.

D

The drain terminal can be an input or an output.

IN

Logic control input.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT(ON)}

The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

The off switch source capacitance is measured with reference to ground.

C_D (Off)

The off switch drain capacitance is measured with reference to ground.

C_D, C_S (On)

The on switch capacitance is measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

The delay between applying the digital control input and when the output switches on. See Figure 16.

t_{OFF}

The delay between applying the digital control input and when the output switches off.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

TEST CIRCUITS

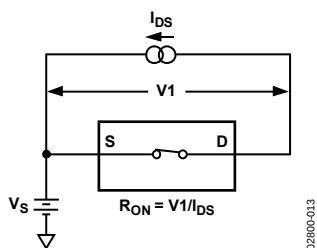


Figure 13. On Resistance

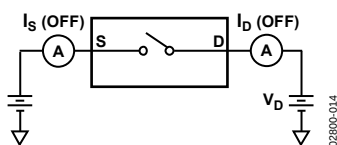


Figure 14. Off Leakage

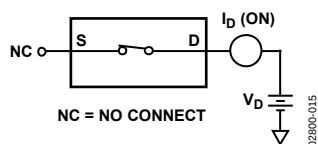


Figure 15. On Leakage

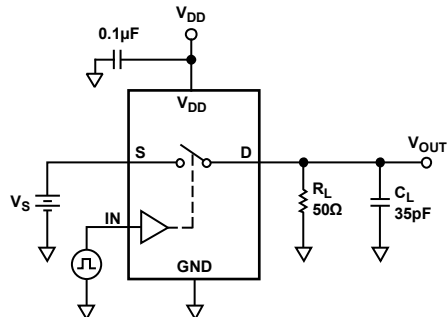


Figure 16. Switching Times

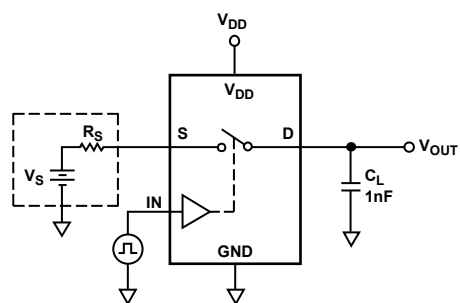
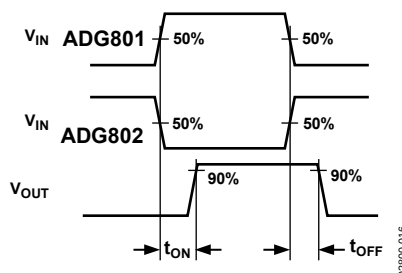
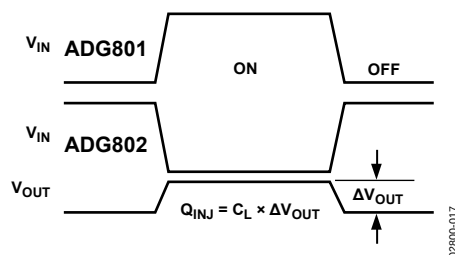


Figure 17. Charge Injection



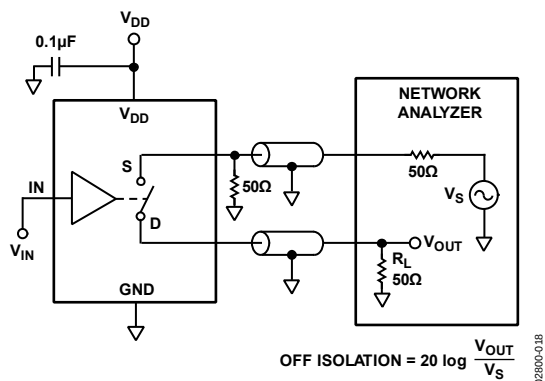


Figure 18. Off Isolation

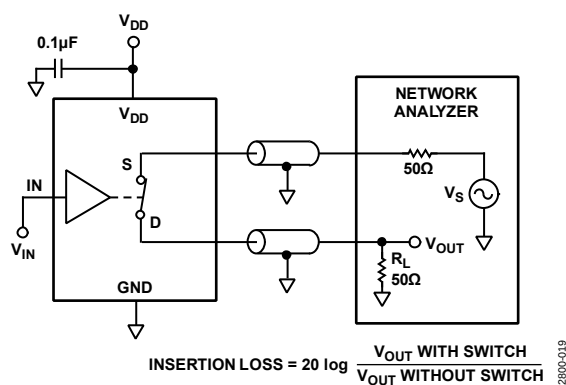
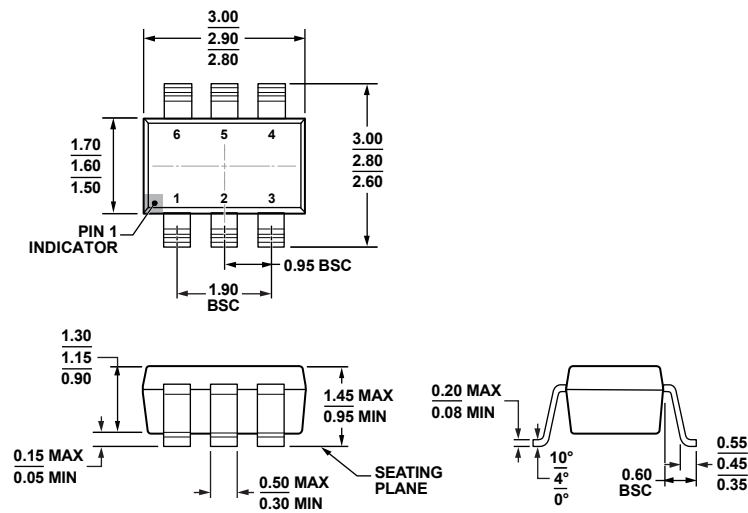


Figure 19. Bandwidth

OUTLINE DIMENSIONS

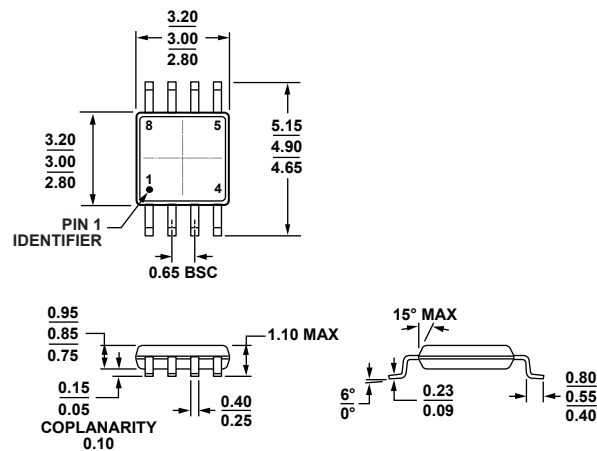


COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 20. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)

Dimensions shown in millimeters

12-16-2008-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 21. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

10-07-2008-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding ²
ADG801BRM	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SLB
ADG801BRM-REEL	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SLB
ADG801BRM-REEL7	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SLB
ADG801BRMZ	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S06
ADG801BRMZ-REEL	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S06
ADG801BRMZ-REEL7	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S06
ADG801BRT-500RL7	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SLB
ADG801BRT-REEL7	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SLB
ADG801BRTZ-500RL7	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S06
ADG801BRTZ-REEL	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S06
ADG801BRTZ-REEL7	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S06
ADG802BRM	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SMB
ADG802BRM-REEL	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SMB
ADG802BRM-REEL7	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SMB
ADG802BRMZ	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S0F
ADG802BRMZ-REEL	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S0F
ADG802BRMZ-REEL7	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S0F
ADG802BRT-500RL7	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SMB
ADG802BRTZ-500RL7	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S0F
ADG802BRTZ-REEL	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S0F
ADG802BRTZ-REEL7	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S0F

¹ Z = RoHS Compliant Part.² Branding on SOT-23 and MSOP packages is limited to three characters due to space constraints.

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