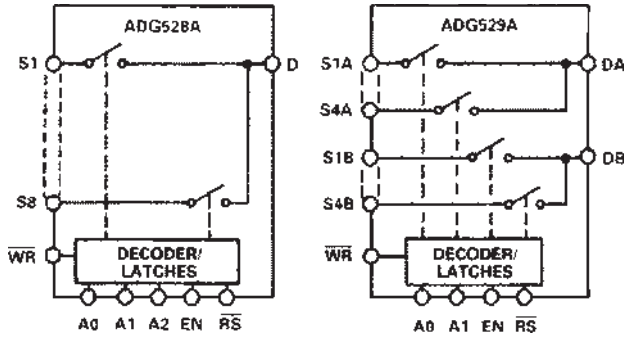
CMOS Latched 4-/8-Channel Analog Multiplexers

ADG528A

FEATURES

44 V Supply Maximum Rating
V_{SS} to V_{DD} Analog Signal Range
Single-/Dual-Supply Specifications
Wide Supply Ranges (10.8 V to 16.5 V)
Microprocessor Compatible (100 ns $\overline{WR}$ Pulse)
Extended Plastic Temperature Range
(–40°C to +85°C)
Low Leakage (20 pA typ)
Low Power Dissipation (28 mW max)
Available in 18-Lead DIP/SOIC and 20-Lead PLCC Packages
Superior Alternative to:
DG528
DG529
ADG529A is obsolete

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG528A and ADG529A are CMOS monolithic analog multiplexers with eight channels and four dual channels, respectively. On-chip latches facilitate microprocessor interfacing. The ADG528A switches one of eight inputs to a common output, depending on the state of three binary addresses and an enable input. The ADG529A switches one of four differential inputs to a common differential output, depending on the state of two binary addresses and an enable input. Both devices have TTL and 5 V CMOS logic-compatible digital inputs.

The ADG528A and ADG529A are designed on an enhanced LC^2MOS process, which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8 V to 16.5 V single- or dual-supply range. These multiplex-ers also feature high switching and low R_{ON}.

The ADG529A is no longer available.

PRODUCT HIGHLIGHTS

1. Single-/dual-supply specifications with a wide tolerance. The devices are specified in the 10.8 V to 16.5 V range for both single- and dual-supplies.
2. Easily Interfaced
   The ADG528A and ADG529A can be easily interfaced with microprocessors. The $\overline{WR}$ signal latches the state of the address control lines and the enable line. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). $\overline{RS}$ can be tied to the microprocessor reset pin.
3. Extended Signal Range
   The enhanced LC^2MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
4. Break-Before-Make Switching
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage
   Leakage currents in the range of 20 pA make these multiplexers suitable for high precision circuits.

ADG528A–SPECIFICATIONS

DUAL SUPPLY (V_{DD} = +10.8 V to +16.5 V, V_{SS} = –10.8 V to –16.5 V, unless otherwise noted.)

Parameter	ADG528A ADG529A K Version +25°C	–40°C to +85°C	ADG528A ADG529A B Version +25°C	–40°C to +85°C	ADG528A ADG529A T Version +25°C	–55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	$-10\ V \le V_S \le +10\ V$, I_{DS} = 1 mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15 V (±10%), V_{SS} = –15 V (±10%)
					300	400	Ω max	V_{DD} = 15 V (±5%), V_{SS} = –15 V (±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	$-10\ V \le V_S \le +10\ V$, I_{DS} = 1 mA
R_{ON} Match	5		5		5		% typ	$-10\ V \le V_S \le +10\ V$, I_{DS} = 1 mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Input Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 3
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 4
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	V1 = ±10 V, V2 = ∓10 V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	µA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	200		200		200		ns typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	Test Circuits 8 and 9
	300	400	300	400	300	400	ns max	
t_{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	Test Circuits 8 and 10
	300	400	300	400	300	400	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H, Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF,
	50		50		50		dB min	V_S = 7 V rms, f = 100 kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D (OFF)								
ADG528A	22		22		22		pF typ	V_{EN} = 0.8 V
ADG529A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0 V; Test Circuit 11

Parameter	ADG528A ADG529A K Version +25°C	–40°C to +85°C	ADG528A ADG529A B Version +25°C	–40°C to +85°C	ADG528A ADG529A T Version +25°C	–55°C to +125°C	Units	Comments
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	$V_{IN} = V_{INL}$ or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		µA typ	$V_{IN} = V_{INL}$ or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		2.8		2.8		2.8	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +10.8 V to +16.5 V, V_{SS} = GND = 0 V, unless otherwise noted.)

Parameter	ADG528A ADG529A K Version +25°C	–40°C to +85°C	ADG528A ADG529A B Version +25°C	–40°C to +85°C	ADG528A ADG529A T Version +25°C	–55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}								
	500		500		500		Ω typ	GND ≤ V_S ≤ +10 V, I_{DS} = 0.5 mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	GND ≤ V_S ≤ +10 V, I_{DS} = 0.5 mA
R_{ON} Match	5		5			5	% typ	GND ≤ V_S ≤ +10 V, I_{DS} = 0.5 mA
I_S (OFF), Off Input								
Leakage	0.02		0.02		0.02		nA typ	V1 = +10 V/GND, V2 = GND/+10 V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Input								
Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/GND, V2 = GND/+10 V;
ADG528A	1	100	1	100	1	100	nA max	Test Circuit 3
ADG529A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel								
Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/GND, V2 = GND/+10 V;
ADG528A	1	100	1	100	1	100	nA max	Test Circuit 4
ADG529A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	V1 = +10 V/GND, V2 = GND/+10 V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	µA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	300		300		300		ns typ	V1 = +10 V/GND, V2 = GND/+10 V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	250		250		250		ns typ	Test Circuits 8 and 9
	450	600	450	600	450	600	ns max	
t_{OFF} (EN, $\overline{RS}$)	250		250		250		ns typ	Test Circuits 8 and 10
	450	600	450	600	450	600	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1

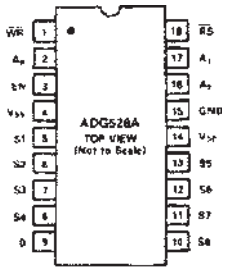
Parameter	ADG528A ADG529A K Version –40°C to +25°C	+85°C	ADG528A ADG529A B Version –40°C to +25°C	+85°C	ADG528A ADG529A T Version –55°C to +25°C	+125°C	Units	Comments
DYNAMIC CHARACTERISTICS[1] (Cont'd)								
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF,
	50		50		50		dB min	V_S = 3.5 V rms, f = 100 kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D (OFF)								
ADG528A	22		22		22		pF typ	V_{EN} = 0.8 V
ADG529A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0 V; Test Circuit 11
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	11		10		10		mW typ	
		25		25		25	mW max	

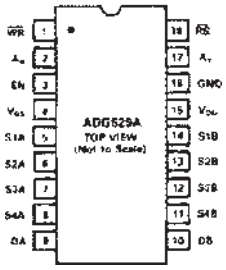
NOTE
[1]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

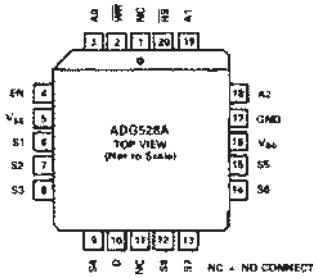
PIN CONFIGURATIONS

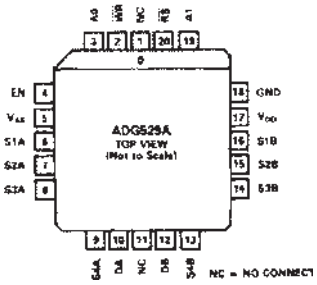
DIP/SOIC





PLCC





ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C, unless otherwise noted)

V_{DD} to V_{SS} . . . . . 44 V
V_{DD} to GND . . . . . 25 V
V_{SS} to GND . . . . . –25 V
Analog Inputs[2]
Voltage at S, D . . . . . V_{SS} – 2 V to V_{DD} + 2 V or 20 mA, whichever Occurs First
Continuous Current, S or D . . . . . 20 mA
Pulsed Current, S or D
1 ms duration, 10% Duty Cycle . . . . . 40 mA
Digital Inputs[1]
Voltage at A, EN, $\overline{WR}$, $\overline{RS}$ . . . . . V_{SS} – 4 V to V_{DD} + 4 V or 20 mA, whichever Occurs First
Power Dissipation (Any Package)
Up to +75°C . . . . . 470 mW
Derates above +75°C . . . . . 6 mW/°C
Operating Temperature
Commercial (K Version) . . . . . –40°C to +85°C
Industrial (B Version) . . . . . –40°C to +85°C
Extended (T Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by diodes. Current should be limited to the maximum rating above.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TRUTH TABLES

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	⌐	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care *ADG528A*

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	⌐	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care *ADG529A*

TIMING DIAGRAMS

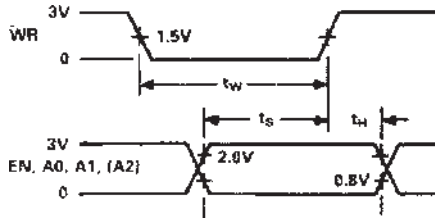


Figure 1.

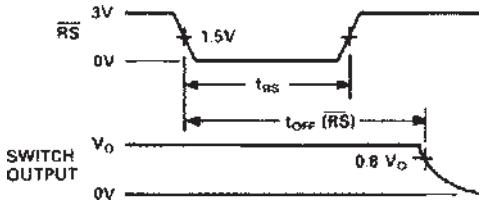


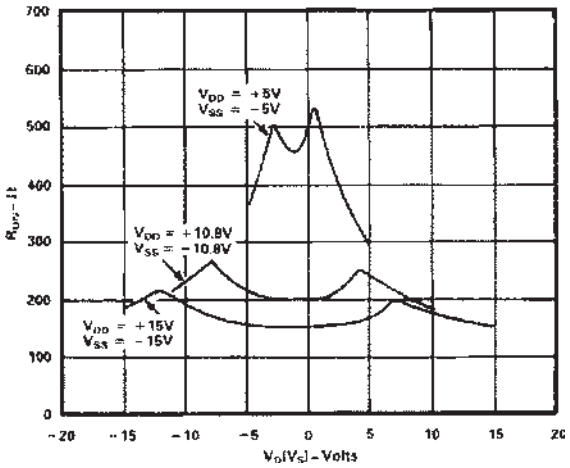
Figure 2.

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

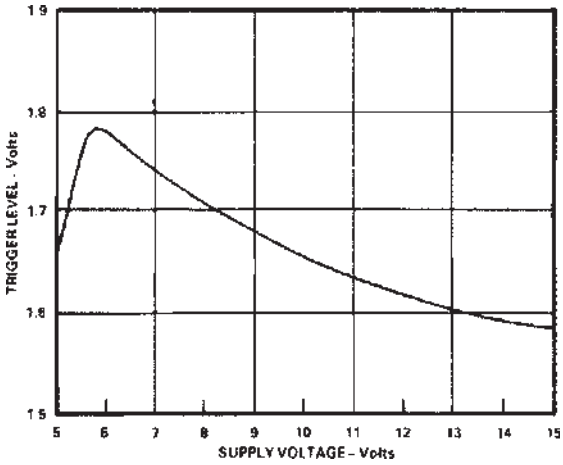
Figure 2 shows the Reset Pulse Width, t_{RS}, and Reset Turn-off Time, t_{OFF} ($\overline{RS}$).

Note: All digital input signals rise and fall times measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.

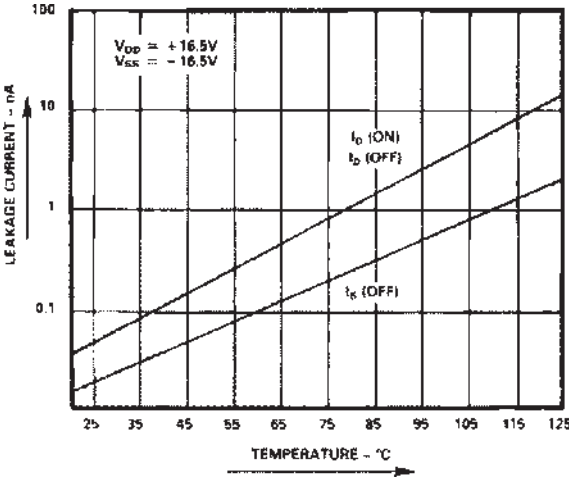
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.



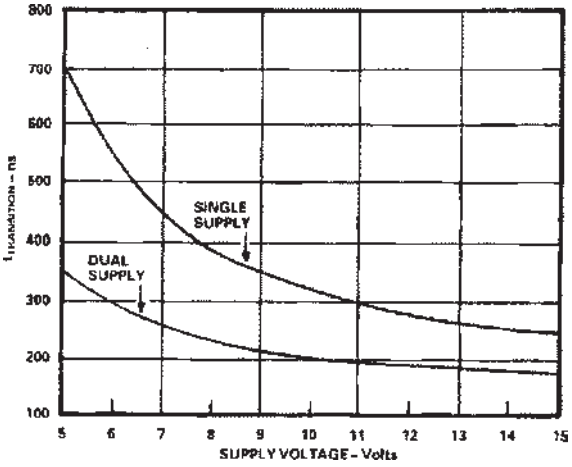
TPC 1. R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



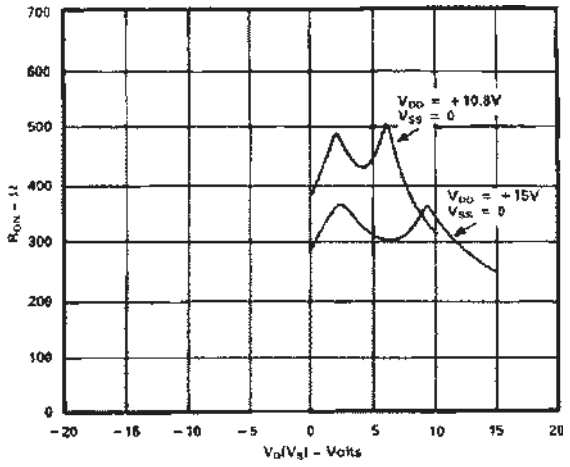
TPC 4. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C



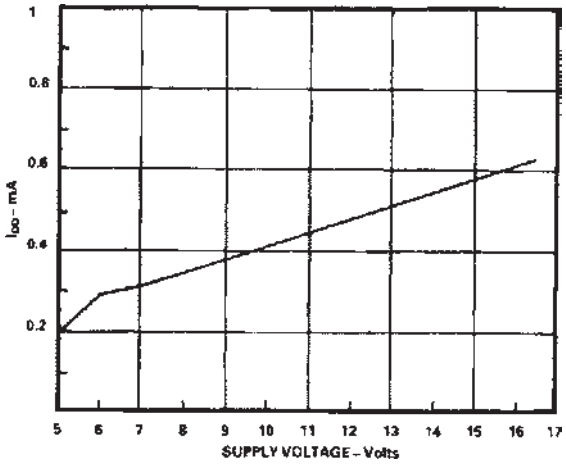
TPC 2. Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



TPC 5. $t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = +25°C (Note: For V_{DD} and $|V_{SS}| < 10$ V; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)

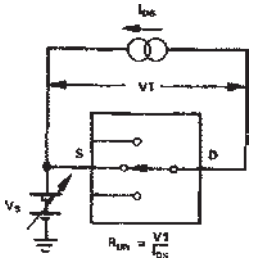


TPC 3. R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C

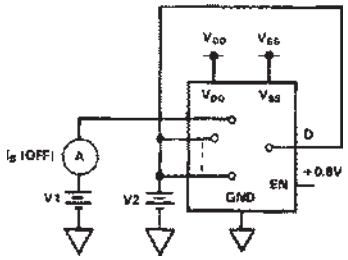


TPC 6. I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

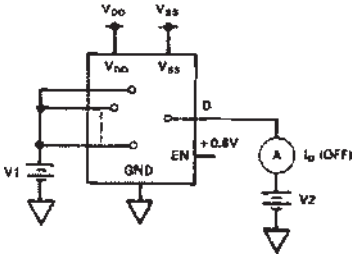
Test Circuits



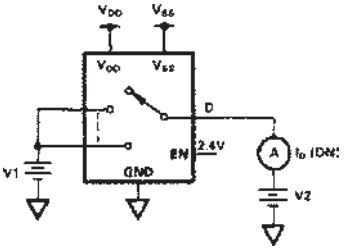
Test Circuit 1. R_{ON}



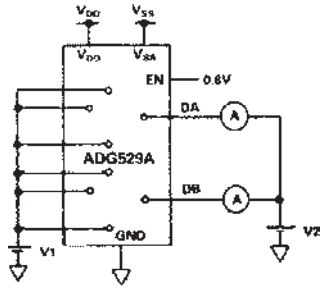
Test Circuit 2. I_S (OFF)



Test Circuit 3. I_D (OFF)

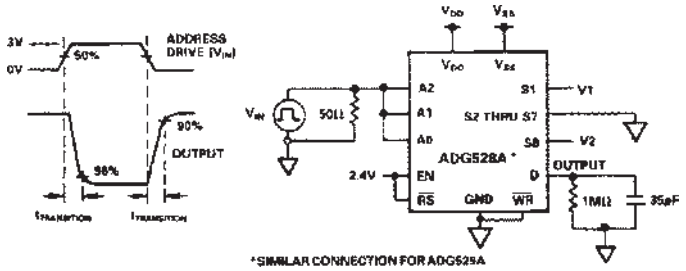


Test Circuit 4. I_D (ON)

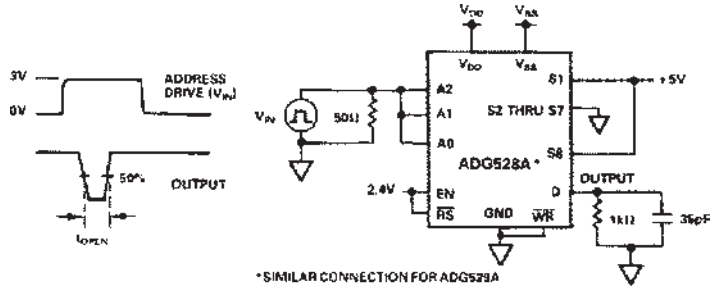


$I_{DIFF} = I_{DA}(OFF) - I_{DB}(OFF)$

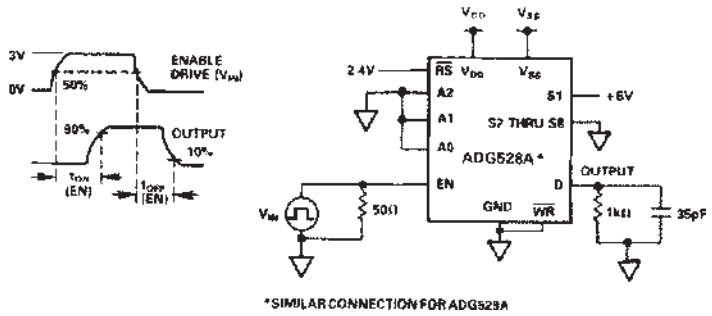
Test Circuit 5. I_{DIFF}



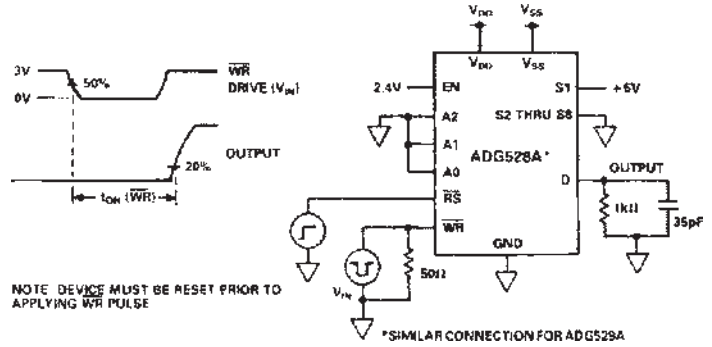
Test Circuit 6. Switching Time of Multiplexer, $t_{TRANSITION}$



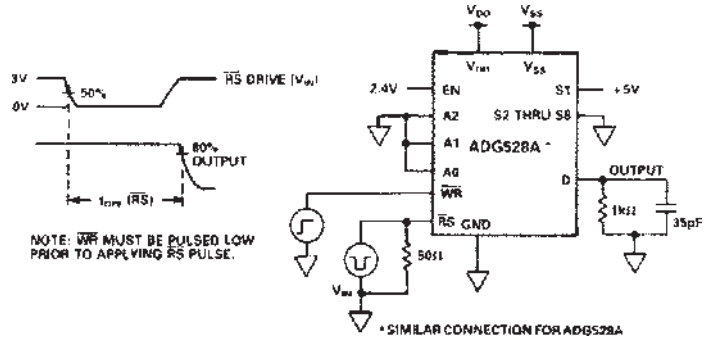
Test Circuit 7. Break-Before-Make Delay, t_{OPEN}



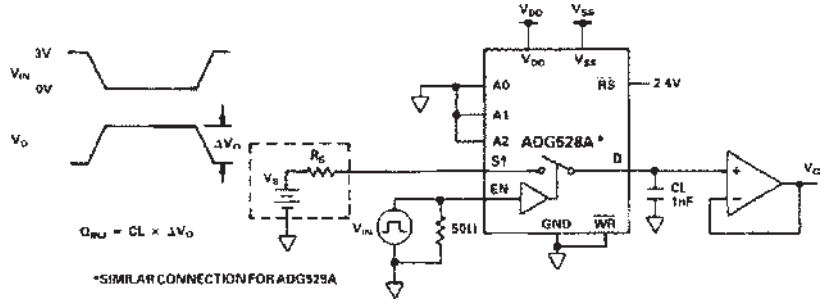
Test Circuit 8. Enable Delay, t_{ON} (EN), t_{OFF} (EN)



Test Circuit 9. Write Turn-On Time, t_{ON} ($\overline{WR}$)



Test Circuit 10. Reset Turn-Off Time, t_{OFF} ($\overline{RS}$)

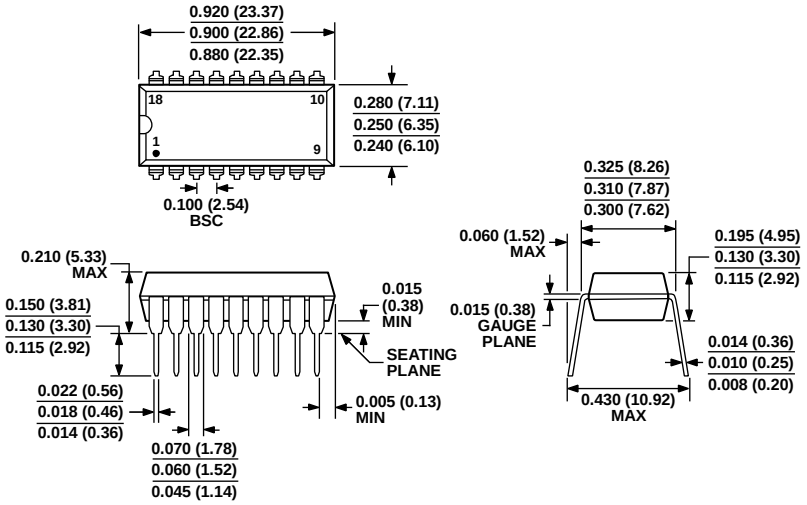


Test Circuit 11. Charge Injection

TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the RON of any two channels
R_{ON} Drift	Change in RON versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off.
I_D (OFF)	Drain terminal leakage current when the switch is off.
I_D (ON)	Leakage current that flows from the closed switch into the body.
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

OUTLINE DIMENSIONS

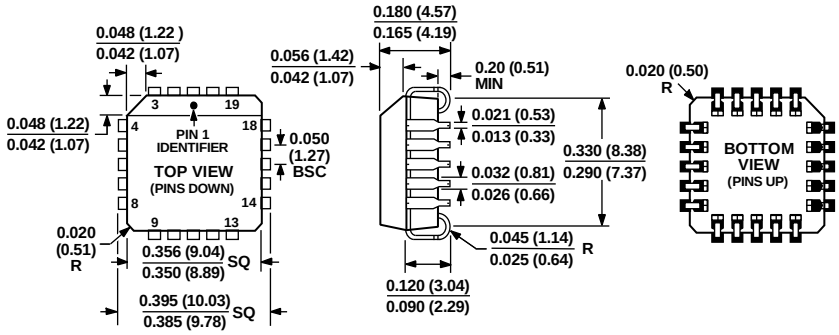


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070706-A

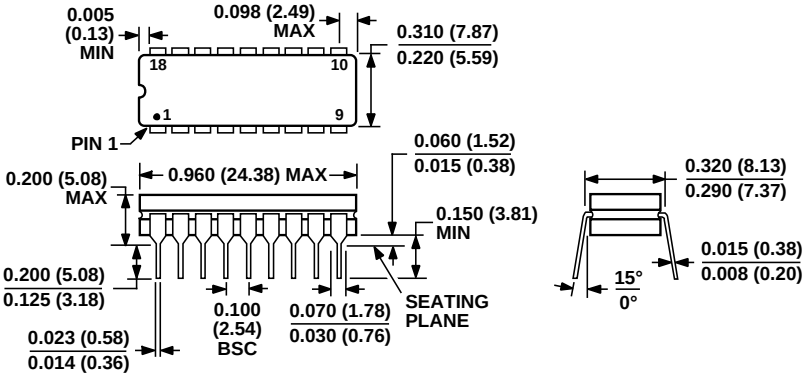
Figure 1. 18-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-18)
Dimensions Shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 2. 20-Lead Plastic Leaded Chip Carrier [PLCC]
(P-20)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 3. 18-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-18)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG528AKN	−40°C to +85°C	18-Lead Plastic Dual In-Line Package [PDIP]	N–18
ADG528AKNZ	−40°C to +85°C	18-Lead Plastic Dual In-Line Package [PDIP]	N–18
ADG528AKP	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P–20
ADG528AKP-REEL	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P–20
ADG528AKPZ	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG528AKPZ-REEL	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG528ATQ	−55°C to +125°C	18-Lead Ceramic Dual In-Line Package [CERDIP]	Q-18
ADG528ABCHIPS	−55°C to +125°C	DIE	

[1] Z = RoHS Compliant Part.

REVISION HISTORY

8/2017—Rev. B to Rev. C

Added ADG529A Obsolete Note....1
Updated Outline Dimensions....11
Changes to Ordering Guide` 12

10/2004—Rev. A to Rev. B

Deleted 20-Lead LCC Package .... Universal
Changes to Features 5
Changes to Ordering Guide....6
SOIC added to DIP Pin Configuration 5

D03337-0-8/17(C)