4 GHz to 18 GHz Divide-by-8 Prescaler

ADF5002

FEATURES

- Divide-by-8 prescaler
- High frequency operation: 4 GHz to 18 GHz
- Integrated RF decoupling capacitors
- Low power consumption
  - Active mode: 30 mA
  - Power-down mode: 7 mA
- Low phase noise: −153 dBc/Hz
- Single dc supply: 3.3 V compatible with ADF4xxx PLLs
- Temperature range: −40°C to +105°C
- Small package: 3 mm × 3 mm LFCSP

APPLICATIONS

- PLL frequency range extender
- Point-to-point radios
- VSAT radios
- Communications test equipment

GENERAL DESCRIPTION

The ADF5002 prescaler is a low noise, low power, fixed RF divider block that can be used to divide down frequencies as high as 18 GHz to a lower frequency suitable for input to a PLL IC, such as the ADF4156 or the ADF4106. The ADF5002 provides a divide-by-8 function. The ADF5002 operates from a 3.3 V supply and has differential 100 Ω RF outputs to allow direct interface to the differential RF inputs of PLLs such as the ADF4156 and ADF4106.

FUNCTIONAL BLOCK DIAGRAM

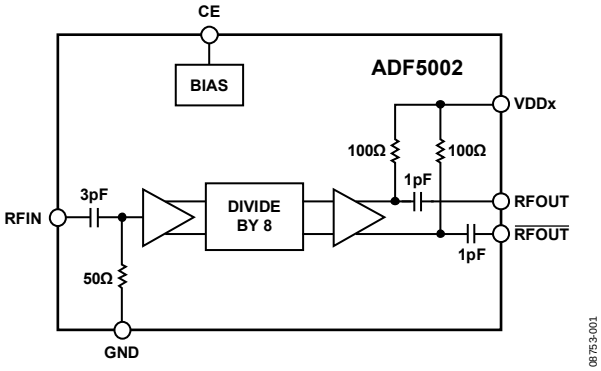


Figure 1.

Rev. 0
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
©2010 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

Features 1
Applications 1
General Description 1
Functional Block Diagram 1
Revision History 2
Specifications 3
Absolute Maximum Ratings 4
ESD Caution 4
Pin Configuration and Function Descriptions 5
Typical Performance Characteristics 6
Evaluation Board PCB 7
PCB Material Stack-Up 7
Bill of Materials 7
Application Circuit 8
Outline Dimensions 9
Ordering Guide 9

REVISION HISTORY

6/10—Revision 0: Initial Version

SPECIFICATIONS

VDD1 = VDD2 = 3.3 V ± 10%, GND = 0 V; dBm referred to 50 Ω; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +105°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
Input Frequency	4		18	GHz	
RF Input Sensitivity	−10		+10	dBm	4 GHz to 18 GHz
Output Power	−10	−5		dBm	Single-ended output connected into a 50 Ω load
	−7	−2		dBm	Differential outputs connected into a 100 Ω differential load
Output Voltage Swing	200	330		mV p-p	Peak-to-peak voltage swing on each single-ended output, connected into a 50 Ω load
	400	660		mV p-p	Peak-to-peak voltage swing on differential output, connected into a 100 Ω differential load
		1000		mV p-p	Peak-to-peak voltage swing on each single-ended output, no load condition
Phase Noise		−153		dBc/Hz	Input frequency (f_{IN}) = 12 GHz, offset = 100 kHz
Reverse Leakage		−60		dBm	RF input power (P_{IN}) = 0 dBm, RF_{OUT} = 4 GHz
Second Harmonic Content		−38		dBc	
Third Harmonic Content		−12		dBc	
Fourth Harmonic Content		−20		dBc	
Fifth Harmonic Content		−19		dBc	
CE INPUT					
Input High Voltage, V_{IH}	2.2			V	
Input Low Voltage, V_{IL}			0.3	V	
POWER SUPPLIES					
Voltage Supply	3.0	3.3	3.6	V	
I_{DD} (I_{DD1} + I_{DD2})					
Active		30	60	mA	CE is high
Power-Down		7	25	mA	CE is low

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VDDx to GND	−0.3 V to +3.9 V
RFIN	10 dBm
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
LFCSP Thermal Impedance	
Junction-to-Ambient (θ_{JA})	90°C/W
Junction-to-Case (θ_{JC})	30°C/W
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of 2 kV, human body model (HBM), and is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

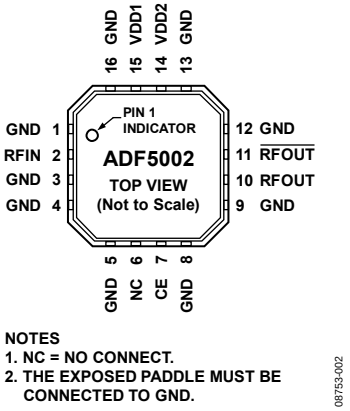


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 5, 8, 9, 12, 13, 16	GND	RF Ground. All ground pins should be tied together.
2	RFIN	Single-Ended 50 Ω Input to the RF Prescaler. This pin is ac-coupled internally via a 3 pF capacitor.
6	NC	No Connect. This pin can be left unconnected.
7	CE	Chip Enable. This pin is active high. When CE is brought low, the part enters power-down mode. If this functionality is not required, the pin can be left unconnected because it is pulled up internally through a weak pull-up resistor.
10	RFOUT	Divided-Down Output of the Prescaler. This pin has an internal 100 Ω load resistor tied to VDD2 and an ac-coupling capacitor of 1 pF.
11	$\overline{\text{RFOUT}}$	Complementary Divided-Down Output of the Prescaler. This pin has an internal 100 Ω load resistor tied to VDD2 and an ac-coupling capacitor of 1 pF.
14	VDD2	Voltage Supply for the Output Stage. This pin should be decoupled to ground with a 0.1 µF capacitor in parallel with a 10 pF capacitor and can be tied directly to VDD1.
15	VDD1	Voltage Supply for the Input Stage and Divider Block. This pin should be decoupled to ground with a 0.1 µF capacitor in parallel with a 10 pF capacitor.
	EPAD	The LFCSP has an exposed paddle that must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

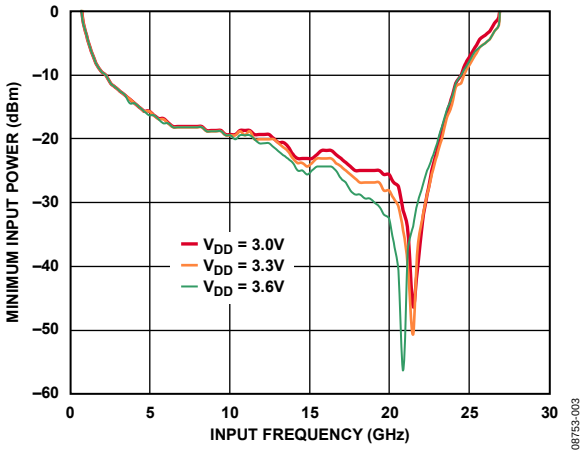


Figure 3. RF Input Sensitivity

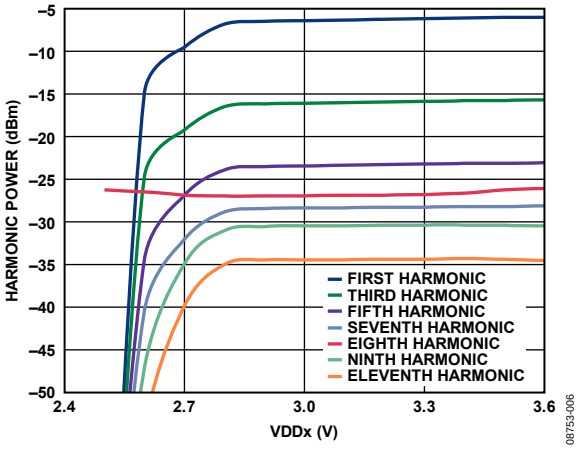


Figure 6. RF Output Harmonic Content vs. VDDx

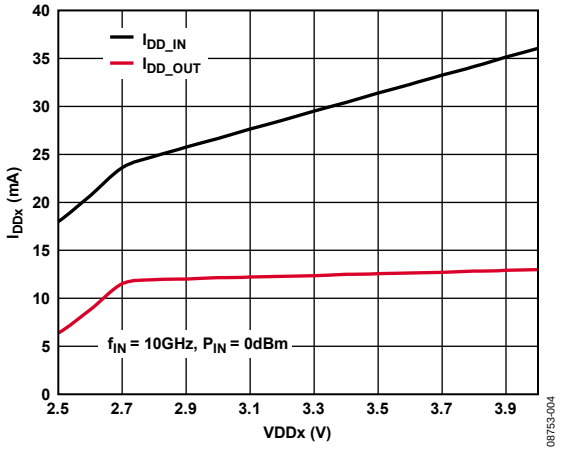


Figure 4. I_{DD1} and I_{DD2} vs. VDDx, f_{IN} = 10 GHz, P_{IN} = 0 dBm

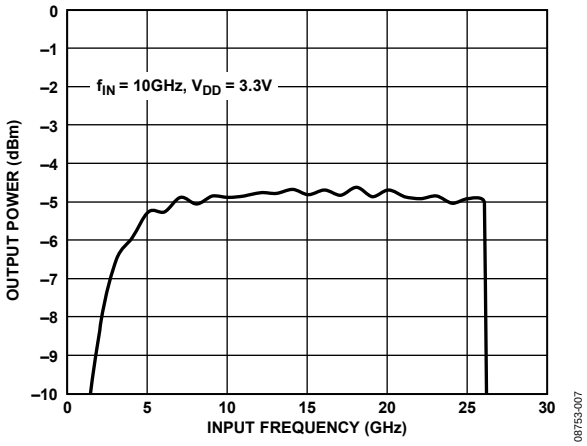


Figure 7. RF Output Power vs. RF Input Frequency, f_{IN} = 10 GHz, V_{DD} = 3.3 V

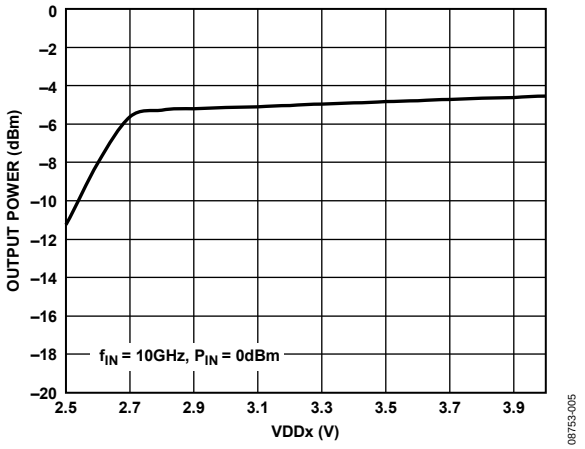


Figure 5. RF Output Power (Single-Ended) vs. VDDx, f_{IN} = 10 GHz, P_{IN} = 0 dBm

EVALUATION BOARD PCB

The evaluation board has four connectors as shown in Figure 8. The RF input connector (J4) is a high frequency precision SMA connector from Emerson. This connector is mechanically compatible with SMA, 3.5 mm, and 2.92 mm cables.

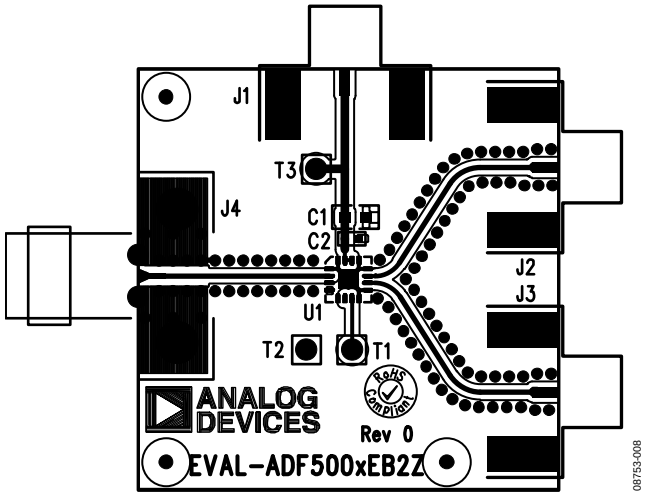


Figure 8. Evaluation Board Silkscreen—Top View

The evaluation board is powered from a single 3.0 V to 3.6 V supply, which should be connected to the J1 SMA connector. The power supply can also be connected using the T3 (VDDx) and T2 (GND) test points.

The differential RF outputs are brought out on the J2 and J3 SMA connectors. If only one of the outputs is being used, the unused output should be correctly terminated using a 50 Ω SMA termination.

The chip enable (CE) pin can be controlled using the T1 test point. If this function is not required, the test point can be left unconnected.

PCB MATERIAL STACK-UP

The evaluation board is built using Rogers RO4003C material (0.008 inch). RF track widths are 0.015 inch to achieve a controlled 50 Ω characteristic impedance. The complete PCB stack-up is shown in Figure 9.

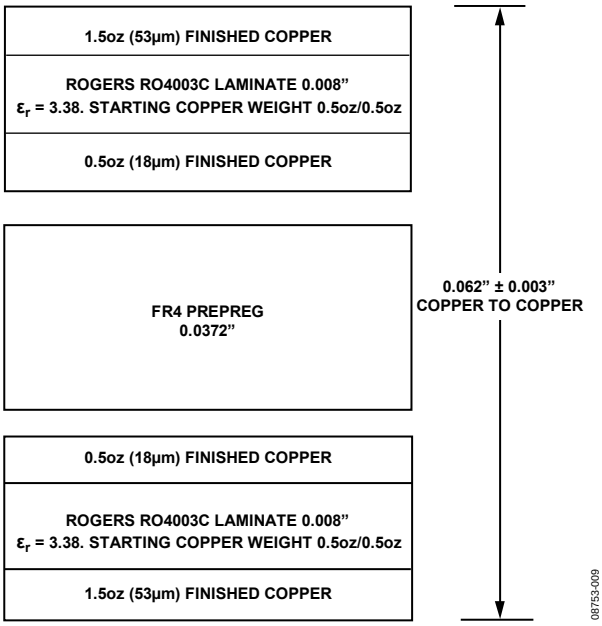


Figure 9. Evaluation Board PCB Layer Stack-Up

BILL OF MATERIALS

Table 4.

Qty	Reference Designator	Description	Supplier	Part Number
1	C1	0.1 µF, 0603 capacitor	Murata	GRM188R71H104KA93D
1	C2	10 pF, 0402 capacitor	Murata	GRM1555C1H100JZ01D
3	J1, J2, J3	SMA RF connector	Emerson	142-0701-851
1	J4	SMA RF connector	Emerson	142-0761-801
3	T1, T2, T3	Test points	Vero	20-2137
1	U1	ADF5002 RF prescaler	Analog Devices, Inc.	ADF5002BCPZ

APPLICATION CIRCUIT

The ADF5002 can be connected either single-ended or differentially to any of the Analog Devices PLL family of ICs. It is recommended that a differential connection be used for best performance and to achieve maximum power transfer. The application circuit shown in Figure 10 shows the ADF5002 used as the RF prescaler in a microwave 16 GHz PLL loop. The ADF5002 divides the 16 GHz RF signal down to 2 GHz, which is input differentially into the ADF4156 PLL. An active filter topology, using the OP184 op amp, is used to provide the wide tuning ranges typically required by microwave VCOs.

The positive input pin of the OP184 is biased at half the ADF4156 charge pump supply (V_P). This can be easily achieved using a simple resistor divider, ensuring sufficient decoupling close to the +IN A pin of the OP184. This configuration, in turn, allows the use of a single positive supply for the op amp. Alternatively, to optimize performance by ensuring a clean bias voltage, a low noise regulator such as the ADP150 can be used to power the resistor divider network or the +IN A pin directly.

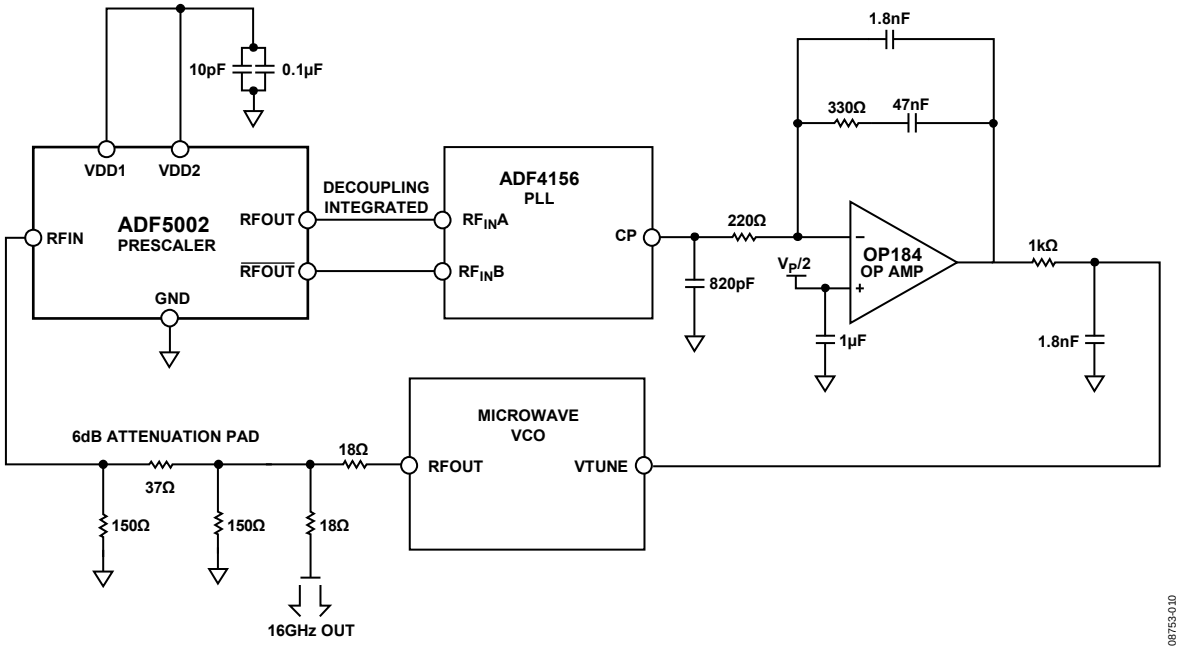


Figure 10. ADF5002 Used as the RF Prescaler in a Microwave 16 GHz PLL Loop

OUTLINE DIMENSIONS

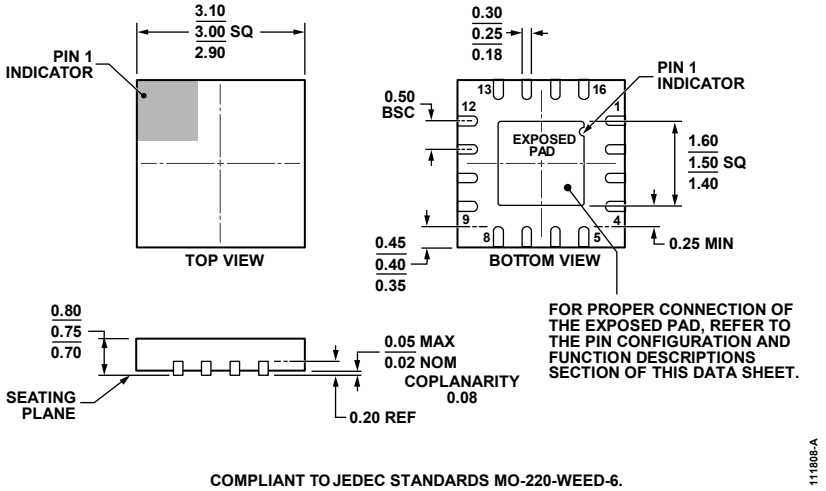


Figure 11. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-18)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADF5002BCPZ	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-16-18	Q1U
ADF5002BCPZ-RL7	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ), 7″ Tape and Reel	CP-16-18	Q1U
EVAL-ADF5002EB2Z		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

©2010 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D08753-0-6/10(0)