Polyphase Energy Metering IC with Phase Drop Indication

Preliminary Technical Data

ADE7762

FEATURES

- **High accuracy supports 50 Hz/60 Hz IEC62053-21**
- **Less than 0.1% error over a dynamic range of 500 to 1**
- **Compatible with 3-phase 3-wire delta and 3-phase 4-wire Wye configurations**
- **Supplies average active power on the frequency outputs F1 and F2**
- **High frequency output (CF) is intended for calibration and supplies instantaneous active power**
- **Logic output REVP indicates a potential miswiring or negative power on the sum of all phases**
- **Dropout indication for each phase on LED driver pins**
- **Phase sequence error detection**
- **Direct drive for electromechanical counters and 2-phase stepper motors (F1 and F2)**
- **Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time**
- **On-chip power supply monitoring**
- **On-chip creep protection (no load threshold)**
- **On-chip reference 2.4 V ± 8% (25 ppm/°C typical) with external overdrive capability**
- **Single 5 V supply, low power (TBD mW typical)**
- **Low cost CMOS process**

GENERAL DESCRIPTION

The ADE7762[1] is a high accuracy polyphase electrical energy measurement IC. The ADE7762 specifications surpass the accuracy requirements as quoted in the IEC62053-21 standard.

The only analog circuitry used in the ADE7762 is in the analog-to-digital converters (ADCs) and reference circuit. All other signal processing (for example, multiplication, filtering, and summation) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The ADE7762 supplies average active power information on the low frequency outputs, F1 and F2. These logic outputs can be used to directly drive an electromechanical counter or to interface with an MCU. The CF logic output gives instantaneous active power information. This output is intended to be used for calibration purposes.

The ADE7762 includes a power supply monitoring circuit on the V_{DD} pin. The ADE7762 remains inactive until the supply voltage on V_{DD} reaches 4 V. If the supply falls below 4 V, the ADE7762 also resets and no pulses are issued on F1, F2, and CF.

A multiple multiplexed logic output provides phase dropout per phase, reverse polarity per phase, and a phase sequence error.

Internal phase matching circuitry ensures that the voltage and current channels are phase matched. An internal no load threshold ensures the ADE7762 does not exhibit any creep when there is no load.

The ADE7762 is available in a 28-lead SOIC package.

[1] Patent pending.

FUNCTIONAL BLOCK DIAGRAM

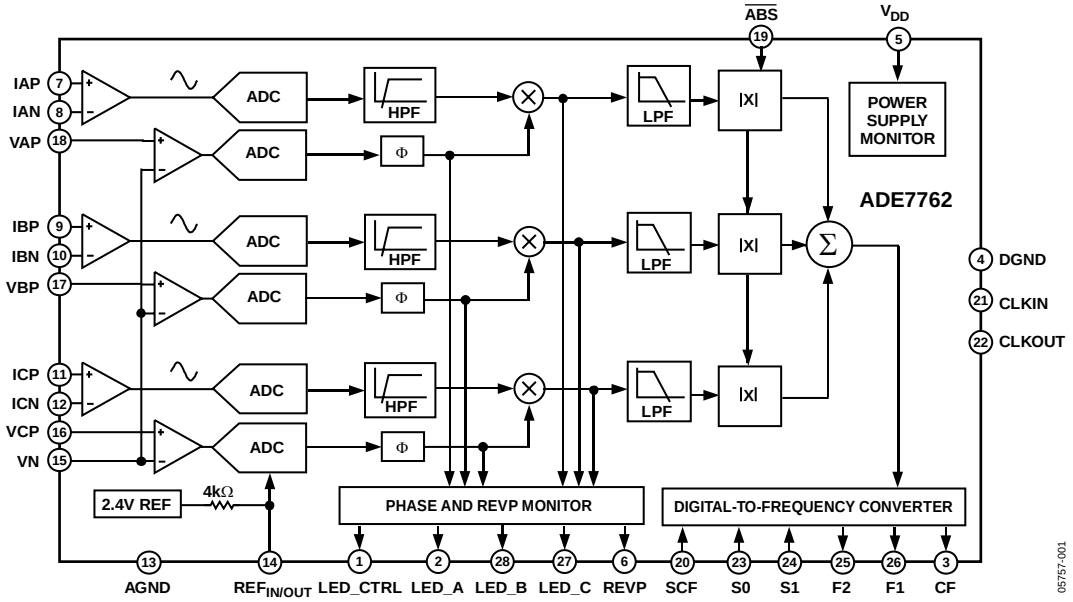


Figure 1.

Rev. PrB

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SPECIFICATIONS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
ACCURACY[1, 2]					
Measurement Error on Current Channel	Voltage channel with full-scale signal (±500 mV), 25°C, over a dynamic range of 500 to 1		0.1		% Reading
Phase Error Between Channels					
PF = 0.8 Capacitive				±0.1	Degrees
PF = 0.5 Capacitive				±0.1	Degrees
AC Power Supply Rejection	SCF = 0, S0 = S1 = 1				
Output Frequency Variation (CF)	IA = IB = IC = 100 mV rms, VA = VB = VC = 100 mV rms @ 50 Hz, Ripple on V_{DD} of 200 mV rms @ 100 Hz		0.01		% Reading
DC Power Supply Rejection	S1 = 1; S0 = SCF = 0				
Output Frequency Variation (CF)	V1 = 100 mV rms, V2 = 100 mV rms, V_{DD} = 5 V ± 250 mV		0.1		% Reading
ANALOG INPUTS	See Analog Inputs section				
Maximum Signal Levels	$V_{AP} - V_N$, $V_{BP} - V_N$, $V_{CP} - V_N$, $I_{AP} - I_{AN}$, $I_{BP} - I_{BN}$, $I_{CP} - I_{CN}$			±0.5	V peak difference
Input Impedance (DC)	CLKIN = 10 MHz	370	410		kΩ
Bandwidth (−3 dB)	CLKIN/256, CLKIN = 10 MHz		14		kHz
ADC Offset Error[1, 2]				±25	mV
Gain Error	External 2.5 V reference, IA = IB = IC = 500 mV dc		±9		% Ideal
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	2.4 V + 8%			2.6	V
	2.4 V − 8%	2.2			V
Input Impedance		3.3			kΩ
Input Capacitance				10	pF
ON-CHIP REFERENCE	Nominal 2.4 V				
Reference Error				±200	mV
Temperature Coefficient			25		ppm/°C
CLKIN	All specifications for CLKIN of 10 MHz				
Input Clock Frequency			10		MHz
LOGIC INPUTS[3]					
ACF, S0, S1, and $\overline{ABS}$					
Input High Voltage, V_{INH}	V_{DD} = 5 V ± 5%	2.4			V
Input Low Voltage, V_{INL}	V_{DD} = 5 V ± 5%			0.8	V
Input Current, I_{IN}	Typically 10 nA, V_{IN} = 0 V to V_{DD}			±3	µA
Input Capacitance, C_{IN}				10	pF
LOGIC OUTPUTS[3]					
F1 and F2					
Output High Voltage, V_{OH}	I_{SOURCE} = 10 mA, V_{DD} = 5 V	4.5			V
Output Low Voltage, V_{OL}	I_{SINK} = 10 mA, V_{DD} = 5 V			0.5	V
CF and NEGP					
Output High Voltage, V_{OH}	V_{DD} = 5 V, I_{SOURCE} = 5 mA	4.5			V
Output Low Voltage, V_{OL}	V_{DD} = 5 V, I_{SINK} = 5 mA			0.5	V
LED_CTRL	V_{DD} = 5 V, CLKIN = 10 MHz				
Output Frequency			17.39		kHz
Output High Voltage	V_{DD} = 5 V, I_{SOURCE} = 10 mA	4.5			V
Output Low Voltage	V_{DD} = 5 V, I_{SINK} = 10 mA			TBD	V

Parameter	Conditions	Min	Typ	Max	Unit
LED_A, LED_B, LED_C					
Output Low I_{SINK}	V_{DD} = 4.75 V	TBD			mA
Output High Source	V_{DD} = 4.75 V	TBD			mA
POWER SUPPLY	For specified performance				
V_{DD}	5 V ± 5%	4.75		5.25	V
I_{DD}			TBD	TBD	mA

[1] See the Terminology section for explanation of specifications.
[2] See the plots in the Typical Performance Characteristics section.
[3] Sample tested during initial release and after any redesign or process changes that might affect this parameter.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter[1,2]	Conditions	Specification	Unit
t_1 [3]	F1 and F2 pulse width (logic high)	120	ms
t_2	Output pulse period (see the Transfer Function section)	See Figure 2	sec
t_3	Time between F1 falling edge and F2 falling edge	1/2 t_2	sec
t_4[3, 4]	CF pulse width (logic high)	90	ms
t_5[5]	CF pulse period (see the Transfer Function section)	See Table 7	sec
t_6	Minimum time between F1 and F2 pulse	4/CLKIN	sec
t_7	LED_CTRL pulse width	28.8	µs
t_8	LED_CTRL period	57.5	µs
t_9	LED pulse width	7.2	µs

[1] Sample tested during initial release and after any redesign or process changes that might affect this parameter.
[2] See Figure 2.
[3] The pulse widths of F1, F2, and CF are not fixed for higher output frequencies (see the Frequency Outputs section).
[4] CF is not synchronous to F1 or F2 frequency outputs.
[5] The CF pulse is always 1 µs in the high frequency mode (see the Frequency Outputs section).

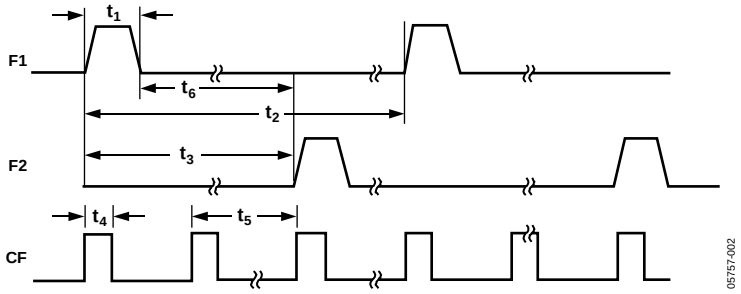


Figure 2. Timing Diagram for Frequency Outputs

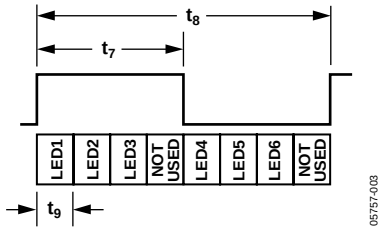


Figure 3: Timing Diagram for LED Drivers

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
Analog Input Voltage to AGND	
VAP, VBP, VCP, VN, IAP, IAN, IBP, IBN, ICP, and ICN	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
28-Lead SOIC, Power Dissipation	63 mW
θ_{JA} Thermal Impedance	55°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

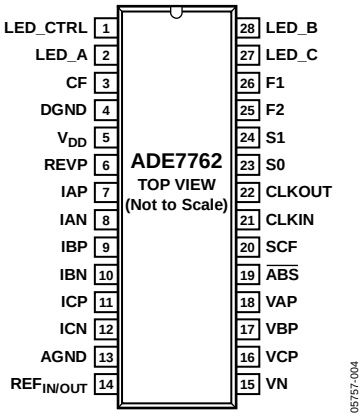


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	LED_CTRL	LED Control Output. The LED_CTRL signal multiplexes the indication of phase drop, phase sequence error, and per phase reverse power on the LED_A, LED_B, and LED_C pins.
2	LED_A	Phase A Phase Monitor Output. LEDs are connected to this pin to indicate phase drop or reverse power on phase A (see the Phase Monitor section).
3	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous active power information. This output is intended to be used for calibration purposes.
4	DGND	This provides the ground reference for the digital circuitry in the ADE7762, that is, multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the ADE7762 are small, it is acceptable to connect this pin to the analog ground plane of the whole system.
5	V_{DD}	Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7762. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a 100 nF ceramic capacitor.
6	REVP	This logic output goes logic high when negative power is detected on the sum of the three phase powers. This output is not latched and resets when positive power is once again detected (see the Negative Power Information section).
7, 8; 9, 10; 11, 12	IAP, IAN; IBP, IBN; ICP, ICN	Analog Inputs for Current Channels. These channels are intended for use with current transducers and are referenced in this document as current channels. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V (see the Analog Inputs section). Both inputs have internal ESD protection circuitry; in addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
13	AGND	This pin provides the ground reference for the analog circuitry in the ADE7762 (ADCs and reference). This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, such as, anti-aliasing filters and current and voltage transducers. To keep ground noise around the ADE7762 to a minimum, the quiet ground plane should only connect to the digital ground plane at one point. It is acceptable to place the entire device on the analog ground plane.
14	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4 V ±8% and a typical temperature coefficient of 25 ppm/°C. An external reference source can also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor.
15, 16, 17, 18	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channels. These channels are intended for use with voltage transducers and are referenced in this document as voltage channels. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. All inputs have internal ESD protection circuitry; in addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
19	$\overline{ABS}$	This logic input is used to select the method by which the three active energies from each phase are summed. It selects between the arithmetical sum of the three energies ($\overline{ABS}$ logic high) or the sum of the absolute values ($\overline{ABS}$ logic low). See the Mode Selection of the Sum of the Three Active Energies section.
20	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table 7 shows how the calibration frequencies are selected.

Pin No.	Mnemonic	Description
21	CLKIN	Master Clock for the ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7762. The clock frequency for the specified operation is 10 MHz. Ceramic load capacitors between 22 pF and 33 pF should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for the load capacitance requirements.
22	CLKOUT	A crystal can be connected across this pin and CLKIN as described previously to provide a clock source for the ADE7762. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN or when a crystal is being used.
23, 24	S0, S1	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion for design flexibility.
25, 26	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply average active power information. The logic outputs can be used to drive electromechanical counters and 2-phase stepper motors directly (see the Transfer Function section).
27	LED_C	Phase C Phase Monitor Output. LEDs are connected to this pin to indicate phase drop or reverse power on phase C (see the Phase Monitor section).
28	LED_B	Phase B Phase Monitor Output. LEDs are connected to this pin to indicate phase drop or reverse power on phase B (see the Phase Monitor section).

TYPICAL PERFORMANCE CHARACTERISTICS

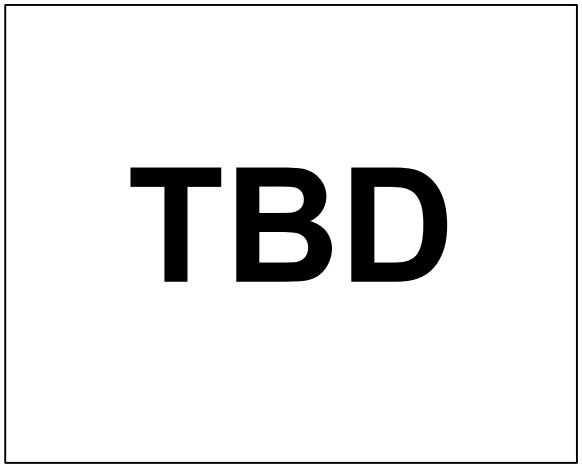


Figure 5. Error as a Percent of Reading with Internal Reference (Wye Connection)

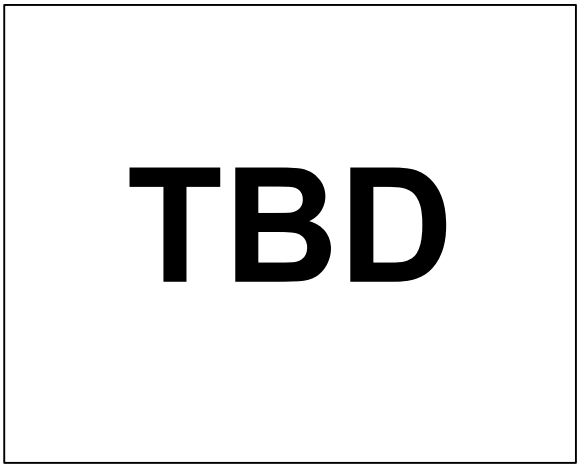


Figure 8. Error as a Percent of Reading over Temperature with Internal Reference (Wye Connection)

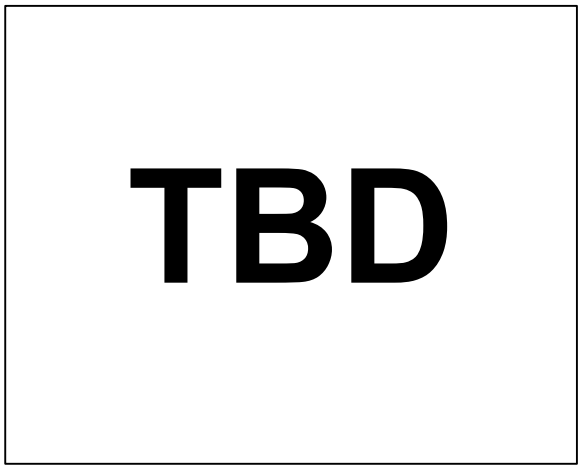


Figure 6. Error as a Percent of Reading over Power Factor with Internal Reference (Wye Connection)

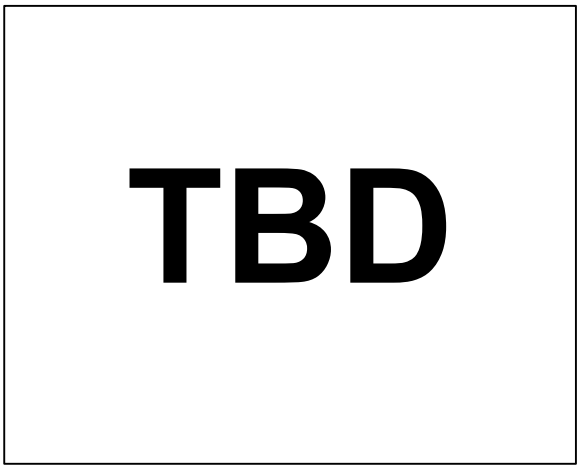


Figure 9. Error as a Percent of Reading over Power Factor with Internal Reference (Delta Connection)

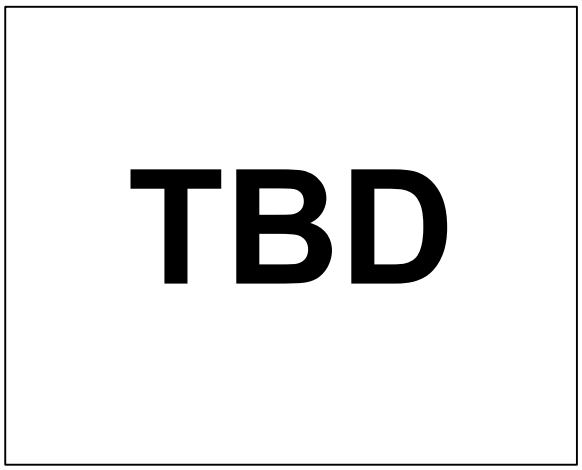


Figure 7. Error as a Percent of Reading over Power Factor with External Reference (Wye Connection)

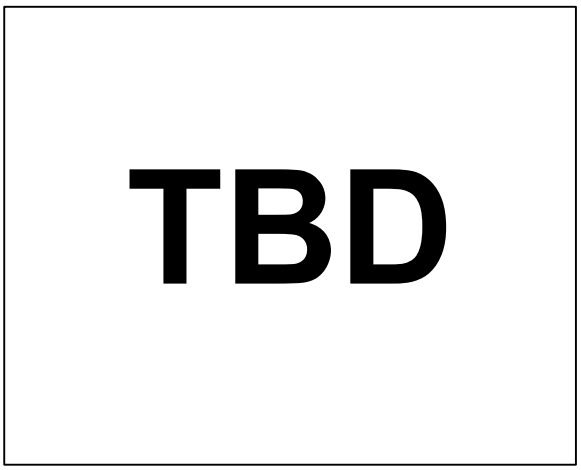


Figure 10. Error as a Percent of Reading over Temperature with External Reference (Wye Connection)

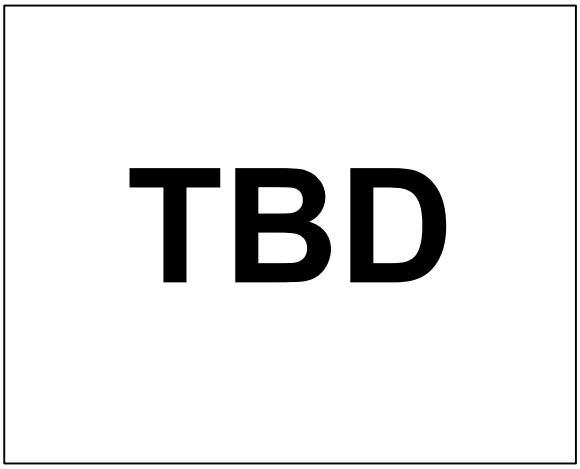


Figure 11. Error as a Percent of Reading over Frequency with an Internal Reference (Wye Connection)

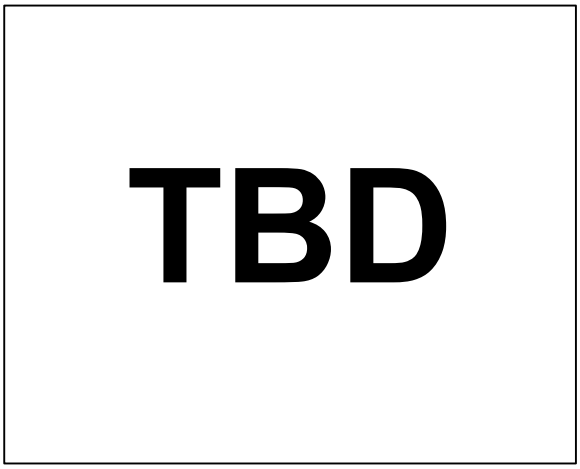


Figure 13. Channel 1 Offset Distribution

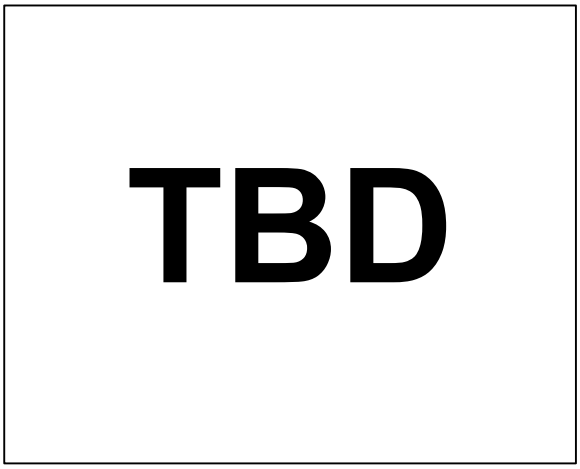


Figure 12. Error as a Percent of Reading over Power Supply with External Reference (Wye Connection)

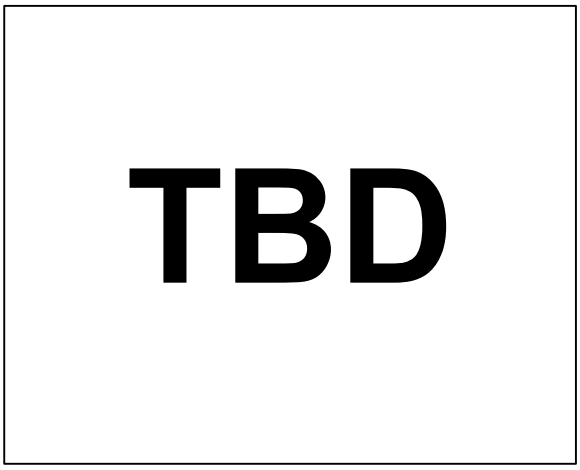


Figure 14. Error as a Percent of Reading over Power Supply with Internal Reference (Wye Connection)

TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7762 is defined by the following formula:

$$\text{Percentage Error} = \left\{\frac{\text{Energy Registered by ADE7762} - \text{True Energy}}{\text{True Energy}}\right\} \times 100\%$$

Error between Channels
The high-pass filter (HPF) in the current channel has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is placed in the current channel. The phase correction network ensures a phase match between the current channels and voltage channels to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz (see Figure 28 and Figure 29).

Power Supply Rejection (PSR)
This quantifies the ADE7762 measurement error as a percentage of reading when the power supplies are varied.

For the ac PSR measurement, a reading at a nominal supply (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supply and a second reading is obtained under the same input signal levels. Any error introduced is expressed as a percentage of reading. See definition for Measurement Error.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. The supply is then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see an analog input signal offset. However, because the HPF is always present, the offset is removed from the current channel and the power calculation is not affected by this offset.

Gain Error
The gain error of the ADE7762 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7762 transfer function (see the Transfer Function section).

TEST CIRCUIT

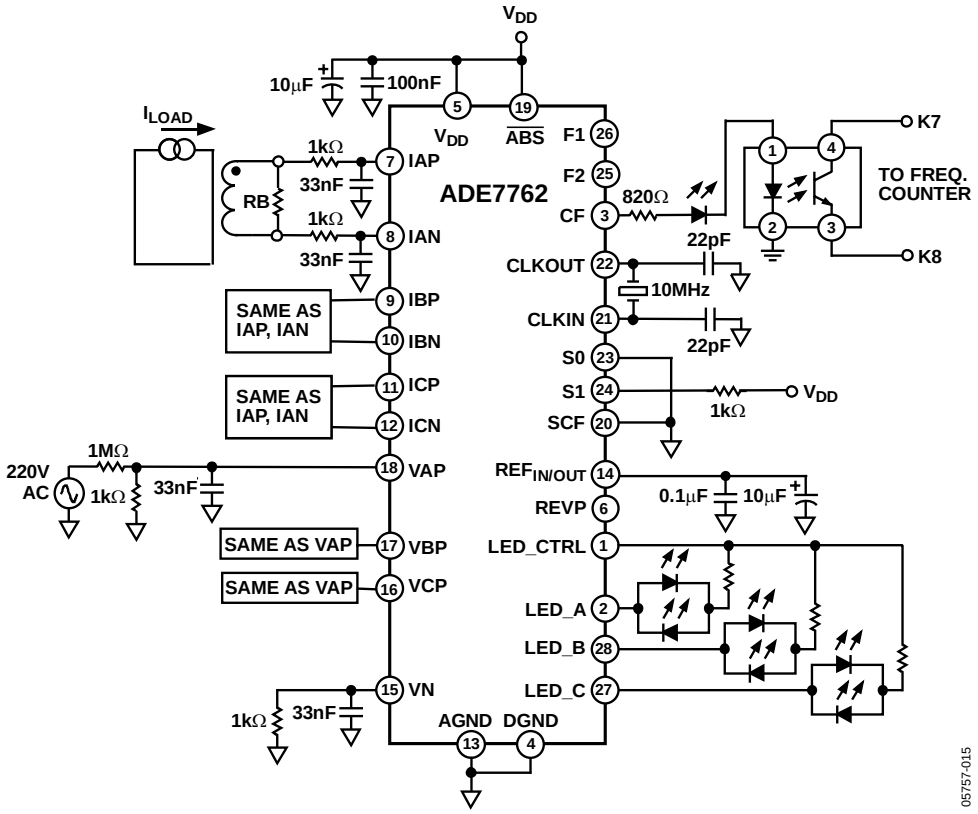


Figure 15. Test Circuit for Performance Curves

THEORY OF OPERATION

The six signals from the current and voltage transducers are digitized with ADCs. These ADCs are 16-bit second-order Σ-Δ with an oversampling rate of 833 kHz. This analog input structure greatly simplifies transducer interface by providing a wide dynamic range and bipolar input for direct connection to the transducer. High-pass filters in the current channels remove the dc component from the current signals. This eliminates any inaccuracies in the active power calculation due to offsets in the voltage or current signals (see the HPF and Offset Effects section).

The active power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals of each phase. In order to extract the active power component, the dc component, the instantaneous power signal is low-pass filtered on each phase. Figure 16 illustrates the instantaneous active power signal and shows how the active power information can be extracted by low-pass filtering the instantaneous power signal. This method is used to extract the active power information on each phase of the polyphase system. The total active power information is then obtained by adding the individual phase active power. This scheme correctly calculates active power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

The low frequency output of the ADE7762 is generated by accumulating the total active power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average active power. This average active power information can, in turn, be accumulated (for example, by a counter) to generate active energy information. Because of its high output frequency and therefore shorter integration time, the CF output is proportional to the instantaneous active power. This pulse is useful for system calibration purposes that would take place under steady load conditions.

POWER FACTOR CONSIDERATIONS

Low-pass filtering, the method used to extract the active power information from the individual instantaneous power signal, is still valid when the voltage and current signals of each phase are not in phase. Figure 17 displays the unity power factor condition and a displacement power factor (DPF) = 0.5, that is, current signal lagging the voltage by 60°, for one phase of the polyphase. Assuming that the voltage and current waveforms are sinusoidal, the active power component of the instantaneous power signal (the dc term) is given by

$$\left(\frac{V \times 1}{2}\right) \times \cos(60°) \quad (1)$$

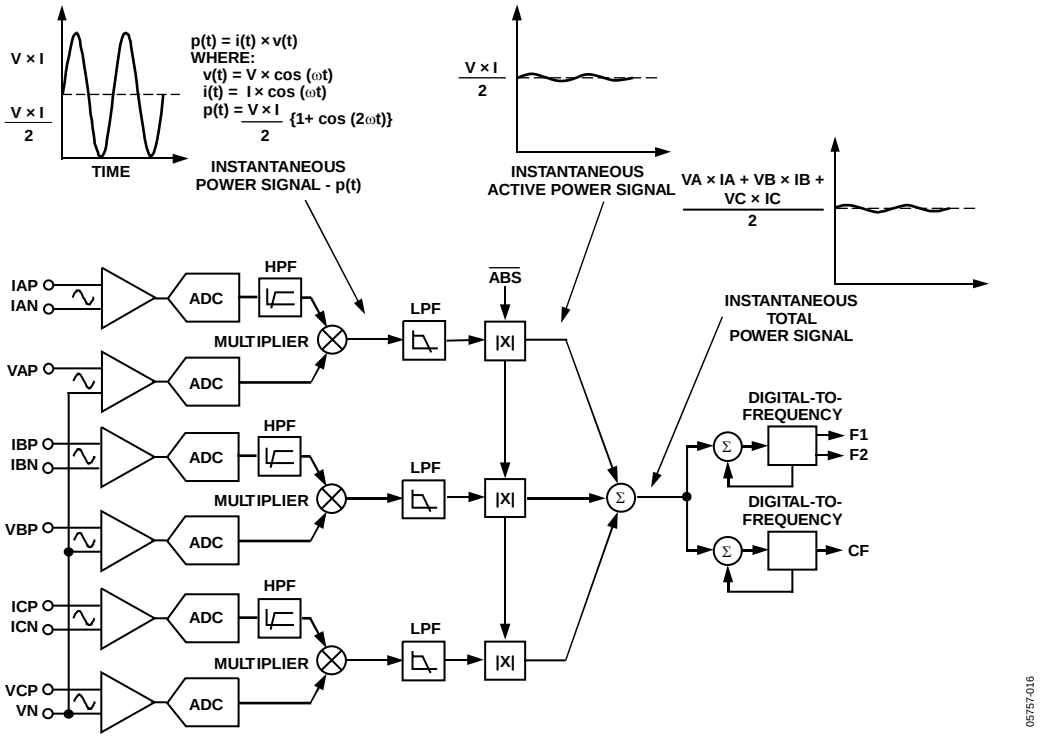


Figure 16. Signal Processing Block Diagram

This is the correct active power calculation.

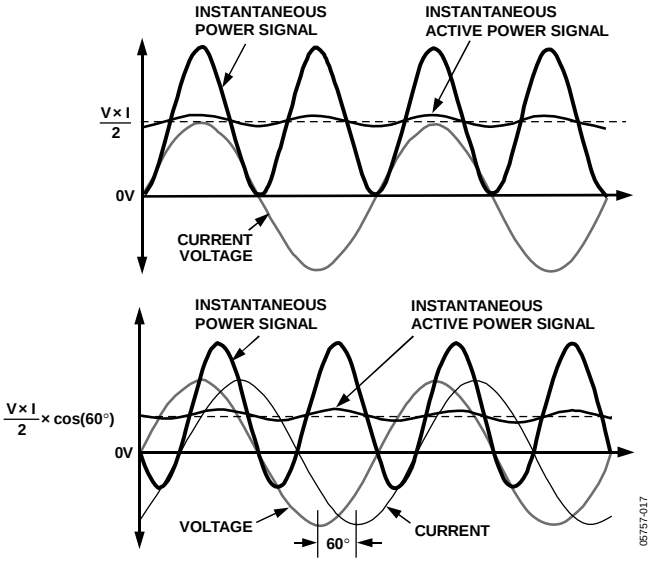


Figure 17. DC Component of Instantaneous Power Signal

NONSINUSOIDAL VOLTAGE AND CURRENT

The active power calculation method also holds true for non-sinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications have some harmonic content. Using the Fourier Transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content

$$v(t) = V_o + \sqrt{2} \times \sum_{n=0}^{\infty} V_n \times \sin\left(n\omega t + \alpha_n\right) \quad (2)$$

where:
$v(t)$ is the instantaneous voltage.
V_O is the average value.
V_n is the rms value of voltage harmonic n.
and α_n is the phase angle of the voltage harmonic.

$$i(t) = I_O + \sqrt{2} \times \sum_{n=0}^{\infty} V_n I \times \sin\left(n\omega t\, \beta_n\right) \quad (3)$$

where:
$i(t)$ is the instantaneous current.
I_O is the dc component.
I_n is the rms value of current harmonic n.
β_n is the phase angle of the current harmonic.

Using Equations 2 and 3, the active power, P, can be expressed in terms of its fundamental active power (P_1) and harmonic active power (P_H).

$$P = P_1 + P_H$$

where:

$$P_1 = V_1 \times I_1 \cos\phi_1 \quad (4)$$
$$\phi_1 = \alpha_1 - \beta_1$$

$$P_H = \sum_{n=1}^{\infty} V_n \times I_n \cos\phi_n \quad (5)$$
$$\phi n = \alpha_n - \beta_n$$

As can be seen from Equation 5, a harmonic active power component is generated for every harmonic, provided that harmonic is present in both the voltage and current waveforms. The power factor calculation has been shown to be accurate in the case of a pure sinusoid. Therefore, the harmonic active power also correctly accounts for power factor since harmonics are made up of a series of pure sinusoids. A limiting factor on harmonic measurement is the bandwidth. On the ADE7762, the bandwidth of the active power measurement is 14 kHz with a master clock frequency of 10 MHz.

ANALOG INPUTS

CURRENT CHANNELS

The voltage outputs from the current transducers are connected to the ADE7762 current channels, which are fully differential voltage inputs. IAP, IBP, and ICP are the positive inputs for IAN, IBN, and ICN, respectively.

The maximum peak differential signal on the current channel should be less than ±500 mV (353 mV rms for a pure sinusoidal signal) for the specified operation.

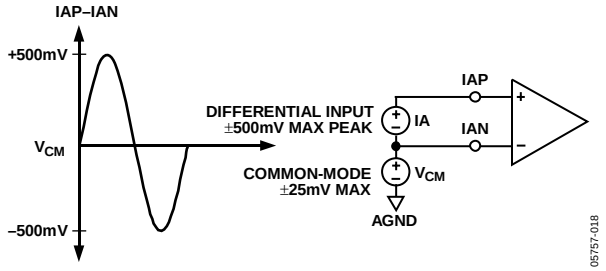


Figure 18. Maximum Signal Levels, Current Channel

The maximum signal levels on IAP and IAN are shown in Figure 18. The maximum differential voltage between IAP and IAN is ±500 mV. The differential voltage signal on the inputs must be referenced to a common mode, for example, AGND. The maximum common-mode signal shown in Figure 18 is ±25 mV.

VOLTAGE CHANNELS

The output of the line voltage transducer is connected to the ADE7762 at this analog input. Voltage channels are a pseudo-differential voltage input. VAP, VBP, and VCP are the positive inputs with respect to VN.

The maximum peak differential signal on the voltage channel is ±500 mV (353 mV rms for a pure sinusoidal signal) for specified operation.

Figure 19 illustrates the maximum signal levels that can be connected to the ADE7762 voltage channels.

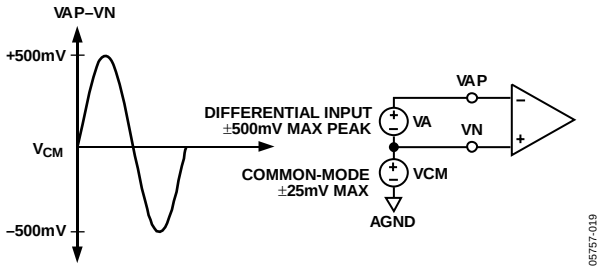


Figure 19. Maximum Signal Levels, Voltage Channel

Voltage channels must be driven from a common-mode voltage, that is, the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the ADE7762 can be driven with common-mode voltages of up to 25 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

TYPICAL CONNECTION DIAGRAMS

CURRENT CHANNEL CONNECTION

Figure 20 shows a typical connection diagram for the current channel (IA). A current transformer (CT) is the current transducer selected for this example. Notice the common-mode voltage for the current channel is AGND and is derived by center tapping the burden resistor to AGND. This provides the complementary analog input signals for IAP and IAN. The CT turns ratio and burden resistor Rb are selected to give a peak differential voltage of ±500 mV at maximum load.

In theory it is better to center tap Rb; however, this requires very careful attention to the layout and matching of the resistors to ensure that the channels have the same resistance. A single resistor may be more practical and is a valid design choice.

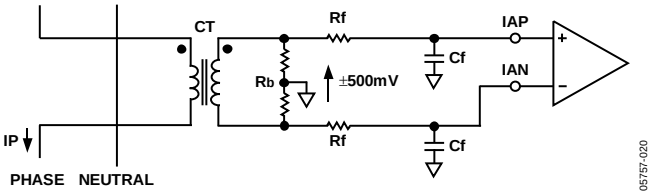


Figure 20. Typical Connection for Current Channels

VOLTAGE CHANNELS CONNECTION

Figure 21 shows two typical connections for the voltage channel. The first option uses a potential transformer (PT) to provide complete isolation from the main voltage. In the second option, the ADE7762 is biased around the neutral wire, and a resistor divider is used to provide a voltage signal proportional to the line voltage. Adjusting the ratio of Ra, Rb, and VR is a convenient way of carrying out a gain calibration on the meter. VR can be implemented using either a potentiometer or a binary weighted series of resistors. Either configuration works, however, the potentiometer is subject to noise over time. Two fixed value resistors can be used in place of VR to minimize the noise.

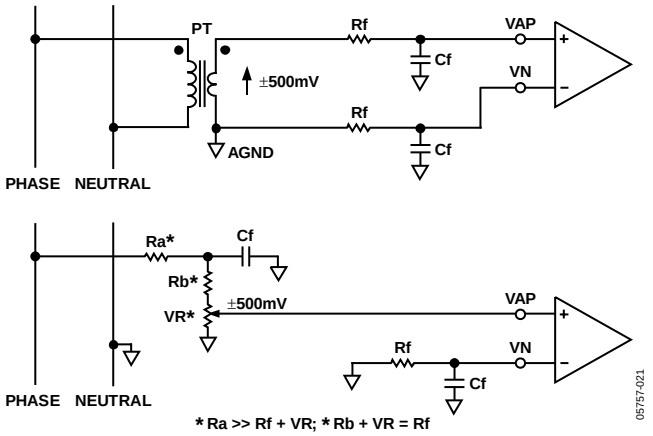


Figure 21. Typical Connections for Voltage Channels

METER CONNECTIONS

In 3-phase service, two main power distribution services exist: 3-phase 4-wire or 3-phase 3-wire. The additional wire in the 3-phase 4-wire arrangement is the neutral wire. The voltage lines have a phase difference of ±120° (±2π/3 radians) between each other (see Equation 6).

$$V_A(t) = \sqrt{2} \times V_A \times \cos(\omega_l t)$$
$$V_B(t) = \sqrt{2} \times V_B \times \cos\left(\omega_l t + \frac{2\pi}{3}\right) \quad (6)$$
$$V_C(t) = \sqrt{2} \times V_C \times \cos\left(\omega_l t + \frac{4\pi}{3}\right)$$

where V_A, V_B, and V_C represent the voltage rms values of the different phases.

The current inputs are represented by

$$I_A(t) = \sqrt{2}\, I_A \times \cos\left(\omega_l t + \phi_A\right)$$
$$I_B(t) = \sqrt{2}\, I_B \times \cos\left\{\omega_l t + \frac{2\pi}{3} + \phi_B\right\} \quad (7)$$
$$I_C(t) = \sqrt{2}\, I_C \times \cos\left\{\omega_l t + \frac{4\pi}{3} + \phi_C\right\}$$

where:

I_A, I_B, and I_C represent the rms value of the current of each phase.
ϕ_A, ϕ_B, and ϕ_C represent the phase difference of the current and voltage channel of each phase.

The instantaneous powers can then be calculated as follows:

$P_A(t) = V_A(t) \times I_A(t)$
$P_B(t) = V_B(t) \times I_B(t)$
$P_C(t) = V_C(t) \times I_C(t)$

Then:

$$P_A(t) = V_A \times I_A \times \cos(\phi_A) - V_A \times I_A \times \cos\left(2\omega_l t + \phi_A\right)$$
$$P_B(t) = V_B \times I_B \times \cos(\phi_B) - V_B \times I_B \times \cos\left(2\omega_l t + \frac{4\pi}{3} + \phi_B\right) \quad (8)$$
$$P_C(t) = V_C \times I_C \times \cos(\phi_C) - V_C \times I_C \times \cos\left(2\omega_l t + \frac{8\pi}{3} + \phi_C\right)$$

As shown in Equation 8, in the ADE7762, the active power calculation per phase is made when current and voltage inputs of one phase are connected to the same channel (A, B, or C). Then the summation of each individual active power calculation gives the total active power information, $P(t) = P_A(t) + P_B(t) + P_C(t)$.

Figure 22 shows the connections of the ADE7762 analog inputs with the power lines in a 3-phase 3-wire delta service.

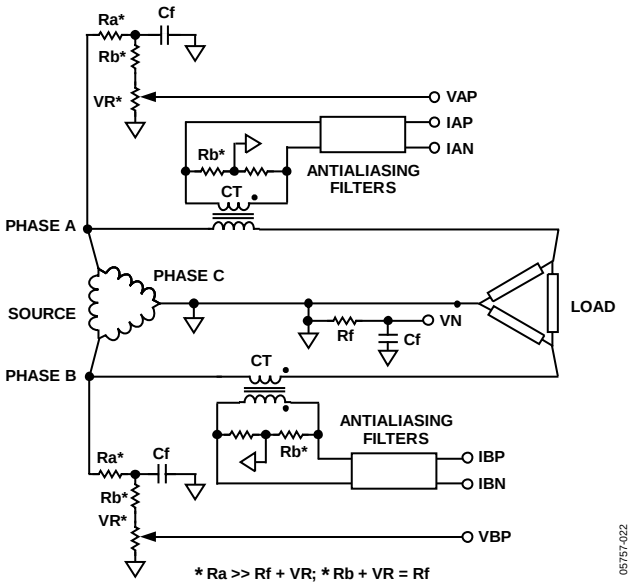


Figure 22. 3-Phase 3-Wire Meter Connection with ADE7762

Note that only two current inputs and two voltage inputs of the ADE7762 are used in this case. The active power calculated by the ADE7762 does not depend on the selected channels.

Figure 23 shows the connections of the ADE7762 analog inputs with the power lines in a 3-phase 4-wire Wye service.

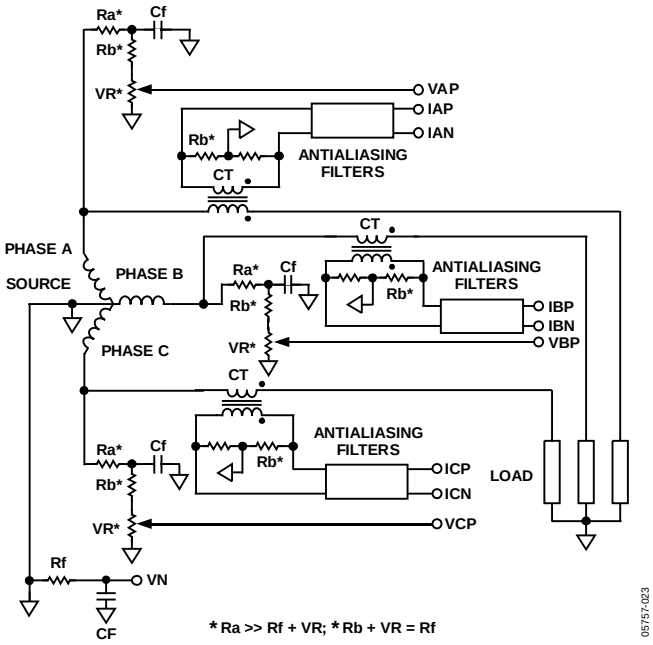


Figure 23. 3-Phase 4-Wire Meter Connection with ADE7762

POWER SUPPLY MONITOR

The ADE7762 contains an on-chip power supply monitor. The power supply (V_{DD}) is monitored continuously by the ADE7762. At power up, when the supply is less than 4V ±2% and V_{REF} is less than 1.9 V (typ), the outputs of the ADE7762 are inactive and the data path is held in reset. Once V_{DD} is greater than 4V ±2% and V_{REF} is greater than 1.9 V (typ), the chip is active and energy accumulation begins. At power-down, when V_{DD} falls below 4 V or V_{REF} falls below 1.9 V (typ), the data path is again held in reset. This implementation ensures correct device operation at power-up and at power-down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

The power supply and decoupling for the part should be such that the ripple at V_{DD} does not exceed ±5% as specified for normal operation.

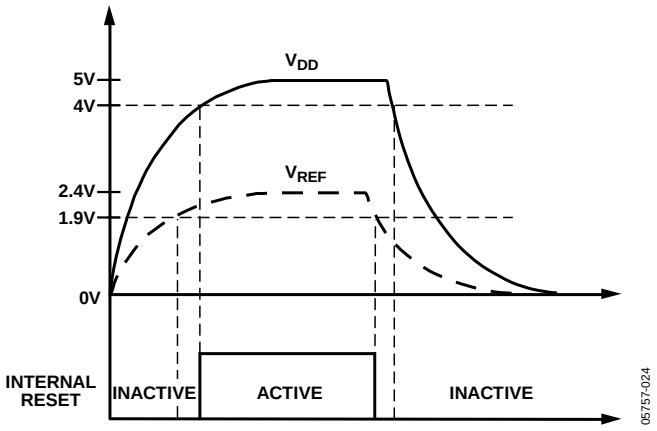


Figure 24. On-Chip Power Supply Monitor

PHASE MONITOR

The ADE7762 has phase monitoring functions to detect phase dropout, phase sequence error, and reverse polarity using four pins. Phase dropout has the highest priority, and reverse polarity has lowest priority. If a phase dropout occurs, phase sequence error indication is disabled until all three phases are above the phase dropout level (see the Phase Dropout Error section). Because the dropout detection level is not set to zero, a phase can have some small voltage during phase dropout condition. Therefore, reverse polarity is still indicated on that phase if the proper conditions occur.

The phase monitor circuit functions by multiplexing signals onto the four pins. The four multiplexed pins are LED_CTRL, LED_A, LED_B, and LED_C. Two LEDs can be connected to each pin as shown in Figure 25. When LED_CTRL is high, LED_A would be low to turn on an LED and indicate a phase drop condition on Phase A. When LED_CTRL is low, LED_A is high to indicate a reverse polarity (REVP) condition on phase A. Phase sequence error is indicated by blinking the Phase Seq/Drop LEDs.

LED_CTRL switches at a rate of 131 kHz so that both the Phase Seq/Drop LEDs and REVP LEDs can appear to be on simultaneously, which allows indication of phase dropout and REVP at the same time. For the timing diagram, see Figure 3.

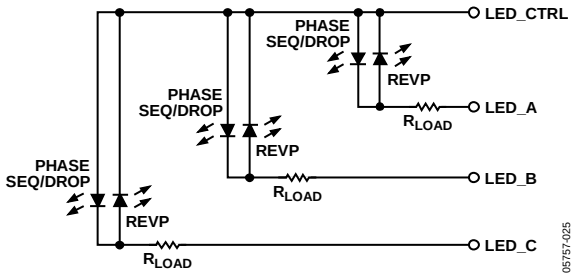


Figure 25. Phase Monitor Circuit

Phase Dropout Error

The ADE7762 indicates a phase drop condition when there is low voltage signal or no voltage signal on a phase. The phase dropout condition occurs when the amplitude of the phase drops below 20% of full-scale analog input voltage or when a zero crossing is not followed by another zero crossing on that phase for 150 ms. When this occurs, a phase dropout signal is generated and the Phase Seq/Drop LED is turned on for the missing phase. The delay between the phase drop condition occurring at the analog inputs and indication of the condition on the LED outputs is approximately 150 ms. During a phase dropout condition, energy continues to accumulate on the dropped channel, as well as the other channels, and phase sequence error indication is disabled. The Phase Seq/Drop LED for the dropped phase is turned off when the zero crossings return for more than 150 ms and there is more than 20% of full-scale input voltage on the voltage input of that phase.

Phase Sequence Error

The ADE7762 detects the zero crossing of each phase. A phase sequence error occurs when the sequence A>B>C>A> … is violated. If a phase sequence error occurs, the Phase Seq/Drop LEDs blink at 1 Hz (see Figure 26).

Phase sequence error and REVP can be displayed simultaneously. The REVP LEDs continue to indicate reverse polarity if the proper conditions exist. For example, if the phase sequence becomes A>C>B>A… and phase B has negative active energy accumulated, then the REVP LED for phase B is on solid and all of the Phase Seq/Drop LEDs would be blinking at 1 Hz. The delay in indicating the phase sequence error with blinking LEDs is approximately 150 ms from the time that a phase sequence error occurs.

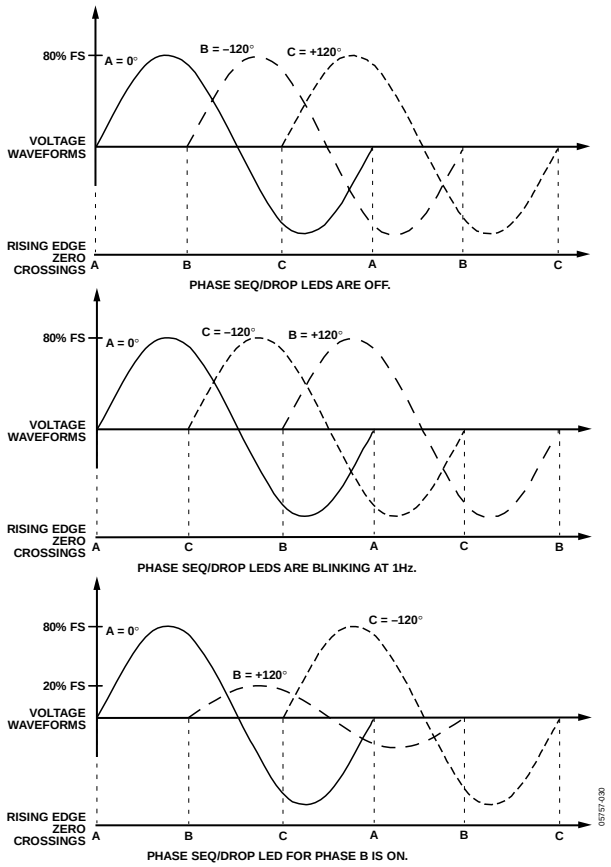


Figure 26. Phase Sequence Detection

Reverse Polarity Error

When reverse power is detected on any phase, the corresponding REVP LED turns on for that phase. For example, if the power for phase A is negative, the REVP LED connected to LED_A turns on. The indication of REVP on the LED_A, LED_B, or LED_C pins is nearly instantaneous. As soon as the input to the ADCs changes and the power is calculated such that there is a reverse power condition on any phase, the appropriate LED is turned on.

HPF AND OFFSET EFFECTS

Figure 27 shows the effect of offsets on the active power calculation. An offset on the current channel and voltage channel contributes a dc component after multiplication as shown in Figure 27. Since this dc component is extracted by the LPF and is used to generate the active power information for each phase, the offsets can contribute a constant error to the total active power calculation. The HPF in the current channels avoids this problem easily. By removing the offset from at least one channel, no error component can be generated at dc by the multiplication. Error terms at cos(ωt) are removed by the LPF and the digital-to-frequency conversion (see the Digital-to-Frequency Conversion) section.

$$\{V\cos(\omega t)+V_{OS}\}\times\{I\cos(\omega t)+I_{OS}\}=$$
$$\frac{V\times I}{2}+V_{OS}\times I_{OS}+V_{OS}\times I\cos(\omega t)+I_{OS}\times V\cos(\omega t)+\frac{V\times I}{2}\times\cos(2\omega t) \quad (9)$$

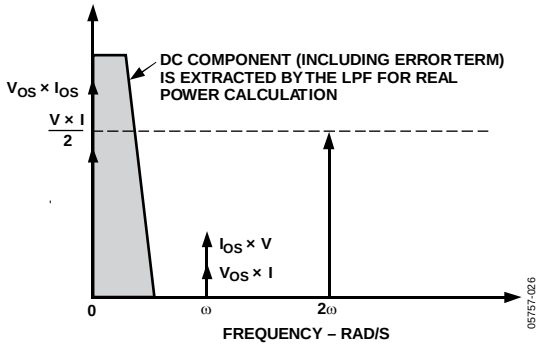


Figure 27. Effect of Channel Offset on the Active Power Calculation

The HPF in the current channels has an associated phase response that is compensated for on-chip. Figure 28 and Figure 29 show the phase error between channels with the compensation network.

The ADE7762 is phase compensated up to 1 kHz as shown. This ensures correct active harmonic power calculation even at low power factors.

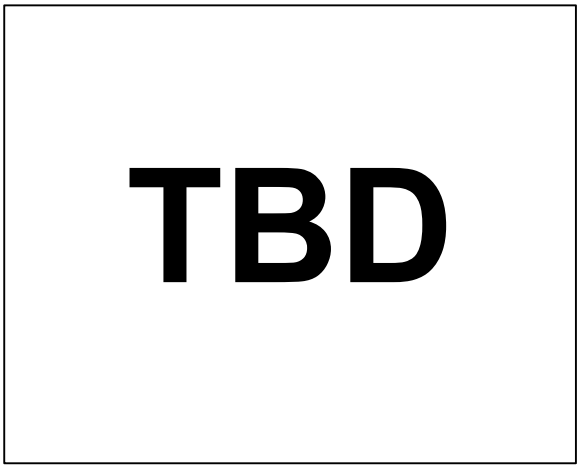


Figure 28. Phase Error between Channels (0 Hz to 1 kHz)

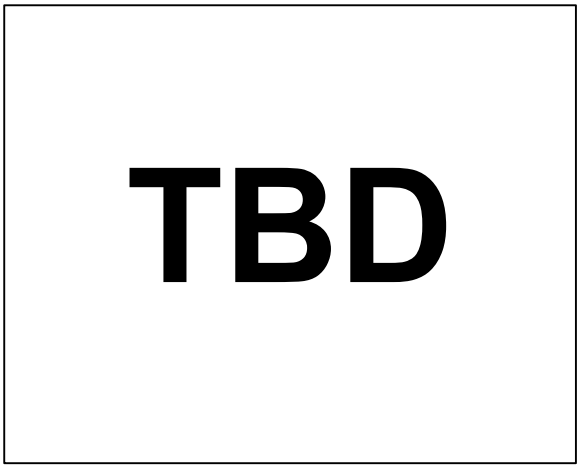


Figure 29. Phase Error Between Channels (40 Hz to 70 Hz)

DIGITAL-TO-FREQUENCY CONVERSION

After multiplication, the digital output of the low-pass filter contains the active power information of each phase. However, since this LPF is not an ideal brick wall filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, that is, cos(hωt), where h = 1, 2, 3 ….

The magnitude response of the filter is given by

$$|H(f)| = \frac{1}{\sqrt{1+\left\{\frac{f}{8}\right\}^2}} \quad (10)$$

where the −3 dB cutoff frequency of the low-pass filter is 8 Hz.

For a line frequency of 50 Hz, this would give an attenuation of the 2ω(100 Hz) component of approximately −22 dB. The dominating harmonic is twice the line frequency, that is, cos(2ωt), due to the instantaneous power signal. Figure 30 shows the instantaneous active power signal at the output of the CF, which still contains a significant amount of instantaneous power information, cos(2ωt).

This signal is then passed to the digital-to-frequency converter where it is integrated (accumulated) over time to produce an output frequency. This accumulation of the signal suppresses or averages out any non-dc component in the instantaneous active power signal.

The average value of a sinusoidal signal is zero. Thus, the frequency generated by the ADE7762 is proportional to the average active power. Figure 30 shows the digital-to-frequency conversion for steady load conditions, that is, constant voltage and current.

The frequency output CF varies over time, even under steady load conditions (see Figure 30). This frequency variation is primarily due to the cos(2ωt) components in the instantaneous active power signal. The output frequency on CF can be up to 160× higher than the frequency on F1 and F2. The higher output frequency is generated by accumulating the instantaneous active power signal over a much shorter time, while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2ωt) component. Therefore, some of this instantaneous power signal passes through the digital-to-frequency conversion.

Where CF is used for calibration purposes, the frequency counter should average the frequency to remove the ripple and obtain a stable frequency. If CF is being used to measure energy, for example, in a microprocessor-based application, the CF output should also be averaged to calculate power. Because the outputs F1 and F2 operate at a much lower frequency, significant averaging of the instantaneous active power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output on F1 and F2, which are used to measure energy in a stepper-motor based meter.

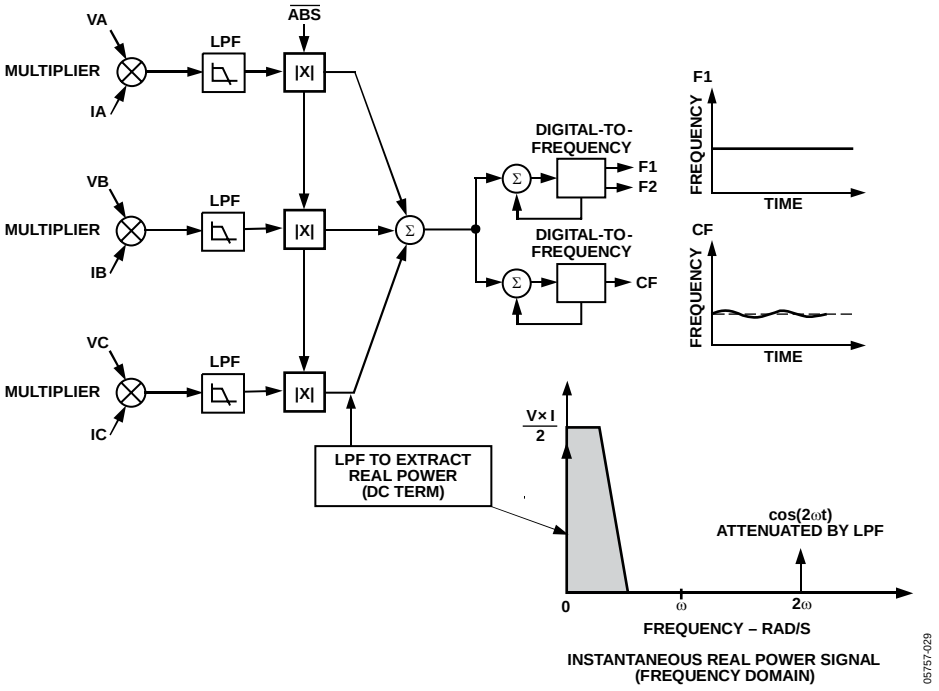


Figure 30. Active Power-to-Frequency Conversion

POWER MEASUREMENT CONSIDERATIONS

Calculating and displaying power information always have some associated ripple that depends on the integration period used in the MCU to determine average power as well as the load. For example, at light loads, the output frequency can be 10 Hz. With an integration period of two seconds, only about 20 pulses are counted. The possibility of missing one pulse always exists since the ADE7762 output frequency is running asynchronously to the MCU timer. This would result in a 1-in-20 or 5% error in the power measurement. To remedy this, an appropriate integration time should be considered to achieve the desired accuracy.

MODE SELECTION OF THE SUM OF THE THREE ACTIVE ENERGIES

The ADE7762 can be configured to execute the arithmetic sum of the three active energies, $Wh = Wh_{\Phi A} + Wh_{\Phi B} + Wh_{\Phi C}$, or the sum of the absolute value of these energies, $Wh = |Wh_{\Phi A}| + |Wh_{\Phi B}| + |Wh_{\Phi C}|$. The selection between the two modes can be made by setting the $\overline{ABS}$ pin. Logic high and logic low applied on the $\overline{ABS}$ pin correspond to the arithmetic sum and the sum of absolute values, respectively.

When the sum of the absolute values is selected, the active energy from each phase is always counted positive in the total active energy. It is particularly useful in 3-phase 4-wire instillation where the sign of the active power should always be the same. If the meter is misconnected to the power lines, that is, CT connected in the wrong direction then the total active energy recorded without this solution can be reduced by two-thirds.

The sum of the absolute values assures that the active energy recorded represents the actual active energy delivered. In this mode, the reverse power pin still detects when negative power is present on any of the three phase inputs, but energy continues to accumulate regardless of the sign.

TRANSFER FUNCTION

FREQUENCY OUTPUTS F1 AND F2

The ADE7762 calculates the product of six voltage signals (on current channel and voltage channel) and then low-pass filters this product to extract active power information. This active power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active high pulses. The pulse rate at these outputs is relatively low, for example, 2.01 Hz maximum for ac signals with SCF = S0 = 0; S1 = 1 (see Table 6). This means that the frequency at these outputs is generated from active power information accumulated over a relatively long period. The result is an output frequency that is proportional to the average active power. The averaging of the active power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation:

$$\text{Freq} = \frac{6.181 \times \left(V_{AN} \times I_A + V_{BN} \times I_B + V_{CN} \times I_C\right) \times F_{1-7}}{V_{REF}^2} \quad (11)$$

where:
Freq = output frequency on F1 and F2 (Hz).
V_{AN}, V_{BN}, and V_{CN} = differential rms voltage signal on voltage channels (V).
I_A, I_B, and I_C = differential rms voltage signal on current channels (V).
V_{REF} = the reference voltage (2.4 V ±8%) (V).
F_{1-7} = one of seven possible frequencies selected by using the logic inputs SCF, S0, and S1 (see Table 5).

Table 5. F_{1-7} Frequency Selection[1]

SCF	S1	S0	F_{1-7} (Hz)
0	0	0	2.30
1	0	0	4.61
0	0	1	1.15
1	0	1	4.61
0	1	0	5.22
1	1	0	1.15
0	1	1	0.58
1	1	1	0.58

[1] F_{1-7} is a fraction of the master clock and therefore varies if the specified CLKIN frequency is altered.

Example 1

Thus, if full-scale differential dc voltages of +500 mV are applied to VA, VB, VC, IA, IB, and IC, respectively (500 mV is the maximum differential voltage that can be connected to current and voltage channels), then the expected output frequency is calculated as follows:

F_{1-7} = 0.58 Hz, SCF = S0 = S1 = 1
$V_{AN} = V_{BN} = V_{CN} = IA = IB = IC$
= 500 mV dc = 0.5 V(rms of dc = dc)
V_{REF} = 2.4 V (nominal reference value)

Note that if the on-chip reference is used, actual output frequencies can vary from device to device due to reference tolerance of ±8%.

$$\text{Freq} = 3 \times \frac{6.181 \times 0.5 \times 0.5 \times 0.58}{2.4^2} = 0.467 \text{ Hz} \quad (12)$$

Example 2

In this example, with ac voltages of ±500 mV peak applied to the voltage channels and current channels, the expected output frequency is calculated as follows:

$$\begin{aligned} &F_{1-7} = 0.58 \text{ Hz, SCF} = S0 = S1 = 1 \\ &V_{AN} = V_{BN} = V_{CN} = IA = IB = IC \\ &\quad = 500 \text{ mV peak AC} = \frac{0.5}{\sqrt{2}} \text{ Vrms} \\ &V_{REF} = 2.4 \text{ V (nominal reference value)} \end{aligned} \quad (13)$$

Note that if the on-chip reference is used, actual output frequencies can vary from device to device due to reference tolerance of ±8%.

$$\text{Freq} = 3 \times \frac{6.181 \times 0.5 \times 0.5 \times 0.58}{\sqrt{2} \times \sqrt{2} \times 2.4^2} = 0.233 \text{ Hz} \quad (14)$$

As can be seen from these two example calculations, the maximum output frequency for ac inputs is always half of that for dc input signals. The maximum frequency also depends on the number of phases connected to the ADE7762. In a 3-phase 3-wire delta service, the maximum output frequency is different from the maximum output frequency in a 3-phase 4-wire Wye service. The reason is that there are only two phases connected to the analog inputs, but also that in a delta service, the current channel input and voltage channel input of the same phase are not in phase in normal operation.

Example 3

In this example, the ADE7762 is connected to a 3-phase 3-wire delta service as shown in Figure 22. The total active energy calculation processed in the ADE7762 can be expressed as

$$\textit{Total Active Power} = (V_A - V_C) \times I_A + (V_B - V_C) \times I_B$$

where:

V_A, V_B, and V_C represent the voltage on phase A, phase B, and phase C, respectively.
I_A and I_B represent the current on phase A and phase B, respectively.

As the voltage and current inputs respect Equations 5 and 6, the total active power (P) is

$$\begin{aligned} P &= (VA - VC)\ \ (IAP - IAN) + (VB - VC) \times (IBP - IBN) \\ P &= \left(\sqrt{2} \times V_A \times \cos(\omega_l t) - \sqrt{2} \times V_C \times \cos\left(\omega_l t + \frac{4\pi}{3}\right)\right) \\ &\quad \times \sqrt{2} \times I_A \times \cos(\omega_l t) \\ &\quad + \left(\sqrt{2} \times V_B \times \cos\left(\omega_l t + \frac{2\pi}{3}\right) - \nu\sqrt{2} \times V_C \times \cos\left(\omega_l t + \frac{4\pi}{3}\right)\right) \\ &\quad \times \sqrt{2} \times I_B \times \cos\left(\omega_l t + \frac{2\pi}{3}\right) \end{aligned} \quad (15)$$

For simplification, assume that $\Phi_A = \Phi_B = \Phi_C = 0$ and $V_A = V_B = V_C = V$. The preceding equation becomes

$$\begin{aligned} P &= 2 \times V \times I_A \times \sin\left(\frac{2\pi}{3}\right) \times \sin\left(\omega_l t + \frac{2\pi}{3}\right) \times \cos(\omega_l t) \\ &\quad + 2 \times V \times I_B \times \sin\left(\frac{\pi}{3}\right) \times \sin(\omega_l t + \pi) \times \cos\left(\omega_l t + \frac{2\pi}{3}\right) \end{aligned} \quad (16)$$

P then becomes

$$\begin{aligned} P &= VAN \times I_A \times \left(\sin\left(\frac{2\pi}{3}\right) + \sin\left(2\omega_l t + \frac{2\pi}{3}\right)\right) \\ &\quad + VBN \times I_B \times \left(\sin\left(\frac{\pi}{3}\right) + \sin\left(2\omega_l t + \frac{\pi}{3}\right)\right) \end{aligned} \quad (17)$$

where:

$VAN = V \times \sin(2\pi/3)$.
$VBN = V \times \sin(\pi/3)$.

As the LPF on each channel eliminates the $2\omega_l$ component of the equation, the active power measured by the ADE7762 is

$$P = V_{AN} \times I_A \times \frac{\sqrt{3}}{2} + V_{BN} \times I_B \times \frac{\sqrt{3}}{2} \quad (18)$$

If full-scale ac voltage of ±500 mV peak is applied to the voltage channels and current channels, the expected output frequency is calculated as follows:

$$\begin{aligned} &F_{1-7} = 0.60\text{Hz}, \text{SCF} = \text{S0} = \text{S1} = 1 \\ &V_{AN} = V_{BN} = \text{IA} = \text{IB} = \text{IC} = 500\ \text{mV peak ac} = \frac{0.5}{\sqrt{2}}\ \text{V rms} \\ &V_{CN} = \text{IC} = 0 \\ &V_{REF} = 2.4\text{V nominal reference value} \end{aligned} \quad (19)$$

Note that if the on-chip reference is used, actual output frequencies can vary from device to device due to reference tolerance of ±8%.

$$\text{Freq} = 2 \times \frac{6.181 \times 0.5 \times 0.5 \times 0.60}{\sqrt{2} \times \sqrt{2} \times 2.4^2} \times \frac{\sqrt{3}}{2} = 0.139\ \text{Hz} \quad (20)$$

Table 6 shows a complete listing of all maximum output frequencies when using all three channel inputs.

Table 6: Maximum Output Frequency on F1 and F2

SCF	S1	S0	Maximum Frequency for AC Inputs (Hz)	Maximum Frequency for DC Inputs (Hz)
0	0	0	0.93	1.85
1	0	1	1.86	3.71
0	0	1	0.46	0.93
1	0	1	1.86	3.71
0	1	0	2.10	4.20
1	1	0	0.46	0.93
0	1	1	0.23	0.47
1	1	1	0.23	0.47

FREQUENCY OUTPUT CF

The pulse output calibration frequency (CF) is intended for use during calibration. The output pulse rate on CF can be up to 64× the pulse rate on F1 and F2. Table 7 shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF. Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous active power. As is the case with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, since the output frequency is high, this active power information is accumulated over a much shorter time. Thus, less averaging is carried out in the digital-to-frequency conversion. The CF output is much more responsive to power fluctuations with much less averaging of the active power signal (see Figure 16).

Table 7. Maximum Output Frequency on CF

SCF	S1	S0	F_{1-7} (Hz)	CF Maximum for AC Signals (Hz)
0	0	0	2.3	16 × F1, F2 = 14.88
1	0	0	4.61	8 × F1, F2 = 14.88
0	0	1	1.15	32 × F1, F2 = 14.88
1	0	1	4.61	16 × F1, F2 = 29.76
0	1	0	5.22	160 × F1, F2 = 336
1	1	0	1.15	16 × F1, F2 = 7.36
0	1	1	0.58	32 × F1, F2 = 7.36
1	1	1	0.58	16 × F1, F2 = 3.68

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION

As shown in Table 5, the user can select one of seven frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended to be used to drive the energy register (electromechanical or other). Since seven different output frequencies can be selected, the available frequency selection has been optimized for a 3-phase 4-wire service with a meter constant of 100 imp/kWhr and a maximum current of between 10 A and 100 A. Table 8 shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 220 V (phase neutral). In all cases, the meter constant is 100 imp/kWhr.

Table 8. F1 and F2 Frequency at 100 imp/kWhr

I_{MAX} (A)	F1 and F2 (Hz)
10	0.18
25	0.46
40	0.73
60	1.10
80	1.47
100	1.83

The F_{1-7} frequencies allow complete coverage of this range of output frequencies on F1 and F2. When designing an energy meter, the nominal design voltage on the voltage channels should be set to half scale to allow for calibration of the meter constant. The current channel should also be no more than half scale when the meter sees maximum load. This allows overcurrent signals and signals with high crest factors to be accommodated. Table 9 shows the output frequency on F1 and F2 when all six analog inputs are half scale.

Table 9. F1 and F2 Frequency with Half-Scale AC Inputs

SCF	S1	S0	F_{1-7} (Hz)	Frequency on F1 and F2 (Half-Scale AC Inputs) (Hz)
0	0	0	2.3	0.23
1	0	0	4.61	0.46
0	0	1	1.15	0.12
1	0	1	4.61	0.46
0	1	0	5.22	0.53
1	1	0	1.15	0.12
0	1	1	0.58	0.06
1	1	1	0.58	0.06

When selecting a suitable F_{1-7} frequency for a meter design, the frequency output at I_{MAX} (maximum load) with a 100 imp/kWhr meter constant should be compared with Column 5 of Table 9. The frequency that is closest in Table 9 determines the best choice of frequency (F_{1-7}). For example, if a 3-phase 4-wire Wye meter with a 25 A maximum current is being designed, the output frequency on F1 and F2 with a 100 imp/kWhr meter constant is 0.46 Hz at 25 A and 220 V (see Table 8). Looking at Table 9, the closest frequency to 0.46 Hz in Column 5 is 0.53 Hz. Therefore, F_{1-7} = 5.22 Hz is selected for this design.

FREQUENCY OUTPUTS

Figure 2 shows a timing diagram for the various frequency outputs. The outputs F1 and F2 are the low frequency outputs that can be used to directly drive a stepper motor or electro-mechanical impulse counter. The F1 and F2 outputs provide two alternating high going pulses. The pulse width (t_1) is set at 120 ms, and the time between the rising edges of F1 and F2 (t_3) is approximately half the period of F1 (t_2). If, however, the period of F1 and F2 falls below 550 ms (1.81 Hz), the pulse width of F1 and F2 is set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table 6.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90 ms-wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are given in Table 7. As in the case of F1 and F2, if the period of CF (t_5) falls below 190 ms, the CF pulse width is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulse width is 25 ms.

NO LOAD THRESHOLD

The ADE7762 includes no load threshold and start-up current circuitry features that eliminate any creep effects in the meter. The circuit is designed to issue a minimum output frequency. Any load generating a frequency lower than this minimum output frequency does not cause a pulse to be issued on F1, F2, or CF. The no-load threshold is determined by the sum of all phases. The minimum output frequency is given as 0.0075% of the full-scale output frequency for each of the F_{1-7} frequency selections, or approximately 0.0029% of the F_{1-7} frequency (see Table 10). For example, for an energy meter with a 100 imp/kWhr meter constant using F_{1-7} (4.61 Hz), the minimum output frequency at F1 or F2 would be 13.35×10^{-5} Hz. This would be 2.13×10^{-3} Hz at CF (16 × F1 Hz). In this example, the no load threshold would be equivalent to 4.8 W of load or a start-up current of 20.03 mA at 240 V.

Table 10. CF, F1, and F2 Minimum Frequency at No Load Threshold

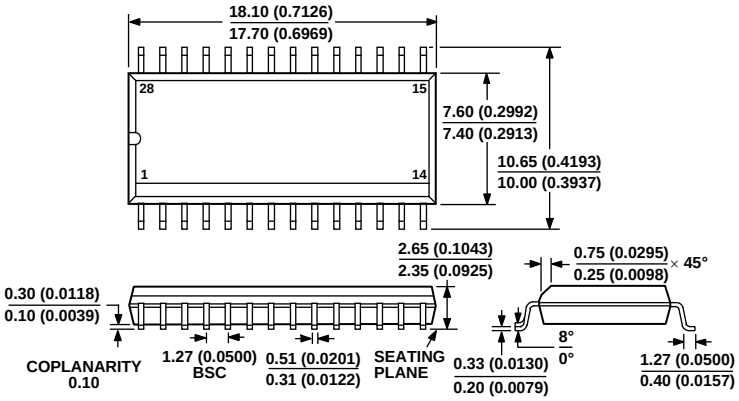
SCF	S1	S0	F1, F2 Minimum (Hz)	CF Minimum (Hz)
0	0	0	6.94E – 05	1.11E – 03
1	0	0	1.39E – 04	1.11E – 03
0	0	1	3.47E – 05	1.11E – 03
1	0	1	1.39E – 04	2.23E – 03
0	1	0	1.58E – 04	2.52E – 02
1	1	0	3.47E – 05	5.55E – 04
0	1	1	1.75E – 05	5.60E – 04
1	1	1	1.75E – 05	2.80E – 04

NEGATIVE POWER INFORMATION

The ADE7762 detects when total power, calculated as the sum of the three phases, is negative. This mechanism can detect an incorrect connection of the meter or generation of negative active energy. The REVP pin output goes active high when negative power is detected on the sum of the three phase inputs. If positive active power is detected on the sum of three phases, then REVP pin output is low.

The REVP pin output changes state at the same time as a pulse is issued on CF. If the sum of the phases measure negative power, then the REVP pin output stays high until the sum of the phases measures positive power.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Package Description	Package Option
ADE7762ARWZ[1]	28-Lead Standard Small Outline Package [SOIC_W]	RW-28[2]
ADE7762ARWZ-RL[1]	28-Lead Standard Small Outline Package [SOIC_W]	RW-28 on 13" Reels
ADE7762ARW	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADE7762ARW-RL	28-Lead Standard Small Outline Package [SOIC_W]	RW-28 on 13" Reels
EVAL-ADE7762EB	ADE7762 Evaluation Board	

[1] Z = Pb-free part.
[2] RW = small outline wide body package in tubes.

NOTES

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D05757-0-1/06(PrB)