Dual, High Speed ECL Comparators

Data Sheet

ADCMP563/ADCMP564

FEATURES

- Differential ECL-compatible outputs
- 700 ps propagation delay input to output
- 75 ps propagation delay dispersion
- Input common-mode range: −2.0 V to +3.0 V
- Robust input protection
- Differential latch control
- Internal latch pull-up resistors
- Power supply rejection greater than 85 dB
- 700 ps minimum pulse width
- 1.5 GHz equivalent input rise time bandwidth
- Typical output rise/fall time of 500 ps
- ESD protection > 4kV HBM, >200V MM
- Programmable hysteresis

APPLICATIONS

- Automatic test equipment
- High speed instrumentation
- Scope and logic analyzer front ends
- Window comparators
- High speed line receivers
- Threshold detection
- Peak detection
- High speed triggers
- Patient diagnostics
- Hand-held test instruments
- Zero crossing detectors
- Line receivers and signal restoration
- Clock drivers

GENERAL DESCRIPTION

The ADCMP563/ADCMP564 are high speed comparators fabricated on Analog Devices' proprietary XFCB process. The devices feature a 700 ps propagation delay with less than 75 ps overdrive dispersion. Dispersion, a measure of the difference in propagation delay under differing overdrive conditions, is a particularly important characteristic of high speed comparators. A separate programmable hysteresis pin is available on the ADCMP564.

A differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from −2.0 V to +3.0 V. Outputs are complementary digital signals that are fully compatible with ECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to −2 V. A latch input, which is included, permits tracking, track-and-hold, or sample-and-hold modes of operation. The latch input pins contain internal pull-ups that set the latch in tracking mode when left open.

The ADCMP563/ADCMP564 are specified over the industrial temperature range (−40°C to +85°C).

FUNCTIONAL BLOCK DIAGRAMS

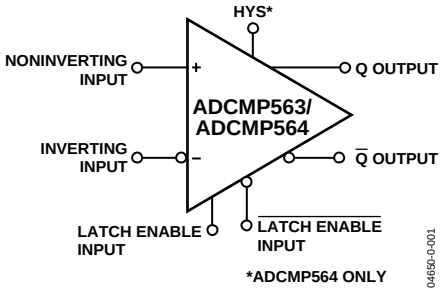


Figure 1.

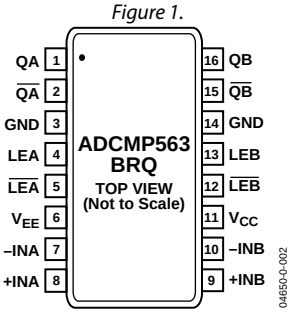


Figure 2. ADCMP563 16-Lead QSOP

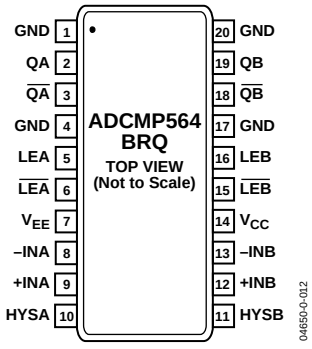
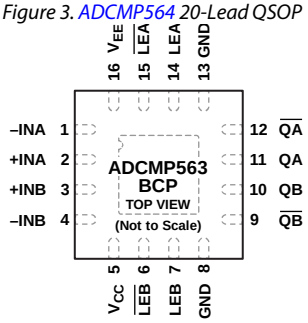


Figure 3. ADCMP564 20-Lead QSOP



NOTES
1. THE EXPOSED PAD SHOULD BE EITHER CONNECTED TO VEE OR LEFT FLOATING.

Figure 4. ADCMP563 16-Lead LFCSP

Rev. D
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagrams ... 1
Specifications ... 3
Absolute Maximum Ratings ... 5
Thermal Considerations ... 5
ESD Caution ... 5
Pin Configurations and Function Descriptions ... 6
Typical Performance Characteristics ... 8
Timing Information ... 10
Application Information ... 11
Clock Timing Recovery ... 11
Optimizing High Speed Performance ... 11
Comparator Propagation Delay Dispersion ... 11
Comparator Hysteresis ... 12
Minimum Input Slew Rate Requirement ... 12
Typical Application Circuits ... 13
Outline Dimensions ... 14
Ordering Guide ... 15

REVISION HISTORY

4/16—Rev. C to Rev. D

Changes to Figure 4 ... 1
Changes to Figure 7 ... 6
Updates Outline Dimensions ... 15
Changes to Ordering Guide ... 15

6/11—Rev. B to Rev. C

Changes to Figure 4 ... 1
Changes to Figure 7 and LFCSP Pin Numbers (Table 3) ... 6
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

5/05—Rev. A to Rev. B

Added 16-Lead LFCSP ... Universal
Changes to Applications ... 1
Changes to Table 1 ... 3
Changes to Optimizing High Speed Performance Section ... 11
Changes to Comparator Hysteresis Section ... 12
Changes to Minimum Input Slew Rate Requirement Section ... 12
Changes to Ordering Guide ... 14

7/04—Rev. 0 to Rev. A

Changes to Specification Table ... 4
Changes to Figure 14 ... 9
Changes to Figure 21 ... 12
Changes to Figure 23 ... 13

4/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = +5.0 V, V_{EE} = −5.2 V, T_A = −40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Input Voltage Range			−2.0		3.0	V
Input Differential Voltage			−5		+5	V
Input Offset Voltage	V_{OS}	V_{CM} = 0 V	−10.0	±2.0	+10.0	mV
Input Offset Voltage Channel Matching				±2.0		mV
Offset Voltage Temperature Coefficient	$\Delta V_{OS}/d_T$			2.0		µV/°C
Input Bias Current	I_{BC}	@ −IN = −2 V, +IN = +3 V	−10.0	±3	+10.0	µA
Input Bias Current Temperature Coefficient				0.5		nA/°C
Input Offset Current				±1.0		µA
Input Capacitance	C_{IN}			0.75		pF
Input Resistance, Differential Mode				750		kΩ
Input Resistance, Common Mode				1800		kΩ
Active Gain	A_V			63		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.0 V to +3.0 V		80		dB
Hysteresis		R_{HYS} = ∞		±1.0		mV
LATCH ENABLE CHARACTERISTICS						
Latch Enable Voltage Range			−2.0		0	V
Latch Enable Differential Input Voltage			0.4		2.0	V
Latch Enable Input High Current		@ 0.0 V	−300		+300	µA
Latch Enable Input Low Current		@ −2.0 V	−300		+300	µA
LE Voltage, Open		Latch inputs not connected	−0.2	0	+0.1	V
$\overline{LE}$ Voltage, Open		Latch inputs not connected	−2.8	−2.6	−2.4	V
Latch Setup Time	t_S	V_{OD} = 250 mV		200		ps
Latch Hold Time	t_H	V_{OD} = 250 mV		200		ps
Latch to Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 250 mV		500		ps
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 250 mV		500		ps
DC OUTPUT CHARACTERISTICS						
Output Voltage—High Level	V_{OH}	ECL 50 Ω to −2.0 V	−1.15		−0.81	V
Output Voltage—Low Level	V_{OL}	ECL 50 Ω to −2.0 V	−1.95		−1.54	V
Rise Time	t_R	10% to 90%		530		ps
Fall Time	t_F	10% to 90%		450		ps
AC PERFORMANCE						
Propagation Delay	t_{PD}	V_{OD} = 1 V		700		ps
		V_{OD} = 20 mV		830		ps
Propagation Delay Temperature Coefficient	$\Delta t_{PD}/d_T$	V_{OD} = 1 V		0.25		ps/°C
Prop Delay Skew—Rising Transition to Falling Transition		V_{OD} = 1 V		50		ps
Within Device Propagation Delay Skew—Channel-to-Channel		V_{OD} = 1 V		50		ps
Overdrive Dispersion		20 mV ≤ V_{OD} ≤ 100 mV		75		ps
		100 mV ≤ V_{OD} ≤ 1.5 V		75		ps
Slew Rate Dispersion		0.4 V/ns ≤ SR ≤ 1.33 V/ns		50		ps
Pulse Width Dispersion		750ps ≤ PW ≤ 10 ns		25		ps
Duty Cycle Dispersion		33 MHz, 1 V/ns, 0.5 V		10		ps
Common-Mode Voltage Dispersion		1 V swing, −1.5 V ≤ V_{CM} ≤ +2.5 V		10		ps

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AC PERFORMANCE (Continued)						
Equivalent Input Rise Time Bandwidth[1]	BW_{EQ}	0 V to 1 V swing, 2 V/ns		1500		MHz
Maximum Toggle Rate		>50% output swing, 50% duty cycle		800		MHz
Minimum Pulse Width	PW_{MIN}	Δt_{PD} < 25 ps		700		ps
RMS Random Jitter		V_{OD} = 400 mV, 1.3 V/ns, 312 MHz, 50% duty cycle		1.0		ps
Unit to Unit Propagation Delay Skew				100		ps
POWER SUPPLY						
Positive Supply Current	I_{VCC}	@ +5.0 V	2	3.2	5	mA
Negative Supply Current	I_{VEE}	@ −5.2 V	10	19	25	mA
Positive Supply Voltage	V_{CC}	Dual	4.75	5.0	5.25	V
Negative Supply Voltage	V_{EE}	Dual	−4.96	−5.2	−5.45	V
Power Dissipation	P_D	Dual, without load	90	120	150	mW
		Dual, with load	150	180	230	mW
DC Power Supply Rejection Ratio—V_{CC}	$PSRR_{VCC}$			85		dB
DC Power Supply Rejection Ratio—V_{EE}	$PSRR_{VEE}$			85		dB
HYSTERESIS (ADCMP564 Only)						
Hysteresis		R_{HYS} = 23.5 kΩ		20		mV
		R_{HYS} = 9.0 kΩ		70		mV
Hysteresis Pin Bias Voltage		Referred to AGND		−1		V
Hysteresis Pin Series Resistance				3		kΩ

[1] Equivalent input rise time bandwidth assumes a first-order input response and is calculated by the following formula: $BW_{EQ} = 0.22/\sqrt{(tr_{COMP}^2 - tr_{IN}^2)}$, where tr_{IN} is the 20/80 input transition time applied to the comparator and tr_{COMP} is the effective transition time, as digitized by the comparator input.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages	
Positive Supply Voltage (V_{CC} to GND)	−0.5 V to +6.0 V
Negative Supply Voltage (V_{EE} to GND)	−6.0 V to +0.5 V
Ground Voltage Differential	−0.5 V to +0.5 V
Input Voltages	
Input Common-Mode Voltage	−3.0 V to +4.0 V
Differential Input Voltage	−7.0 V to +7.0 V
Input Voltage, Latch Controls	V_{EE} to +0.5 V
Output	
Output Current	30 mA
Temperature	
Operating Temperature, Ambient	−40°C to +85°C
Operating Temperature, Junction	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CONSIDERATIONS

The ADCMP563 QSOP 16-lead package option has a θ_{JA} (junction-to-ambient thermal resistance) of 104°C/W in still air.

The ADCMP563 LFCSP 16-lead package option has a θ_{JA} (junction-to-ambient thermal resistance) of 70°C/W in still air.

The ADCMP564 QSOP 20-lead package option has a θ_{JA} (junction-to-ambient thermal resistance) of 80°C/W in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

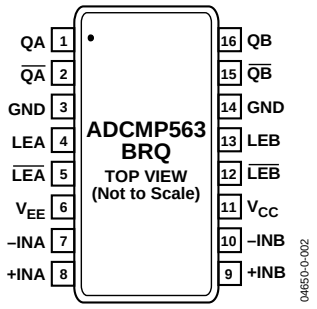
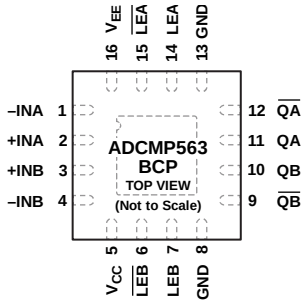


Figure 5. ADCMP563 16-Lead QSOP
Pin Configuration



NOTES
1. THE EXPOSED PAD SHOULD BE EITHER CONNECTED TO VEE OR LEFT FLOATING.

Figure 7. ADCMP563 16-Lead LFCSP
Pin Configuration

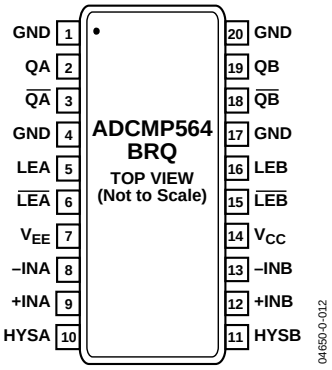


Figure 6. ADCMP564 20-Lead QSOP
Pin Configuration

Table 3. Pin Function Descriptions

Pin No.				
ADCMP563 16-Lead QSOP	ADCMP563 16-Lead LFCSP	ADCMP564 20-Lead QSOP	Mnemonic	Function
		1	GND	Analog Ground.
1	11	2	QA	One of Two Complementary Outputs for Channel A. QA is logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in compare mode). See the description of the LEA pin for more information.
2	12	3	$\overline{QA}$	One of Two Complementary Outputs for Channel A. $\overline{QA}$ is logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in compare mode). See the description of the LEA pin for more information.
3	13	4	GND	Analog Ground.
4	14	5	LEA	One of Two Complementary Inputs for Channel A Latch Enable. In compare mode (logic high), the output tracks change at the input of the comparator. In latch mode (logic low), the output reflects the input state just prior to the comparator being placed in the latch mode. $\overline{LEA}$ must be driven in conjunction with LEA. If left unconnected, the comparator defaults to compare mode.
5	15	6	$\overline{LEA}$	One of Two Complementary Inputs for Channel A Latch Enable. In compare mode (logic low), the output tracks change at the input of the comparator. In latch mode (logic high), the output reflects the input state just prior to the

Pin No.				
ADCMP563 16-Lead QSOP	ADCMP563 16-Lead LFCSP	ADCMP564 20-Lead QSOP	Mnemonic	Function
				comparator being placed in the latch mode. LEA must be driven in conjunction with $\overline{LEA}$. If left unconnected, the comparator defaults to compare mode.
6	16	7	V_{EE}	Negative Supply Terminal.
7	1	8	−INA	Inverting Analog Input of the Differential Input Stage for Channel A. The Inverting A input must be driven in conjunction with the Noninverting A input.
8	2	9	+INA	Noninverting Analog Input of the Differential Input Stage for Channel A. The Noninverting A input must be driven in conjunction with the Inverting A input.
		10	HYSA	Programmable Hysteresis Input.
		11	HYSB	Programmable Hysteresis Input.
9	3	12	+INB	Noninverting Analog Input of the Differential Input Stage for Channel B. The Noninverting B input must be driven in conjunction with the Inverting B input.
10	4	13	−INB	Inverting Analog Input of the Differential Input Stage for Channel B. The Inverting B input must be driven in conjunction with the Noninverting B input.
11	5	14	V_{CC}	Positive Supply Terminal.
12	6	15	$\overline{LEB}$	One of Two Complementary Inputs for Channel B Latch Enable. In compare mode (logic low), the output tracks change at the input of the comparator. In latch mode (logic high), the output reflects the input state just prior to the comparator being placed in the latch mode. LEB must be driven in conjunction with $\overline{LEB}$. If left unconnected, the comparator defaults to compare mode.
13	7	16	LEB	One of Two Complementary Inputs for Channel B Latch Enable. In compare mode (logic high), the output tracks change at the input of the comparator. In latch mode (logic low), the output reflects the input state just prior to the comparator being placed in the latch mode. $\overline{LEB}$ must be driven in conjunction with LEB. If left unconnected, the comparator defaults to compare mode.
14	8	17	GND	Analog Ground.
15	9	18	$\overline{QB}$	One of Two Complementary Outputs for Channel B. $\overline{QB}$ is logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in compare mode). See the description of the LEB pin for more information.
16	10	19	QB	One of Two Complementary Outputs for Channel B. QB is logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in compare mode). See the description of the LEB pin for more information.
		20	GND	Analog Ground.
	EPAD		EPAD	Exposed Pad. The exposed pad should be either connected to VEE or left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C, unless otherwise noted.

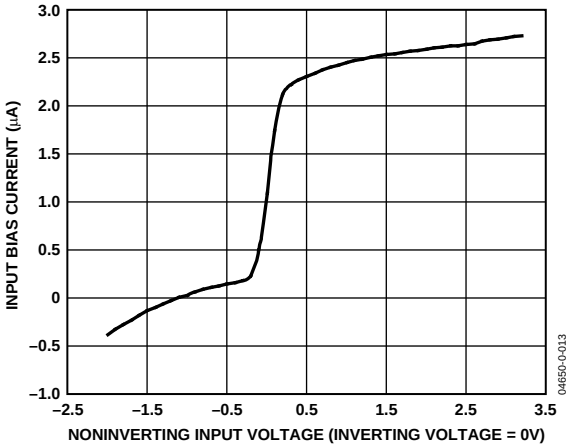


Figure 8. Input Bias Current vs. Input Voltage

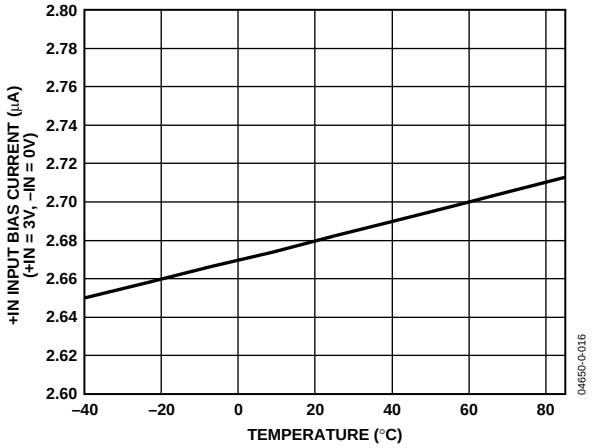


Figure 11. Input Bias Current vs. Temperature

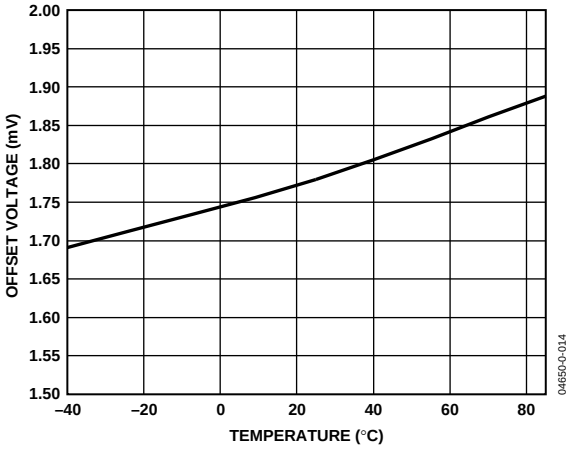


Figure 9. Input Offset Voltage vs. Temperature

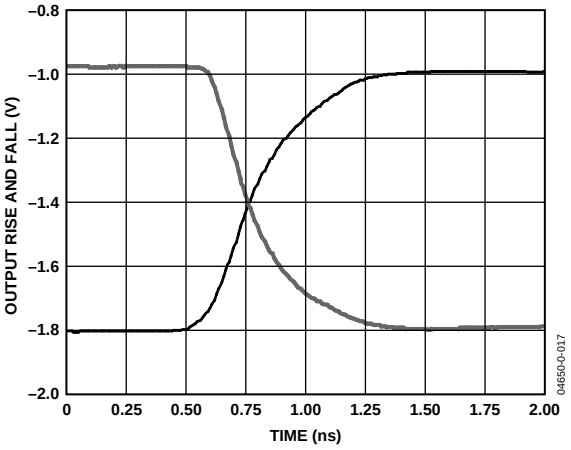


Figure 12. Rise and Fall of Outputs vs. Time

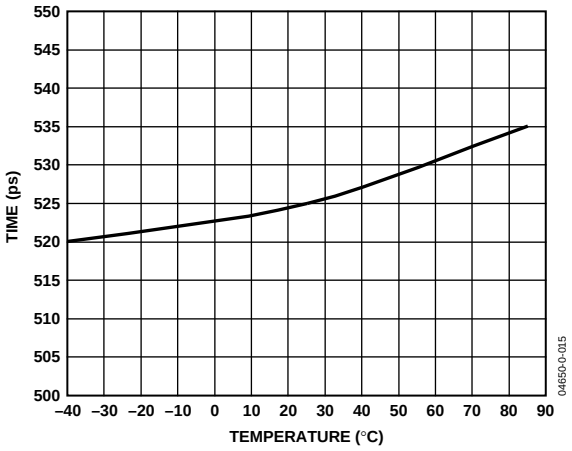


Figure 10. Rise Time vs. Temperature

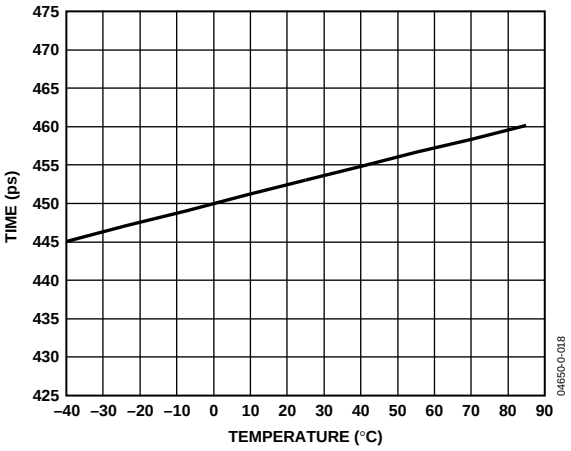


Figure 13. Fall Time vs. Temperature

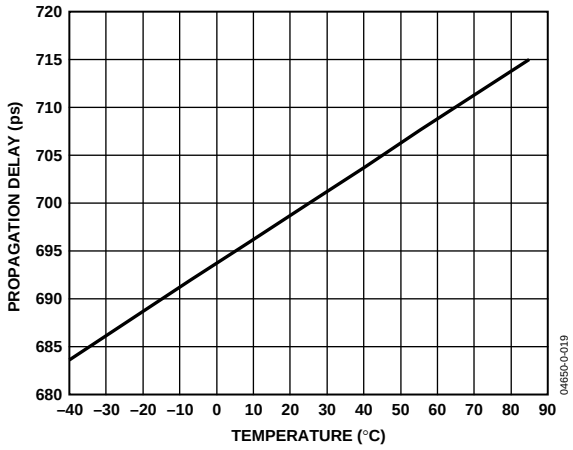


Figure 14. Propagation Delay vs. Temperature

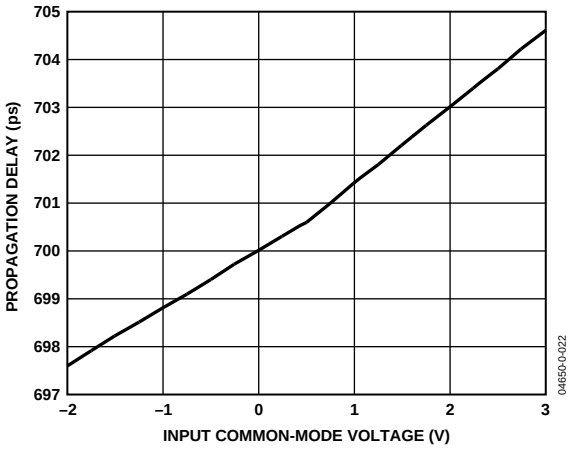


Figure 17. Propagation Delay vs. Common-Mode Voltage

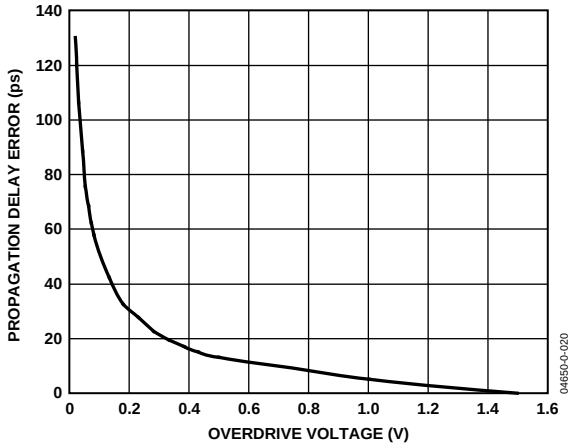


Figure 15. Propagation Delay Error vs. Overdrive Voltage

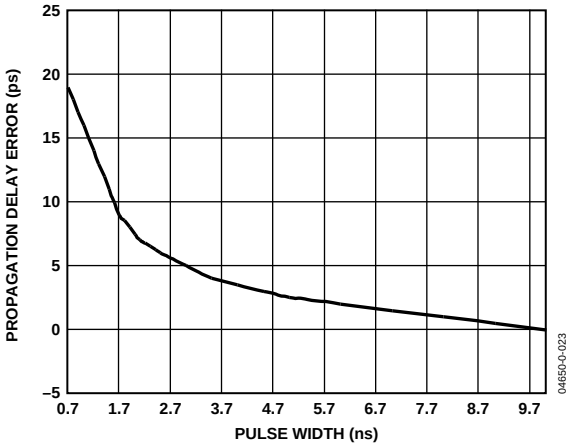


Figure 18. Propagation Delay Error vs. Pulse Width

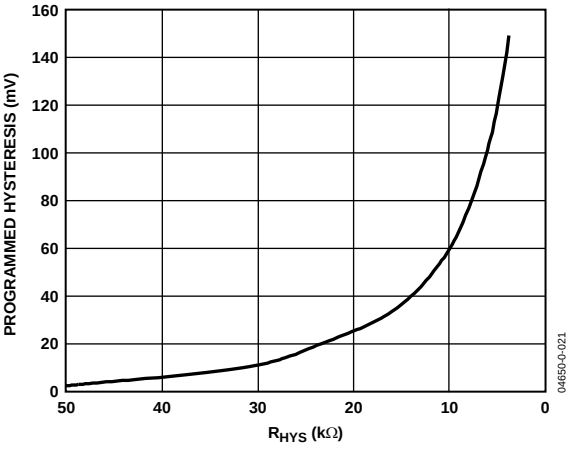


Figure 16. Comparator Hysteresis vs. R_{HYS}

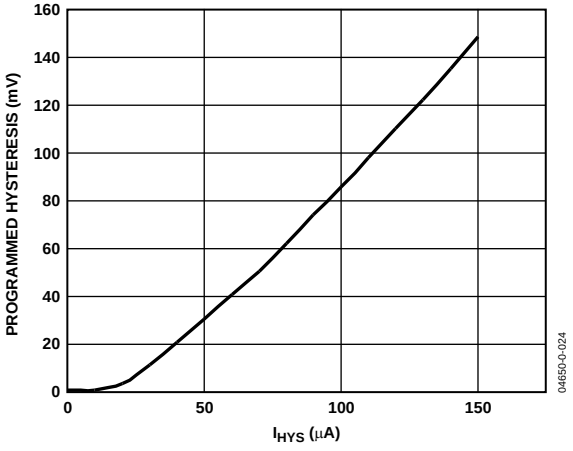


Figure 19. Comparator Hysteresis vs. I_{HYS}

TIMING INFORMATION

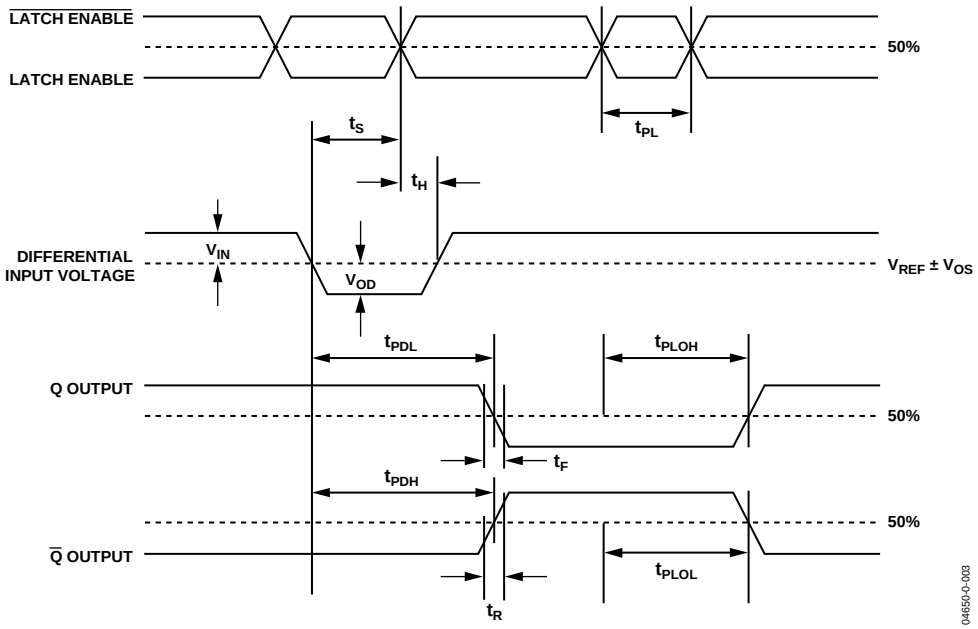


Figure 20. System Timing Diagram

Figure 20 shows the compare and latch features of the ADCMP563. Table 4 describes the terms in the diagram.

Table 4. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input-to-Output High Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input-to-Output Low Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch Enable to Output High Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch Enable to Output Low Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum Hold Time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum Latch Enable Pulse Width	Minimum time the latch enable signal must be high to acquire an input signal change.
t_S	Minimum Setup Time	Minimum time before the negative transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs.
t_R	Output Rise Time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output Fall Time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage Overdrive	Difference between the differential input and reference input voltages.

APPLICATION INFORMATION

The ADCMP563/ADCMP564 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any ADCMP563/ADCMP564 design is the use of a low impedance ground plane. A ground plane, as part of a multilayer board, is recommended for proper high speed performance. Using a continuous conductive plane over the surface of the circuit board can create this, allowing breaks in the plane only for necessary signal paths. The ground plane provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused by ground bounce. A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1 µF electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin to ground. These capacitors reduce any potential voltage ripples from the power supply. In addition, a 10 nF ceramic capacitor should be placed as close as possible from the power supply pins on the ADCMP563/ADCMP564 to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

The LATCH ENABLE input is active low (latched). If the latching function is not used, the LATCH ENABLE input can be left open or grounded (ground is an ECL logic high). The complementary input, $\overline{\text{LATCH ENABLE}}$, can be left open or tied to −2.0 V. Leaving the latch inputs unconnected or providing the proper voltages disables the latching function.

Occasionally, one of the two comparator stages within the ADCMP563/ADCMP564 is not used. The inputs of the unused comparator should not be allowed to float. The high internal gain can cause the output to oscillate (possibly affecting the comparator that is being used), unless the output is forced into a fixed state. This is easily accomplished by ensuring that the two inputs are at least one diode drop apart, while also appropriately connecting the LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ inputs as described previously.

The best performance is achieved with the use of proper ECL terminations. The open emitter outputs of the ADCMP563/ADCMP564 are designed to be terminated through 50 Ω resistors to −2.0 V, or any other equivalent ECL termination. If a −2.0 V supply is not available, an 82 Ω resistor to ground and a 130 Ω resistor to −5.2 V provide a suitable equivalent. If high speed ECL signals must be routed more than a centimeter, microstrip or stripline techniques may be required to ensure proper transition times and prevent output ringing.

CLOCK TIMING RECOVERY

Comparators are often used in digital systems to recover clock timing signals. High speed square waves transmitted over a distance, even tens of centimeters, can become distorted due to stray capacitance and inductance. Poor layout or improper termination can also cause reflections on the transmission line, further distorting the signal waveform. A high speed comparator can be used to recover the distorted waveform while maintaining a minimum of delay.

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator amplifier, proper design and layout techniques should be used to ensure optimal performance from the ADCMP563/ADCMP564. The performance limits of high speed circuitry all too often are the result of stray capacitance, improper ground impedance, or other layout issues.

Minimizing resistance from source to the input is an important consideration in maximizing the high speed operation of the ADCMP563/ADCMP564. Source resistance, in combination with equivalent input capacitance, could cause a lagged response at the input, thus delaying the output. The input capacitance of the ADCMP563/ADCMP564, in combination with stray capacitance from an input pin to ground, could result in several picofarads of equivalent capacitance. A combination of 3 kΩ source resistance and 5 pF input capacitance yields a time constant of 15 ns, which is significantly slower than the 750 ps capability of the ADCMP563/ADCMP564. Source impedances should be significantly less than 100 Ω for best performance.

Sockets should be avoided due to stray capacitance and inductance. If proper high speed techniques are used, the devices should be free from oscillation when the comparator input signal passes through the switching threshold.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP563/ADCMP564 have been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100 mV to 1.5 V. Propagation delay overdrive dispersion is the change in propagation delay that results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy because the ADCMP563/ADCMP564 are far less sensitive to input variations than most comparator designs.

Propagation delay dispersion is important in critical timing applications such as ATE, bench instruments, and nuclear instrumentation. Overdrive dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (Figure 21). For the ADCMP563/ADCMP564, overdrive dispersion is typically 75 ps as the overdrive is changed from 100 mV to 1.5 V. This specification applies for both positive and negative overdrive because the ADCMP563 and the ADCMP564 have equal delays for positive and negative going inputs.

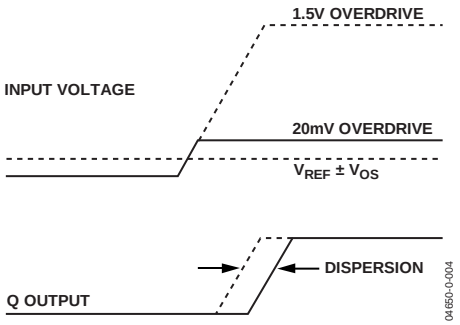


Figure 21. Propagation Delay Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often useful in a noisy environment, or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 22. If the input voltage approaches the threshold from the negative direction, the comparator switches from 0 to 1 when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in a 1 state until the threshold $-V_H/2$ is crossed while coming from the positive direction. In this manner, noise centered on 0 V input does not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. A limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that can be load dependent and is not symmetrical about the threshold. The external feedback network can also introduce significant parasitics, which reduce high speed performance and can induce oscillation in some cases.

In the ADCMP564, hysteresis is generated through the programmable hysteresis pin. A resistor from the HYS pin to GND creates a current into the part that is used to generate hysteresis. Hysteresis generated in this manner is independent of output swing and is symmetrical around the trip point. The hysteresis vs. resistance curve is shown in Figure 23.

A current may be sourced into the HYS pin. The pin is biased approximately 1 V below AGND and has a 3 kΩ series resistance. The relationship between the current applied to the HYS pin and the resulting hysteresis is shown in Figure 19.

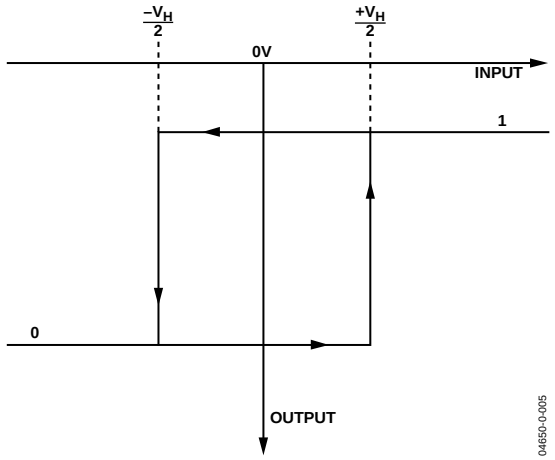


Figure 22. Comparator Hysteresis Transfer Function

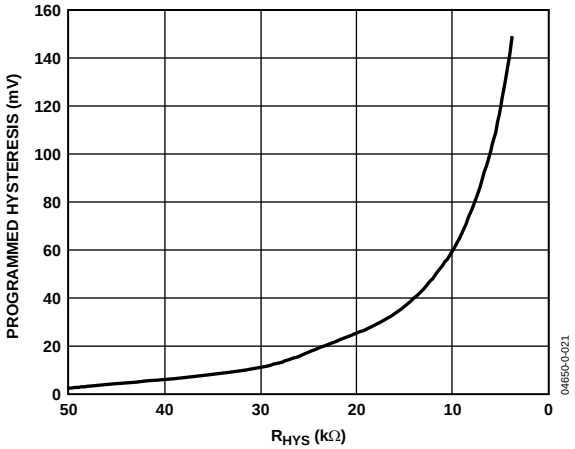


Figure 23. Comparator Hysteresis vs. R_{HYS}

MINIMUM INPUT SLEW RATE REQUIREMENT

As for all high speed comparators, a minimum slew rate must be met to ensure that the device does not oscillate as the input crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the parasitics of the package. ADI recommends a slew rate of 1 V/µs or faster to ensure a clean output transition. If slew rates less than 1 V/µs are used, hysteresis can be added to prevent the oscillation.

TYPICAL APPLICATION CIRCUITS

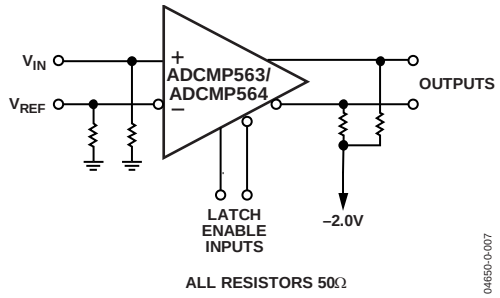


Figure 24. High Speed Sampling Circuits

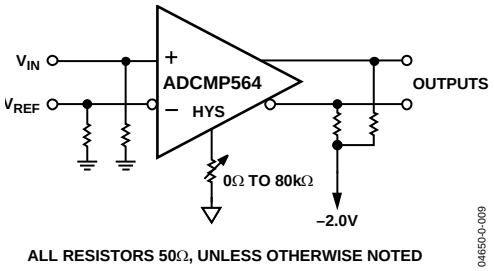


Figure 26. Adding Hysteresis Using the HYS Control Pin

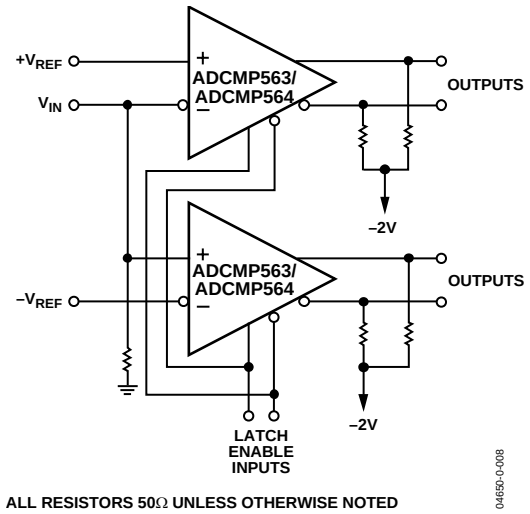


Figure 25. High Speed Window Comparator

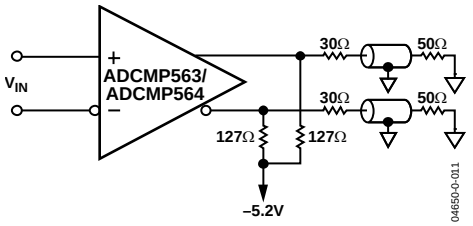
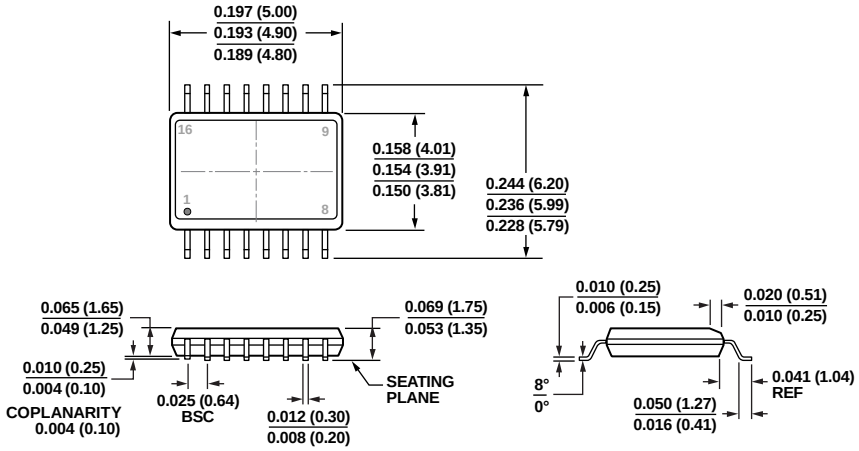


Figure 27. One Method to Interface an ECL Output to an Instrument with a 50 Ω to Ground Input

OUTLINE DIMENSIONS

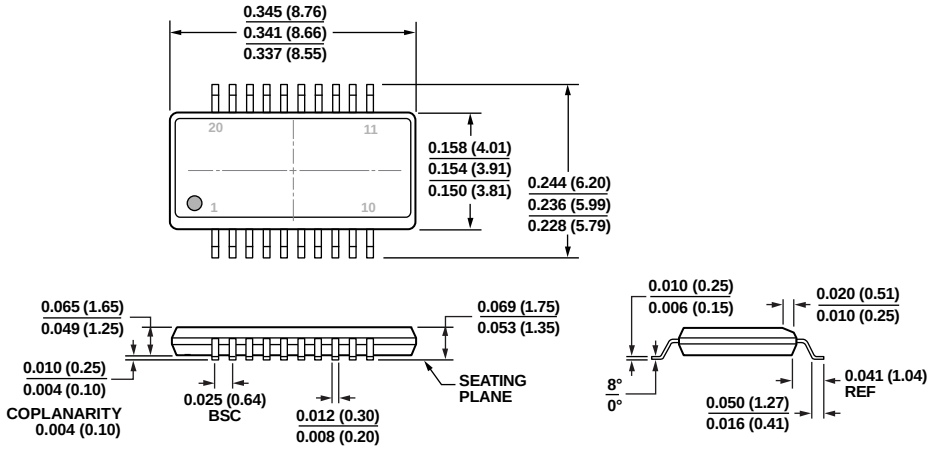


COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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Figure 28. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

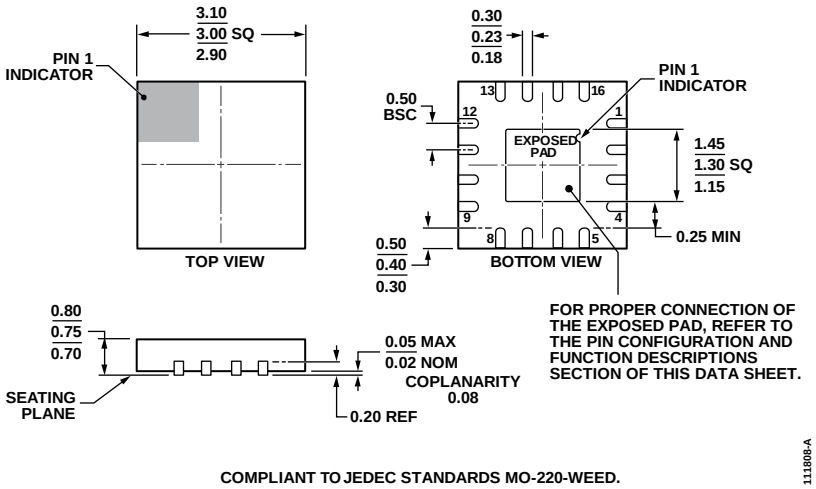


COMPLIANT TO JEDEC STANDARDS MO-137-AD

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09-12-2014-A

Figure 29. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 30. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-21)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADCMP563BRQZ	−40°C to +85°C	16-Lead QSOP	RQ-16	
ADCMP563BCPZ-R2	−40°C to +85°C	16-Lead LFCSP 250 Unit Reel	CP-16-21	G01
ADCMP563BCPZ-RL7	−40°C to +85°C	16-Lead LFCSP 1,500 Unit Reel	CP-16-21	G01
ADCMP563BCPZ-WP	−40°C to +85°C	16-Lead LFCSP 50 Unit Waffle Pack	CP-16-21	G01
ADCMP564BRQZ	−40°C to +85°C	20-Lead QSOP	RQ-20	
EVAL-ADCMP563BRQZ		Evaluation Board		
EVAL-ADCMP564BRQZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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