Ultralow Power Voltage Comparator with Reference

Data Sheet

ADCMP380

FEATURES

- Comparator with on-chip reference
- Ultralow power consumption with I_{CC} = 92 nA (typical)
- Precision low voltage monitoring down to 0.5 V
- Accurate internal reference level over full temperature range
  - ±1.6% at 1 V
  - ±2.2% at 0.5 V
- Enable input
- 23 µs typical propagation delay
- Open-drain type output
- Input glitch immunity
- Available in a 1.46 mm × 0.96 mm WLCSP
- Operational temperature range: −40°C to +85°C

APPLICATIONS

- Portable/battery-operated equipment
- Battery monitors
- Energy harvesting

FUNCTIONAL BLOCK DIAGRAM

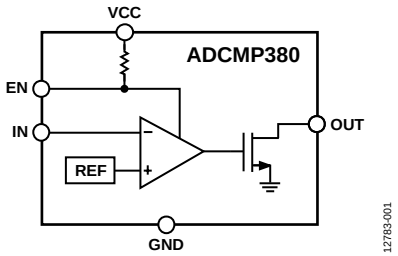


Figure 1.

GENERAL DESCRIPTION

The ADCMP380 is an ultralow power voltage comparator with internal reference suitable for use in general-purpose applications. The ultralow power consumption of this device makes it suitable for power efficiency sensitive systems, such as battery-powered portable devices and energy meters.

The ADCMP380 is available with a 0.5 V and 1 V internal reference with ±2.2% and ±1.6% accuracy, respectively, over the full temperature range; this internal reference enables the device to monitor the node of interest accurately to 0.5 V. The enable input allows the user to hold the output low regardless of the state of the input.

The ADCMP380 is available in a 6-ball, 1.46 mm × 0.96 mm WLCSP and is specified over the temperature range of −40°C to +85°C.

Table 1. Selection Table

Part No.	Reference Voltage (V)	Output
ADCMP380-1	1	Open-drain
ADCMP380-2	0.5	Open-drain

Rev. A
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REVISION HISTORY

2/16—Rev. 0 to Rev. A

Changes to Ordering Guide 10

3/15—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2 V to 5.5 V, V_{IN} < V_{CC} + 0.3 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING VOLTAGE RANGE	V_{CC}	2		5.5	V	Guarantees valid OUT output
		0.9			V	Guarantees OUT low
UNDERVOLTAGE LOCKOUT (UVLO)						
Input Voltage Rising	$UVLO_{RISE}$			1.95	V	
Input Voltage Falling	$UVLO_{FALL}$	1.65			V	
Hysteresis	$UVLO_{HYS}$		90		mV	
INPUT CURRENT						
VCC Quiescent Current	I_{CC}		92	190	nA	OUT high
				110	nA	OUT high, T_A = 25°C
IN Average Input Current	I_{VIN}		4	8.5	nA	V_{IN} = 2 V, V_{CC} = 5.5 V
			4	32	nA	V_{IN} = 2 V, V_{CC} = 2 V
REFERENCE VOLTAGE	V_{REF}					Input falling
ADCMP380-1		0.984	1	1.016	V	V_{REF} = 1 V
ADCMP380-2		0.489	0.5	0.511	V	V_{REF} = 0.5 V
INPUT HYSTERESIS	V_{HYST}		10.3		mV	
PROPAGATION DELAY						
IN to OUT	t_{PD}	13.5	23	35	µs	IN falling with V_{REF} × 10% overdrive
		22	39.5	61	µs	IN rising with V_{REF} × 10% overdrive
IN GLITCH REJECTION	t_{GR_IN}		21		µs	IN falling with V_{REF} × 10% overdrive
			38		µs	IN rising with V_{REF} × 10% overdrive
OUT OUTPUT						
Output Voltage Low	V_{OUT_OL}			0.4	V	V_{CC} > 4.25 V, I_{SINK} = 6.5 mA
				0.4	V	V_{CC} > 2.5 V, I_{SINK} = 6 mA
				0.4	V	V_{CC} > 1.2 V, I_{SINK} = 4.6 mA
				0.4	V	V_{CC} > 0.9 V, I_{SINK} = 0.9 mA
Leakage Current				5	nA	V_{OUT} = V_{CC} = 5.5 V
EN INPUT						
V_{IL}				0.4	V	
V_{IH}		0.9			V	
EN Glitch Rejection			0.4		µs	
EN to OUT Delay	t_{D_EN}		0.65		µs	EN falling
EN Pull-Up Resistance		0.5	0.6	0.82	MΩ	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VCC	−0.3 V to +6 V
OUT	−0.3 V to +6 V
IN	−0.3 V to +6 V
EN	−0.3 V to V_{CC} + 0.3 V
Input/Output Current	10 mA
Storage Temperature Range	−40°C to +150°C
Operating Temperature Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on an FR4 board with a minimum footprint.

Table 4.

Package Type	θ_{JA}	Unit
6-Ball WLCSP	105.6	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

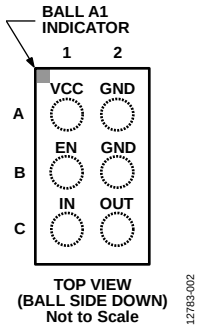


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. It is recommended to place a 0.1 µF decoupling capacitor between the VCC pin and the GND pin.
A2	GND	Ground. Both GND pins on the ADCMP380 must be grounded.
B1	EN	Active High Output Enable Input. If required, a 0.1 µF capacitor between the EN pin and ground provides additional noise immunity.
B2	GND	Ground. Both GND pins on the ADCMP380 must be grounded.
C1	IN	Comparator Input.
C2	OUT	Open-Drain Comparator Output.

TYPICAL PERFORMANCE CHARACTERISTICS

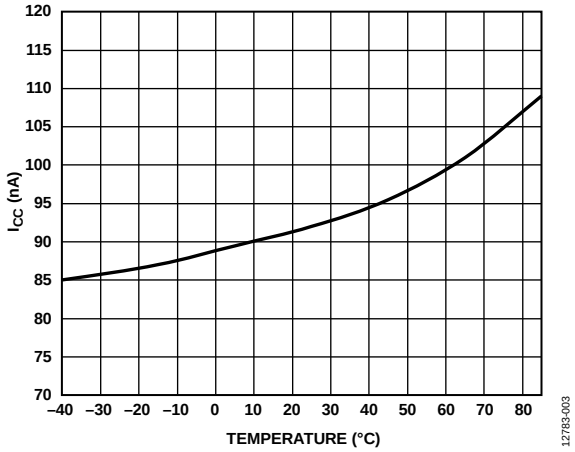


Figure 3. Supply Current (I_{CC}) vs. Temperature

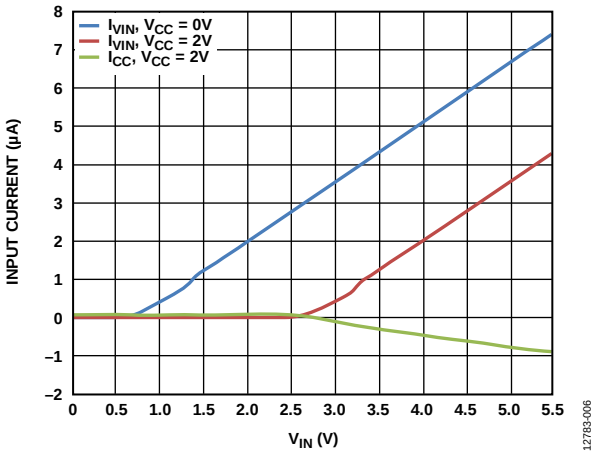


Figure 6. Input Current for IN and VCC vs. V_{IN}

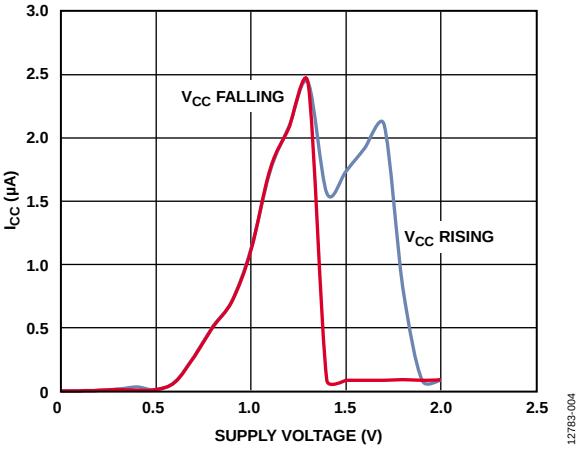


Figure 4. Supply Current (I_{CC}) vs. Supply Voltage, V_{CC} < 2 V

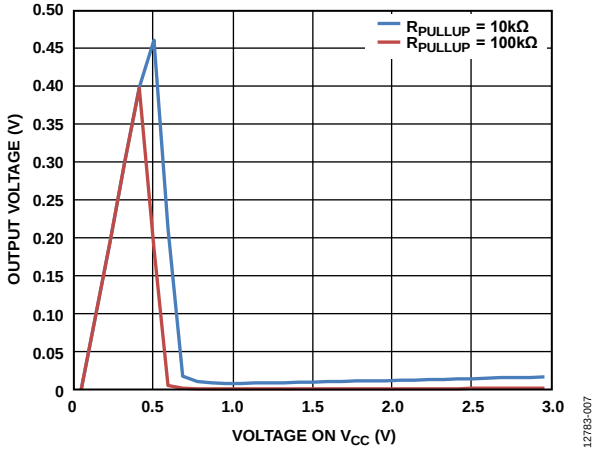


Figure 7. Output Voltage vs. Voltage on VCC
(with the OUT Pin Pulled up to the VCC Pin Through R_{PULLUP})

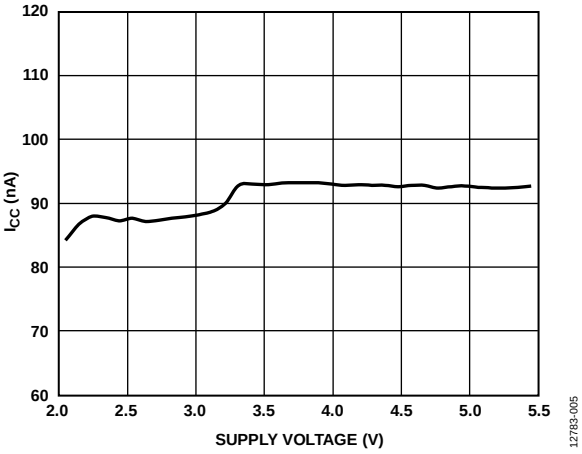


Figure 5. Supply Current (I_{CC}) vs. Supply Voltage

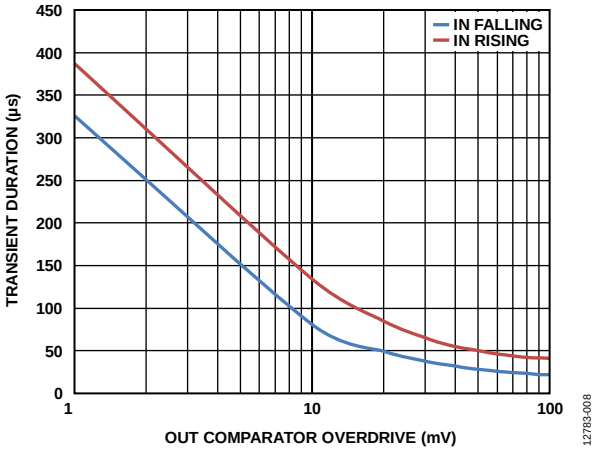


Figure 8. Maximum Transient Duration vs. OUT Comparator Overdrive

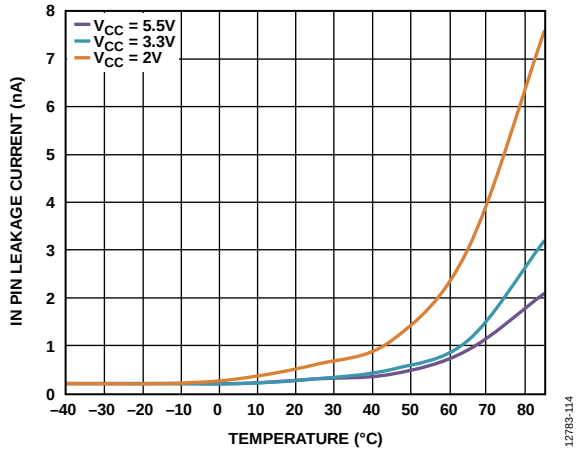


Figure 9. IN Pin Leakage Current vs. Temperature

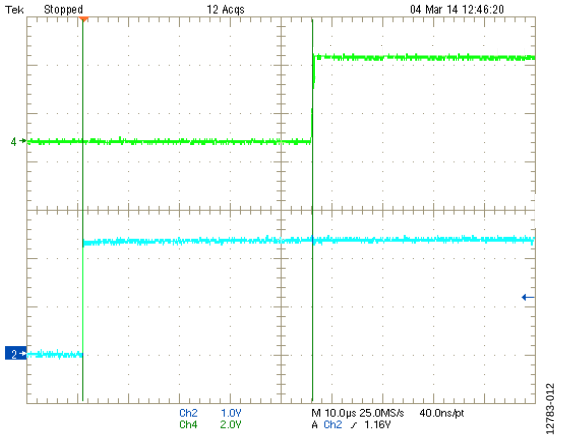


Figure 12. OUT Delay With IN Rising, Channel 2 = IN, Channel 4 = OUT

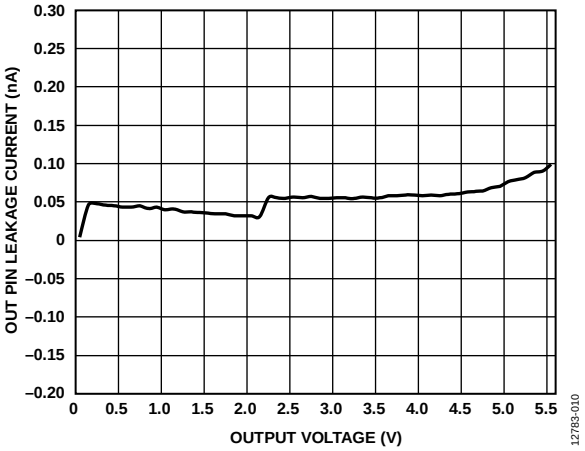


Figure 10. OUT Pin Leakage Current vs. Output Voltage, OUT Logic High

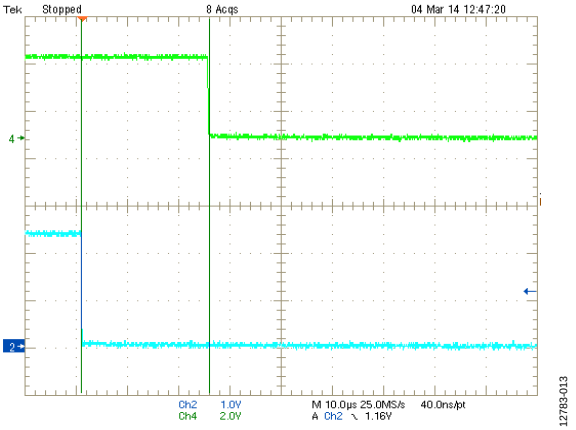


Figure 13. OUT Delay With IN Falling, Channel 2 = IN, Channel 4 = OUT

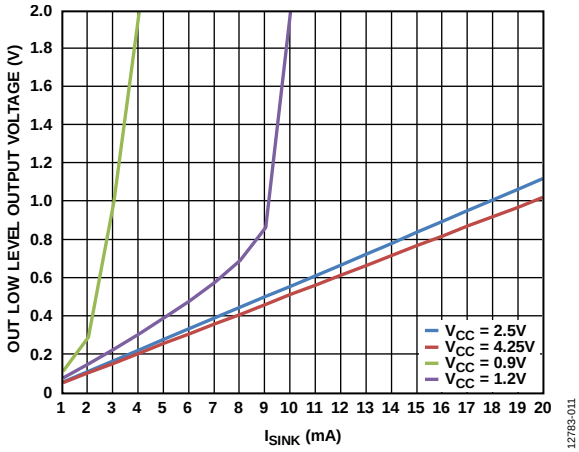


Figure 11. OUT Low Level Output Voltage (V_{OUT_OL}) vs. Sink Current (I_{SINK})

THEORY OF OPERATION

The ADCMP380 ultralow power voltage comparator is especially suited for battery-powered applications due to the maximum 190 nA quiescent current. The internal precision reference and the low input leakage current allow the user to monitor the voltage of interest accurately through external resistor dividers. The device features internal input hysteresis and an open-drain output. The output remains logic high after the voltage on the IN pin is above the internal reference voltage. The device keeps the output in a logic low state whenever the supply voltage on the VCC pin is below the UVLO threshold. The output can be disabled and remains low if the EN pin is pulled low, regardless of the status of the IN pin.

TRANSIENT IMMUNITY

To avoid unnecessary output state change caused by fast power supply transients, an input glitch filter is added to the IN pin of the ADCMP380 to filter out the transient glitches on the pin.

Figure 8 shows the comparator overdrive (that is, the maximum magnitude of positive and negative going pulses with respect to the reference voltage) vs. the pulse duration without changing the state of the output.

OUTPUT

The output of ADCMP380 comparator is open-drain. The output is guaranteed to be logic low from when V_{CC} = 0.9 V to when the device exits ULVO.

When the IN voltage falls below the internal reference voltage, the OUT pin asserts low within 23 µs (typical). When the monitored voltage rises above the reference voltage plus hysteresis, the OUT pin asserts high within 39.5 µs.

EN INPUT

Driving EN low asserts the output low. The EN input has a 0.6 MΩ internal pull-up resistor so that the input is always high when unconnected. To drive the EN input, use an external signal or a push-button switch to ground; debounce circuitry is integrated on-chip for this purpose. Noise immunity is provided on the EN input, and fast, negative going transients of up to 0.4 µs (typical) are ignored. If required, a 0.1 µF capacitor between the EN pin and ground provides additional noise immunity.

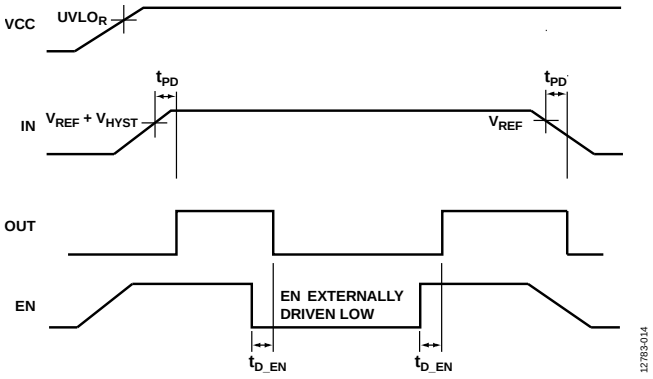


Figure 14. Timing Diagram

ADDING HYSTERESIS

To prevent oscillations at the output caused by noise or slowly moving signals passing the switching threshold, positive feedback can add hysteresis to the input.

For the configuration shown in Figure 15, connect the bottom end of the input resistor divider to the output; the effective threshold is altered based on the output state.

The input falling threshold level is given by

$$V_{IN_FALL} = \frac{V_{REF}(R1 + R2 + R_{PULLUP}) - V_{SUPPLY}R1}{R2 + R_{PULLUP}}$$

where V_{REF} = 0.6 V, assuming $R_{LOAD} >> R2$ and R_{PULLUP}, where R_{LOAD} is the resistance on the load.

The input rising threshold level is given by

$$V_{IN_RISE} = \frac{V_{REF}(R1 + R2)}{R2}$$

The additional hysteresis is the difference between these voltage levels and is given by

$$\Delta V_{IN} = \frac{V_{REF}R1R_{PULLUP} + V_{SUPPLY}R1R2}{R2 \times R2 + R2 \times R_{PULLUP}}$$

Note that the built in hysteresis of the device is neglected in this calculation.

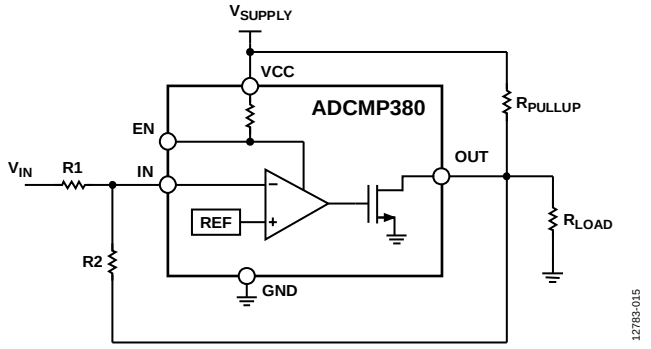


Figure 15. Configuration with Added Hysteresis

DEVICE OPTIONS

Table 6. Reference Voltage (V_{REF}) Options (T_A= −40°C to +85°C)

Model Number	Min	Typ	Max	Unit
ADCMP380-1	0.984	1	1.016	V
ADCMP380-2	0.489	0.5	0.511	V

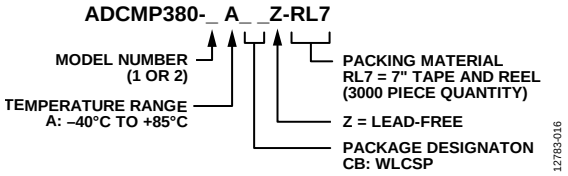


Figure 16. Ordering Code Structure

OUTLINE DIMENSIONS

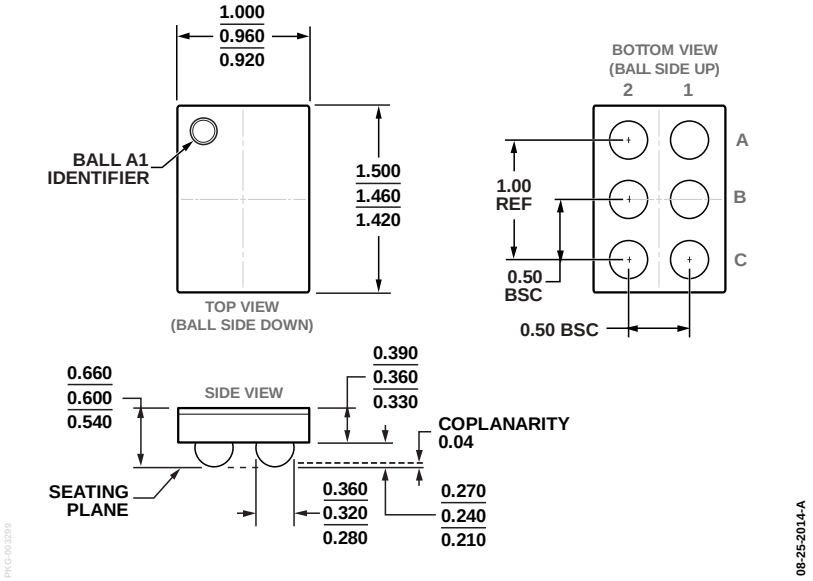


Figure 17. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADCMP380-1ACBZ-RL7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	CW
ADCMP380-2ACBZ-RL7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	LQZ
ADCMP380-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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