ADC16DX370EVM

User's Guide

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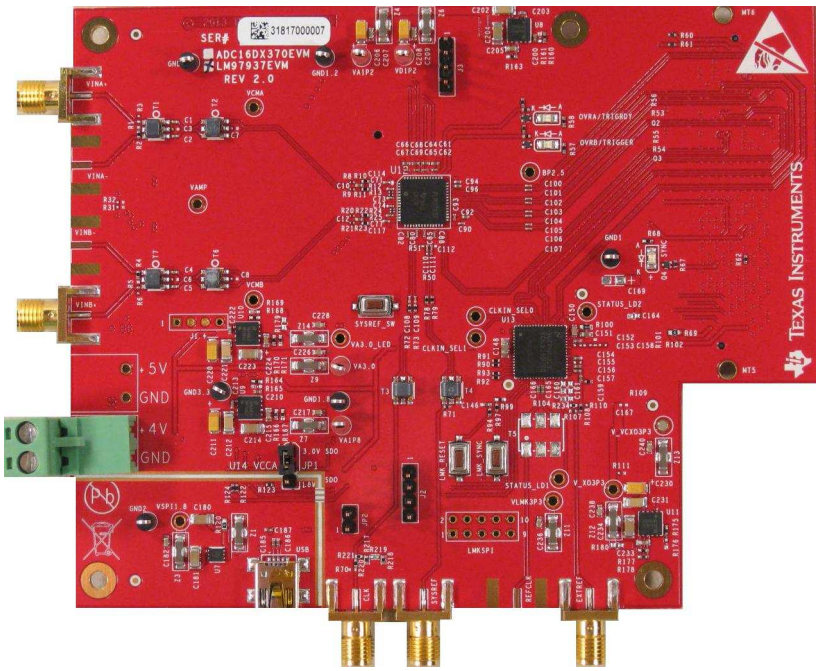
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ADC16DX370EVM User's Guide



1 Introduction

The ADC16DX370EVM is an evaluation board used to evaluate the ADC16DX370 analog-to-digital converter (ADC) from TI. The ADC16DX370 device is a dual-channel, 16-bit ADC capable of operating at sampling rates up to 370 Mega samples per second (MSPS). The ADC16DX370 device output data is transmitted over a standard JESD204B high-speed serial interface.

This evaluation board also includes the following important features:

- Transformer-coupled signal input network allowing a single-ended signal source from 5 MHz to 1 GHz
- LMK04828 system clock generator that generates FPGA reference clocks for the high-speed serial interface and may be used to generate the ADC sampling clock
- Transformer-coupled clock input network to test the ADC performance with a very low-noise clock source
- High-speed serial data output over a standard FMC interface connector
- Device register programming via USB connector and FTDI USB-to-SPI bus translator

The digital data from the ADC16DX370EVM board can be quickly and easily captured with the TSW14J56EVM data capture board. The TSW14J56EVM captures the high-speed serial data, decodes the data, stores the data in memory, then uploads it to a connected PC through a USB interface for analysis. The High Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

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With proper hardware selection in the HSDC Pro software, the TSW14J56 device is automatically configured to support a wide range of operating speeds of the ADC16DX370EVM, but it may not cover the full operating range of the ADC device. Serial data rates (and corresponding sampling rates) of 7.4 Gb/s (370 MSPS) down to 1.6 Gb/s (80 MSPS) are supported.

For the rest of this document, the ADC16DX370EVM evaluation board is referred to as EVM and the ADC16DX370 device is referred to as ADC device.

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2 Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the ADC device.

2.1 Evaluation Board Feature Identification Summary

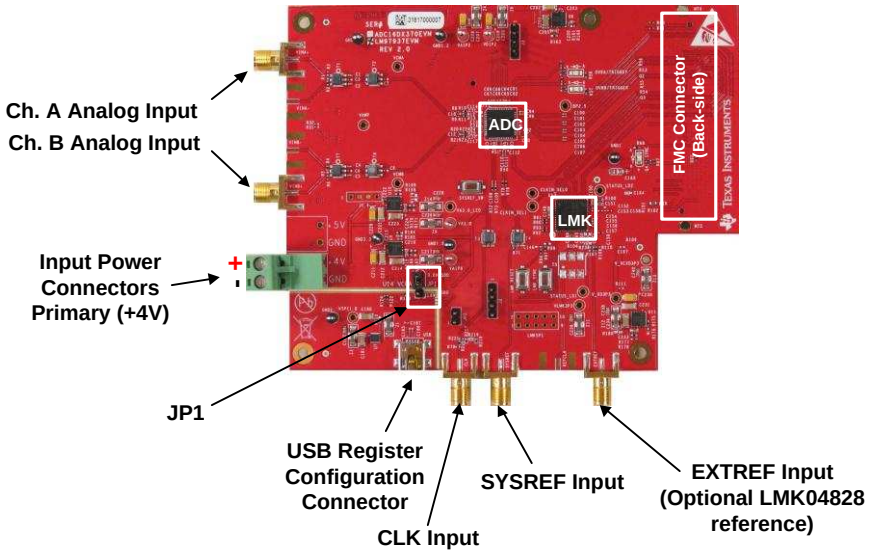


Figure 1. EVM Feature Locations

2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- Mini-USB cable

The following equipment is not included in the EVM evaluation kit, but is required for evaluation of this product.

- TSW14J56EVM data capture board plus +5-V power supply and mini-USB cable
- High Speed Data Converter Pro software
- PC computer running Windows XP, 7, or 8
- Two low-noise signal generators. TI recommends the following generators:
  - RF generator, > +17 dBm, < –40 dBc harmonics, < 500 fs jitter 20 kHz to 20 MHz, 10 MHz to 2 GHz frequency range
  - HP HP8644B
  - Rohde & Schwarz™ SMA100A
- Bandpass filter for clock input (370MHz or desired frequency). The following filters are recommended:
  - Bandpass filter, ≥ 60 dB harmonic attenuation, ≤ 5% bandwidth, > +18 dBm power, < 5 dB insertion loss
  - Trilithic™ 5VH-series tunable BPF
  - K&L Microwave™ BT-series tunable BPF
  - TTE KC6 or KC7-series fixed BPF
- Bandpass filter for analog input signal. Recommended filters similar to the clock path filter.
- 6-dB resistive attenuator, SMA, 50 Ω
- Signal-path and clock-path cables, SMA or BNC (or both SMA and BNC)
- +4 V, 2-A power supply and cable

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3 Setup Procedure

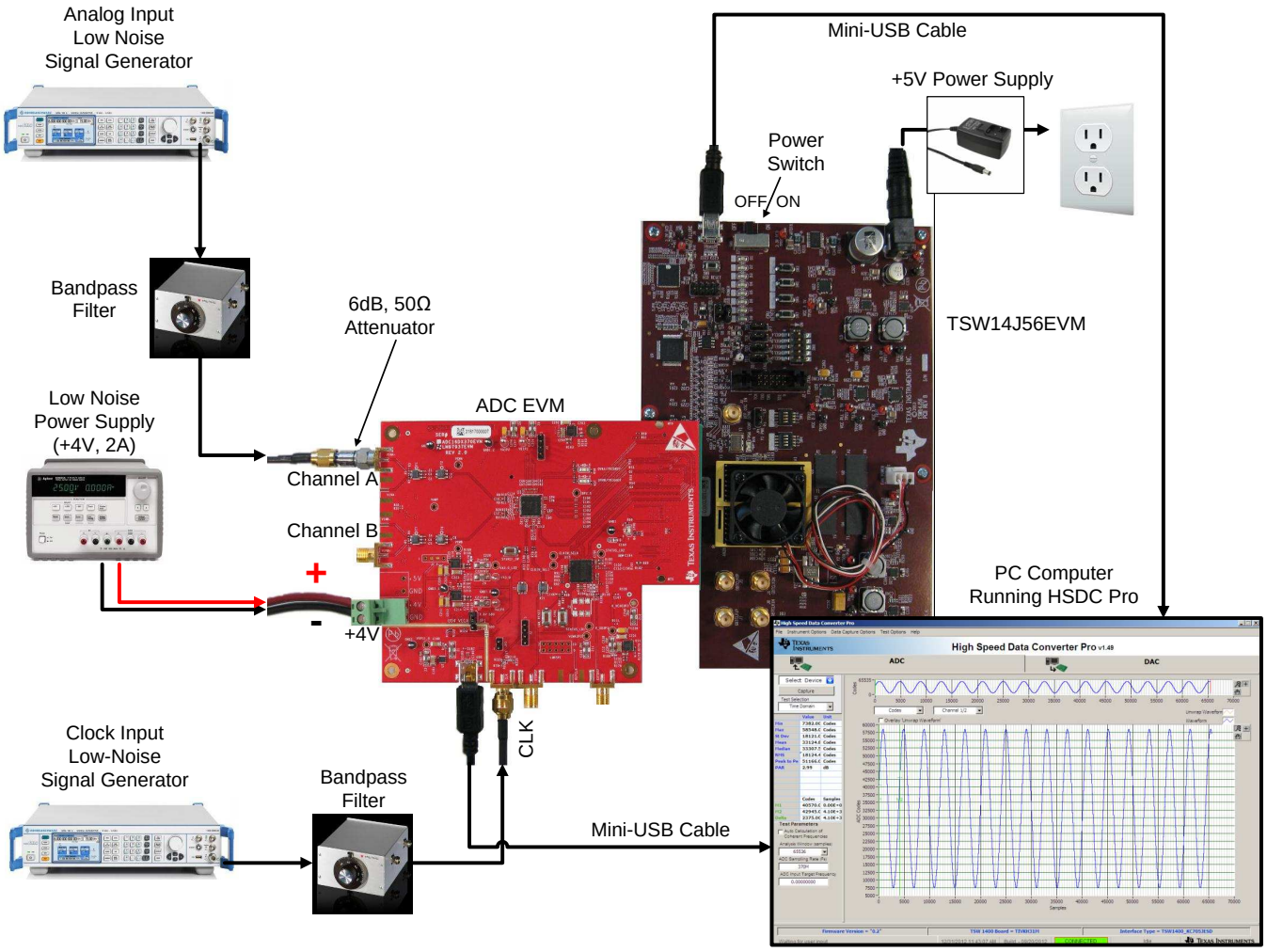


Figure 2. EVM Test Setup

NOTE: The HSDP software must be installed before connecting the TSW14J56EVM to the PC for the first time.

3.1 Install the High Speed Data Converter Pro (HSDP) Software

Download the most recent version of the HSDP software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

3.2 Install the Configuration GUI Software

1. Download the Configuration GUI software from the EVM product page at www.ti.com.
2. Extract files from the zip file.
3. Run “setup.exe” and follow the instructions.

3.3 Connect the EVM and TSW14J56EVM

With the power off, connect the EVM to the TSW14J56EVM via the FMC connector as shown in Figure 2. Check that the standoffs provide the proper height for robust connector connections.

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3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm that the power switch on the TSW14J56EVM is in the off position. Connect the +5-V power supply adapter to the TSW14J56EVM.
2. Confirm that the +4-V power supply for the EVM is turned off. Connect the +4-V power supply to the green power connector (closest to the USB connector).

CAUTION

Do not turn on the power to any board. Powering up the boards in the incorrect order could potentially cause damage to one of the boards.

3.5 Connect the Signal Generators to the EVM (RF Signal Off)

1. Connect a signal generator to the CLK input of the EVM through a bandpass filter. This must be a low-noise signal generator. TI recommends a Trilithic™ tunable bandpass filter to filter the signal coming from the generator. Configure the signal generator for 370 MHz. When using an RF signal generator, the power input to the CLK SMA connector should be +11 dBm (2.2 Vpp into 50 Ω) for best performance and must be at least +4 dBm to function. Therefore, the signal generator should be increased above +11 dB by an amount equal to any additional attenuation in the clock signal path, such as the insertion loss of the bandpass filter. For example, if the filter insertion loss is 2 dB, the signal generator should be set to +11 dBm + 2 dB = +13 dBm.
2. Connect a signal generator to the VINA+ input of the EVM through a bandpass filter and attenuator at the SMA connector. This must be a low-noise signal generator. TI recommends a Trilithic™ tunable bandpass filter to filter the signal from the generator. Configure the signal generator for 70 MHz, +0 dBm.
3. It is important to frequency lock the input signal generator to the clock signal generator using the 10-MHz reference. This is required to achieve coherent sampling of the input signal and is recommended, if possible. Frequency locking this signal generator is not required for non-coherent sampling.

NOTE: Do not yet turn on the RF output of any signal generator.

3.6 Turn the TSW14J56EVM Power on and Connect to the PC

1. Turn the power switch of the TSW14J56EVM on.
2. Connect a mini-USB cable from the PC to the TSW14J56EVM.
3. If this is the first time connecting the TSW14J56EVM to the PC, then follow the on-screen instructions to automatically install the device drivers. See the TSW14J56EVM User's Guide for more specific instructions.

3.7 Turn the EVM Power Supplies on and Connect to the PC

1. Turn the +4-V power supply on to power up the EVM.
2. Connect the EVM to the PC with the mini-USB cable.

3.8 Turn the Signal Generator RF Outputs on

Turn on the RF signal outputs of the signal generators connector to CLK and VINA-.

3.9 Open the HSDP Software and Load the FPGA Image to the TSW14J56EVM

1. Open the HSDP software.
2. Press OK to confirm the serial number of the TSW14J56EVM device.
3. Select the 'ADC16DX370_LMF_222' device from the ADC select drop-down in the top left corner and press 'Yes' to update the firmware.

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NOTE: If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See the Appendix A for more details.

4. Enter the ADC sampling rate (Fs) as 370M or the desired sampling rate. This number should be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.10 Program the LMK04828 Using the Configuration Tab on the HSDC Pro Software

1. Note that selecting the EVM in the ADC select drop-down menu made an additional tab appear in HSDC Pro. Select the tab in the HSDC Pro software and navigate to the 'Clock Dist' sub-tab.
2. Press the 'Configuration 1' button. Verify that pressing the button changes the state of the LEDs on the translation card, or that it changes the current draw from the +4-V power supply.

NOTE: The EVM configuration tabs in HSDC Pro may have a procedure that instructs the user to program the LMK04828 using a 'Configuration 1' button on a different tab. The Configuration 1' button on either tab performs the same function.

3.11 Calibrate the ADC Device on the EVM

1. With the FTDI SPI GUI open on the PC, navigate to the 'Intro' tab.
2. Press the calibrate button to calibrate the ADC.

NOTE: This calibrate button sets the ADC in power-down mode and then returns the ADC to normal operation which executes core calibration. Post-power-up calibration is only mandatory if the CLKDIV value is changed or if the sampling rate is changed.

3.12 Verify the TSW14J56EVM Switch Settings, Initialize the JESD204B Link (CPU_RESET), and Verify TSW14J56EVM Status LEDs

1. Observe the switches and jumpers on the TSW14J56EVM and verify that they are in the correct position. The required switch settings are shown in Table 4.
2. Press the CPU_RESET button (SW7) on the TSW14J56EVM. This button is used to reset the JESD204B receiver core in the receiving FPGA and should be pressed after power-up, after changing the test setup, or after changing particular device configuration registers.
3. Verify the status of the D1 to D8 LEDs on the TSW14J56EVM. See the Appendix A for more information regarding the status LEDs.

Table 1. Default State of LEDs on the TSW14J56EVM During Typical Operation

LED	Status
D1	Blinking
D2	On
D3	Blinking
D4	On
D5	On
D6	Off
D7	Off
D8	On
FPGA_DONE	On

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3.13 Capture Data Using the HSDP Software

1. Verify that ‘ADC16DX370_LMF_222’ is the selected device.
2. Enter the ‘ADC sampling rate (Fs)’ as the desired sampling rate. This value must be equal to the operating sampling rate of the device.
3. It is important to check the ‘Auto Calculate Coherent Frequencies’ checkbox. Enter the frequency of the analog input signal generator into the ‘ADC Input Target’ box and press Enter. Update the analog input signal generator to the calculated frequency.
4. Select the test to perform.
5. Select the data view.
6. Select the channel to view.
7. Press the capture button to capture new data.

Additional tips:

- Use the ‘Notch Frequency Bins’ from the 'Test Options' file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the ‘Capture Option’ dialog from the 'Data Capture Options' file menu to change the capture depth or to enable FFT averaging.
- For analyzing only a portion of the spectrum, use the ‘Single Tone’ test with the ‘Bandwidth Integration Markers’ from the ‘Test Options’ file menu. The ‘Channel Power’ test may also be useful.
- For analyzing only a subset of the captured data, set the ‘Analysis Window (samples)’ setting to a value less than the number total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.

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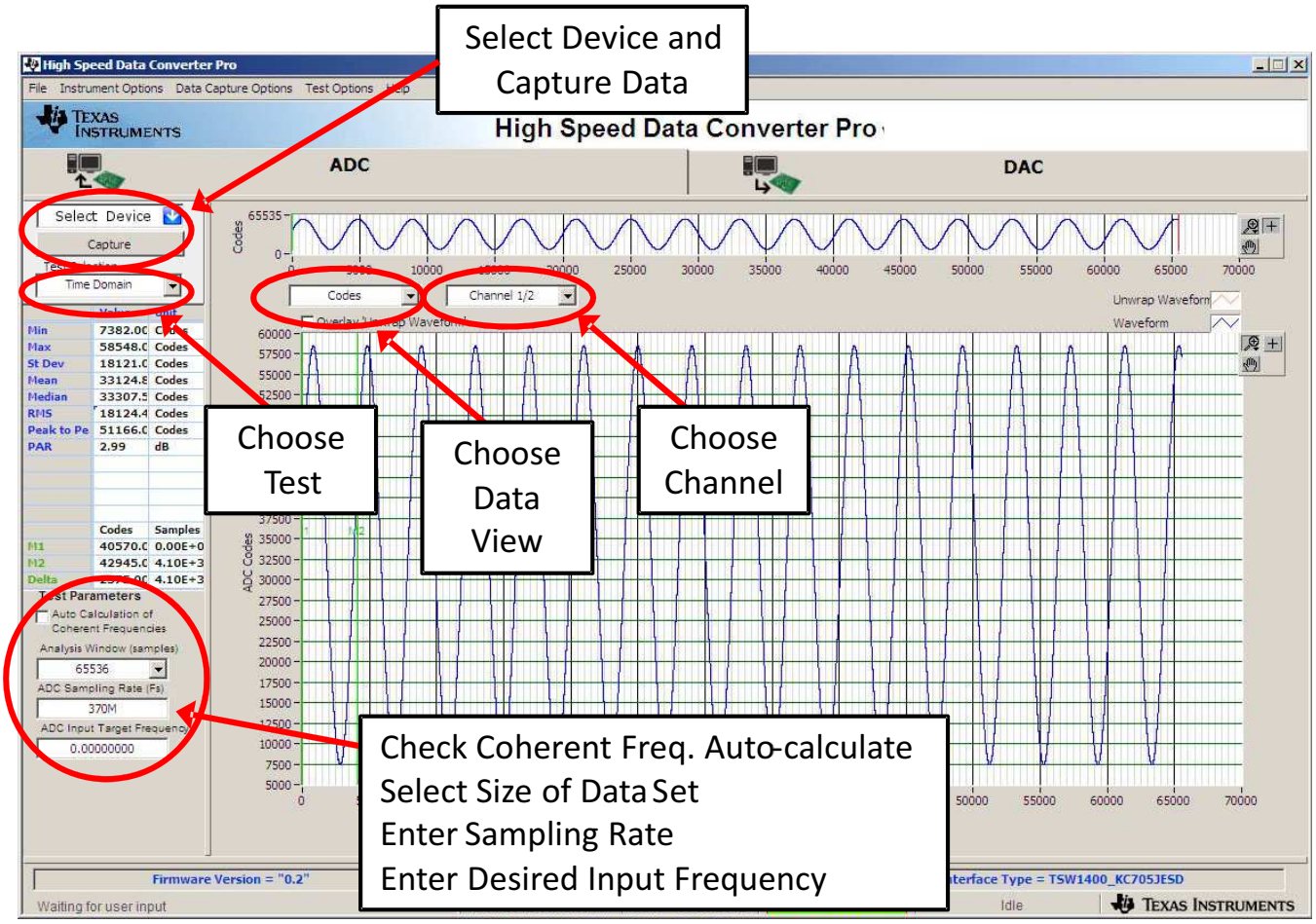


Figure 3. High Speed Data Converter Pro (HSDP) GUI

3.14 Re-Verify TSW14J56EVM Status LEDs

Verify the status of the D1 to D8 LEDs on the TSW14J56EVM. See the Appendix A for more information regarding the status LEDs.

NOTE: Note that D4 has changed to indicate that the JESD204B link is established.

Table 2. Default State of LEDs on the TSW14J56EVM during Typical Operation

LED	Status
D1	Blinking
D2	On
D3	Blinking
D4	Off
D5	On
D6	Off
D7	Off
D8	On
FPGA_DONE	On

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4 Device Configuration

The ADC device is programmable via the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

See the data sheet, SNVS990, for more information about the registers in the ADC device.

4.1 Supported JESD204B Device Features

The ADC device supports some configuration of the JESD204B interface. Due to limitations in the STW14J56EVM firmware, all JESD204B link features of the ADC device are not supported. Table 3 describes the supported and non-supported features.

Table 3. Supported and Non-Supported Features of the JESD204B Device

JESD204B Feature	Supported by ADC Device	Supported by TSW14J56EVM
Number of lanes per channel (L)	L = 1 or 2	L = 1 supported L= 2 supported with special instructions for configuring HSDC Pro software
Number of frames per multiframe (K)	K = 9 to 32	K = 32 supported Other K values not supported at this time
Scrambling	Scrambling supported	Scrambling not supported at this time
Test patterns	PRBS7, PRBS15, PRBS23 supported D21.5, K28.5, ILA, ramp patterns supported	ILA and RAMP supported PRBS7, PRBS15, PRBS23, D21.5, K28.5 not supported at this time
Speed	Lane rates from 7.4 down to 1 Gb/s	Lane rates from 7.4 Gb/s (Fs = 370 MSPS) down to 1.6 Gb/s (Fs = 80 MSPS) The Fs parameter must be properly set in HSDC Pro

4.2 Using the Device Configuration GUI

The Device Configuration GUI must be installed separately from the HSDC Pro installation, but the Configuration GUI automatically integrates into the HSDC Pro software. If HSDC Pro is opened the device is selected corresponding to a Configuration GUI that is already installed, then the Configuration GUI automatically loads as a selectable tab. If the Configuration GUI is opened before HSDC Pro, it opens as a standalone GUI.

Figure 4 and Figure 5 show the GUI open to the INTRO tab and ADC CORE Tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has two configurable devices, namely the ADC16DX370 and LMK04828. The register map for each device is provided in the data sheets SNVS990 and SNAS605, respectively.

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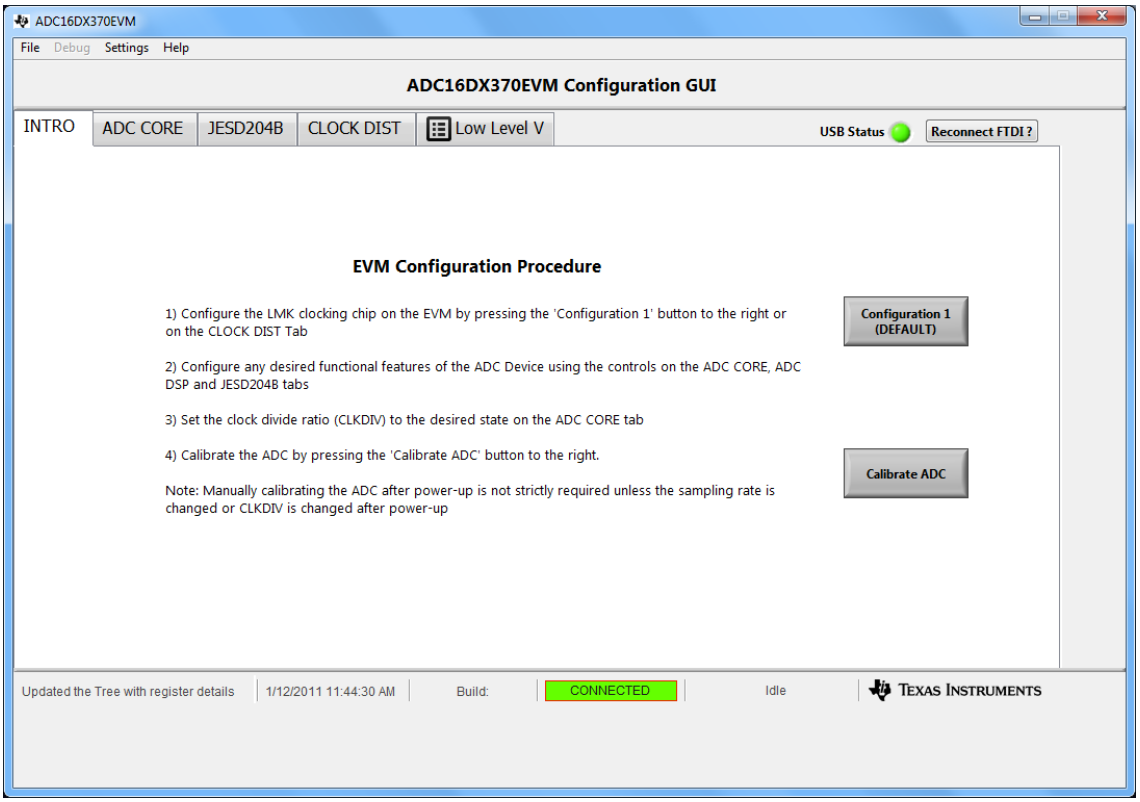


Figure 4. Configuration GUI Intro Tab

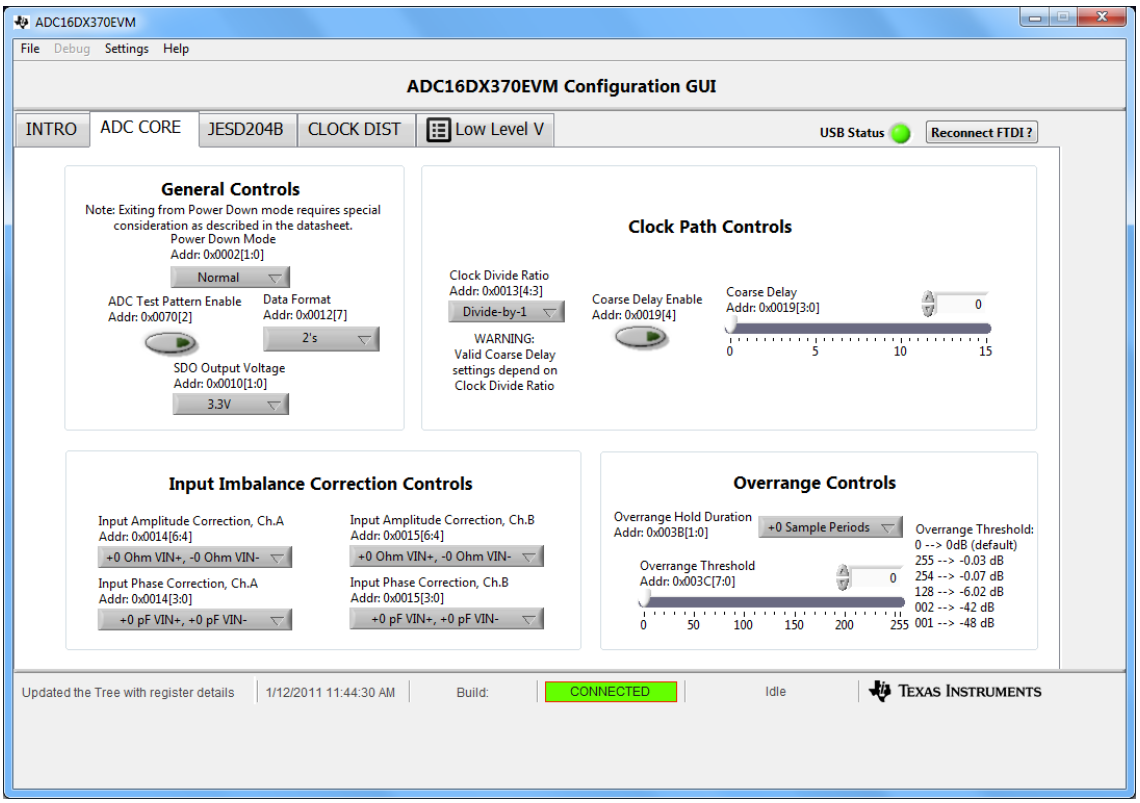


Figure 5. Configuration GUI ADC Core Tab

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4.3 Tab Organization

Control of the ADC device features is available in the ADC Core, ADC DSP, and JESD204B tabs. Simplified configuration controls for the LMK04828 are available in the Clock Dist tab. All features of the ADC Device are configurable using this GUI, although the controls for the LMK04828 are simplified or restricted to avoid unnecessary complexity.

4.4 Low-Level Control

The Low-Level tab, shown in Figure 6, allows configuration of the devices at the bit-field level. At any time, the following controls may be used to configure or read from the device.

Table 4. Low-Level Controls

Control	Description
Register Map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers • Clicking on a register field allows individual bit manipulation in the Register Data Cluster • The value column shows the value of the register at the time the GUI was last updated • The LR column shows the value of the register at the time the register was last read
Write Register button	Write to the register highlighted in the Register Map Summary with the value in the Write Data field
Write All button	Update all registers shown in the Register Map Summary with the values shown in the Register Map Summary Can be used to re-synchronize the GUI with the state of the hardware
Read Register button	Read from the register highlighted in the Register Map Summary and display the results in the Read Data field
Read All button	Read from all register in the Register Map Summary and display current state of hardware
Load Config button	Load a configuration file from disk and execute the commands in the file
Save Config button	Save a configuration file to disk that contains the current state of configuration
Register Data Cluster	Manipulate individual accessible bits of the register highlighted in the Register Map Summary
Individual Register Cluster with Read or Write Register buttons	Perform a generic read or write command to the device shown in the ‘Block’ drop-down box using the address and write data information

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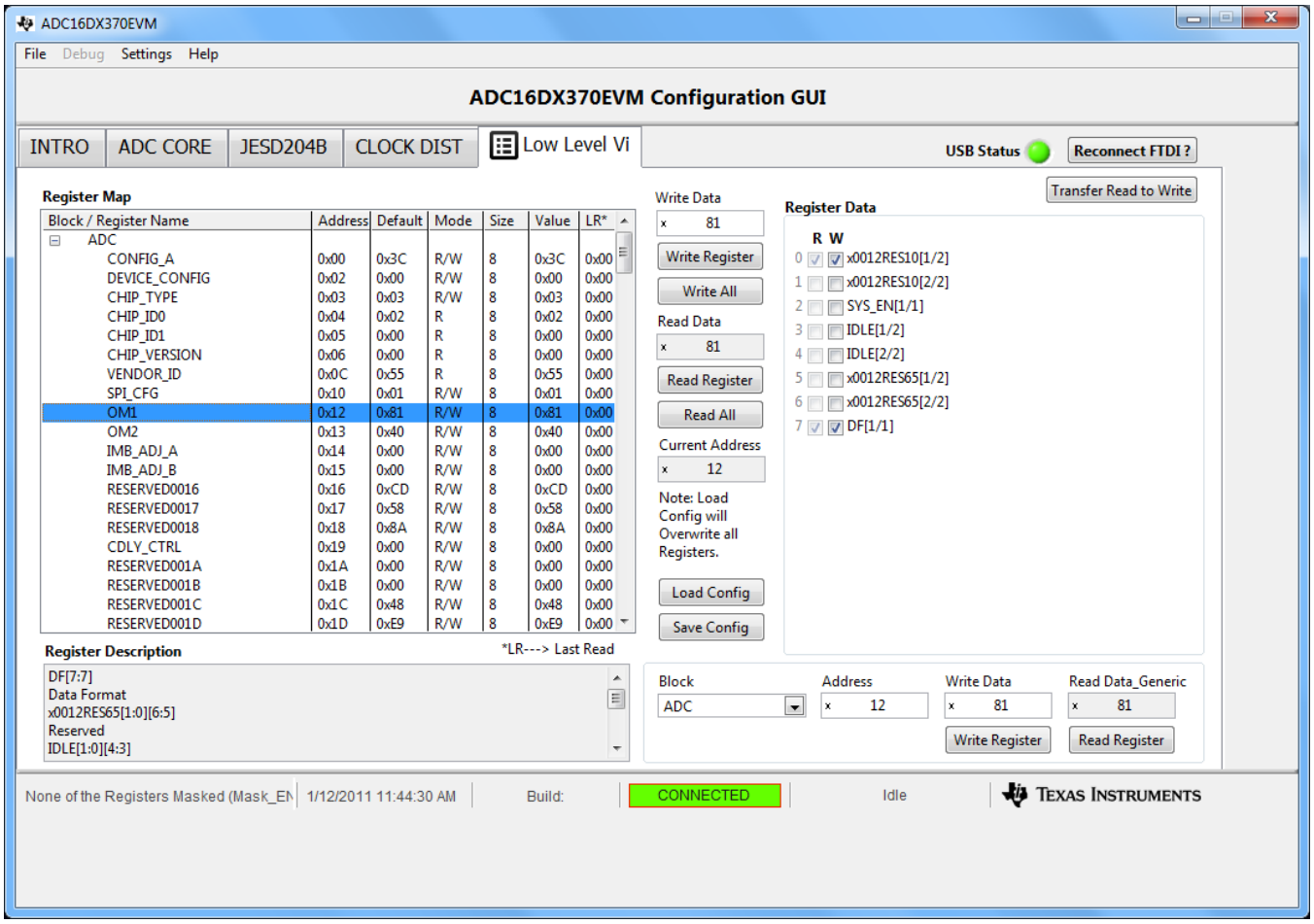


Figure 6. Low-Level Register Control Tab

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5 Evaluation Troubleshooting

Table 5. Troubleshooting

Issue	Troubleshoot
General problems	• Verify the test setup shown in Figure 2, and repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J56EVM. Verify that the power switches are in the on position. • Check signal and clock connections to EVM. • Visually check the top and bottom layers of the board to verify that nothing looks discolored or damaged. • Check the connection of all boards together. • Try pressing the CPU_RESET button on the TSW14J56EVM. • Try power-cycling the external power supply to the EVM, and reprogram the LMK and ADC devices.
TSW14J56 LEDs are not correct	• Verify the settings of the configuration switches on the TSW14J56EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the ADC device internal registers are configured properly. • If LEDs are not blinking, reprogram the LMK device. • Try pressing the CPU_RESET button on the TSW14J56EVM. • Try capturing data in HSDC Pro to force an LED status update
Configuration GUI is not working properly	• Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a 'USB serial device' is recognized when the EVM is connected to the PC. • Verify that the green 'USB Status' LED light in the top right corner of the GUI is lit. If it is not lit, press 'Reconnect FTDI' button. • Try restarting the configuration GUI.
Configuration GUI is not able to connect to the EVM	• Use the free FT_PROG software from FTDI chip and verify that the on-board FTDI chip is programmed with the product description 'ADC16DX370EVM'.
HSDP software is not capturing good data or analysis results are incorrect.	• Verify that the TSW14J56EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDP software. • Check that the proper ADC device is selected. In default conditions, 'ADC16DX370_LMF_222' should be selected. • Check that the analysis parameters are properly configured.
HSDP software gives a time-out error when capturing data	• Try to reprogram the LMK device and reset the JESD204 link. • Verify that the ADC sampling rate is correctly set in the HSDP software.
Sub-optimal measured performance	• Try pressing the 'Calibrate ADC' button on the Intro tab of the configuration GUI to recalibrate the ADC. • Check that the spectral analysis parameters are properly configured. • Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.

6 References

- ADC16DX370 data sheet, TI literature number SNVS990
- TSW14J56EVM User's Guide, TI literature number SLWU086
- High Speed Data Converter Pro Software User's Guide, also available in the help menu of the software
- LMK04828 data sheet
- FTD245 Driver Installation Manual

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Appendix A

A.1 TSW14J56EVM LED Bank and Switch Configuration

The LEDs on the TSW14J56EVM indicate the status of the capture board and the status of the JESD204B link. The LEDs have the following meaning:

Table 6. Meaning of LEDs on the TSW14J56EVM

Column Head 1	Column Head 2
FPGA_DONE	**FPGA Programming** On: FPGA has been programmed Off: FPGA has not been programmed, or is being programmed
D1	**TX SYNC~** On: Synchronization being requested (code group synchronization phase of link initialization) Off: Synchronization not request (code group synchronization complete) Note: The status of this LED is only valid after attempting a data capture in HSDC Pro
D2	**TX Device Clock** Blinking: Device clock is being received from the LMK device on the EVM Not blinking: Device clock not received
D3	**SYNC~** On: Synchronization being requested (code group synchronization phase of link initialization) Off: Synchronization not request (code group synchronization complete) The status of this LED is only valid after attempting a data capture in HSDC Pro
D4	**RX Device Clock** Blinking: Device clock is being received from the LMK device on the EVM Not blinking: Device clock not received.
D5	No Function
D6	**DDR3 Memory Calibration Done** On: Calibration not done Off: Calibration done, typical operation
D7	**DDR3 Memory Calibration Success** On: Calibration not successful Off: Calibration successful, typical operation
D8	**DDR3 Memory Calibration Fail** On: Calibration not failed, typical operation Off: Calibration failed

Table 7. Required State of Switches on the TSW14J56EVM

Switch	Status
SW1[1]	Off
SW1[2]	Off
SW1[3]	Off
SW1[4]	Off
SW4[1]	Off
SW4[2]	Off
SW4[3]	Off
SW4[4]	Off
SW8, MSEL0-MSEL4	All on
TDI, TDO, TCK, TMS jumpers	All should be shorting pins 1 to 2
JP1 (Y1 PWR)	Short pins 1 to 2 (HI setting)
J8 (USB PWR)	Short pins 1 to 2
JP9 (U8 ENB)	Short pins 2 to 3

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A.2 HSDC Pro Settings for Optional ADC Device Configuration

A.2.1 Changing the Number of Serial Output Lanes (L)

The ADC device outputs data on two lanes (one lane per channel) by default, but the device may also be configured to output on four total lanes. This option is selected using the L parameter on the JESD204B tab in the Configuration GUI. In this case, 'ADC16DX370EVM_421' must be selected as the device in HSDC Pro.

A.2.2 Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitter (ADC device) is configured using the K parameter on the JESD204B tab in the Configuration GUI. This parameter must be matched by the receiving device, but configuration of the K parameter of the receiver is not supported at this time.

A.3 Exercising the SYSREF Input of the ADC

The SYSREF input is used to align the phase of the internal local multi-frame clock (LMFC) of the ADC, according to the JESD204B interface specification, but it is not required to establish a link and evaluate the analog performance of the ADC with this EVM. Upon power-up, the ADC assumes a default alignment for its LMFC and proceeds to synchronize with the receiving device without requiring a SYSREF input event.

A SYSREF signal may be applied to the ADC via the SYSREF SMA connector on the EVM to validate the response of the ADC to a SYSREF event. The SYSREF signal path is AC coupled; therefore only periodic signals with frequencies > 5 MHz are supported.

TI does not recommend use of the SYSREF SMA input of the EVM to ensure deterministic latency across the serial link, due to difficulties of controlling timing requirements. The on-board LMK04828 may be used in an optional configuration to clock both the ADC and receiving device to achieve deterministic latency.

A.4 Customizing the EVM for Optional Clocking Support

By default, the LMK04828 is configured as a clock distributer and divider and only provides clock signals to the receiving FPGA device. The EVM is configured to require an ADC device clock from an external signal generator source through the CLK SMA connector. These default configurations are intentional as they allow the most flexibility for ADC sampling rates and they allow the highest ADC performance possible.

The LMK04828 may be reconfigured to exercise more features, but this EVM is not intended to be a full evaluation platform for the LMK04828. A full evaluation platform can be found on the LMK04828 product page.

A.4.1 LMK04828 Configuration Options

Configuring the LMK04828 is possible in a couple different ways. TI recommends to use the 'Configuration 3' button on the LMK tab of the Configuration GUI. By pressing this button, a text file containing register values is accessed and the contents are written to the device registers. The text file is stored in the Configuration GUI installation directory in the '\Configuration Files' folder and is called 'LMK04828_config3.cfg'. The register values in this file may be edited manually. The LMK04828 data sheet and the CodeLoader 4 software may aid the design and editing process.

A second method for configuring the LMK04828 is to populate the programming header 'LMKSPI' with associated passive components to enable communication over the header and disable access of the SPI bus via the USB-to-SPI FTDI chip by placing a jumper on the JP2 header. Once the EVM is reconfigured to support this option, the CodeLoader 4 software and associated programming cable may be used to directly configure the LMK04828. Refer to the LMK04828 evaluation platform for proper configuration of the LMKSPI header.

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A.4.2 Configuring the ADC Device to Use a Device Clock and SYSREF from the LMK04828

The EVM may alternatively be reconfigured to route a device clock and SYSREF clock from the LMK04828 to the ADC device. This configuration represents a more realistic system configuration, but the data converter noise performance is affected by the noise of the clock signal from the LMK device.

To provide a device clock and SYSREF from the LMK04828 to the ADC device, the following EVM changes must be made:

- Remove R72, R73, R78, and R79 and place 0-Ω resistors on R74, R75, R80, and R81.
- Configure the LMK04828 to output an LVPECL device clock from its DCLKout2 port and an LVPECL SYSREF signal from its SDCLKout3 port.

A.4.3 Providing an Alternate LMK04828 Reference Clock

In the EVM default configuration, the CLK input signal is split to go to the ADC and LMK04828 to act as a reference clock. If deviation from the default configuration is desired, providing an alternate reference clock for the LMK04828 may be required. Possible options for providing the reference clock include:

- Using an external signal generator to provide the reference via the EXTREF SMA connector. If a separate signal generator is also used to provide the ADC device clock, these two generators must be frequency locked together.
- Placing a crystal oscillator module on Y1, Y2, or Y3. Additional configuration is required to provide power to the module and connect to the signal to the appropriate LMK04828 clock input port.

Revision History

Changes from Original (February 2014) to A Revision **Page**

- Changed 'ADC16DX370EVM_222' to 'ADC16DX370_LMF_222' in the *Open the HSDP Software and Load the FPGA Image to the TSW14J56EVM* section. 8
- Changed 'ADC16DX370EVM_222' to 'ADC16DX370_LMF_222' in the *Capture Data Using the HSDP Software* section. 10
- Changed 'ADC16DX370EVM_222' to 'ADC16DX370_LMF_222' in the *Evaluation Troubleshooting* section. 16

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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