



ADC128S102 8-Channel, 500-ksps to 1-Msps, 12-Bit A/D Converter

1 Features

- Eight Input Channels
- Variable Power Management
- Independent Analog and Digital Supplies
- SPI/QSPI™/MICROWIRE™/DSP Compatible
- Packaged in 16-Lead TSSOP
- Key Specifications
 - Conversion Rate 500 kps to 1 MSPS
 - DNL ($V_A = V_D = 5.0\text{ V}$) $+1.5 / -0.9$
 - LSB (maximum) INL ($V_A = V_D = 5.0\text{ V}$) ± 1.2 LSB (maximum)
 - Power Consumption
 - 3V Supply 2.3 mW (typical)
 - 5V Supply 10.7 mW (typical)

2 Applications

- Automotive Navigation
- Portable Systems
- Medical Instruments
- Mobile Communications
- Instrumentation and Control Systems

3 Description

The ADC128S102 is a low-power, eight-channel CMOS 12-bit analog-to-digital converter specified for conversion throughput rates of 500 kps to 1 MSPS. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept up to eight input signals at inputs IN0 through IN7.

The output serial data is straight binary and is compatible with several standards, such as SPI, QSPI, MICROWIRE, and many common DSP serial interfaces.

The ADC128S102 may be operated with independent analog and digital supplies. The analog supply (V_A) can range from +2.7 V to +5.25 V, and the digital supply (V_D) can range from +2.7 V to V_A . Normal power consumption using a +3-V or +5-V supply is 2.3 mW and 10.7 mW, respectively. The power-down feature reduces the power consumption to 0.06 μW using a +3-V supply and 0.25 μW using a +5-V supply.

The ADC128S102 is packaged in a 16-lead TSSOP package. Operation over the extended industrial temperature range of -40°C to $+105^\circ\text{C}$ is ensured.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC128S102	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

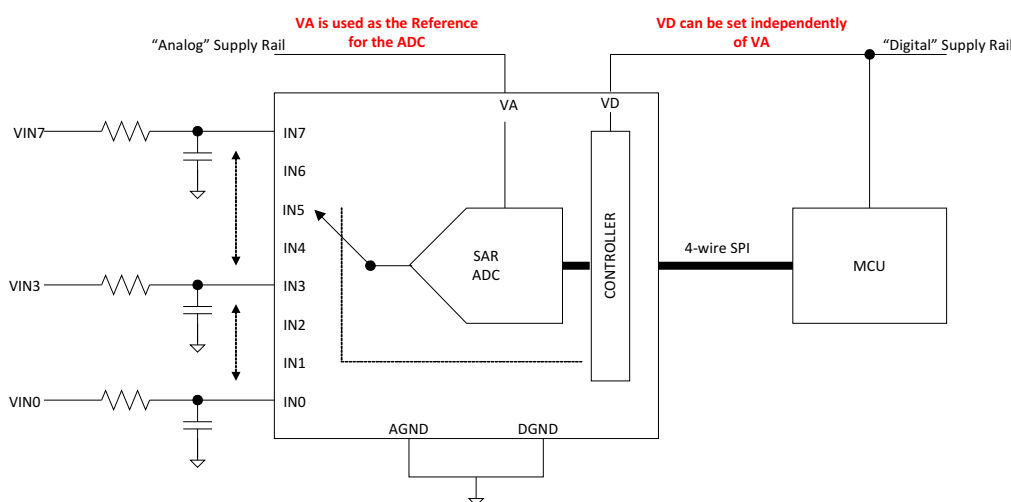


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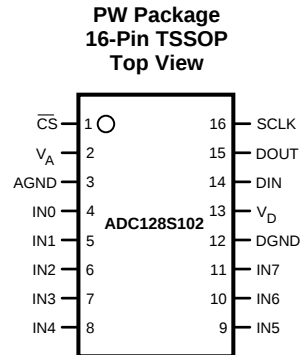
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2013) to Revision G	Page
Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

Changes from Revision D (March 2013) to Revision E	Page
Changed layout of National Data Sheet to TI format	20

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
3	AGND	Supply	The ground return for the analog supply and signals.
1	CS	IN	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
12	DGND	Supply	The ground return for the digital supply and signals.
14	DIN	IN	Digital data input. The ADC128S102's Control Register is loaded through this pin on rising edges of the SCLK pin.
15	DOUT	OUT	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
4 - 11	IN0 to IN7	IN	Analog inputs. These signals can range from 0 V to V_{REF} .
16	SCLK	IN	Digital clock input. The ensured performance range of frequencies for this input is 8 MHz to 16 MHz. This clock directly controls the conversion and readout processes.
2	V_A	Supply	Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet +2.7-V to +5.25-V source and bypassed to GND with 1- μ F and 0.1- μ F monolithic ceramic capacitors located within 1 cm of the power pin.
13	V_D	Supply	Positive digital supply pin. This pin should be connected to a +2.7 V to V_A supply, and bypassed to GND with a 0.1- μ F monolithic ceramic capacitor located within 1 cm of the power pin.

6 Specifications

6.1 Absolute Maximum Ratings

 See ⁽¹⁾⁽²⁾.

	MIN	MAX	UNIT
Analog Supply Voltage V_A	-0.3	6.5	V
Digital Supply Voltage V_D	-0.3	$V_A + 0.3$, max 6.5	V
Voltage on Any Pin to GND	-0.3	$V_A + 0.3$	V
Input Current at Any Pin ⁽³⁾	-10	10	mA
Package Input Current ⁽³⁾	-20	20	mA
Power Dissipation at $T_A = 25^\circ\text{C}$		See ⁽⁴⁾	
Junction Temperature		150	$^\circ\text{C}$
Storage temperature, T_{stg}	-65	150	$^\circ\text{C}$
For soldering specifications: see product folder at www.ti.com and SNOA549			

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) When the input voltage at any pin exceeds the power supplies (that is, $V_{\text{IN}} < \text{AGND}$ or $V_{\text{IN}} > V_A$ or V_D), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
- (4) The absolute maximum junction temperature (T_{Jmax}) for this device is 150°C . The maximum allowable power dissipation is dictated by T_{Jmax} , the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{\text{DMAX}} = (T_{\text{Jmax}} - T_A)/\theta_{\text{JA}}$. In the 16-pin TSSOP, θ_{JA} is 96°C/W , so $P_{\text{DMAX}} = 1,200$ mW at 25°C and 625 mW at the maximum operating ambient temperature of 105°C . Note that the power consumption of this device under normal operation is a maximum of 12 mW. The values for maximum power dissipation listed above will be reached only when the ADC128S102 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

6.2 ESD Ratings

		VALUE	UNIT
$V_{\text{(ESD)}}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2500	V
	Machine model (MM)	± 250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Operating Temperature, T_A	-40	105	$^\circ\text{C}$
V_A Supply Voltage	2.7	5.25	V
V_D Supply Voltage	2.7	V_A	V
Digital Input Voltage	0	V_A	V
Analog Input Voltage	0	V_A	V
Clock Frequency	8	16	MHz

- (1) All voltages are measured with respect to GND = 0V, unless otherwise specified.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ADC128S102	UNIT
		PW	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	110	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	42	
R _{θJB}	Junction-to-board thermal resistance	56	
ψ _{JT}	Junction-to-top characterization parameter	5	
ψ _{JB}	Junction-to-board characterization parameter	55	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

The following specifications apply for T_A = 25°C, AGND = DGND = 0 V, f_{SCLK} = 8 MHz to 16 MHz, f_{SAMPLE} = 500 kpsps to 1 MSPS, C_L = 50pF, unless otherwise noted. MIN and MAX limits apply for T_A = T_{MIN} to T_{MAX}.⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX ⁽²⁾	UNIT
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				12	Bits
INL	Integral Non-Linearity (End Point Method)	V _A = V _D = +3.0V	–1	±0.4	1	LSB
		V _A = V _D = +5.0V	–1.2	±0.5	1.2	LSB
DNL	Differential Non-Linearity	V _A = V _D = +3.0V		+0.4	0.9	LSB
			–0.7	–0.2		LSB
		V _A = V _D = +5.0V		+0.7	1.5	LSB
			–0.9	–0.4		LSB
V _{OFF}	Offset Error	V _A = V _D = +3.0V	–2.3	+0.8	2.3	LSB
		V _A = V _D = +5.0V	–2.3	+1.1	2.3	LSB
OEM	Offset Error Match	V _A = V _D = +3.0V	–1.5	±0.1	1.5	LSB
		V _A = V _D = +5.0V	–1.5	±0.3	1.5	LSB
FSE	Full Scale Error	V _A = V _D = +3.0V	–2.0	+0.8	2.0	LSB
		V _A = V _D = +5.0V	–2.0	+0.3	2.0	LSB
FSEM	Full Scale Error Match	V _A = V _D = +3.0V	–1.5	±0.1	1.5	LSB
		V _A = V _D = +5.0V	–1.5	±0.3	1.5	LSB
DYNAMIC CONVERTER CHARACTERISTICS						
FPBW	Full Power Bandwidth (–3dB)	V _A = V _D = +3.0V		8		MHz
		V _A = V _D = +5.0V		11		MHz
SINAD	Signal-to-Noise Plus Distortion Ratio	V _A = V _D = +3.0V, f _{IN} = 40.2 kHz, –0.02 dBFS	70	73		dB
		V _A = V _D = +5.0V, f _{IN} = 40.2 kHz, –0.02 dBFS	70	73		dB
SNR	Signal-to-Noise Ratio	V _A = V _D = +3.0V, f _{IN} = 40.2 kHz, –0.02 dBFS	70.8	73		dB
		V _A = V _D = +5.0V, f _{IN} = 40.2 kHz, –0.02 dBFS	70.8	73		dB
THD	Total Harmonic Distortion	V _A = V _D = +3.0V, f _{IN} = 40.2 kHz, –0.02 dBFS		–88	–74	dB
		V _A = V _D = +5.0V, f _{IN} = 40.2 kHz, –0.02 dBFS		–90	–74	dB

(1) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.

(2) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

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Electrical Characteristics (continued)

The following specifications apply for $T_A = 25^\circ\text{C}$, $\text{AGND} = \text{DGND} = 0\text{ V}$, $f_{\text{SCLK}} = 8\text{ MHz to } 16\text{ MHz}$, $f_{\text{SAMPLE}} = 500\text{ kpsps to } 1\text{ MSPS}$, $C_L = 50\text{ pF}$, unless otherwise noted. MIN and MAX limits apply for $T_A = T_{\text{MIN}}$ to T_{MAX} .⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX ⁽²⁾	UNIT
SFDR	Spurious-Free Dynamic Range	V _A = V _D = +3.0V, f _{IN} = 40.2 kHz, −0.02 dBFS	75	91		dB
		V _A = V _D = +5.0V, f _{IN} = 40.2 kHz, −0.02 dBFS	75	92		dB
ENOB	Effective Number of Bits	V _A = V _D = +3.0V, f _{IN} = 40.2 kHz	11.3	11.8		Bits
		V _A = V _D = +5.0V, f _{IN} = 40.2 kHz, −0.02 dBFS	11.3	11.8		Bits
ISO	Channel-to-Channel Isolation	V _A = V _D = +3.0V, f _{IN} = 20 kHz		82		dB
		V _A = V _D = +5.0V, f _{IN} = 20 kHz, −0.02 dBFS		84		dB
IMD	Intermodulation Distortion, Second Order Terms	V _A = V _D = +3.0V, f _a = 19.5 kHz, f _b = 20.5 kHz		−89		dB
		V _A = V _D = +5.0V, f _a = 19.5 kHz, f _b = 20.5 kHz		−91		dB
	Intermodulation Distortion, Third Order Terms	V _A = V _D = +3.0V, f _a = 19.5 kHz, f _b = 20.5 kHz		−88		dB
		V _A = V _D = +5.0V, f _a = 19.5 kHz, f _b = 20.5 kHz		−88		dB
ANALOG INPUT CHARACTERISTICS						
V _{IN}	Input Range		0 to V _A			V
I _{DCL}	DC Leakage Current		−1		1	μA
C _{INA}	Input Capacitance	Track Mode		33		pF
		Hold Mode		3		pF
DIGITAL INPUT CHARACTERISTICS						
V _{IH}	Input High Voltage	V _A = V _D = +2.7V to +3.6V	2.1			V
		V _A = V _D = +4.75V to +5.25V	2.4			V
V _{IL}	Input Low Voltage	V _A = V _D = +2.7V to +5.25V			0.8	V
I _{IN}	Input Current	V _{IN} = 0V or V _D	−1	±0.01	1	μA
C _{IND}	Digital Input Capacitance			2	4	pF
DIGITAL OUTPUT CHARACTERISTICS						
V _{OH}	Output High Voltage	I _{SOURCE} = 200 μA, V _A = V _D = +2.7V to +5.25V	V _D − 0.5			V
V _{OL}	Output Low Voltage	I _{SINK} = 200 μA to 1.0 mA, V _A = V _D = +2.7V to +5.25V			0.4	V
I _{OZH} , I _{OZL}	Hi-Impedance Output Leakage Current	V _A = V _D = +2.7V to +5.25V	−1		1	μA
C _{OUT}	Hi-Impedance Output Capacitance ⁽¹⁾			2	4	pF
Output Coding			Straight (Natural) Binary			
POWER SUPPLY CHARACTERISTICS (C _L = 10 pF)						
V _A , V _D	Analog and Digital Supply Voltages	V _A ≥ V _D	2.7		5.25	V

Electrical Characteristics (continued)

The following specifications apply for $T_A = 25^\circ\text{C}$, $AGND = DGND = 0\text{ V}$, $f_{\text{SCLK}} = 8\text{ MHz to }16\text{ MHz}$, $f_{\text{SAMPLE}} = 500\text{ kpsps to }1\text{ MSPS}$, $C_L = 50\text{ pF}$, unless otherwise noted. MIN and MAX limits apply for $T_A = T_{\text{MIN}}$ to T_{MAX} .⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX ⁽²⁾	UNIT
$I_A + I_D$	Total Supply Current Normal Mode ($\overline{\text{CS}}$ low)	$V_A = V_D = +2.7\text{ V to }+3.6\text{ V}$, $f_{\text{SAMPLE}} = 1\text{ MSPS}$, $f_{\text{IN}} = 40\text{ kHz}$		0.76	1.5	mA
		$V_A = V_D = +4.75\text{ V to }+5.25\text{ V}$, $f_{\text{SAMPLE}} = 1\text{ MSPS}$, $f_{\text{IN}} = 40\text{ kHz}$		2.13	3.1	mA
	Total Supply Current Shutdown Mode ($\overline{\text{CS}}$ high)	$V_A = V_D = +2.7\text{ V to }+3.6\text{ V}$, $f_{\text{SCLK}} = 0\text{ kpsps}$		20		nA
		$V_A = V_D = +4.75\text{ V to }+5.25\text{ V}$, $f_{\text{SCLK}} = 0\text{ kpsps}$		50		nA
P_C	Power Consumption Normal Mode ($\overline{\text{CS}}$ low)	$V_A = V_D = +3.0\text{ V}$, $f_{\text{SAMPLE}} = 1\text{ MSPS}$, $f_{\text{IN}} = 40\text{ kHz}$		2.3	4.5	mW
		$V_A = V_D = +5.0\text{ V}$, $f_{\text{SAMPLE}} = 1\text{ MSPS}$, $f_{\text{IN}} = 40\text{ kHz}$		10.7	15.5	mW
	Power Consumption Shutdown Mode ($\overline{\text{CS}}$ high)	$V_A = V_D = +3.0\text{ V}$, $f_{\text{SCLK}} = 0\text{ kpsps}$		0.06		μW
		$V_A = V_D = +5.0\text{ V}$, $f_{\text{SCLK}} = 0\text{ kpsps}$		0.25		μW

AC ELECTRICAL CHARACTERISTICS

f_{SCLKMIN}	Minimum Clock Frequency	$V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$	8	0.8		MHz
f_{SCLK}	Maximum Clock Frequency	$V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$			16	MHz
f_s	Sample Rate Continuous Mode	$V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$	500	50		kpsps
					1	MSPS
t_{CONVERT}	Conversion (Hold) Time	$V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$			13	SCLK cycles
DC	SCLK Duty Cycle	$V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$	40%	30		
				70	60%	
t_{ACQ}	Acquisition (Track) Time	$V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$			3	SCLK cycles
	Throughput Time	Acquisition Time + Conversion Time $V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$			16	SCLK cycles
t_{AD}	Aperture Delay	$V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$		4		ns

6.6 Timing Specifications

The following specifications apply for $T_A = 25^\circ\text{C}$, $V_A = V_D = +2.7\text{ V to }+5.25\text{ V}$, $AGND = DGND = 0\text{ V}$, $f_{\text{SCLK}} = 8\text{ MHz to }16\text{ MHz}$, $f_{\text{SAMPLE}} = 500\text{ kpsps to }1\text{ MSPS}$, and $C_L = 50\text{ pF}$. MIN and MAX apply for $T_A = T_{\text{MIN}}$ to T_{MAX} .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX ⁽¹⁾	UNIT
t_{CSH}	$\overline{\text{CS}}$ Hold Time after SCLK Rising Edge		10	0		ns
t_{CSS}	$\overline{\text{CS}}$ Setup Time prior to SCLK Rising Edge		10	4.5		ns
t_{EN}	$\overline{\text{CS}}$ Falling Edge to DOUT enabled			5	30	ns
t_{DACC}	DOUT Access Time after SCLK Falling Edge			17	27	ns
t_{DHLD}	DOUT Hold Time after SCLK Falling Edge			4		ns
t_{DS}	DIN Setup Time prior to SCLK Rising Edge		10	3		ns
t_{DH}	DIN Hold Time after SCLK Rising Edge		10	3		ns
t_{CH}	SCLK High Time		$0.4 \times t_{\text{SCLK}}$			ns
t_{CL}	SCLK Low Time		$0.4 \times t_{\text{SCLK}}$			ns
t_{DIS}	$\overline{\text{CS}}$ Rising Edge to DOUT High-Impedance	DOUT falling		2.4	20	ns
		DOUT rising		0.9	20	ns

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

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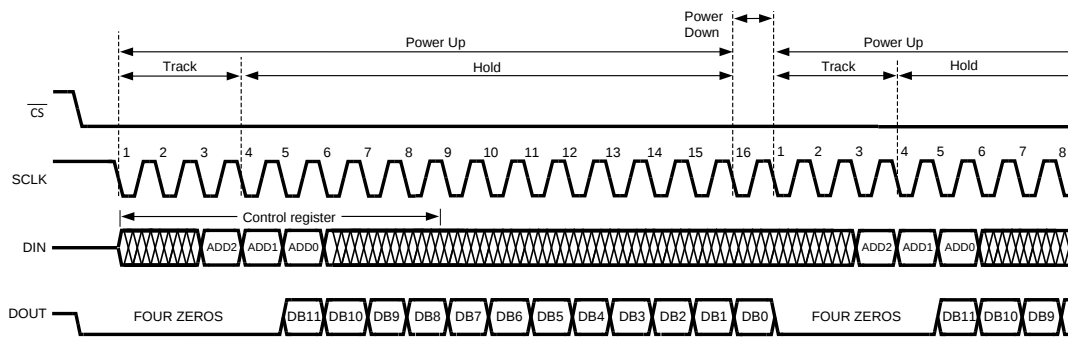


Figure 1. ADC128S102 Operational Timing Diagram

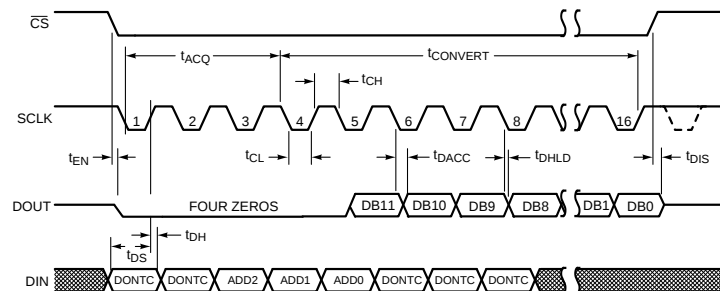


Figure 2. ADC128S102 Serial Timing Diagram

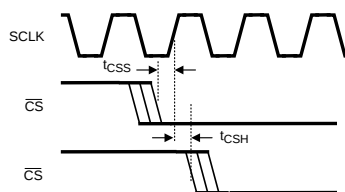


Figure 3. SCLK and $\overline{CS}$ Timing Parameters

6.7 Typical Characteristics

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 1 \text{ MSPS}$, $f_{\text{SCLK}} = 16 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

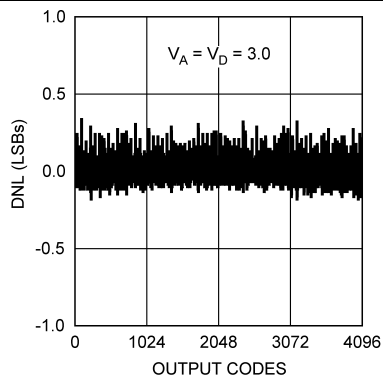


Figure 4. DNL

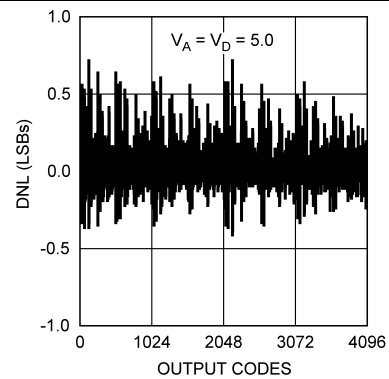


Figure 5. DNL

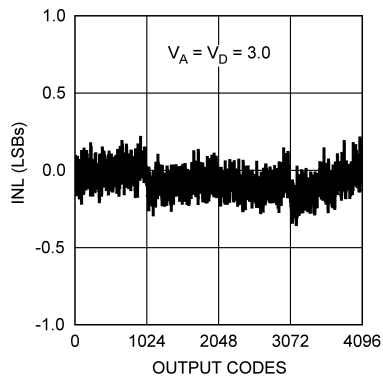


Figure 6. INL

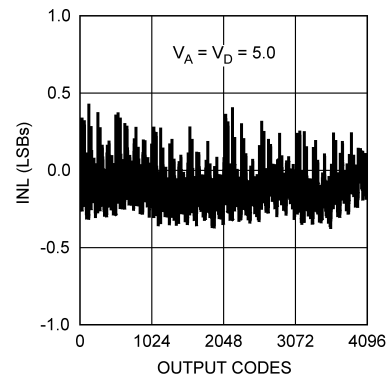


Figure 7. INL

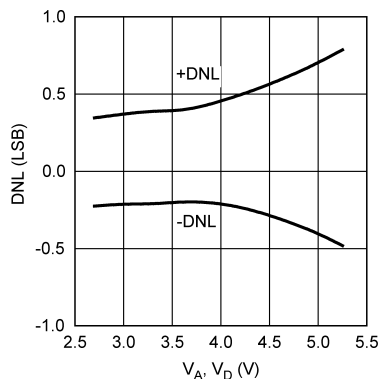


Figure 8. DNL vs. Supply

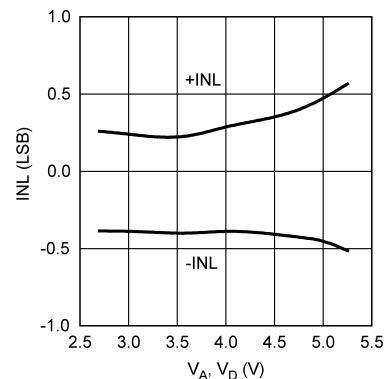


Figure 9. INL vs. Supply

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Typical Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 1 \text{ MSPS}$, $f_{\text{SCLK}} = 16 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

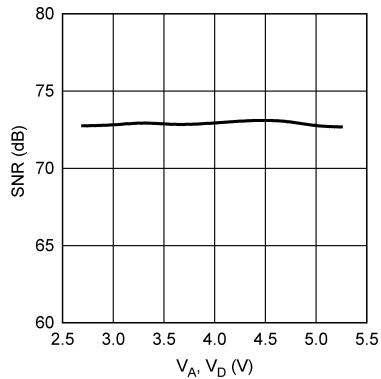


Figure 10. SNR vs. Supply

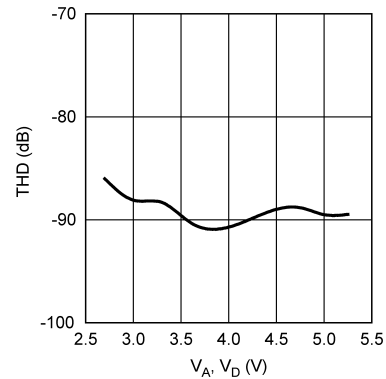


Figure 11. THD vs. Supply

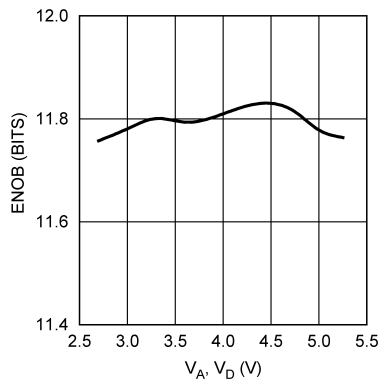


Figure 12. ENOB vs. Supply

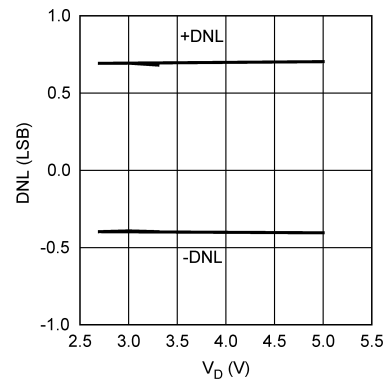


Figure 13. DNL vs. V_D with V_A = 5.0 V

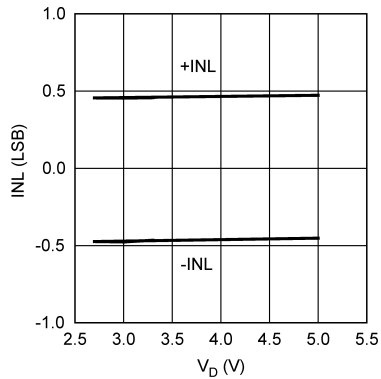


Figure 14. INL vs. V_D with V_A = 5.0 V

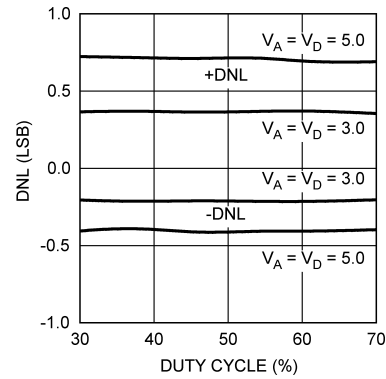


Figure 15. DNL vs. SCLK Duty Cycle

Typical Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 1 \text{ MSPS}$, $f_{\text{SCLK}} = 16 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

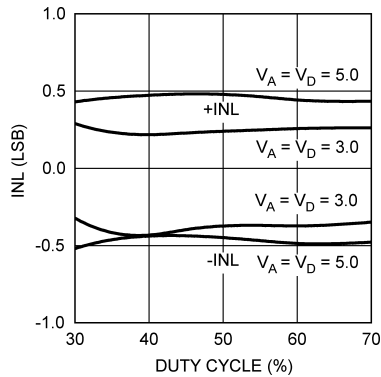


Figure 16. INL vs. SCLK Duty Cycle

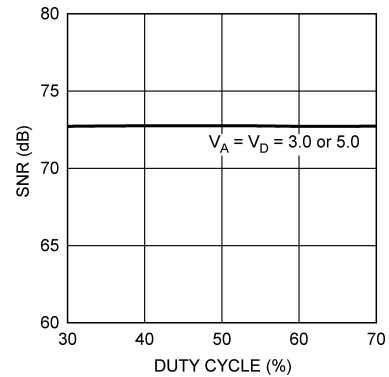


Figure 17. SNR vs. SCLK Duty Cycle

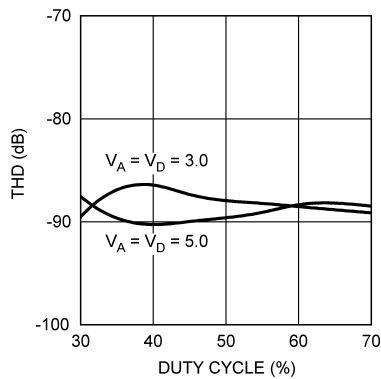


Figure 18. THD vs. SCLK Duty Cycle

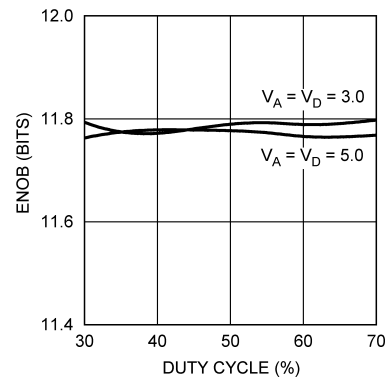


Figure 19. ENOB vs. SCLK Duty Cycle

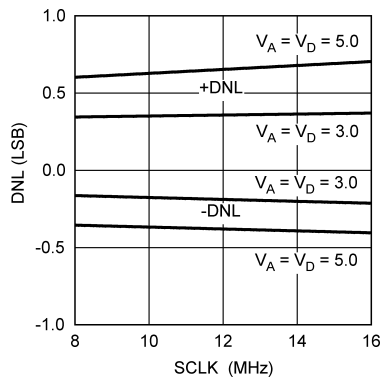


Figure 20. DNL vs. SCLK

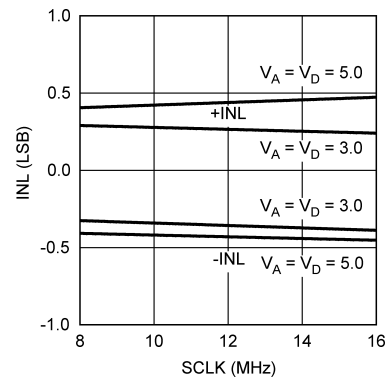


Figure 21. INL vs. SCLK

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Typical Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 1 \text{ MSPS}$, $f_{\text{SCLK}} = 16 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

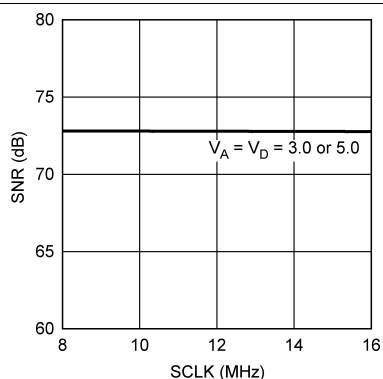


Figure 22. SNR vs. SCLK

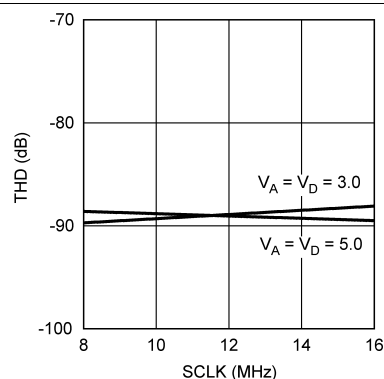


Figure 23. THD vs. SCLK

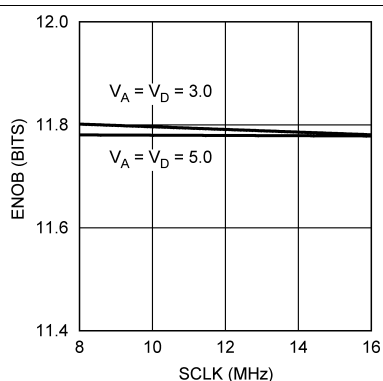


Figure 24. ENOB vs. SCLK

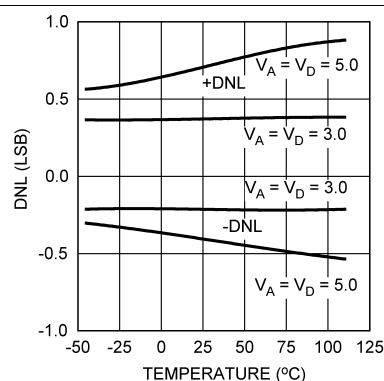


Figure 25. DNL vs. Temperature

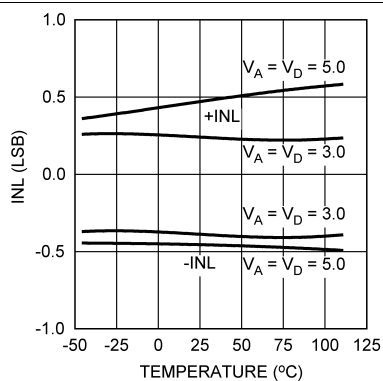


Figure 26. INL vs. Temperature

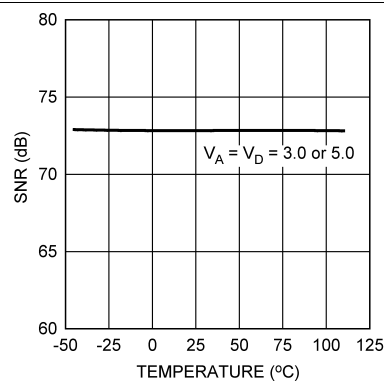


Figure 27. SNR vs. Temperature

Typical Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 1 \text{ MSPS}$, $f_{\text{SCLK}} = 16 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

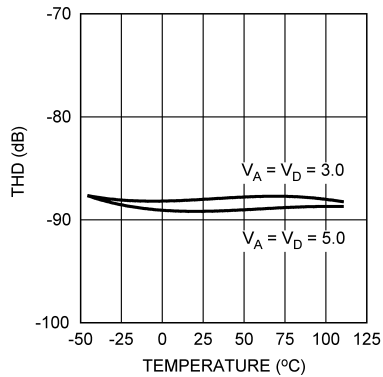


Figure 28. THD vs. Temperature

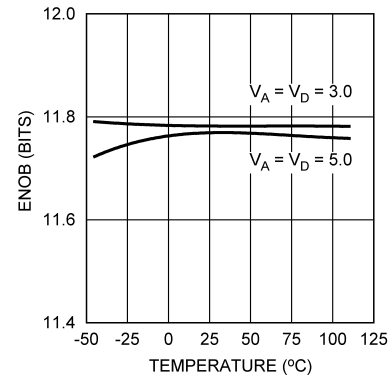


Figure 29. ENOB vs. Temperature

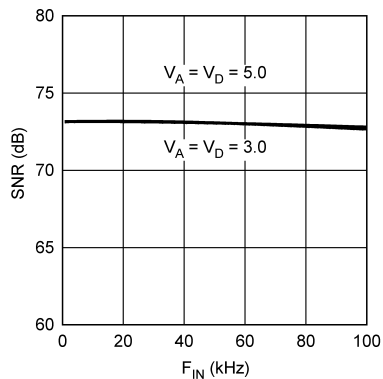


Figure 30. SNR vs. Input Frequency

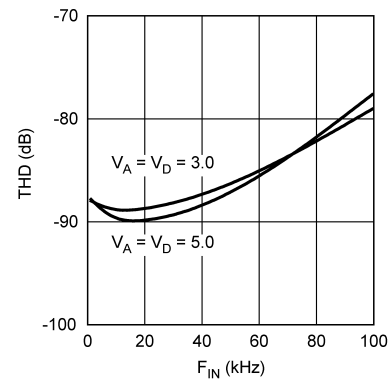


Figure 31. THD vs. Input Frequency

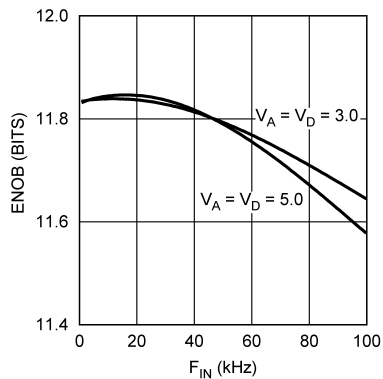


Figure 32. ENOB vs. Input Frequency

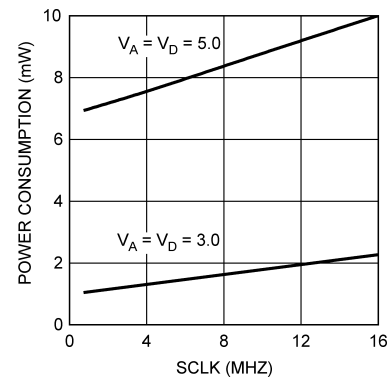


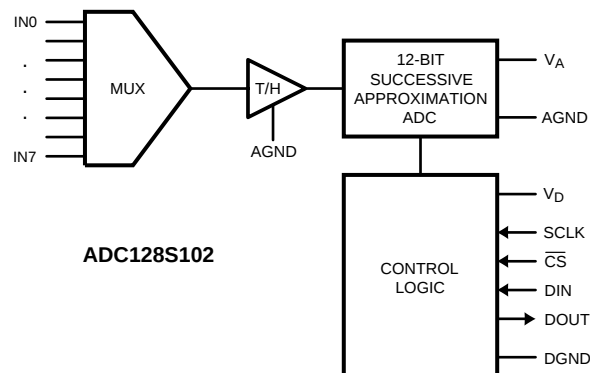
Figure 33. Power Consumption vs. SCLK

7 Detailed Description

7.1 Overview

The ADC128S102 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ADC128S102 Operation

Simplified schematics of the ADC128S102 in both track and hold operation are shown in [Figure 34](#) and [Figure 35](#) respectively. In [Figure 34](#), the ADC128S102 is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC128S102 is in this state for the first three SCLK cycles after CS is brought low.

[Figure 35](#) shows the ADC128S102 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC128S102 is in this state for the last thirteen SCLK cycles after CS is brought low.

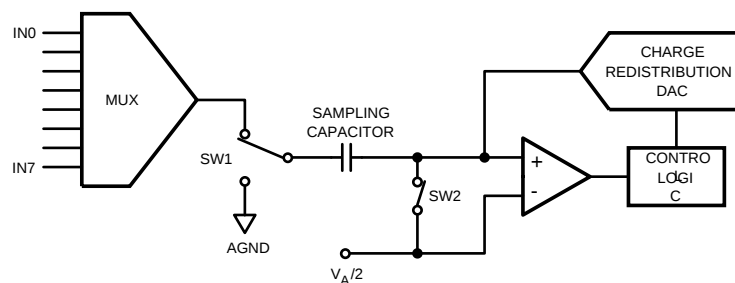


Figure 34. ADC128S102 in Track Mode

Feature Description (continued)

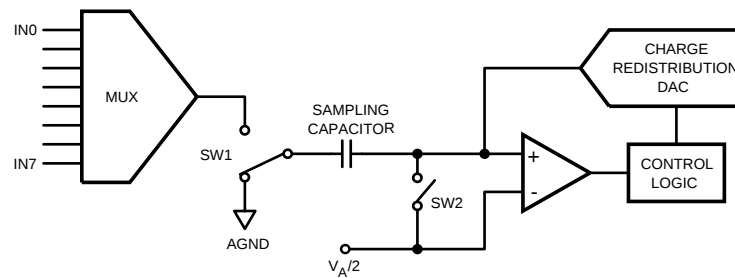


Figure 35. ADC128S102 in Hold Mode

7.3.2 ADC128S102 Transfer Function

The output format of the ADC128S102 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC128S102 is $V_A / 4096$. The ideal transfer characteristic is shown in Figure 36. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of $V_A / 8192$. Other code transitions occur at steps of one LSB.

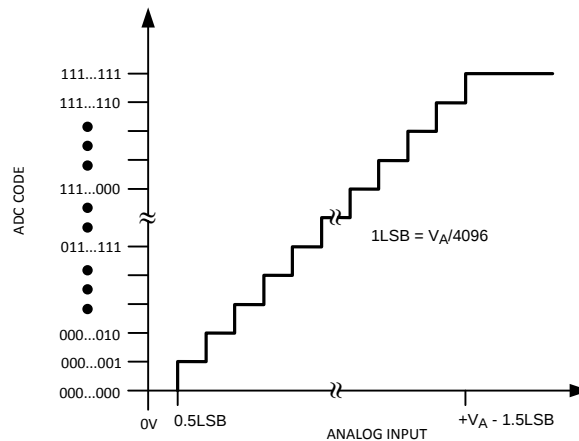


Figure 36. Ideal Transfer Characteristic

7.3.3 Analog Inputs

An equivalent circuit for one of the ADC128S102's input channels is shown in Figure 37. Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to V_A . Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 37 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch and is typically 500 ohms. Capacitor C2 is the ADC128S102 sampling capacitor, and is typically 30 pF. The ADC128S102 will deliver best performance when driven by a low-impedance source (less than 100 ohms). This is especially important when using the ADC128S102 to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonics and noise in the input. These filters are often referred to as anti-aliasing filters.

Feature Description (continued)

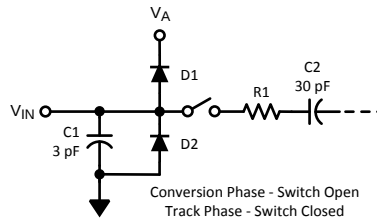


Figure 37. Equivalent Input Circuit

7.3.4 Digital Inputs and Outputs

The ADC128S102's digital inputs (SCLK, $\overline{\text{CS}}$, and DIN) have an operating range of 0 V to V_A . They are not prone to latch-up and may be asserted before the digital supply (V_D) without any risk. The digital output (DOUT) operating range is controlled by V_D . The output high voltage is $V_D - 0.5\text{V}$ (min) while the output low voltage is 0.4V (max).

7.4 Device Functional Modes

The ADC128S102 is fully powered-up whenever $\overline{\text{CS}}$ is low and fully powered-down whenever $\overline{\text{CS}}$ is high, with one exception. If operating in continuous conversion mode, the ADC128S102 automatically enters power-down mode between SCLK's 16th falling edge of a conversion and SCLK's 1st falling edge of the subsequent conversion (see [Figure 1](#)).

In continuous conversion mode, the ADC128S102 can perform multiple conversions back to back. Each conversion requires 16 SCLK cycles and the ADC128S102 will perform conversions continuously as long as $\overline{\text{CS}}$ is held low. Continuous mode offers maximum throughput.

In burst mode, the user may trade off throughput for power consumption by performing fewer conversions per unit time. This means spending more time in power-down mode and less time in normal mode. By utilizing this technique, the user can achieve very low sample rates while still utilizing an SCLK frequency within the electrical specifications. The Power Consumption vs. SCLK curve in the [Typical Characteristics](#) section shows the typical power consumption of the ADC128S102. To calculate the power consumption (P_C), simply multiply the fraction of time spent in the normal mode (t_N) by the normal mode power consumption (P_N), and add the fraction of time spent in shutdown mode (t_S) multiplied by the shutdown mode power consumption (P_S) as shown in [Equation 1](#).

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S \quad (1)$$

7.5 Programming

7.5.1 Serial Interface

An operational timing diagram and a serial interface timing diagram for the ADC128S102 are shown in the [Timing Specifications](#) section. $\overline{\text{CS}}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC128S102's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{\text{CS}}$ and ends on the rising edge of $\overline{\text{CS}}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when $\overline{\text{CS}}$ is high and is active when $\overline{\text{CS}}$ is low. Thus, $\overline{\text{CS}}$ acts as an output enable. Similarly, SCLK is internally gated off when $\overline{\text{CS}}$ is brought high.

Programming (continued)

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out. SCLK falling edges 1 through 4 clock out leading zeros while falling edges 5 through 16 clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the hold/convert mode on the N*16+4th falling edge of SCLK. "N" is an integer value.

The ADC128S102 enters track mode under three different conditions. In [Figure 1](#), $\overline{CS}$ goes low with SCLK high and the ADC enters track mode on the first falling edge of SCLK. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC enters track mode. While there is no timing restriction with respect to the rising edges of $\overline{CS}$ and SCLK, see [Figure 3](#) for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK.

While a conversion is in progress, the address of the next input for conversion is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. See [Table 1](#), [Table 2](#), and [Table 3](#).

There is no need to incorporate a power-up delay or dummy conversions as the ADC128S102 is able to acquire the input signal to full resolution in the first conversion immediately following power-up. The first conversion result after power-up will be that of IN0.

Table 1. Control Register Bits

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

Table 2. Control Register Bit Descriptions

Bit No:	Symbol:	Description
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel will be sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in Table 3 .
4	ADD1	
3	ADD0	

Table 3. Input Channel Selection

ADD2	ADD1	ADD0	Input Channel
0	0	0	IN0 (Default)
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADC128S102 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. Since the ADC128S102 integrates an 8 to 1 MUX on the front end, the device is typically used in applications where multiple voltages need to be monitored. In addition to having 8 input channels, the ADC128S102 can operate at sampling rates up to 1 MSPS. As a result, the ADC128S102 is typically run in burst fashion where a voltage is sampled for several times and then the ADC128S102 can be powered-down. This is a common technique for applications that are power limited. Due to the high bandwidth and sampling rate, the ADC128S102 is suitable for monitoring AC waveforms as well as DC inputs. The following example shows a common configuration for monitoring AC inputs.

8.2 Typical Application

The following sections outline the design principles of data acquisition system based on the ADC128S102.

A typical application is shown in [Figure 38](#). The analog supply is bypassed with a capacitor network located close to the ADC128S102. The ADC128S102 uses the analog supply (V_A) as its reference voltage, so it is very important that V_A be kept as clean as possible. Due to the low power requirements of the ADC128S102, it is also possible to use a precision reference as a power supply.

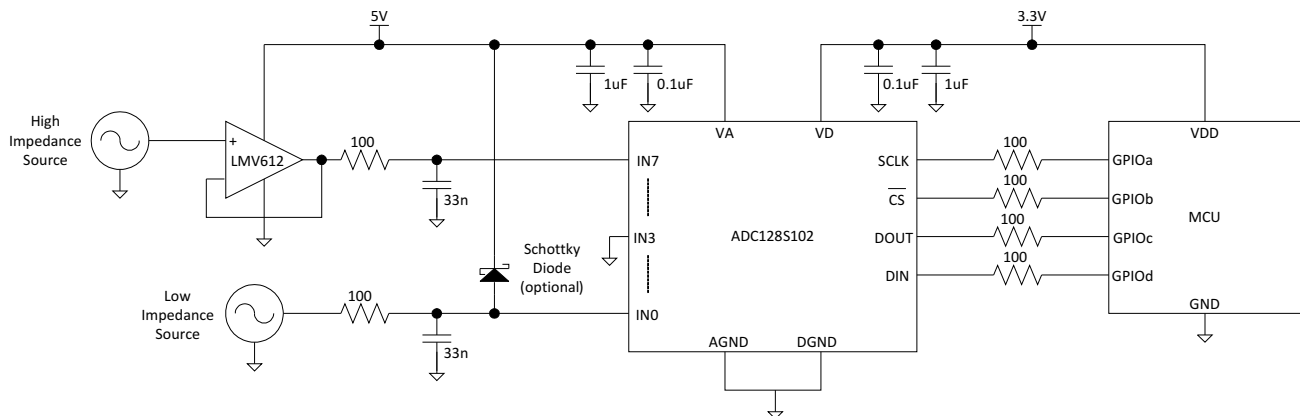


Figure 38. Typical Application Circuit

8.2.1 Design Requirements

A positive supply only data acquisition system capable of digitizing signals ranging 0 to 5 V, BW = 10 kHz, and a throughput of 125 kSPS.

The ADC128S102 has to interface to an MCU whose supply is set at 3.3 V.

8.2.2 Detailed Design Procedure

The signal range requirement forces the design to use 5-V analog supply at V_A , analog supply. This follows from the fact that V_A is also a reference potential for the ADC.

The requirement of interfacing to the MCU which is powered by 3.3-V supply, forces the choice of 3.3-V as a V_D supply.

Sampling is in fact a modulation process which may result in aliasing of the input signal, if the input signal is not adequately band limited. The maximum sampling rate of the ADC128S102 when all channels are enabled is, F_s :

Typical Application (continued)

$$F_s = \frac{F_{SCLK}}{16 \times 8} \quad (2)$$

Note that faster sampling rates can be achieved when fewer channels are sampled. Single channel can be sampled at the maximum rate of:

$$F_{s_single} = \frac{F_{SCLK}}{16} \quad (3)$$

In order to avoid the aliasing the Nyquist criterion has to be met:

$$BW_{signal} < \frac{F_s}{2} \quad (4)$$

Therefore it is necessary to place anti-aliasing filters at all inputs of the ADC. These filters may be single pole low pass filters whose pole location has to satisfy, assuming all channels sampled in sequence:

$$\frac{1}{\pi \times R \times C} < \frac{F_{SCLK}}{16 \times 8} \quad (5)$$

$$R \times C > \frac{128}{\pi \times F_{SCLK}} \quad (6)$$

With $F_{sclk} = 16$ MHz, a good choice for the single pole filter is:

- $R = 100$
- $C = 33$ nF

This reduces the input $BW_{signal} = 48$ kHz. The capacitor at the INx input of the device provides not only the filtering of the input signal, but it also absorbs the charge kick-back from the ADC. The kick-back is the result of the internal switches opening at the end of the acquisition period.

The VA and VD sources are already separated in this example, due to the design requirements. This also benefits the overall performance of the ADC, as the potentially noisy VD supply does not contaminate the VA. In the same vain, further consideration could be given to the SPI interface, especially when the master MCU is capable of producing fast rising edges on the digital bus signals. Inserting small resistances in the digital signal path may help in reducing the ground bounce, and thus improve the overall noise performance of the system.

Care should be taken when the signal source is capable of producing voltages beyond VA. In such instances the internal ESD diodes may start conducting. The ESD diodes are not intended as input signal clamps. To provide the desired clamping action use Schottky diodes as shown in [Figure 38](#).

8.2.3 Application Curve

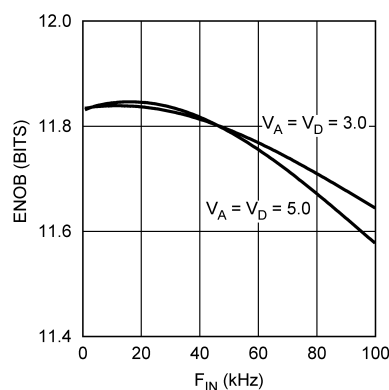


Figure 39. Typical Performance

9 Power Supply Recommendations

There are three major power supply concerns with this product: power supply sequencing, power management, and the effect of digital supply noise on the analog supply.

9.1 Power Supply Sequence

The ADC128S102 is a dual-supply device. The two supply pins share ESD resources, so care must be exercised to ensure that the power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (V_D) cannot exceed the analog supply (V_A) by more than 300 mV. Therefore, V_A must ramp up before or concurrently with V_D .

9.2 Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, V_D . The current pulses required from the supply to charge the output capacitance will cause voltage variations on the digital supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply will be coupled directly into the analog supply, causing greater performance degradation than would noise on the digital supply alone. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance. Since the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

10 Layout

10.1 Layout Guidelines

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC128S102 due to supply noise, do not use the same supply for the ADC128S102 that is used for digital logic.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

We recommend the use of a single, uniform ground plane and the use of split power planes. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point.

10.2 Layout Example

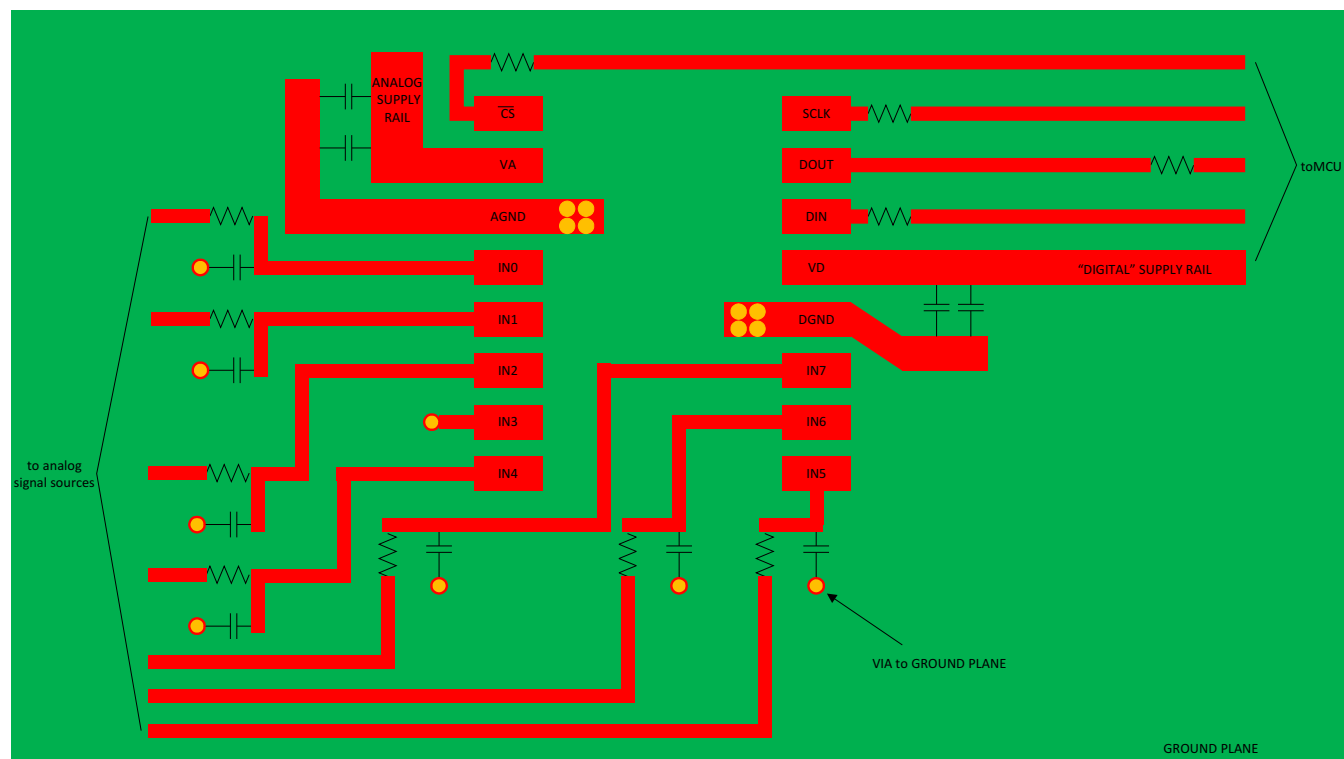


Figure 40. Layout Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 Specification Definitions

ACQUISITION TIME is the time required for the ADC to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CHANNEL-TO-CHANNEL ISOLATION is resistance to coupling of energy from one channel into another channel.

CROSSTALK is the coupling of energy from one channel into another channel. This is similar to Channel-to-Channel Isolation, except for the sign of the data.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as $(\text{SINAD} - 1.76) / 6.02$ and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE ERROR (FSE) is a measure of how far the last code transition is from the ideal $1\frac{1}{2}$ LSB below V_{REF}^+ and is defined as:

$$V_{\text{FSE}} = V_{\text{max}} + 1.5 \text{ LSB} - V_{\text{REF}}^+$$

where

- V_{max} is the voltage at which the transition to the maximum code occurs.
- FSE can be expressed in Volts, LSB or percent of full scale range. (7)

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal ($V_{\text{REF}} - 1.5$ LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale ($\frac{1}{2}$ LSB below the first code transition) through positive full scale ($\frac{1}{2}$ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to an individual ADC input at the same time. It is defined as the ratio of the power in both the second or the third order intermodulation products to the power in one of the original frequencies. Second order products are $f_a \pm f_b$, where f_a and f_b are the two sine wave input frequencies. Third order products are $(2f_a \pm f_b)$ and $(f_a \pm 2f_b)$. IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC outputs. These codes cannot be reached with any input value. The ADC128S102 is ensured not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

Device Support (continued)

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including d.c. or the harmonics included in THD.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

THROUGHPUT TIME is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion and read out times. In the case of the ADC128S102, this is 16 SCLK periods.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as:

$$\text{THD} = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \dots + A_{f10}^2}{A_{f1}^2}}$$

where

- A_{f1} is the RMS power of the input frequency at the output
 - A_{f2} through A_{f10} are the RMS power in the first 9 harmonic frequencies
- (8)

11.2 Trademarks

MICROWIRE is a trademark of Texas Instruments.

QSPI is a trademark of Motorola, Inc..

All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC128S102CIMT	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 105	128S102 CIMT	
ADC128S102CIMT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 105	128S102 CIMT	Samples
ADC128S102CIMTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 105	128S102 CIMT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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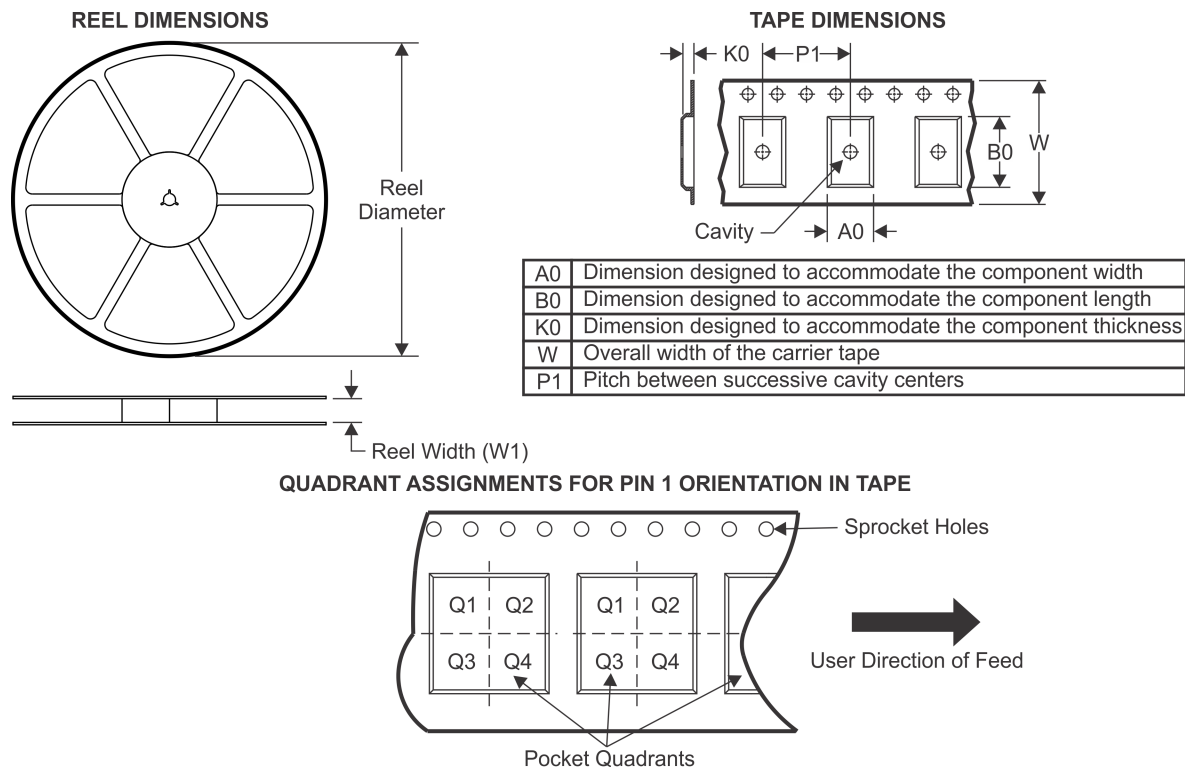


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PACKAGE OPTION ADDENDUM

6-Feb-2020

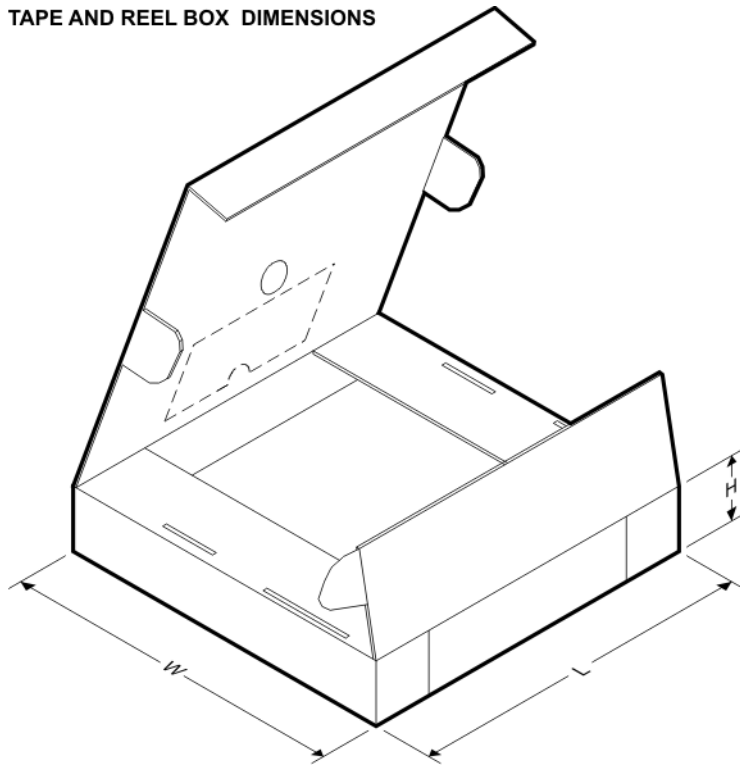
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC128S102CIMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

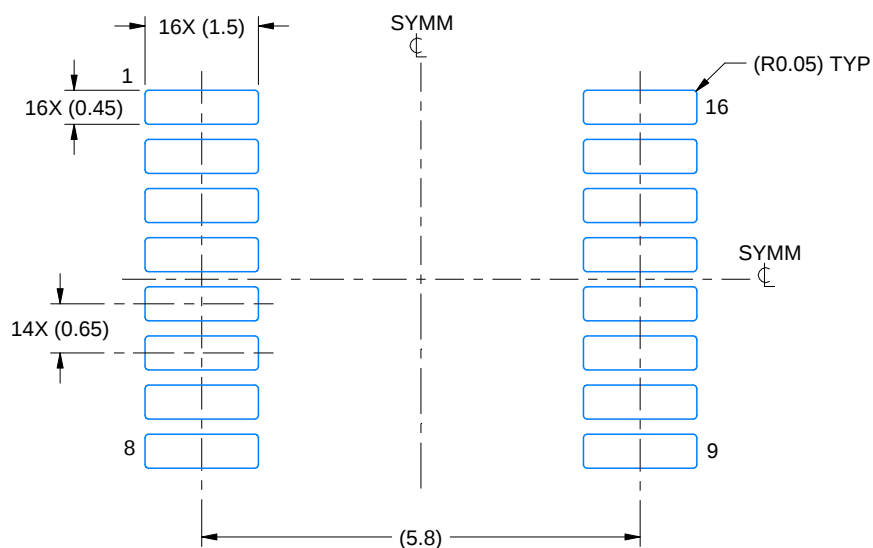
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC128S102CIMTX/NOP B	TSSOP	PW	16	2500	367.0	367.0	35.0

EXAMPLE BOARD LAYOUT

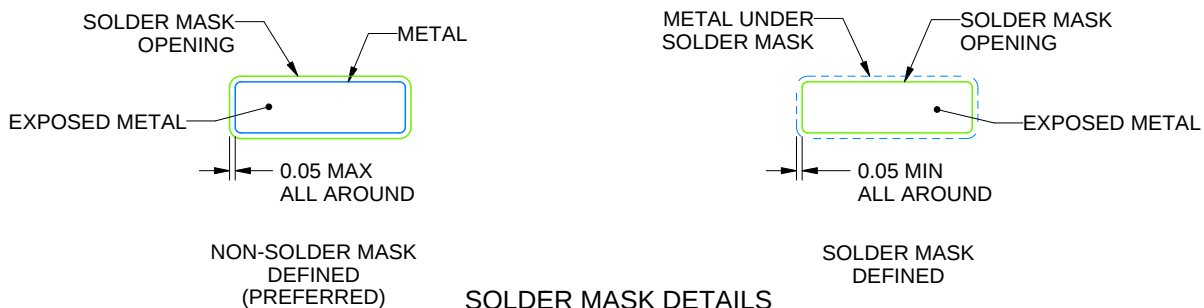
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

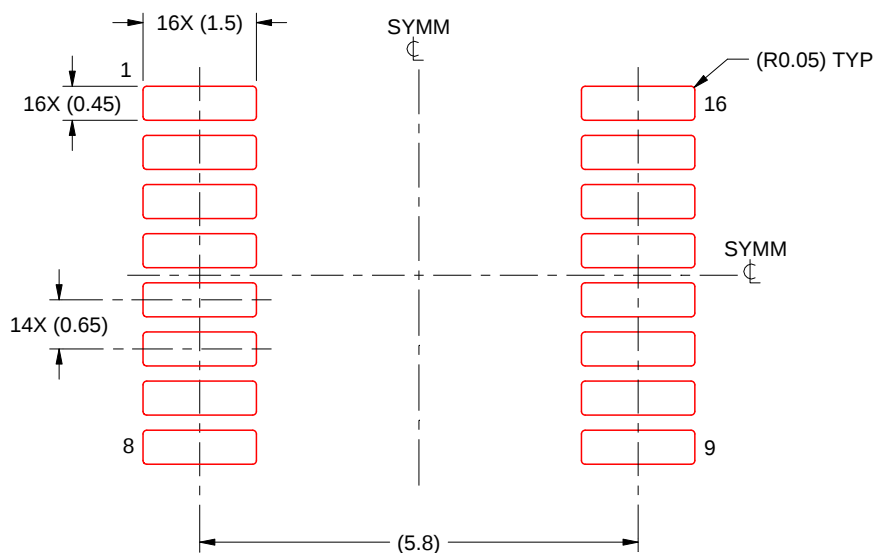
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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