ADC1175-50 8-Bit, 50 MSPS, 125 mW A/D Converter

Check for Samples: ADC1175-50

FEATURES

- **Internal Track-and-Hold Function**
- **Single +5V Operation**
- **Internal Reference Bias Resistors**
- **Industry Standard Pinout**
- **Power-Down Mode (<5 mW)**

APPLICATIONS

- **Digital Still Cameras**
- **CCD Imaging**
- **Electro-Optics**
- **Video Digitization**
- **Multimedia**

KEY SPECIFICATIONS

- **Resolution 8 Bits**
- **Maximum Sampling Frequency 50 MSPS (min)**
- **THD 54 dB (typ)**
- **DNL 0.7 LSB (typ)**
- **ENOB @ f_{IN} = 25 MHz 6.8 Bits (typ)**
- **Ensured No Missing Codes**
- **Power Consumption (Excluding Reference Current) 125 mW (typ) 190 mW (max)**

DESCRIPTION

The ADC1175-50 is a low power, 50 MSPS analog-to-digital converter that digitizes signals to 8 bits while consuming just 125 mW (typ). The ADC1175-50 uses a unique architecture that achieves 6.8 Effective Bits at 25 MHz input and 50 MHz clock frequency. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +5V single supply operation, make it ideally suited for many video and imaging applications, including use in portable equipment. Furthermore, the ADC1175-50 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC1175-50's reference ladder is available for connections, enabling a wide range of input possibilities. The low input capacitance (7 pF, typical) makes this device easier to drive than conventional flash converters and the power down mode reduces power consumption to less than 5 mW.

The ADC1175-50 is offered in 24-pin TSSOP and 24-pin WQFN packages and is designed to operate over the extended commercial temperature range of −20°C to +75°C.

CONNECTION DIAGRAMS

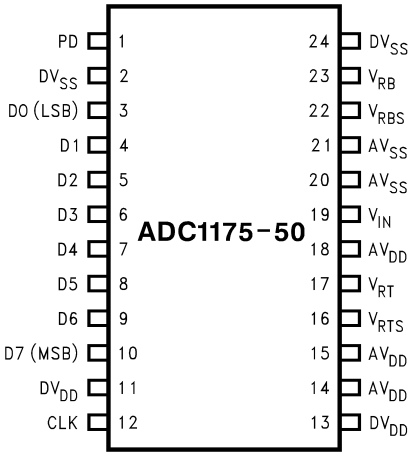

Figure 1. 24-Pin TSSOP - Top View
See PW Package

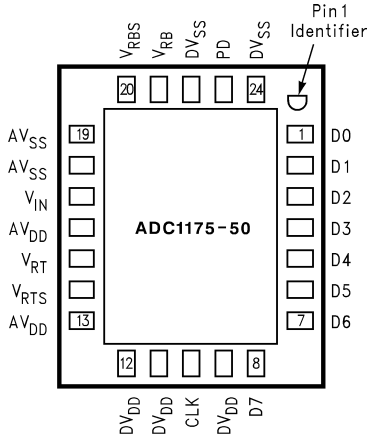

Figure 2. 24-Pin WQFN - Bottom View
See NHW0024B Package

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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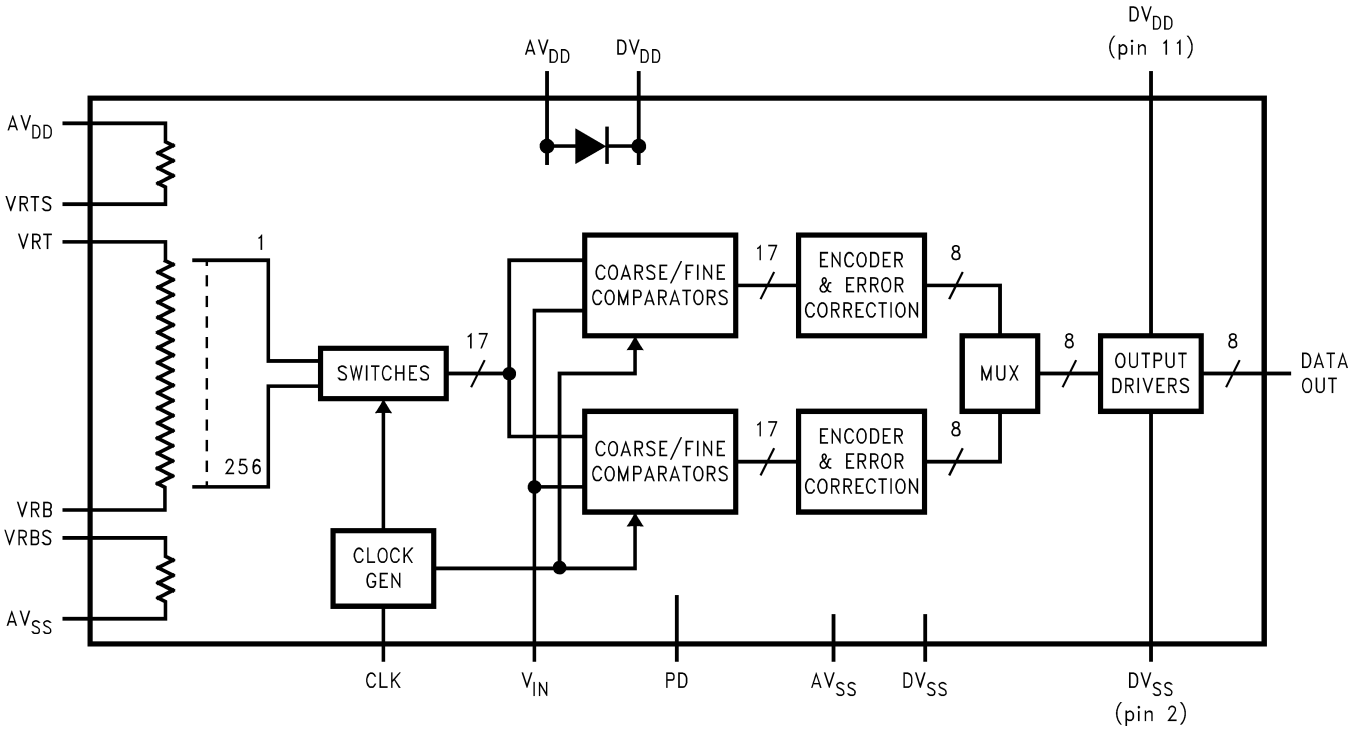
BLOCK DIAGRAM



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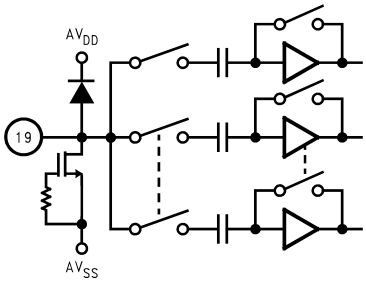
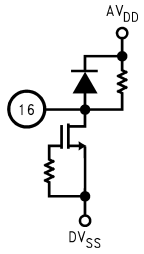
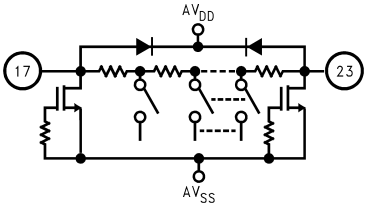
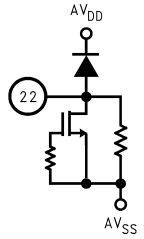
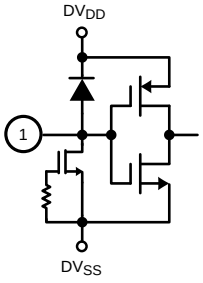
PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS(1)

Pin No.	Symbol	Equivalent Circuit	Description
19 (17)	V_{IN}		Analog signal input. Conversion range is V_{RT} to V_{RB}.
16 (14)	V_{RTS}		Reference Top Bias with internal pull up resistor. Short this pin to V_{RT} to self-bias the reference ladder.
17 (15)	V_{RT}		Analog input that is the high (top) side of the reference ladder of the ADC. Voltages on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See REFERENCE INPUTS for more information.
23 (21)	V_{RB}		Analog input that is the low (bottom) side of the reference ladder of the ADC. Nominal range is 0.0V to 4.0V, with optimized value of 0.6V. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See REFERENCE INPUTS for more information.
22 (20)	V_{RBS}		Reference Bottom Bias with internal pull down resistor. Short to V_{RB} to self-bias the reference ladder. Bypass well (unless grounded). See REFERENCE INPUTS for more information.
1 (23)	PD		CMOS/TTL compatible Digital input that, when high, puts the ADC1175-50 into a power-down mode where total power consumption is typically less than 5 mW. With this pin low, the device is in the normal operating mode.

(1) (WQFN pins in parentheses)

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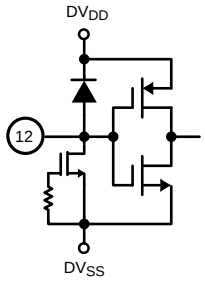
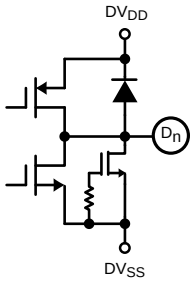
PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS(1) (continued)

Pin No.	Symbol	Equivalent Circuit	Description
12 (10)	CLK		CMOS/TTL compatible digital clock input. V_{IN} is sampled on the falling edge of CLK input.
3 thru 10 (1 thru 8)	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are in a high impedance mode when the PD pin is low.
11, 13, 14 (9, 11, 12)	DV_{DD}		Positive digital supply pin. Connect to a quiet voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. See POWER SUPPLY CONSIDERATIONS for more information.
2, 24 (22, 24)	DV_{SS}		The ground return for the digital supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175-50.
15, 18 (13, 16)	AV_{DD}		Positive analog supply pin. Connect to a quiet voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. See POWER SUPPLY CONSIDERATIONS for more information.
20, 21 (18, 19)	AV_{SS}		The ground return for the analog supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175-50 package.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Supply Voltage (AV_{DD}, DV_{DD})		6.5V
Voltage on Any Input or Output Pin		−0.3V to +6.5V
Reference Voltage (V_{RT}, V_{RB})		AV_{SS} to V_{DD}
CLK, PD Voltage Range		−0.5 to (AV_{DD} +0.5V)
Digital Output Voltage (V_{OH}, V_{OL})		V_{SS} to V_{DD}
Input Current at Any Pin(4)		±25 mA
Package Input Current(4)		±50 mA
Power Dissipation at T_A = 25°C		See (5)
ESD Susceptibility(6)	Human Body Model	2000V
	Machine Model	250V
Soldering Temperature	Infrared (10 sec.)	235°C
Storage Temperature		−65°C to +150°C
Short Circuit Duration (Single High Output to Ground)		1 Second

(1) All voltages are measured with respect to GND = AV_{SS} = DV_{SS} = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, less than AV_{SS} or DV_{SS}, or greater than AV_{DD} or DV_{DD}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature (T_J max) for this device is 150°C. The maximum allowable power dissipation is dictated by T_J max, the junction-to-ambient thermal resistance (θ_{JA}) and the ambient temperature (T_A), and can be calculated using the formula P_D max = (T_J max – T_A)/θ_{JA}. The values for maximum power dissipation listed above will be reached only when the ADC1175-50 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.

OPERATING RATINGS(1)(2)

Operating Temperature Range	−20°C ≤ T_A ≤ +75°C
Supply Voltage (AV_{DD}, DV_{DD})	+4.75V to +5.25V
AV_{DD} − DV_{DD}	<0.5V
Ground Difference |DV_{SS} – AV_{SS}|	0V to 100 mV
Pin 11 to Pin 13 Voltage	<0.5V
Upper Reference Voltage (V_{RT})	1.0V to V_{DD}
Lower Reference Voltage (V_{RB})	0V to 4.0V
V_{RT} - V_{RB}	1V to 2.8V
V_{IN} Voltage Range	V_{RB} to V_{RT}

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AV_{SS} = DV_{SS} = 0V, unless otherwise specified.

PACKAGE THERMAL RESISTANCE

Package	θ_{JA}
TSSOP	92°C / W
WQFN	40°C / W

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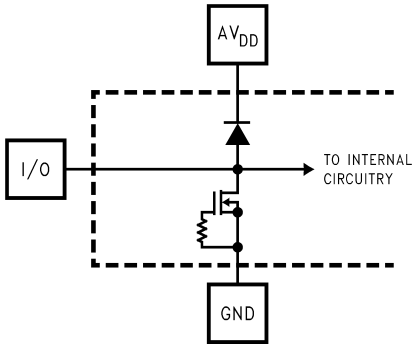
CONVERTER ELECTRICAL CHARACTERISTICS

The following specifications apply for AV_{DD} = DV_{DD} = +5.0 V_{DC}, PD = 0V, V_{RT} = +2.6V, V_{RB} = 0.6V, C_L = 20 pF, f_{CLK} = 50 MHz at 50% duty cycle. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**; all other limits T_A = 25°C (1)(2).

Symbol	Parameter	Conditions		Typical(3)	Limits(3)	Units (Limits)
DC ACCURACY						
INL	Integral Non Linearity Error	V_{IN} = 0.6V to 2.6V		±0.8	**±1.95**	LSB (max)
DNL	Differential Non-Linearity	V_{IN} = 0.6V to 2.6V		+0.7	**+1.75**	LSB (max)
				−0.7	**−1.0**	LSB (min)
	Resolution for No Missing Codes				**8**	Bits
E_{OT}	Top Offset Voltage			−12		mV
E_{OB}	Bottom Offset Voltage			+10		mV
VIDEO ACCURACY						
DP	Differential Phase Error	f_{IN} = 4.43 MHz Modulated Ramp		0.5		deg
DG	Differential Gain Error	f_{IN} = 4.43 MHz Modulated Ramp		1.0		%
ANALOG INPUT AND REFERENCE CHARACTERISTIC						
V_{IN}	Input Range			2.0	**V_{RB}** **V_{RT}**	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 1.5V +0.7 Vrms	(CLK LOW)	4		pF
			(CLK HIGH)	7		pF
R_{IN}	R_{IN} Input Resistance			>1		MΩ
BW	Full Power Bandwidth			120		MHz
R_{RT}	Top Reference Resistor			320		Ω
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		270	**200** **350**	Ω (min) Ω (max)
R_{RB}	Bottom Reference Resistor			80		Ω
I_{REF}	Reference Ladder Current	V_{RT} = V_{RTS}, V_{RB} = V_{RBS}		7	**5.4**	mA (min)
					10.8	mA (max)
		V_{RT} = V_{RTS}, V_{RB} = AV_{SS}		8	**6.1**	mA (min)
					12.3	mA (max)
V_{RT}	Reference Top Self Bias Voltage	V_{RT} Connected to V_{RTS}, V_{RB} Connected to V_{RBS}		2.6		V (min) V (max)
V_{RB}	Reference Bottom Self Bias Voltage	V_{RT} Connected to V_{RTS}, V_{RB} Connected to V_{RBS}		0.6	**0.55** **0.70**	V (min) V (max)

(1) The analog inputs are protected as shown below. Input voltage magnitudes up to 6.5V or 500 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_{DD} or below GND by more than 50 mV. As an example, if AV_{DD} is 4.75 V_{DC}, the full-scale input voltage must be ≤4.80 V_{DC} to ensure accurate conversions.



(2) To ensure accuracy, it is required that AV_{DD} and DV_{DD} be well bypassed. Each V_{DD} pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are ensured to TI's AOQL (Average Outgoing Quality Level).

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CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for AV_{DD} = DV_{DD} = +5.0 V_{DC}, PD = 0V, V_{RT} = +2.6V, V_{RB} = 0.6V, C_L = 20 pF, f_{CLK} = 50 MHz at 50% duty cycle. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**; all other limits T_A = 25°C (1)(2).

Symbol	Parameter	Conditions	Typical(3)	Limits(3)	Units (Limits)
V_{RTS} – V_{RBS}	Self Bias Voltage Delta	V_{RT} Connected to V_{RTS}, V_{RB} Connected to V_{RBS}	2	**1.89** **2.20**	(V min) V (max)
		V_{RT} Connected to V_{RTS}, V_{RB} Connected to AV_{SS}	2.3		V
V_{RT} – V_{RB}	Reference Voltage Differential		2	**1.0** **2.8**	V (min) V (max)
CONVERTER DYNAMIC CHARACTERISTICS					
ENOB	Effective Number of Bits	f_{IN} = 4.4 MHz, f_{CLK} = 40 MHz	7.2	**6.7**	Bits (min)
		f_{IN} = 19.9 MHz, f_{CLK} = 40 MHz	7.0	**6.4**	Bits (min)
		f_{IN} = 1.3 MHz, f_{CLK} = 50 MHz	7.3		Bits
		f_{IN} = 4.4 MHz, f_{CLK} = 50 MHz	7.2		Bits
		f_{IN} = 24.9 MHz, f_{CLK} = 50 MHz	6.8	**6.1**	Bits (min)
SINAD	Signal-to-Noise & Distortion	f_{IN} = 4.4 MHz, f_{CLK} = 40 MHz	45	**42**	dB (min)
		f_{IN} = 19.9 MHz, f_{CLK} = 40 MHz	44	**40**	dB (min)
		f_{IN} = 1.3 MHz, f_{CLK} = 50 MHz	46		dB
		f_{IN} = 4.4 MHz, f_{CLK} = 50 MHz	45		dB
		f_{IN} = 24.9 MHz, f_{CLK} = 50 MHz	43	**38.4**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 4.4 MHz, f_{CLK} = 40 MHz	46	**42.5**	dB (min)
		f_{IN} = 19.9 MHz, f_{CLK} = 40 MHz	44	**41**	dB (min)
		f_{IN} = 1.3 MHz, f_{CLK} = 50 MHz	48		dB
		f_{IN} = 4.4 MHz, f_{CLK} = 50 MHz	45		dB
		f_{IN} = 24.9 MHz, f_{CLK} = 50 MHz	44	**40**	dB (min)
SFDR	Spurious Free Dynamic Range	f_{IN} = 1.3 MHz	57		dB
		f_{IN} = 4.4 MHz	56		dB
		f_{IN} = 24.9 MHz	51		dB
THD	Total Harmonic Distortion	f_{IN} = 1.3 MHz	−55		dB
		f_{IN} = 4.4 MHz	−54		dB
		f_{IN} = 24.9 MHz	−51		dB
POWER SUPPLY CHARACTERISTICS					
IA_{DD}	Analog Supply Current	DV_{DD} = AV_{DD} = 5.25V	13		mA
ID_{DD}	Digital Supply Current	DV_{DD} = AV_{DD} = 5.25V	11		mA
IA_{DD} + ID_{DD}	Total Operating Current	DV_{DD} = AV_{DD} = 5.25V, f_{CLK} = 50 MHz	25	**36**	mA (max)
		DV_{DD} = AV_{DD} = 5.25V, CLK Inactive (low)	14		mA
	Power Consumption	PD pin low	125	**190**	mW (max)
	Power Consumption	PD pin high	<5 mW		mW
CLK, PD DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Logical High Input Voltage			**2.0**	V (min)
V_{IL}	Logical Low Input Voltage			**0.8**	V (max)
I_{IH}	Logical High Input Current	V_{IH} = DV_{DD} = AV_{DD} = +5.25V		**±5**	µA (max)
I_{IL}	Logical Low Input Current	V_{IL} = 0V, DV_{DD} = AV_{DD} = +5.25V		**±5**	µA (max)
C_{IN}	Digital Input Capacitance		4		pF
DIGITAL OUTPUT CHARACTERISTICS					
I_{OH}	Output Current, Logic HIGH	DV_{DD} = 4.75V, V_{OH} = 4.0V		**−1.1**	mA (min)
I_{OL}	Output Current, Logic LOW	DV_{DD} = 4.75V, V_{OL} = 0.4V		**1.8**	mA (min)
I_{OZH}, I_{OZL}	TRI-STATE Output Current	DV_{DD} = 5.25V, PD = DV_{DD}, V_{OL} = DV_{DD}, or V_{OL} = 0V	±20		µA

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CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for AV_{DD} = DV_{DD} = +5.0 V_{DC}, PD = 0V, V_{RT} = +2.6V, V_{RB} = 0.6V, C_L = 20 pF, f_{CLK} = 50 MHz at 50% duty cycle. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**; all other limits T_A = 25°C (1)(2).

Symbol	Parameter	Conditions	Typical(3)	Limits(3)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS					
f_{C1}	Maximum Conversion Rate		55	**50**	MHz (min)
f_{C2}	Minimum Conversion Rate		1		MHz
t_{OD}	Output Delay	CLK high to data valid	14	**5**	ns (min)
				20	ns (max)
	Pipeline Delay (Latency)		2.5		Clock Cycles
t_{DS}	Sampling (Aperture) Delay	CLK low to acquisition of data	3		ns
t_{AJ}	Aperture Jitter		10		ps rms
t_{OH}	Output Hold Time	CLK high to data invalid	10		ns
t_{EN}	PD Low to Data Valid	Loaded as in Figure 16	140		ns

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TYPICAL PERFORMANCE CHARACTERISTICS

AV_{DD} = DV_{DD} = 5V, f_{CLK} = 50 MHz, unless otherwise stated.

INL Plot

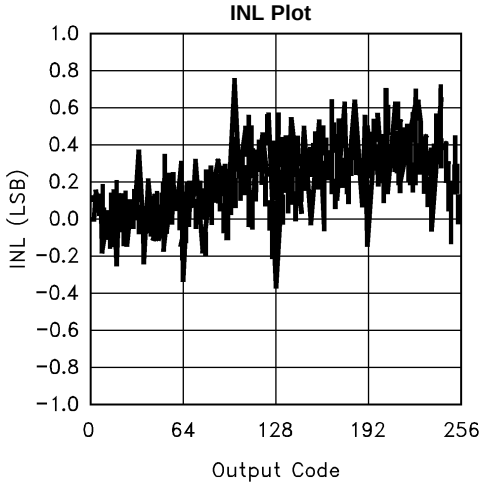

Figure 3.

DNL Plot

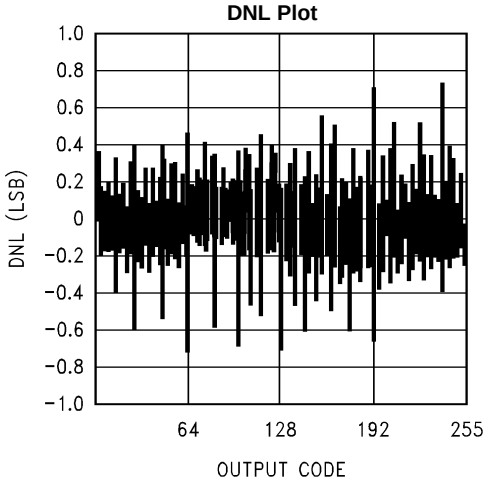

Figure 4.

INL vs. Temperature

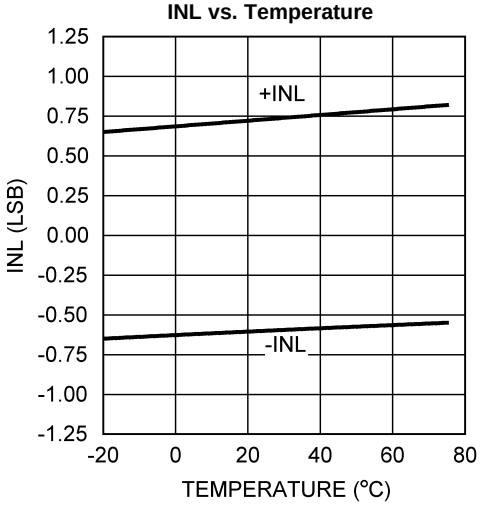

Figure 5.

DNL vs. Temperature

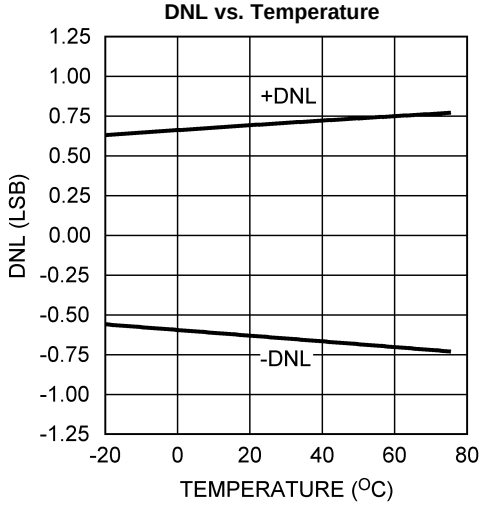

Figure 6.

SNR vs. Temp & f_{IN}

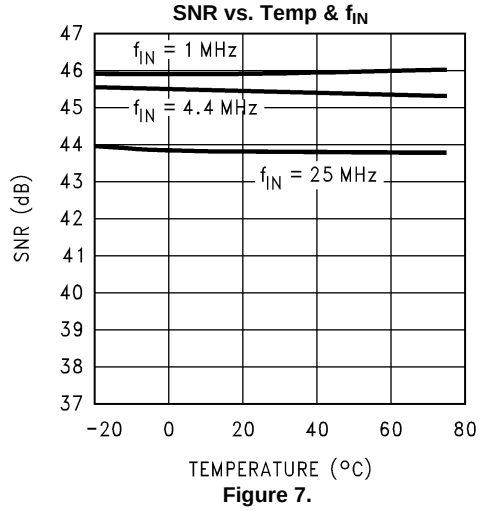

Figure 7.

THD vs. Temp & f_{IN}

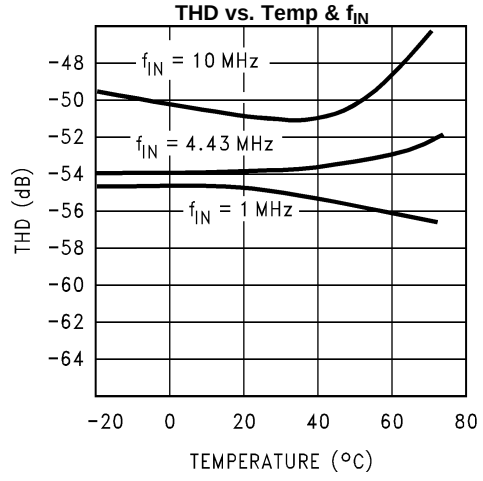

Figure 8.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

AV_{DD} = DV_{DD} = 5V, f_{CLK} = 50 MHz, unless otherwise stated.

SINAD & ENOB vs. Temp & f_{IN}

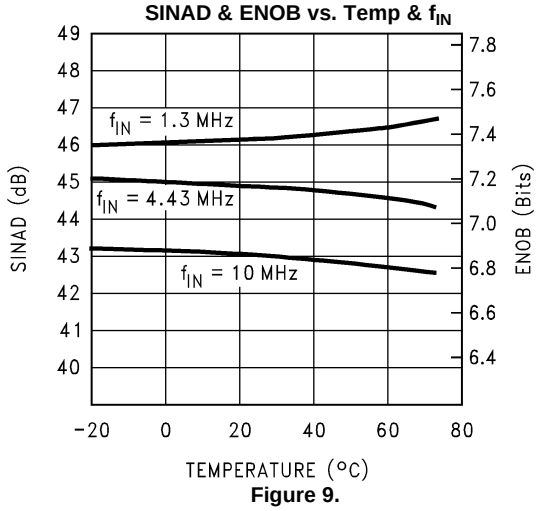

Figure 9.

SINAD & ENOB vs. Clock Duty Cycle

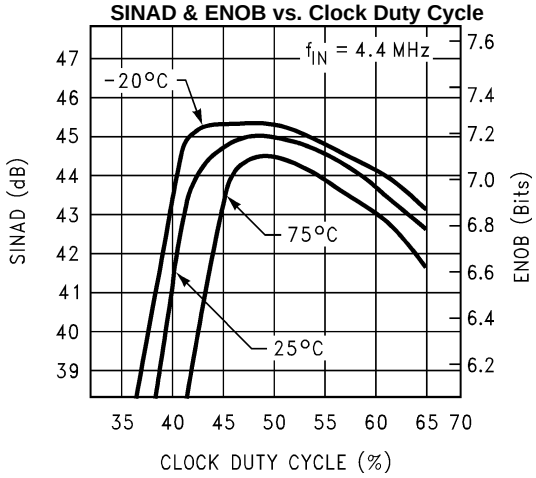

Figure 10.

SFDR vs. Temp & f_{IN}

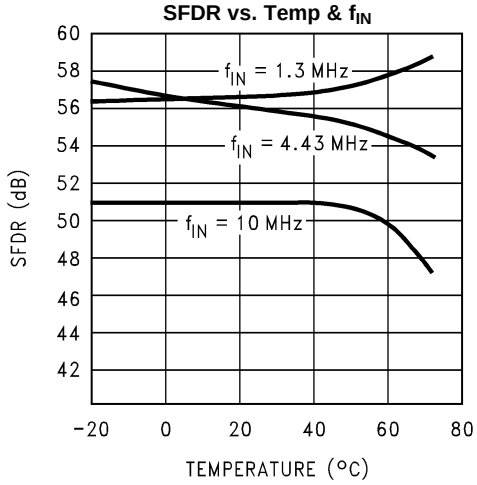

Figure 11.

t_{OD} vs. Temperature

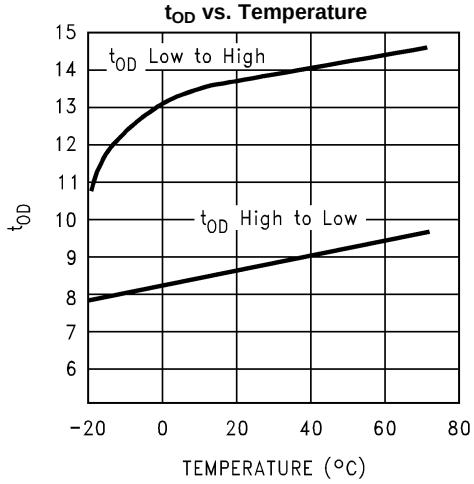

Figure 12.

Power Supply Current vs. f_{CLK}

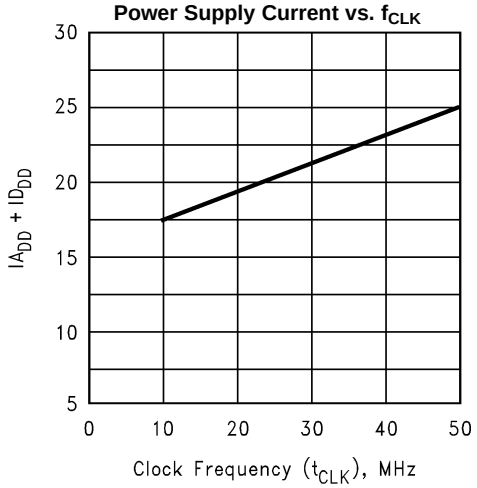

Figure 13.

Spectral Response

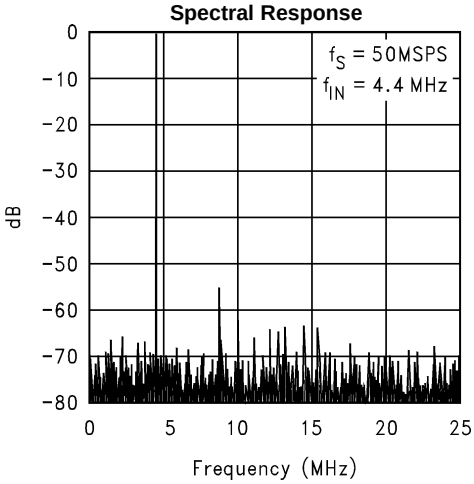

Figure 14.

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SPECIFICATION DEFINITIONS

ANALOG INPUT BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integer multiples of f_{CLK}. The input frequency at which the output is −3 dB relative to the low frequency input signal is the full power bandwidth.

APERTURE JITTER is the time uncertainty of the sampling point (t_{DS}), or the range of variation in the sampling delay.

BOTTOM OFFSET is the difference between the input voltage that just causes the output code to transition to the first code and the negative reference voltage. Bottom Offset is defined as $E_{OB} = V_{ZT} - V_{RB}$, where V_{ZT} is the first code transition input voltage. Note that this is different from the normal Zero Scale Error.

DIFFERENTIAL GAIN ERROR is the percentage difference between the output amplitudes of a high frequency reconstructed sine wave at two different d.c. levels.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. DNL is measured at the rated clock frequency with a ramp input.

DIFFERENTIAL PHASE ERROR is the difference in the output phase of a reconstructed small signal sine wave at two different d.c. levels.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual codes from a line drawn from zero scale (1/2 LSB below the first code transition) through positive full scale (1/2 LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. INL is measured at rated clock frequency with a ramp input.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output stage. Data for any given sample is available the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

SAMPLING (APERTURE) DELAY, or t_{DS}, is the time required after the falling edge of the clock for the sampling switch to open (in other words, for the Sample/Hold circuit to go from the “sample” mode into the “hold” mode). The Sample/Hold circuit effectively stops capturing the input signal and goes into the “hold” mode t_{DS} after the clock goes low.

SIGNAL TO NOISE RATIO (SNR) is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOP OFFSET is the difference between the positive reference voltage and the input voltage that just causes the output code to transition to full scale and is defined as $E_{OT} = V_{FT} - V_{RT}$. Where V_{FT} is the full scale transition input voltage. Note that this is different from the normal Full Scale Error.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first six harmonic components to the rms value of the input signal.

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Timing Diagram

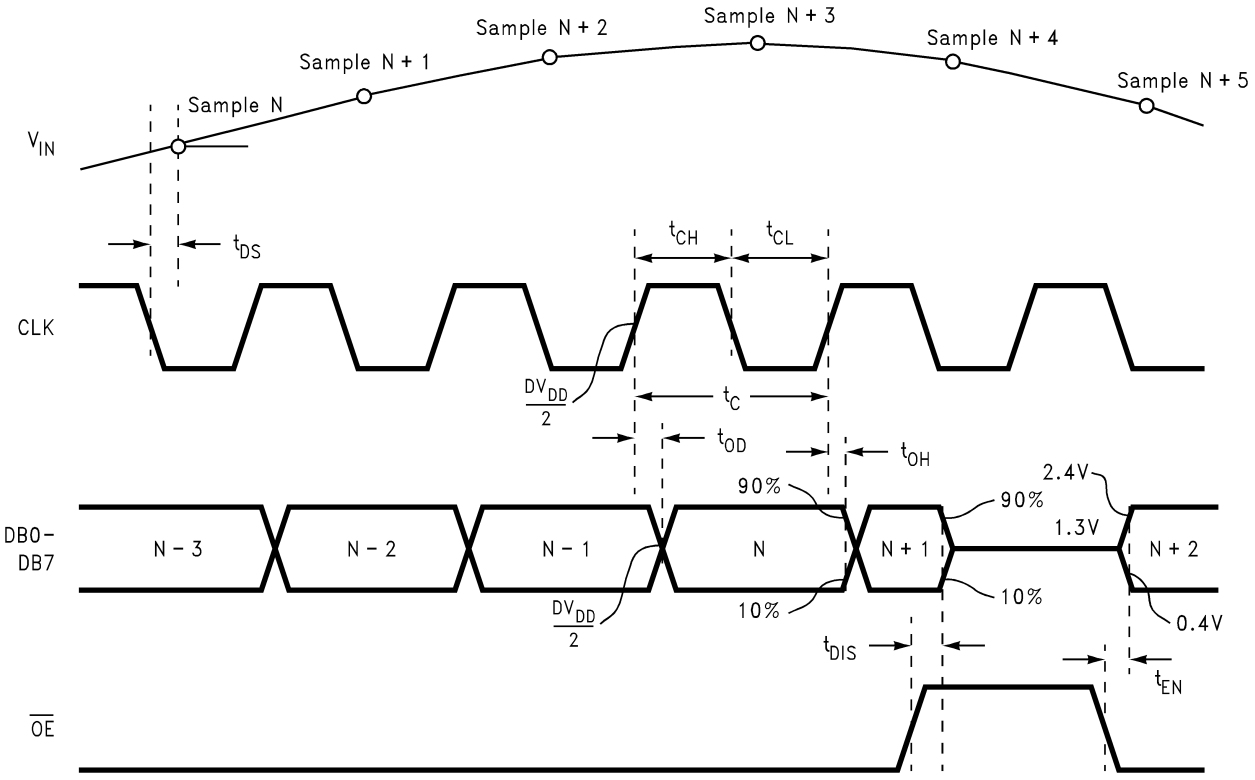

Figure 15. ADC1175-50 Timing Diagram

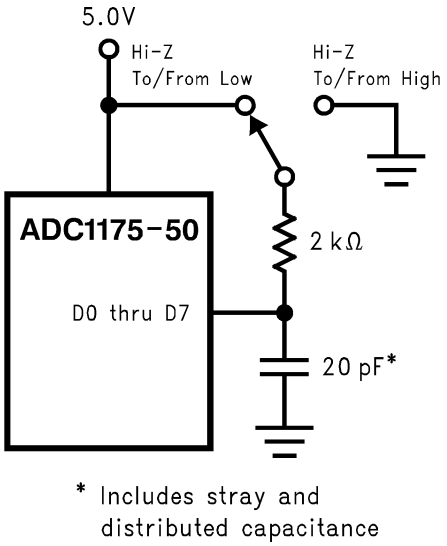

Figure 16. t_{EN}, t_{DIS} Test Circuit

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FUNCTIONAL DESCRIPTION

The ADC1175-50 maintains superior dynamic performance with input frequencies up to 1/2 the clock frequency, achieving 6.8 effective bits with a 50 MHz sampling rate and 25 MHz input frequency.

The analog signal at V_{IN} that is within the voltage range set by V_{RT} and V_{RB} are digitized to eight bits at up to 55 MSPS. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RT} will cause the output word to consist of all ones. While the ADC1175-50 is specified for top and bottom reference voltages (V_{RT} and V_{RB}) or 2.6V and 0.6V, respectively, and will give best performance at these values, V_{RT} has a range of 1.0V to the analog supply voltage, AV_{DD}, while V_{RB} has a range of 0V to 4.0V. V_{RT} should always be at least 1.0V more positive than V_{RB}. With V_{RT} voltages above 2.8V, it is necessary to reduce the clock frequency to maintain SINAD performance. V_{RT} should always be between 1.0V and 2.8V more positive than V_{RB}.

If V_{RT} and V_{RTS} are connected together and V_{RB} and V_{RBS} are connected together, the nominal values of V_{RT} and V_{RB} are 2.6V and 0.6V, respectively. If V_{RT} and V_{RTS} are connected together and V_{RB} is grounded, the nominal value of V_{RT} is 2.3V.

Data is acquired at the falling edge of the clock and the digital equivalent of that data is available at the digital outputs 2.5 clock cycles plus t_{OD} later. The ADC1175-50 will convert as long as the clock signal is present at the CLK pin. The PD pin, when high, puts the device into the Power Down mode. When the PD pin is low, the device is in the normal operating mode.

The Power Down pin (PD), when high, puts the ADC1175-50 into a power down mode where power consumption is typically less than 5 mW. When the part is powered down, the digital output pins are in a high impedance TRI-STATE. It takes about 140 ns for the part to become active upon coming out of the power down mode.

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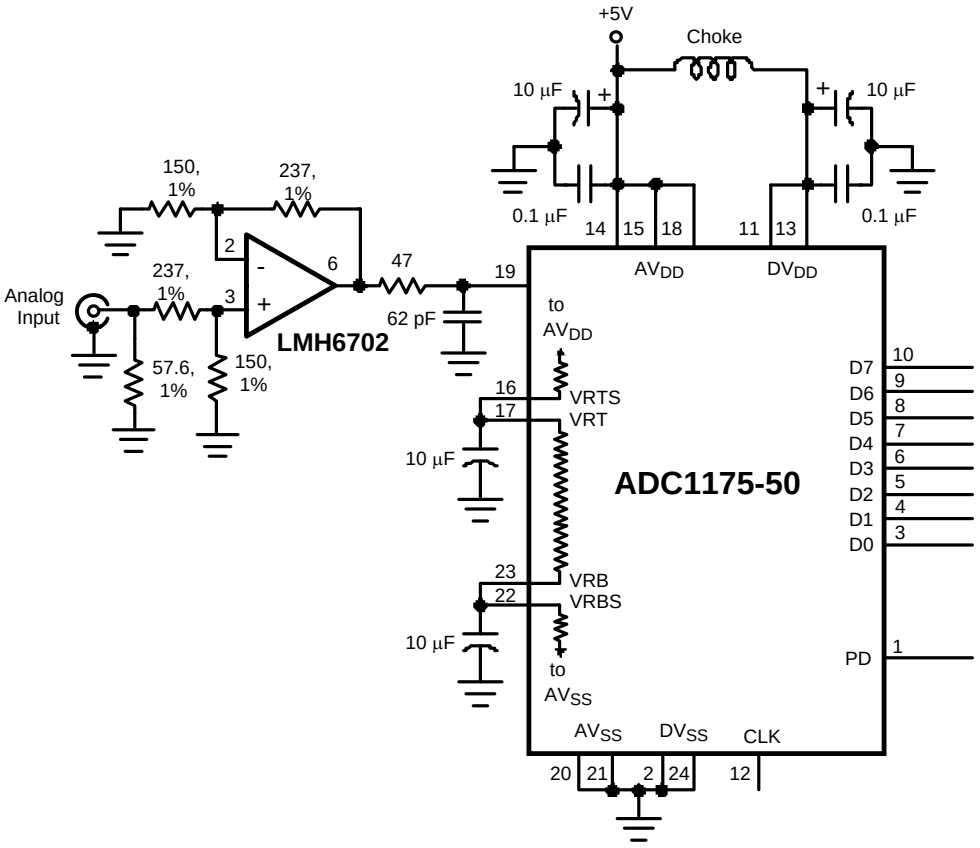
APPLICATIONS INFORMATION

(All Schematic pin numbers refer to the TSSOP.)

THE ANALOG INPUT

The analog input of the ADC1175-50 is a switch followed by an integrator. That is, a switched capacitor input, appearing as 4 pF when the clock is low, and 7 pF when the clock is high. Switched capacitor inputs produce voltage spikes at the input pin at the ADC sample rate. There should be no attempt to eliminate these spikes, but they should settle out during the sample period (the clock high time). An RC at the ADC analog input pin, as shown in Figure 17, will help. For Nyquist applications, the capacitor should be about 10 times ADC track mode input capacitance and the pole frequency of this RC should be about the ADC sample rate. The LMH6702, and the LMH6609 have been found to be excellent amplifiers for driving the ADC1175-50. Do not drive the input beyond the supply rails. Figure 17 shows an example of an input circuit using the LMH6702.

Driving the analog input with input signals up to 2.8 V_{P-P} will result in normal behavior where signals above V_{RT} will result in a code of FFh and input voltages below V_{RB} will result in an output code of zero. Input signals above 2.8 V_{P-P} may result in odd behavior where the output code is not FFh when the input exceeds V_{RT}.



Choose an op-amp that can drive a dynamic capacitance.

Figure 17. Driving the ADC1175-50

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REFERENCE INPUTS

The reference inputs V_{RT} (Reference Top) and V_{RB} (Reference Bottom) are the top and bottom of the reference ladder. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in the Operating Ratings section (1.0V to AV_{DD} for V_{RT} and 0V to (AV_{DD} − 1.0V) for V_{RB}). Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin.

The reference ladder can be self-biased by connecting V_{RT} to V_{RTS} and connecting the V_{RB} to V_{RBS} to provide top and bottom reference voltages of approximately 2.6V and 0.6V, respectively, with V_{CC} = 5.0V. This connection is shown in Figure 17. If V_{RT} and V_{RTS} are tied together, but V_{RB} is tied to analog ground, a top reference voltage of approximately 2.3V is generated. The top and bottom of the ladder should be bypassed with 10 µF tantalum capacitors located close to the reference pins.

The reference self-bias circuit of Figure 17 is very simple and performance is adequate for many applications. Better linearity performance can generally be achieved by driving the reference pins with a low impedance source.

By forcing a little current into or out of the top and bottom of the ladder, as shown in Figure 18, the top and bottom reference voltages can be trimmed and performance improved over the self-bias method of Figure 17. The resistive divider at the amplifier inputs can be replaced with potentiometers, if desired. The LMC662 amplifier shown was chosen for its low offset voltage and low cost. Note that a negative power supply is needed for these amplifiers if the lower one is required to go slightly negative to force the required reference voltage.

If reference voltages are desired that are more than a few tens of millivolts from the self-bias values, the circuit of Figure 19 will allow forcing the reference voltages to whatever levels are desired. This circuit provides the best performance because of the low source impedance of the transistors. Note that the V_{RTS} and V_{RBS} pins are left floating.

To minimize noise effects and ensure accurate conversions, the total reference voltage range (V_{RT} − V_{RB}) should be a minimum of 1.0V and a maximum of about 2.8V.

The ADC1175-50 is designed to operate with top and bottom references of 2.6V and 0.6V, respectively. However, it will function with reduced performance with a top reference voltage as high as AV_{DD} and a bottom reference voltage as low as ground.

If reference voltages are desired that are more than a few tens of millivolts from the self-bias values, the circuit of Figure 19 will allow forcing the reference voltages to whatever levels are desired. This circuit provides the best performance because of the low source impedance of the transistors. Note that the V_{RTS} and V_{RBS} pins are left floating.

V_{RT} can be anywhere between V_{RB} + 1.0V and the analog supply voltage, and V_{RB} can be anywhere between ground and 1.0V below V_{RT}. To minimize noise effects and ensure accurate conversions, the total reference voltage range (V_{RT} - V_{RB}) should be a minimum of 1.0V and a maximum of about 2.8V. If V_{RB} is not required to be below about +700mV, the -5V points in Figure 19 can be returned to ground and the negative supply eliminated.

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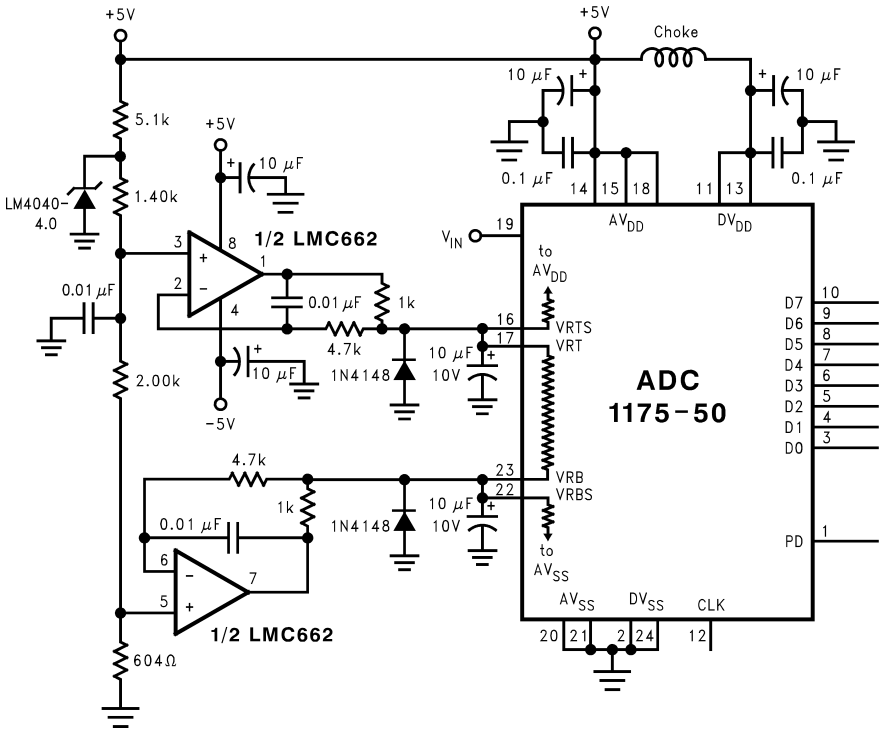
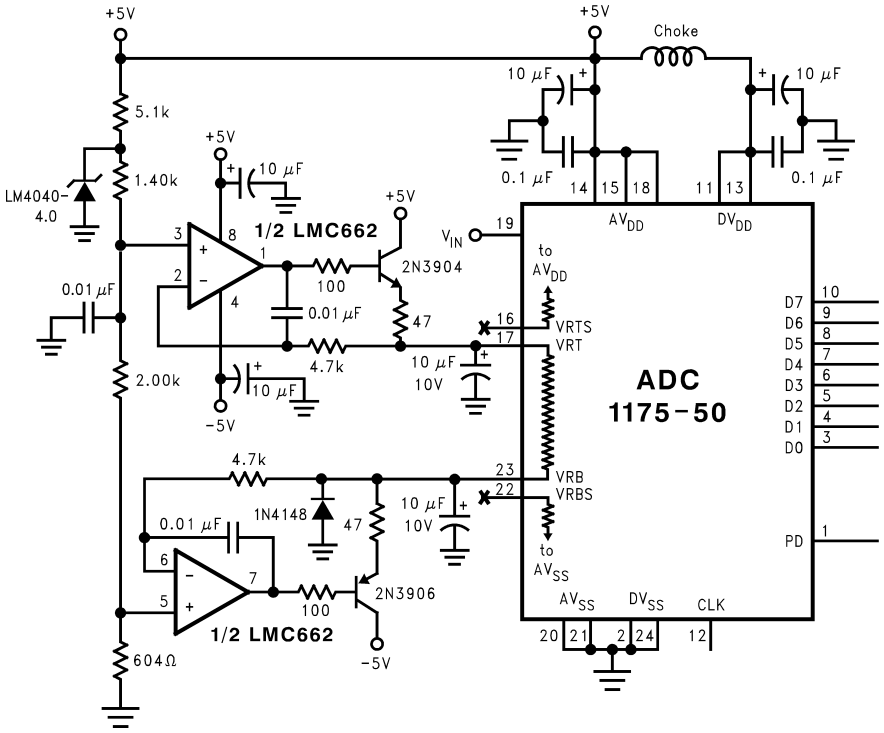


Self bias is still used, but the reference voltages are trimmed by providing a small trim current with the operational amplifiers.

Figure 18. Better Defining the ADC Reference Voltage.



Requires driving with a low impedance source, provided by the transistors. Note that pins 16 and 22 are not connected.

Figure 19. Driving the Reference to Force Desired Values

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OUTPUT DATA TIMING

The Output Delay (t_{OD}) of the ADC1175-50 can be very close to one half clock cycle. Because of this, the output data transition occurs very near the falling edge of the ADC clock. To avoid clocking errors, you should use the *rising* edge of the ADC clock to latch the output data of the ADC1175-50 and *not* use the falling edge.

POWER SUPPLY CONSIDERATIONS

Many A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 µF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 centimeters) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed as close as possible to the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source should be used for the analog and digital supplies of the ADC1175-50, these supply pins should be isolated from each other to prevent any digital noise from being coupled to the analog power pins. We recommended a wide band choke, such as the JW Miller FB20010-3B, be used between the analog and digital supply lines, with a ceramic capacitor close to the analog supply pin. If a resistor is used in place of the choke, a maximum of 10Ω should be used.

The converter digital supply should *not* be the supply that is used for other digital circuitry on the board. It should be the same supply used for the A/D analog supply.

As with all high speed converters, the ADC1175-50 should be assumed to have little a.c. power supply rejection, especially when self biasing is used by connecting V_{RT} and V_{RTS} together.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground, not even on a transient basis. This can be a problem upon application of power to a circuit. Be sure that the supplies to circuits driving the CLK, PD, analog input and reference pins do not come up any faster than does the voltage at the ADC1175-50 power pins.

Pins 11 and 13 are both labeled DV_{DD}. Pin 11 is the supply point for the digital core of the ADC, where pin 13 is used only to provide power to the ADC output drivers. As such, pin 11 may be connected to a voltage source that is less than the +5V used for AV_{DD} and DV_{DD} to ease interfacing to low voltage devices. Pin 11 should never exceed the pin 13 potential by more than 0.5V.

THE ADC1175-50 CLOCK

Although the ADC1175-50 is tested and its performance is ensured with a 50 MHz clock, it typically will function with clock frequencies from 1 MHz to 55 MHz.

The clock should be one of low jitter and close to 50% duty cycle.

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals is essential to ensure accurate conversion. Separate analog and digital ground planes that are connected beneath the ADC1175-50 may be used, but best EMI practices require a single ground plane. However, it is important to keep analog signal lines away from digital signal lines and away from power supply currents. This latter requirement requires the careful separation and placement of power planes. The use of power traces rather than one or more power planes is not recommended as higher frequencies are not well filtered with lumped capacitances. To filter higher frequency noise components it is necessary to have sufficient capacitance between the power and ground planes.

If separate analog and digital ground planes are used, the analog and digital grounds may be in the same layer, but should be separated from each other. If separate analog and digital ground layers are used, they should *never overlap* each other.

Capacitive coupling between a typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

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Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS and the 74HC(T) families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F family. In general, slower logic families will produce less high frequency noise than do high speed logic families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by using a single, solid ground plane and splitting the power plane into analog and digital areas and to have power and ground planes in adjacent board layers. There should be no traces within either the power or the ground layers of the board. The analog and digital power planes should reside in the same board layer so that they can not overlap each other. The analog and digital power planes define the analog and digital areas of the board.

Mount digital components and run digital lines only in the digital areas of the board. Mount the analog components and run analog lines only in the analog areas of the board. Be sure to treat all digital lines greater that one inch for each nanosecond of rise time as transmission lines. That is, they should be of constant, controlled impedance, be properly terminated at the source end and run from one point to another single point.

The back of the WQFN package has a large metal area inside the area bounded by the pins. This metal area is connected to the die substrate (ground). This pad may be left floating if desired. If it is connected to anything, it should be to ground near the connection between analog and digital ground planes. Soldering this metal pad to ground will help keep the die cooler and could yield improved performance because of the lower impedance between die and board grounds. However, a poor layout could compromise performance.

Generally, analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies and at high resolution is obtained with a straight signal path.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side with each other, not even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground plane.

DYNAMIC PERFORMANCE

The ADC1175-50 is a.c. tested and its dynamic performance is ensured. To meet the published specifications, the clock source driving the CLK input must be free of jitter. For best a.c. performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 20.

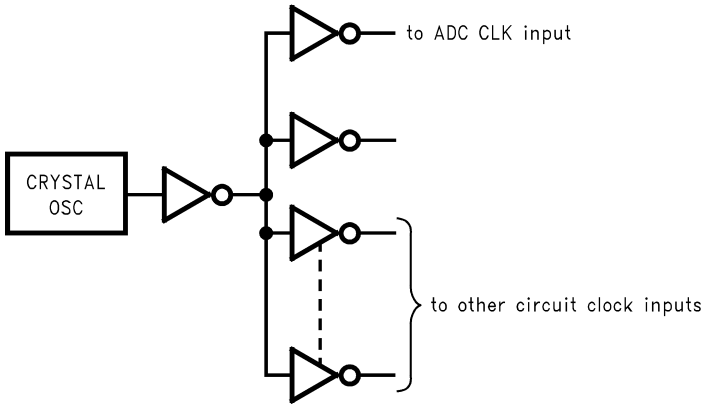

Figure 20. Isolating the ADC Clock from Digital Circuitry

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It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal.

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 50 mV below the ground pins or 50 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground due to improper termination. A resistor of about 50Ω to 100Ω in series with the offending digital input, located close to the signal source, will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC1175-50. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers have to charge for each conversion, the more instantaneous digital current is required from DV_{DD} and DGND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with a 74AC541, for example) may be necessary if the data bus to be driven is heavily loaded. Dynamic performance can also be improved by adding 47Ω series resistors at each digital output, reducing the energy coupled back into the converter output pins.

Using an inadequate amplifier to drive the analog input. As explained in Applications Information, the ADC input is a switched capacitor one and there are voltage spikes present there. This type if input is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device. The LMH6702 and the LMH6609 have been found to be an excellent device for driving the ADC1175-50. Also remember to use the RC between the driving source and the ADC input, as explained in THE ANALOG INPUT.

Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in REFERENCE INPUTS, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. Simple gates with RC timing is generally inadequate as a clock source.

Input test signal contains harmonic distortion that interferes with the measurement of dynamic signal to noise ratio. Harmonic and other interfering signals can be removed by inserting a filter at the signal input. Suitable filters are shown in Figure 21 and Figure 22. The circuit of Figure 21 has a cutoff of about 5.5 MHz and is suitable for input frequencies of 1 MHz to 5 MHz. The circuit of Figure 22 has a cutoff of about 11 MHz and is suitable for input frequencies of 5 MHz to 10 MHz. These filters should be driven by a generator of 75Ω source impedance and terminated with a 75Ω resistor.

Not considering the effect on a driven CMOS digital circuit(s) when the ADC1175-50 is in the power down mode. Because the ADC1175-50 output goes into a high impedance state when in the power down mode, any CMOS device connected to these outputs will have their inputs floating when the ADC is in power down. Should the inputs of the circuit being driven by the ADC digital outputs float to a level near 2.5V, a CMOS device could exhibit relative large supply currents as the input stage toggles rapidly. The solution is to use pull-down resistors at the ADC outputs. The value of these resistors is not critical, as long as they do not cause excessive currents in the outputs of the ADC1175-50. Low pull-down resistor values could result in degraded SNR and SINAD performance of the ADC1175-50. Values between 5 kΩ and 10 kΩ should work well.

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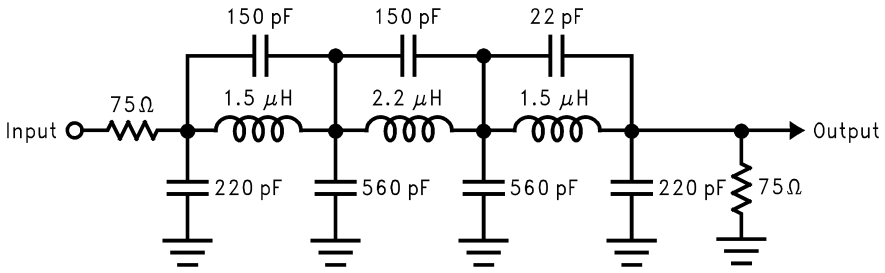
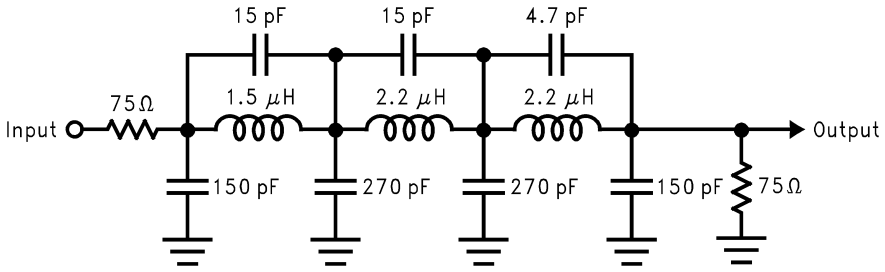


Use with maximum input frequencies of 1 MHz to 5 MHz.

Figure 21. A 5.5 MHz Low Pass filter to eliminate harmonics at the signal input



Use with maximum input frequencies of 5 MHz to 10 MHz.

Figure 22. An 11 MHz Low Pass filter to eliminate harmonics at the signal input

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REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	20

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC1175-50CIMTX/NOPB	ACTIVE	TSSOP	PW	24	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 75	ADC1175-50 CIMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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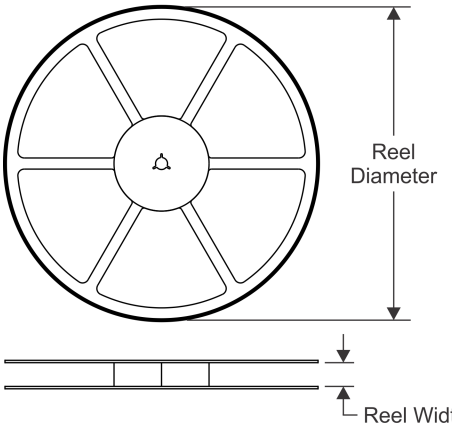
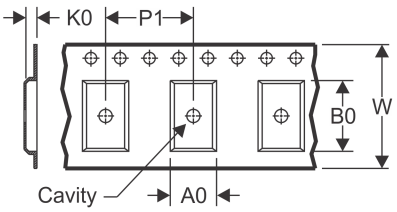
TAPE AND REEL INFORMATION

REEL DIMENSIONS

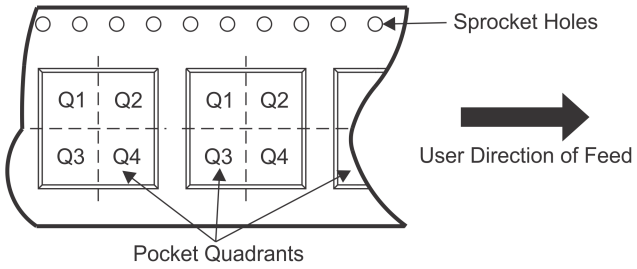


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

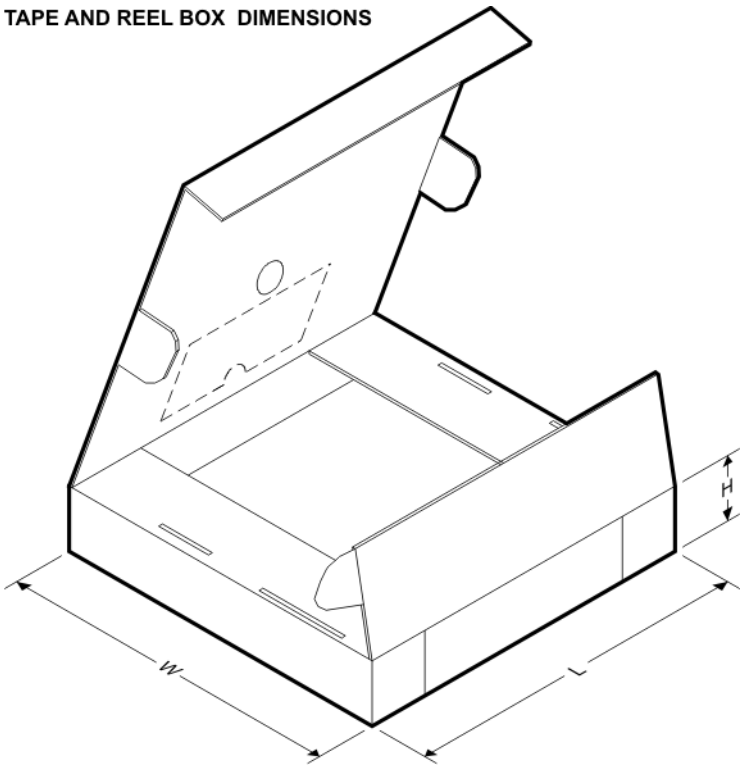
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC1175-50CIMTX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

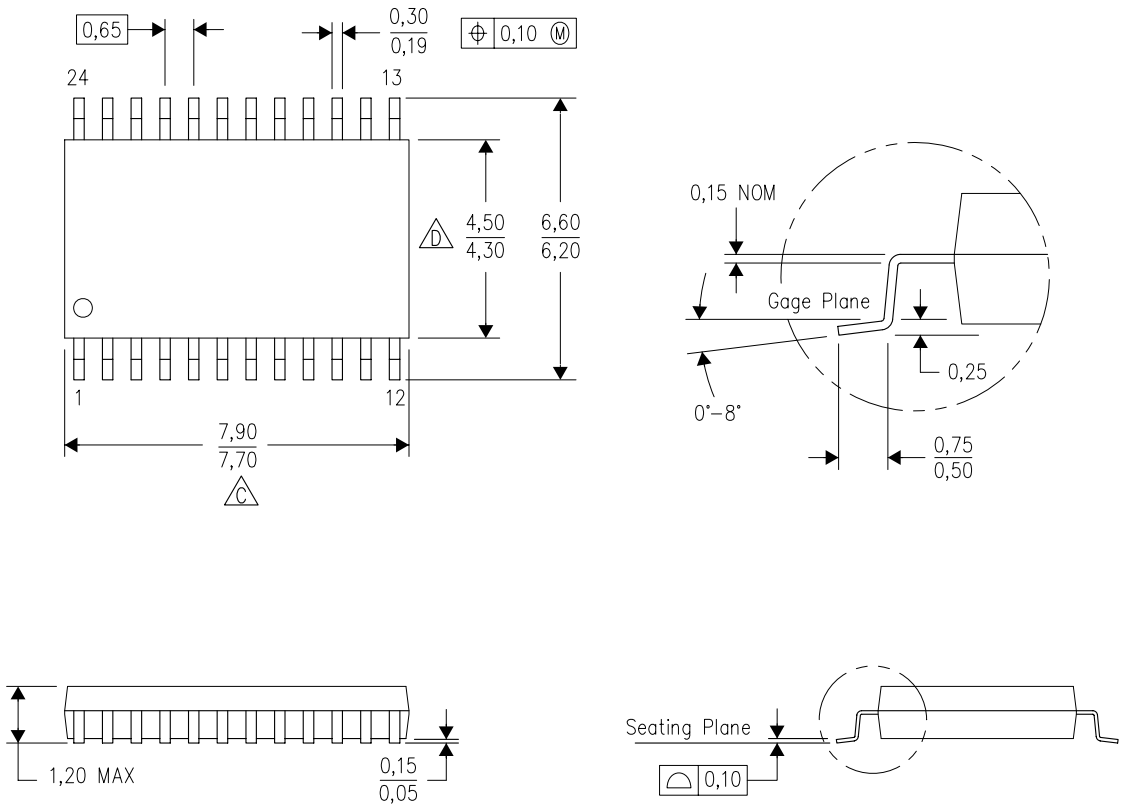
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC1175-50CIMTX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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