ADC10662/ADC10664 10-Bit 360 ns A/D Converter with Input Multiplexer and Sample/Hold

Check for Samples: ADC10662, ADC10664

FEATURES

- **Built-In Sample-and-Hold**
- **Single +5V Supply**
- **No External Clock Required**
- **Speed Adjust Pin for Faster Conversions**

APPLICATIONS

- **Digital Signal Processor Front Ends**
- **Instrumentation**
- **Disk Drives**
- **Mobile Telecommunications**

KEY SPECIFICATIONS

- **Conversion Time 360 ns (Typical)**
- **Max. Sampling Rate: 1.5 MHz (Min)**
- **Low Power Consumption 235 mW (Max)**
- **Total Harmonic Distortion (50 kHz): −60 dB (Max)**
- **No Missing Codes Over Temperature**

DESCRIPTION

NOTE: The ADC10662 is obsolete. It is described here for reference only.

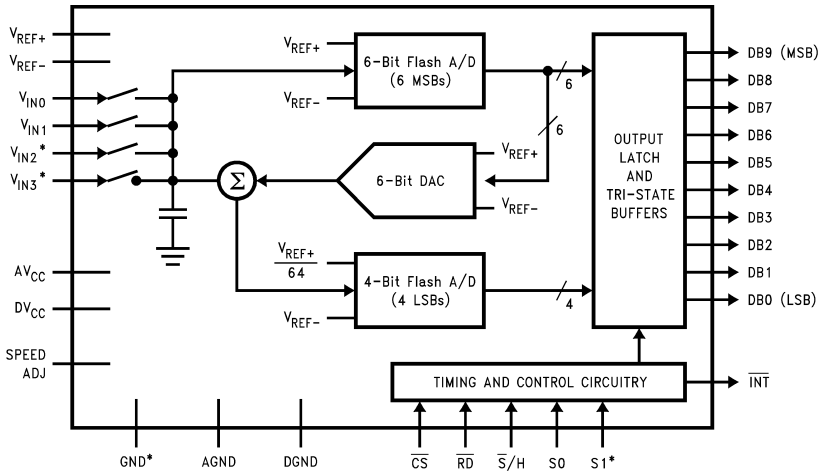
Using an innovative, patented multistep (U.S. Patent Number 4918449) conversion technique, these 10-bit CMOS analog-to-digital converters offer sub-microsecond conversion times yet dissipating a maximum of only 235 mW. These converters perform 10-bit conversions in two lower-resolution “flashes”, yielding a fast A/D without the cost, power consumption, and other problems associated with true flash approaches. In addition to standard static performance specifications (Linearity, Full-Scale Error, etc.), dynamic performance (THD, S/N) is ensured.

The analog input voltage ADC is sampled and held by an internal sampling circuit. Input signals at frequencies from DC to over 250 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

Connecting an external resistor between the “speed-up” pin and ground reduces the typical conversion time to as little as 360 ns for a small linearity sacrifice.

For ease of interface to microprocessors, the ADC10662 and ADC10664 have been designed to appear as a memory location or I/O port without the need for external interface logic.

Simplified Block Diagram



*ADC10664 Only

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Connection Diagram

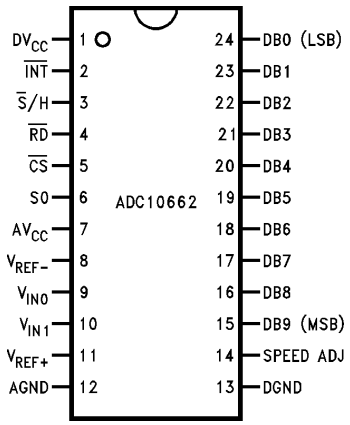


Figure 1. Top View

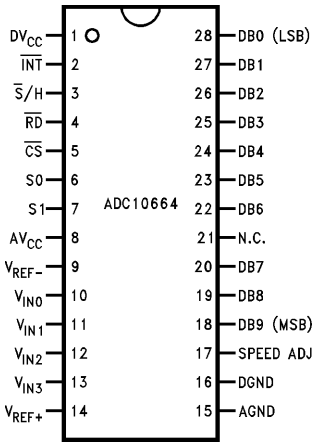


Figure 2. Top View

NOTE: The ADC10662 is obsolete; shown for reference only.

PIN DESCRIPTIONS

Pin Function	Description
DV_{CC}, AV_{CC}	Digital and analog positive supply voltage inputs. Connect both to the same voltage source, but bypass separately with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor to ground at each pin.
$\overline{INT}$	Active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns high following the rising edge of $\overline{RD}$.
$\overline{S}$/H	Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), the analog input signal to be sampled and initiates a new conversion.
$\overline{RD}$	Active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.
$\overline{CS}$	Active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}$/H pins.
S0, S1	These pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}$/H makes its High-to-Low transition (See Timing Diagrams). The ADC10664 includes both S0 and S1. The ADC10662 includes just S0.
V_{REF-}, V_{REF+}	Reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to (V_{REF+} − 1 LSB) produces an output code of 1023.
V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3}	Analog input pins. The ADC10662 has two inputs (V_{IN0} and V_{IN1}) and the ADC10664 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.
GND, AGND, DGND	Power supply ground pins. The ADC10662 and ADC10664 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. Both pins should be returned to the same potential.
DB0–DB9	TRI-STATE output pins.
SPEEDADJ	By connecting a resistor between this pin and ground, the conversion time can be reduced. The specifications listed in the table of Electrical Characteristics apply for a speed adjust resistor (R_{SA}) equal to 14.0 kΩ (Mode 1) or 8.26 kΩ (Mode 2). See Typical Performance Characteristics and the table of Electrical Characteristics.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2][3]

Supply Voltage ($V^+ = AV_{CC} = DV_{CC}$)			−0.3V to +6V
Voltage at Any Input or Output			−0.3V to V^+ + 0.3V
Input Current at Any Pin[4]			5 mA
Package Input Current[4]			20 mA
Power Dissipation[5]			875 mW
ESD Susceptibility[6]			2000V
Soldering Information	N Package (10 Sec)		260°C
	SOIC Package	Vapor Phase (60 Sec)	215°C
		Infrared (15 Sec)	220°C
Storage Temperature Range			−65°C to +150°C
Junction Temperature			150°C

(1) All voltages are measured with respect to GND, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not ensure specific performance limits, however. For ensured specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V^+) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. In most cases, the maximum derated power dissipation will be reached only during fault conditions. For these devices, T_{JMAX} for a board-mounted device can be found in Package Thermal Resistance.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Ratings[1][2]

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$ = −40°C ≤ T_A ≤ +85°C
Supply Voltage Range	+4.5V to +5.5V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not ensure specific performance limits, however. For ensured specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise specified.

Package Thermal Resistance

Device	θ_{JA} (°C/W)
ADC10662CIWM	82
ADC10664CIWM	78

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Converter Characteristics

The following specifications apply for V^+ = +5V, $V_{REF(+)}$ = +5V, $V_{REF(-)}$ = GND, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{Min} to T_{Max};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units (Limit)
	Resolution			**10**	Bits
	Integral Linearity Error		±0.5	±1.0/**±1.5**	LSB (max)
	Offset Error			**±1.5**	LSB (max)
	Full-Scale Error			**±1**	LSB (max)
	Total Unadjusted Error		±0.5	±1.5/**±2.2**	LSB
	Missing Codes			**0**	(max)
	Power Supply Sensitivity	V^+ = 5V ±5%, V_{REF} = 4.5V	±1/16		LSB
		V^+ = 5V ±10%, V_{REF} = 4.5V	±⅛		LSB
THD	Total Harmonic Distortion (3)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P} f_{IN} = 240 kHz, 4.85 V_{P-P}	**−68** **−66** **−62** **−58**	**−60**	dB dB (max) dB dB
SNR	Signal-to-Noise Ratio (3)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P}	**61** **60** **60**	**58**	dB dB (min) dB
ENOB	Effective Number of Bits (3)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P}	**9.6** **9.5**	**9**	Bits Bits (min)
R_{REF}	Reference Resistance		650	**400** **900**	Ω (min) Ω (max)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**V^+ + 0.05**	V (max)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**GND − 0.05**	V (min)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**$V_{REF(-)}$**	V (min)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**$V_{REF(+)}$**	V (max)
V_{IN}	Input Voltage			**V^+ + 0.05**	V (max)
V_{IN}	Input Voltage			**GND − 0.05**	V (min)
	OFF Channel Input Leakage Current	$\overline{CS}$ = V^+, V_{IN} = V^+	0.01	**3**	µA (max)
	ON Channel Input Leakage Current	$\overline{CS}$ = V^+, V_{IN} = V^+	±1	**−3**	µA (max)

(1) Typical figures represent most likely parametric norm.
(2) Tested limits are ensured to AOQL (Average Outgoing Quality Level).
(3) THD, SNR, and ENOB are tested in Mode 1. Measuring these quantities in Mode 2 yields similar values.

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DC Electrical Characteristics

The following specifications apply for V^+ = +5V, $V_{REF(+)}$ = 5V $V_{REF(-)}$ = GND, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = +25°C.

Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage	V^+ = 5.5V		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V^+ = 4.5V		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN(1)}$ = 5V	0.005	**3.0**	µA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN(0)}$ 0V	−0.005	**−3.0**	µA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	V^+ = 4.5V, I_{OUT} = −360 µA V^+ = 4.5V, I_{OUT} = −10 µA		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V^+ = 4.5V, I_{OUT} = 1.6 mA		**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 5V V_{OUT} = 0V	0.1 −0.1	**50** **−50**	µA (max) µA (max)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS}$ = $\overline{S}$/H = $\overline{RD}$ = 0	1.0	**2**	mA (max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS}$ = $\overline{S}$/H = $\overline{RD}$ = 0	30	**45**	mA (max)

(1) Typical figures represent most likely parametric norm.
(2) Tested limits are ensured to AOQL (Average Outgoing Quality Level).

AC Electrical Characteristics

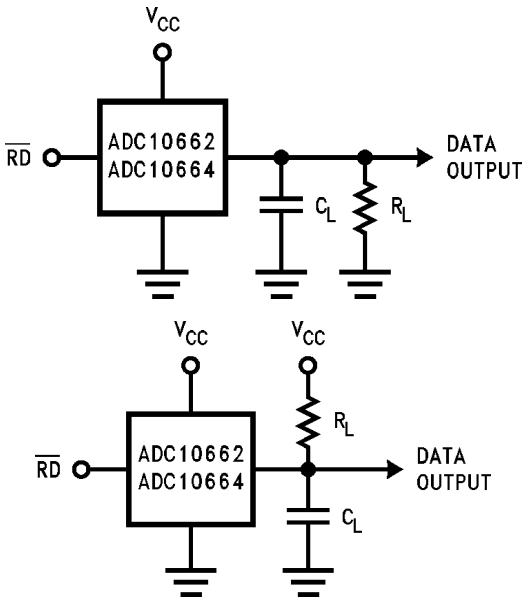
The following specifications apply for V^+ = +5V, $t_r = t_f$ = 20 ns, $V_{REF(+)}$ = 5V, $V_{REF(-)}$ = GND, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = +25°C.

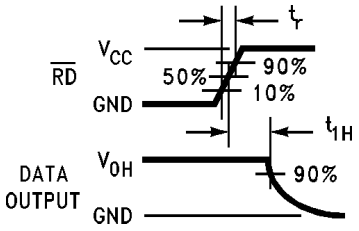
Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units (Limits)
t_{CONV}	Mode 1 Conversion Time from Rising Edge of $\overline{S}$/H to Falling Edge of $\overline{INT}$		360	**466**	ns (max)
t_{CRD}	Mode 2 Conversion Time		470	**610**	ns (max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 1; C_L = 100 pF	30	**50**	ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 2; C_L = 100 pF	475	**616**	ns (max)
t_{SH}	Minimum Sample Time	Mode 1 (Figure 3) (3)		**150**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to High-Z State)	R_L = 1k, C_L = 10 pF	30	**60**	ns (max)
t_{INTH}	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	C_L = 100 pF	25	**50**	ns (max)
t_P	Delay from End of Conversion to Next Conversion			**50**	ns (max)
t_{MS}	Multiplexer Control Setup Time		10	**75**	ns (max)
t_{MH}	Multiplexer Hold Time		10	**40**	ns (max)
C_{VIN}	Analog Input Capacitance		35		pF (max)
C_{OUT}	Logic Output Capacitance		5		pF (max)
C_{IN}	Logic Input Capacitance		5		pF (max)

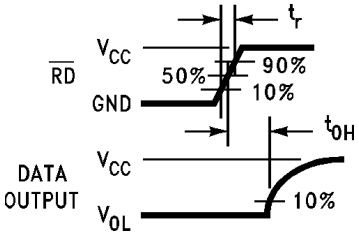
(1) Typical figures represent most likely parametric norm.
(2) Tested limits are ensured to AOQL (Average Outgoing Quality Level).
(3) Accuracy may degrade if t_{SH} is shorter than the value specified. See curves of Accuracy vs. t_{SH}.

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TRI-STATE Test Circuits and Waveforms

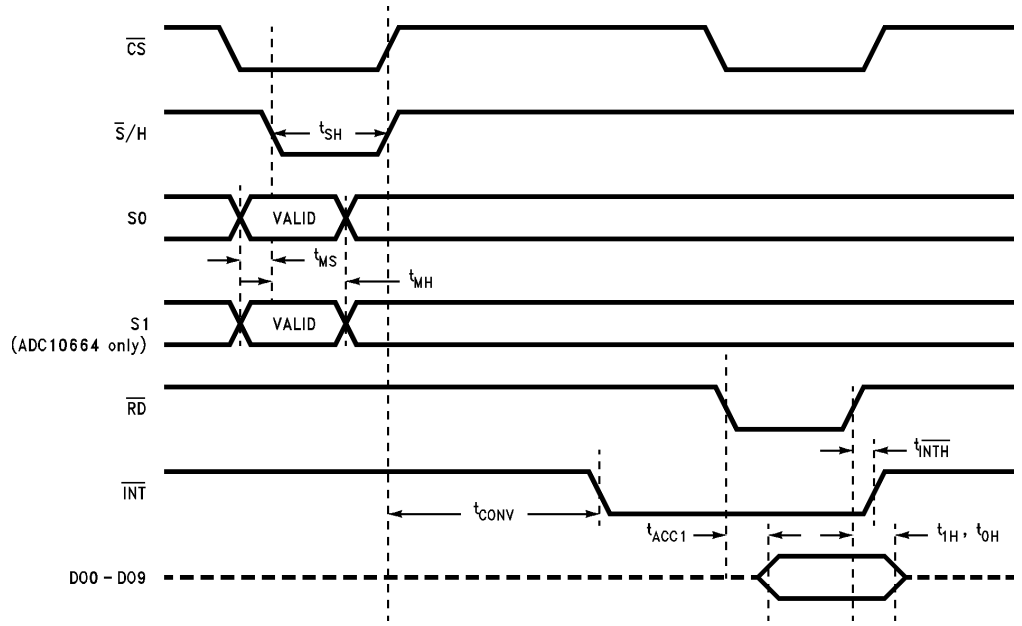






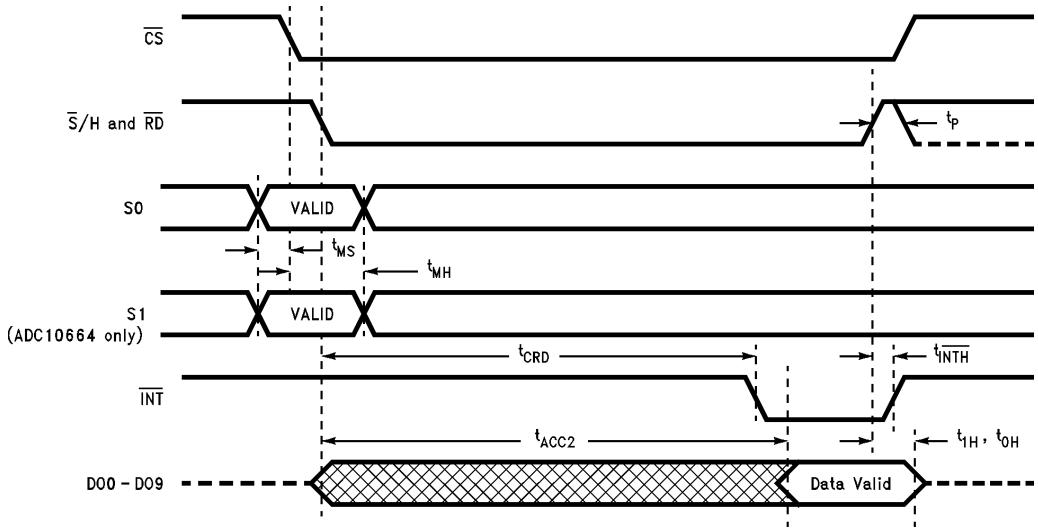
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Timing Diagrams



The conversion time (t_{CONV}) is set by the internal timer.

Figure 3. Mode 1



The conversion time (t_{CRD}) includes the sampling time and is determined by the internal timer.

Figure 4. Mode 2 ($\overline{RD}$ Mode)

Typical Performance Characteristics

Zero (Offset) Error vs. Reference Voltage

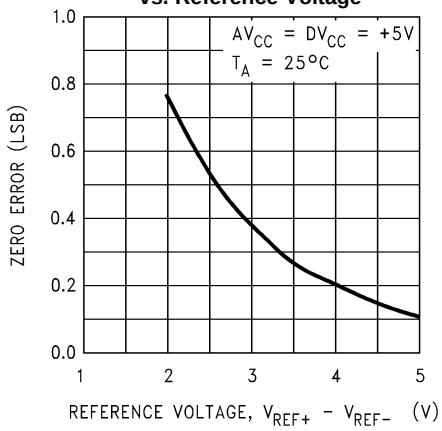


Figure 5.

Linearity Error vs. Reference Voltage

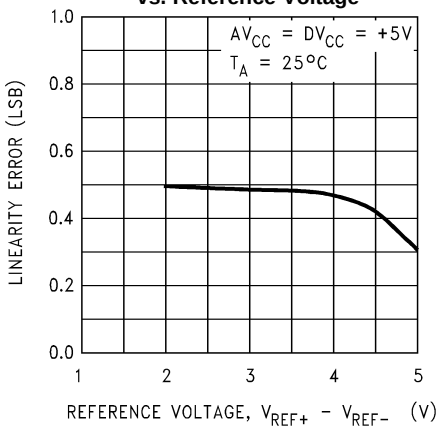


Figure 6.

Analog Supply Current vs. Temperature

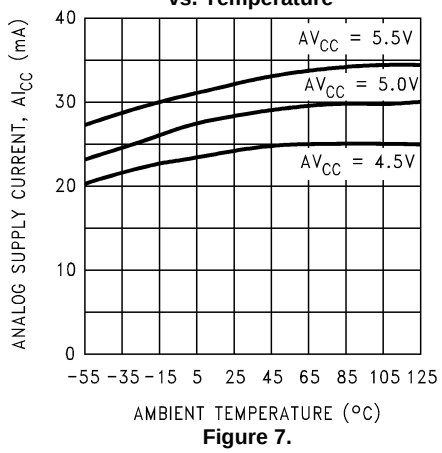


Figure 7.

Digital Supply Current vs. Temperature

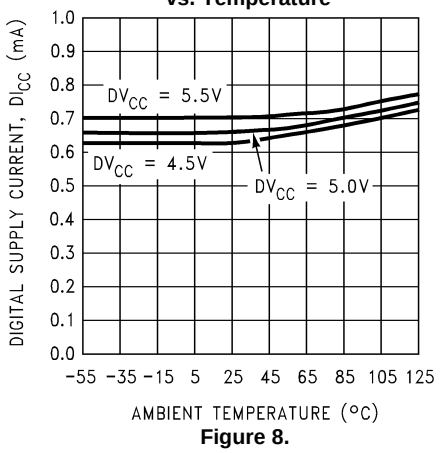


Figure 8.

Conversion Time vs. Temperature

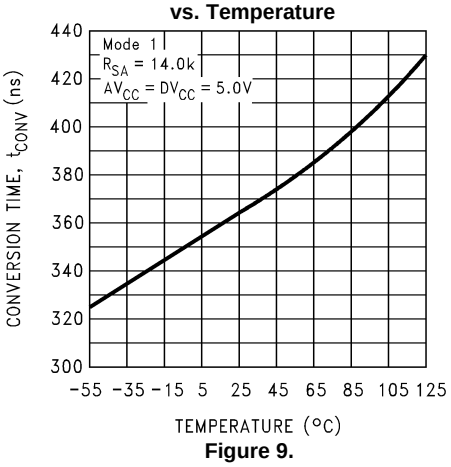


Figure 9.

Conversion Time vs. Temperature

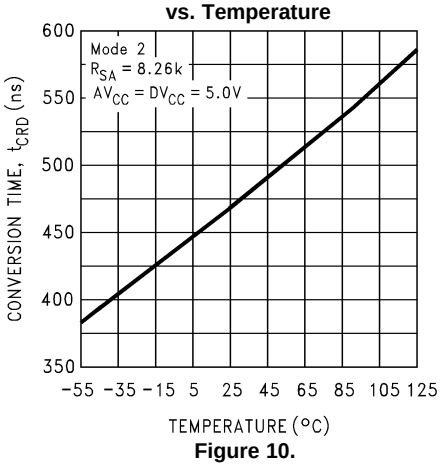


Figure 10.

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Typical Performance Characteristics (continued)

Conversion Time vs. Speed-Up Resistor

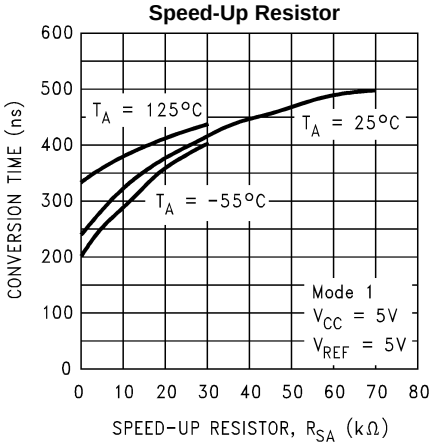


Figure 11.

Conversion Time vs. Speed-Up Resistor

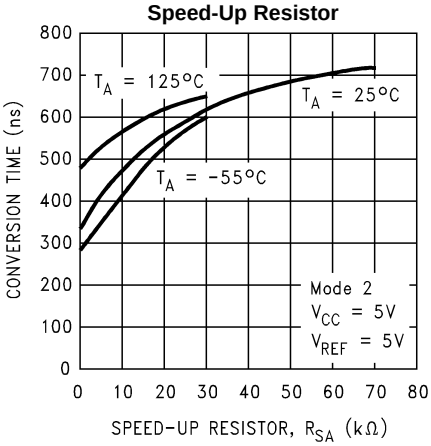


Figure 12.

Spectral Response with 100 kHz Sine Wave Input

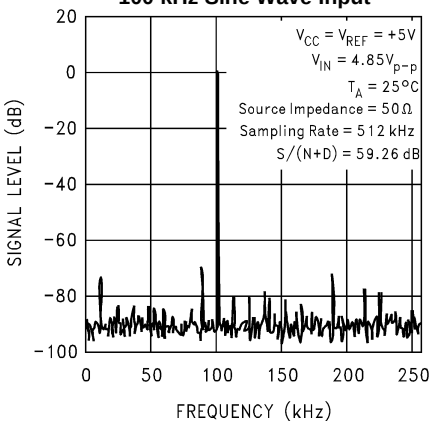


Figure 13.

Spectral Response with 100 kHz Sine Wave Input

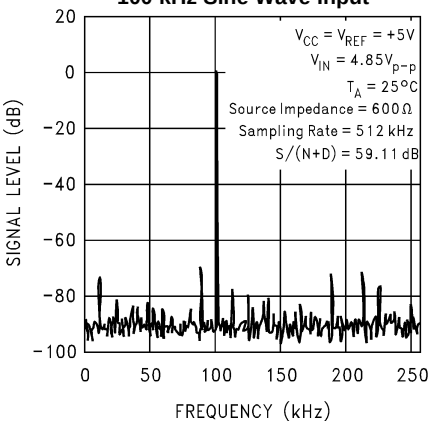


Figure 14.

Signal-to-Noise + THD Ratio vs. Signal Frequency

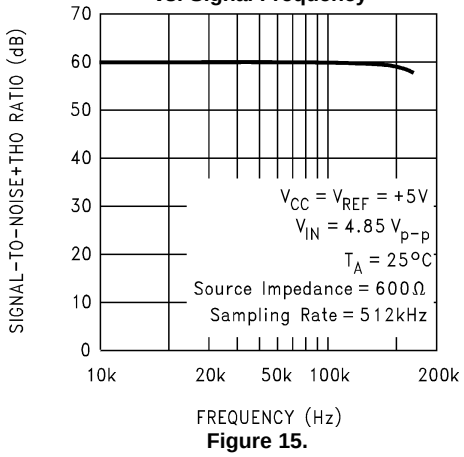


Figure 15.

Linearity Change vs. Speed-Up Resistor

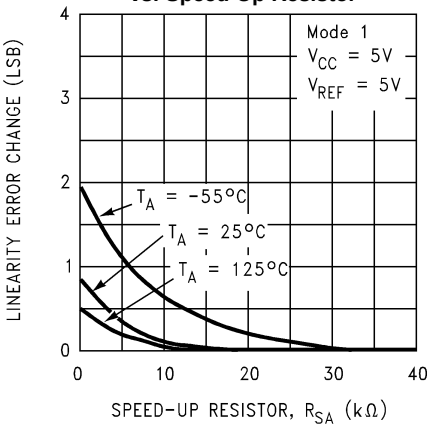


Figure 16.

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Typical Performance Characteristics (continued)

Linearity Change vs. Speed-Up Resistor

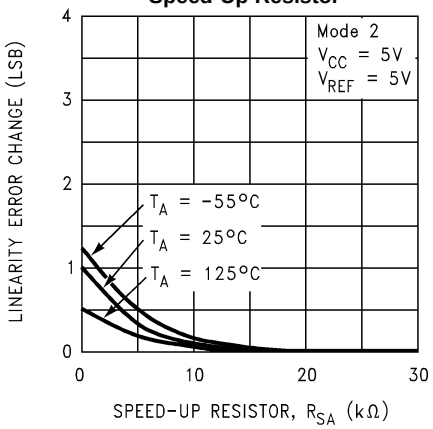


Figure 17.

Linearity Error Change vs. Sample Time

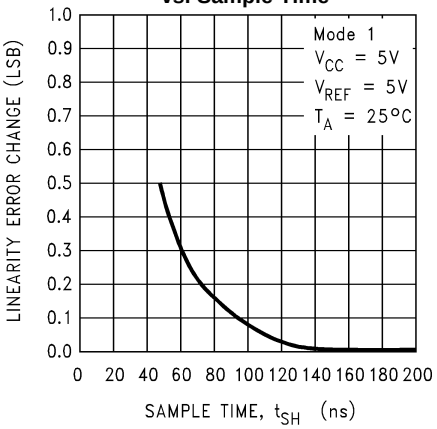


Figure 18.

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FUNCTIONAL DESCRIPTION

The ADC10662 is obsolete. It is discussed here for reference only.

The ADC10662 and ADC10664 digitize an analog input signal to 10 bits accuracy by performing two lower-resolution “flash” conversions. The first flash conversion provides the six most significant bits (MSBs) of data, and the second flash conversion provides the four least significant bits LSBs).

Figure 19 is a simplified block diagram of the converter. Near the center of the diagram is a string of resistors. At the bottom of the string of resistors are 16 resistors, each of which has a value 1/1024 the resistance of the whole resistor string. These lower 16 resistors (the **LSB Ladder**) therefore have a voltage drop of 16/1024, or 1/64 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remainder of the resistor string is made up of eight groups of eight resistors connected in series. These comprise the **MSB Ladder**. Each section of the MSB Ladder has ⅛ of the total reference voltage across it, and each of the LSB resistors has 1/64 of the total reference voltage across it. Tap points across these resistors can be connected, in groups of sixteen, to the sixteen comparators at the right of the diagram.

On the left side of the diagram is a string of seven resistors connected between V_{REF+} and V_{REF-}. Six comparators compare the input voltage with the tap voltages on this resistor string to provide a low-resolution “estimate” of the input voltage. This estimate is then used to control the multiplexer that connects the MSB Ladder to the sixteen comparators on the right. Note that the comparators on the left needn't be very accurate; they simply provide an estimate of the input voltage. Only the sixteen comparators on the right and the six on the left are necessary to perform the initial six-bit flash conversion, instead of the 64 comparators that would be required using conventional half-flash methods.

To perform a conversion, the estimator compares the input voltage with the tap voltages on the seven resistors on the left. The estimator decoder then determines which MSB Ladder tap points will be connected to the sixteen comparators on the right. For example, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of V_{REF}. The estimator decoder will instruct the comparator MUX to connect the 16 comparators to the taps on the MSB ladder between 10/16 and 14/16 of V_{REF}. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as 1/16 of the reference voltage (64 LSBs) will be corrected. This first flash conversion produces the six most significant bits of data—four bits in the flash itself, and 2 bits in the estimator.

The remaining four LSBs are now determined using the same sixteen comparators that were used for the first flash conversion. The MSB Ladder tap voltage just below the input voltage (as determined by the first flash) is subtracted from the input voltage and compared with the tap points on the sixteen LSB Ladder resistors. The result of this second, four-bit flash conversion is then decoded, and the full 10-bit result is latched.

Note that the sixteen comparators used in the first flash conversion are reused for the second flash. Thus, the multistep conversion technique used in the ADC10662 and ADC10664 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the ADC10662 and ADC10664 to perform high-speed conversions without excessive power drain.

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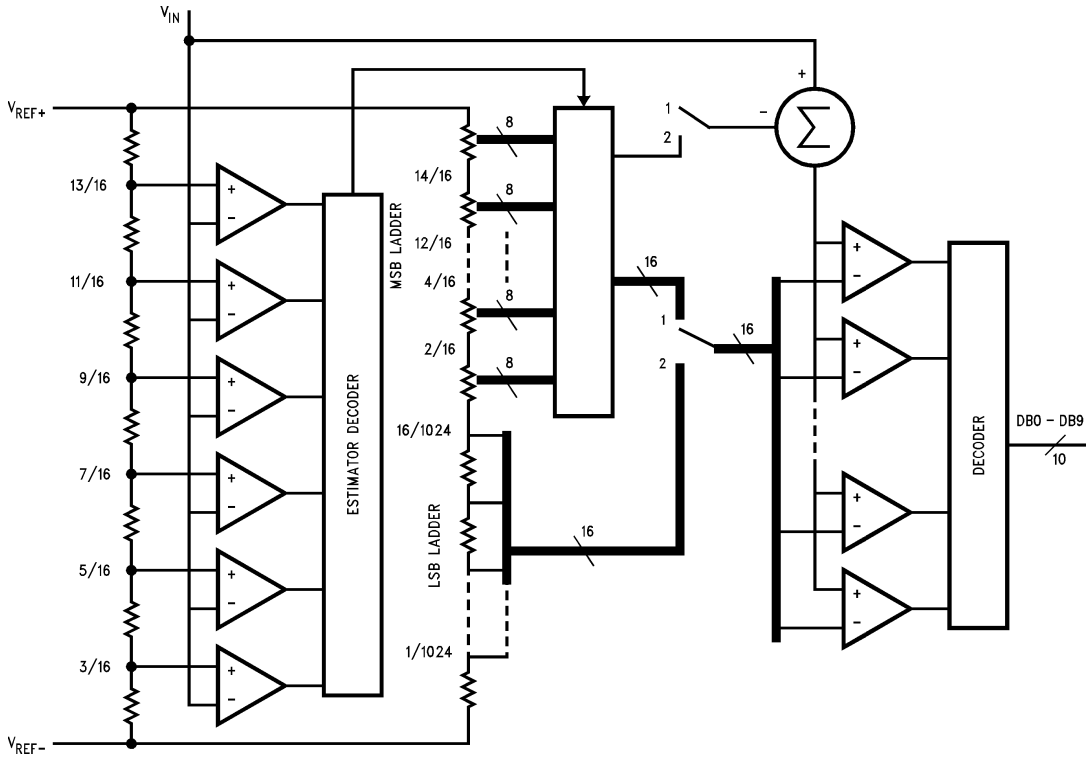


Figure 19. Block Diagram of the Multistep Converter Architecture

SIMILAR PRODUCT DIFFERENCES

The ADC1006x, ADC1046x and ADC1066x (where "x" indicates the number of multiplexer inputs) are similar devices with different specification limits. The differences in these device families are summarized below.

Device Family	ILE, TUE, PSS	THD, SNR, ENOB	Max. Conversion Time
ADC1006x	Verified	-	900ns
ADC1046x	-	Verified	900ns
ADC1066x	-	Verified	466ns

Applications Information

MODES OF OPERATION

The ADC10662 and ADC10664 have two basic digital interface modes. Figure 3 and Figure 4 are timing diagrams for the two modes. The ADC10662 and ADC10664 have input multiplexers that are controlled by the logic levels on pins S_0 and S_1 when $\overline{S}$/H goes low. Table 1 and Table 2 are truth tables showing how the input channels are assigned.

Mode 1

In this mode, the $\overline{S}$/H pin controls the start of conversion. $\overline{S}$/H is pulled low for a minimum of 150 ns. This causes the comparators in the “coarse” flash converter to become active. When $\overline{S}$/H goes high, the result of the coarse conversion is latched and the “fine” conversion begins. After 360 ns (typical), $\overline{INT}$ goes low, indicating that the conversion results are latched and can be read by pulling $\overline{RD}$ low. Note that $\overline{CS}$ must be low to enable $\overline{S}$/H or $\overline{RD}$. $\overline{CS}$ is internally “ANDed” with $\overline{S}$/H and $\overline{RD}$; the input voltage is sampled when $\overline{CS}$ and $\overline{S}$/H are low, and data is read when $\overline{CS}$ and $\overline{RD}$ are low. $\overline{INT}$ is reset high on the rising edge of $\overline{RD}$.

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Table 1. Input Multiplexer Programming ADC10664

S_1	S_0	Channel
0	0	V_{IN0}
0	1	V_{IN1}
1	0	V_{IN2}
1	1	V_{IN3}

Table 2. Input Multiplexer Programming ADC10662

S_0	Channel
0	V_{IN0}
1	V_{IN1}

Mode 2

In Mode 2, also called "$\overline{RD}$ mode", the $\overline{S}$/H and $\overline{RD}$ pins are tied together. A conversion is initiated by pulling both pins low. The A/D converter samples the input voltage and causes the coarse comparators to become active. An internal timer then terminates the coarse conversion and begins the fine conversion. 470 ns (typical) after $\overline{S}$/H and $\overline{RD}$ are pulled low, $\overline{INT}$ goes low, indicating that the conversion is completed. Approximately 20 ns later the data appearing on the TRI-STATE output pins will be valid. Note that data will appear on these pins throughout the conversion, but until $\overline{INT}$ goes low the data at the output pins will be the result of the previous conversion.

REFERENCE CONSIDERATIONS

The ADC10662 and ADC10664 each have two reference inputs. These inputs, V_{REF+} and V_{REF-}, are fully differential and define the zero to full-scale range of the input signal. The reference inputs can be connected to span the entire supply voltage range (V_{REF-} = 0V, V_{REF+} = V_{CC}) for ratiometric applications, or they can be connected to different voltages (as long as they are between ground and V_{CC}) when other input spans are required.

Reducing the overall V_{REF} span to less than 5V increases the sensitivity of the converter (e.g., if V_{REF} = 2V, then 1 LSB = 1.953 mV). Note, however, that linearity and offset errors become larger when lower reference voltages are used. See Typical Performance Characteristics for more information. For this reason, reference voltages less than 2V are not recommended.

In most applications, V_{REF-} will simply be connected to ground, but it is often useful to have an input span that is offset from ground. This situation is easily accommodated by the reference configuration used in the ADC10662 and ADC10664. V_{REF-} can be connected to a voltage other than ground as long as the voltage source connected to this pin is capable of sinking the converter's reference current (12.5 mA Max @ V_{REF} = 5V). If V_{REF-} is connected to a voltage other than ground, bypass it with multiple capacitors.

Since the resistance between the two reference inputs can be as low as 400Ω, the voltage source driving the reference inputs should have low output impedance. Any noise on either reference input is a potential cause of conversion errors, so each of these pins must be supplied with a clean, low noise voltage source. Each reference pin should be bypassed with a 10 µF tantalum and a 0.1 µF ceramic.

THE ANALOG INPUT

The ADC10662 and ADC10664 sample the analog input voltage once every conversion cycle. When this happens, the input is briefly connected to an impedance approximately equal to 600Ω in series with 35 pF. Short-duration current spikes can be observed at the analog input during normal operation. These spikes are normal and do not degrade the converter's performance.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (250 ns maximum). If the sampling time is increased, the source impedance can be larger. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be well-behaved when driving a switched 35 pF/600Ω load. Any ringing or voltage shifts at the op-amp's output during the sampling period can result in conversion errors.

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Correct conversion results will be obtained for input voltages greater than GND − 50 mV and less than V^+ + 50 mV. Do not allow the signal source to drive the analog input pin beyond the Absolute Maximum Rating. If an analog input pin is forced beyond these voltages, the current flowing through the pin should be limited to 5 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than the Absolute Maximum Rating for Package Input Current. When the input signal is expected to extend beyond this limit, an input protection scheme should be used. A simple input protection network using diodes and resistors is shown in Figure 20. Note the multiple bypass capacitors on the reference and power supply pins. If V_{REF-} is not grounded, it should also be bypassed to analog ground using multiple capacitors (see POWER SUPPLY CONSIDERATIONS). AGND and DGND should be at the same potential. V_{IN0} is shown with an input protection network.

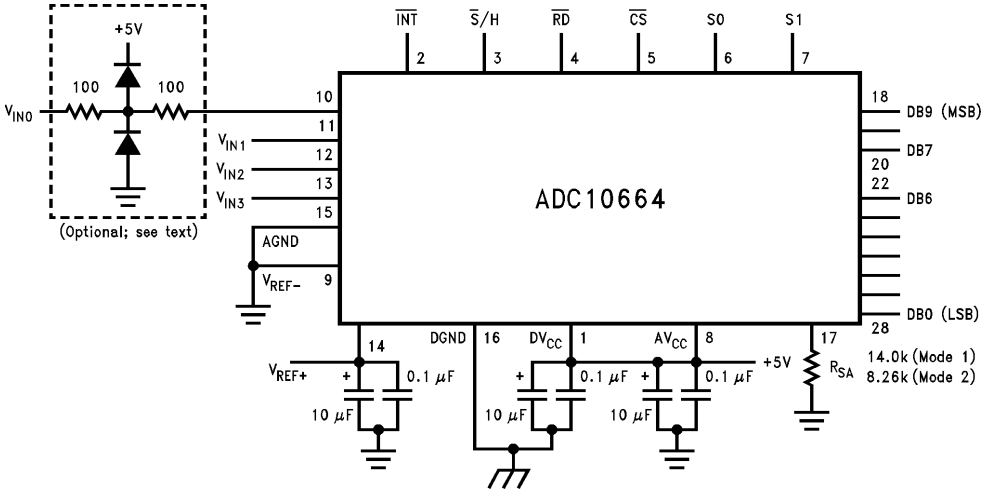


Figure 20. Typical Connection

INHERENT SAMPLE-AND-HOLD

Because the ADC10662 and ADC10664 sample the input signal once during each conversion, they are capable of measuring relatively fast input signals without the help of an external sample-hold. In a non-sampling successive-approximation A/D converter, regardless of speed, the input signal must be stable to better than ±1/2 LSB during each conversion cycle or significant errors will result. Consequently, even for many relatively slow input signals, the signals must be externally sampled and held constant during each conversion if a SAR with no internal sample-and-hold is used.

Because they incorporate a direct sample/hold control input, the ADC10662 and ADC10664 are suitable for use in DSP-based systems. The $\overline{S}$/H input allows synchronization of the A/D converter to the DSP system's sampling rate and to other ADC10662s, and ADC10664s.

POWER SUPPLY CONSIDERATIONS

The ADC10662 and ADC10664 are designed to operate from a +5V (nominal) power supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To ensure accurate conversions, the two supply pins should be connected to the same voltage source, and each should be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor. Depending upon the circuit board layout and other system considerations, more bypassing may be necessary.

The ADC10662 and ADC10664 have separate analog and digital ground pins for separate bypassing of the analog and digital supplies. Their ground pins should be connected to the same potential, and all grounds should be “clean” and free of noise.

In systems with multiple power supplies, careful attention to power supply sequencing may be necessary to avoid over-driving inputs. The A/D converter's power supply pins should be at the proper voltage before digital or analog signals are applied to any of the other pins.

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LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC10662 and ADC10664, it is necessary to use appropriate circuit board layout techniques. The analog ground return path should be low-impedance and free of noise from other parts of the system. Noise from digital circuitry can be especially troublesome.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean ground return point. Grounding the component at the wrong point will result in reduced conversion accuracy.

DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but conventional DC integral and differential nonlinearity specifications don't accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD), are quantitative measures of this capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. The resulting spectral plot might look like the ones shown in the typical performance curves. The large peak is the fundamental frequency, and the noise and distortion components (if any are present) are visible above and below the fundamental frequency. Harmonic distortion components appear at whole multiples of the input frequency. Their amplitudes are combined as the square root of the sum of the squares and compared to the fundamental amplitude to yield the THD specification. Ensured limits for THD are given in the table of Electrical Characteristics.

Signal-to-noise ratio is the ratio of the amplitude at the fundamental frequency to the rms value at all other frequencies, excluding any harmonic distortion components. Ensured limits are given in the Electrical Characteristics table. An alternative definition of signal-to-noise ratio includes the distortion components along with the random noise to yield a signal-to-noise-plus-distortion ration, or S/(N + D).

The THD and noise performance of the A/D converter will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. One way of describing the A/D's performance as a function of signal frequency is to make a plot of “effective bits” versus frequency. An ideal A/D converter with no linearity errors or self-generated noise will have a signal-to-noise ratio equal to (6.02n + 1.76) dB, where n is the resolution in bits of the A/D converter. A real A/D converter will have some amount of noise and distortion, and the effective bits can be found by:

$$\text{n (effective)} = \frac{\text{S/(N + D) (dB)} - 1.76}{6.02} \quad (1)$$

where

- S/(N + D) is the ratio of signal to noise and distortion, which can vary with frequency

As an example, an ADC10662 with a 4.85 V_{P-P}, 100 kHz sine wave input signal will typically have a signal-to-noise-plus-distortion ratio of 59.2 dB, which is equivalent to 9.54 effective bits. As the input frequency increases, noise and distortion gradually increase, yielding a plot of effective bits or S/(N + D) as shown in the typical performance curves.

SPEED ADJUST

The speed adjust pin is connected to an on-chip current source that determines the converter's internal timing. By connecting a resistor between the speed adjust pin and ground as shown in Figure 20, the internal programming current is increased, which reduces the conversion time. The ADC10662 and ADC10664 are specified and ensured for operation with R_{SA} = 14.0 kΩ (Mode 1) or R_{SA} = 8.26k (Mode 2). Smaller resistors will result in faster conversion times, but linearity will begin to degrade as R_{SA} becomes smaller (see Typical Performance Characteristics).

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REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	15

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC10664CIWM	NRND	SOIC	DW	28	26	TBD	Call TI	Call TI	-40 to 85	ADC10664 CIWM	
ADC10664CIWM/NOPB	ACTIVE	SOIC	DW	28	26	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC10664 CIWM	Samples
ADC10664CIWMX/NOPB	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC10664 CIWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

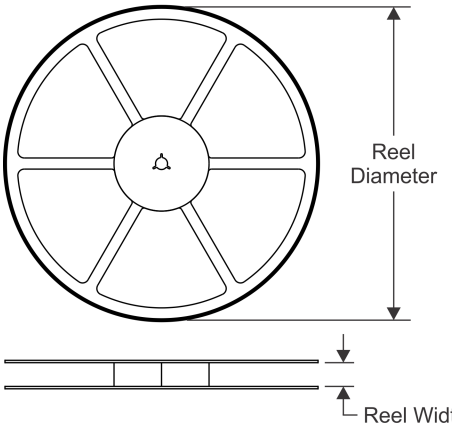
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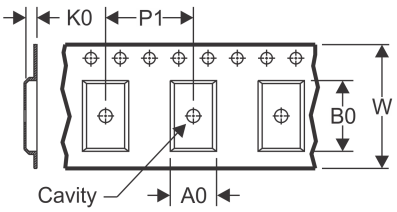
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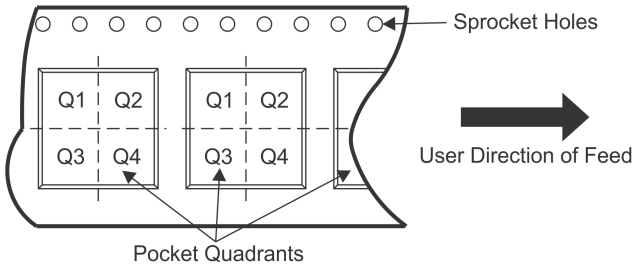


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

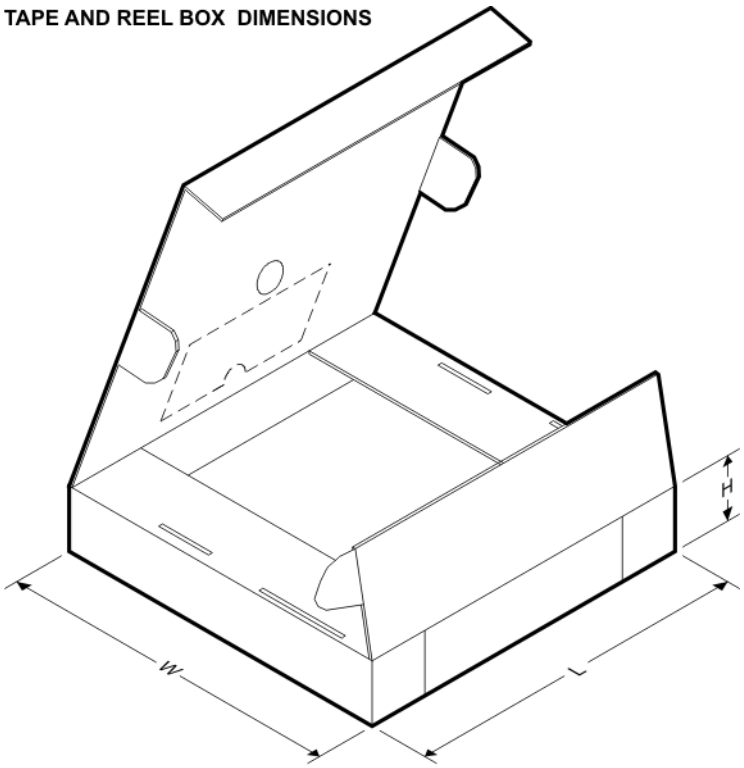
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC10664CIWMX/NOPB	SOIC	DW	28	1000	330.0	24.4	10.8	18.4	3.2	12.0	24.0	Q1

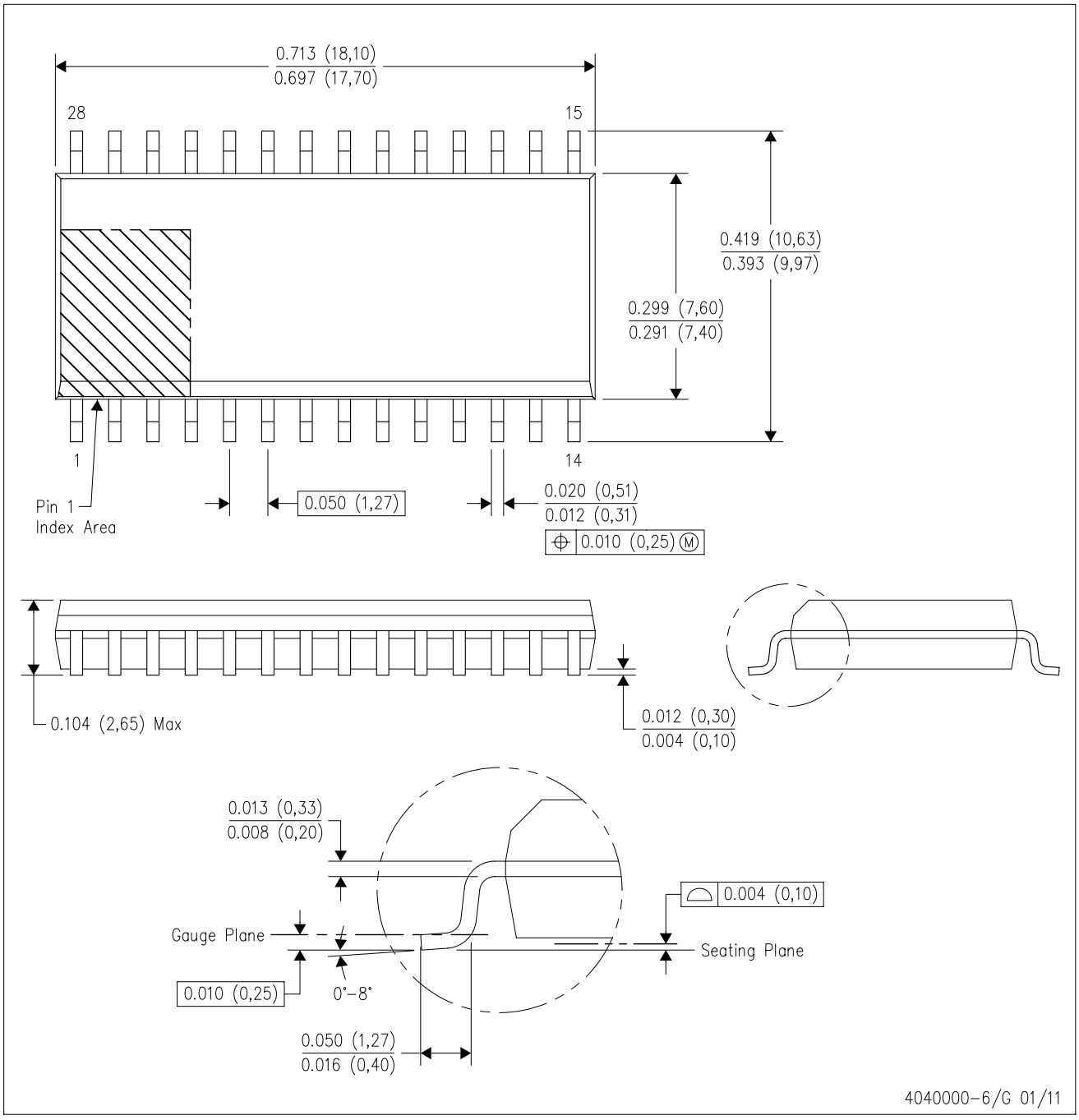
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC10664CIWMX/NOPB	SOIC	DW	28	1000	367.0	367.0	45.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

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