November 2002

National Semiconductor

ADC08L060
8-Bit, 10 MSPS to 60 MSPS, 0.65 mW/MSPS A/D Converter with Internal Sample-and-Hold

General Description

The ADC08L060 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates of 10 MSPS to 60 MSPS while consuming just 0.65 mW per MHz of clock frequency, or 39 mW at 60 MSPS. Raising the PD pin puts the ADC08L060 into a Power Down mode where it consumes < 1.0 mW.

The unique architecture achieves 7.6 Effective Bits. The ADC08L060 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08L060's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 1.8V to 3V logic. The digital inputs (CLK and PD) are TTL/CMOS compatible.

The ADC08L060 is offered in a 24-lead plastic package (TSSOP) and is specified over the industrial temperature range of –40˚C to +85˚C.

Features

- Single-ended input
- Internal sample-and-hold function
- Low voltage (single +3V) operation
- Small package
- Power-down feature

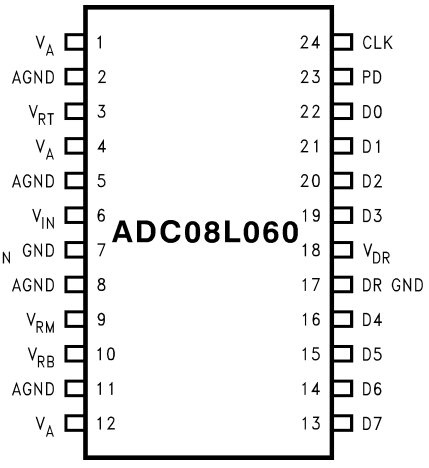
Key Specifications

Resolution	8 bits
Conversion rate	60 MSPS
DNL	±0.25 LSB (typ)
INL	+0.5/–0.2 LSB (typ)
SNR (10.1 MHz)	48 dB (typ)
ENOB (10.1 MHz)	7.6 bits (typ)
THD (10.1 MHz)	–57 dB (typ)
Latency	5 Clock Cycles
No missing codes	Guaranteed
Power Consumption	
Operating	0.65 mW/MSPS (typ)
Power down	< 1.0 mW (typ)

Applications

- Digital Imaging
- Set-top boxes
- Portable Instrumentation
- Communication Systems
- X-ray imaging
- Viterbi decoders

Pin Configuration



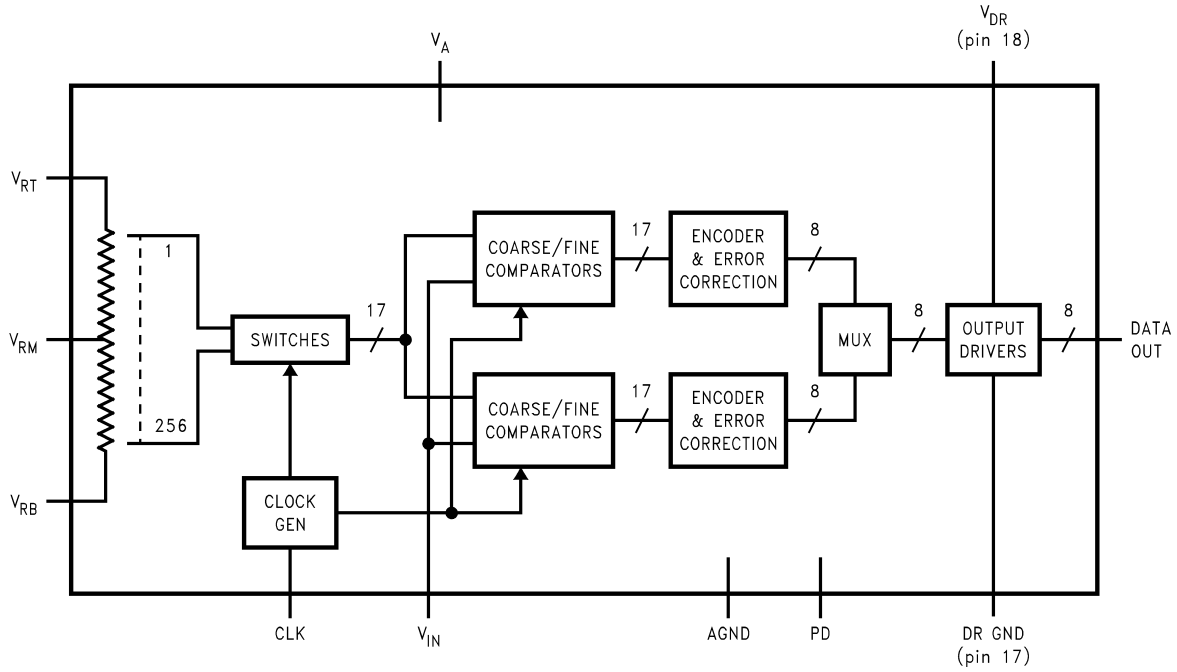
20041701

© 2002 National Semiconductor Corporation

Ordering Information

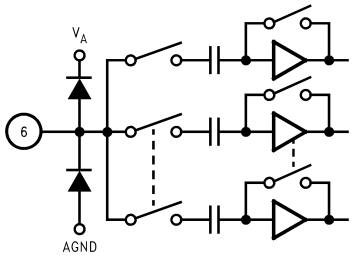
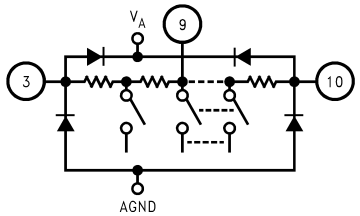
ADC08L060CIMT	TSSOP
ADC08L060CIMTX	TSSOP (tape and reel)
ADC08L060EVAL	Evaluation Board

Block Diagram

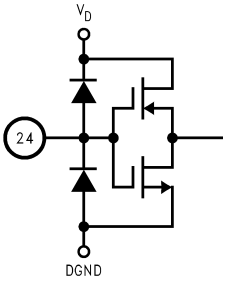
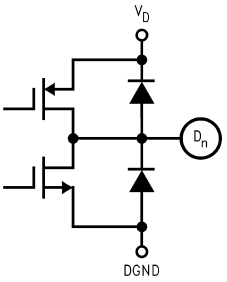


20041702

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 0.5V to V_A. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a quiet point in the analog ground plane with a 0.1 µF capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to (V_{RT} – 0.5V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the rising edge of CLK input.
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN}.
1, 4, 12	V_A		Positive analog supply pin. Connect to a quiet voltage source of +3V. V_A should be bypassed with a 0.1 µF ceramic chip capacitor for each pin, plus one 10 µF capacitor. See Section 3.0 for more information.
18	V_{DR}		Power supply for the output drivers. If connected to V_A, decouple well from V_A.
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A)	3.8V
Driver Supply Voltage (V_{DR})	V_A +0.3V
Voltage on Any Input or Output Pin	−0.3V to V_A
Reference Voltage (V_{RT}, V_{RB})	V_A to AGND
CLK, PD Voltage Range	−0.05V to (V_A + 0.05V)
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	200V
Soldering Temperature, Infrared, 10 seconds (Note 6)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage, V_A	+2.4V to +3.6V
Driver Supply Voltage, V_{DR}	+2.4V to V_A
Output Driver Voltage, V_{DR}	1.8V to V_A
Ground Difference |GND - DR GND|	0V to 300 mV
Upper Reference Voltage (V_{RT})	0.5V to (V_A −0.3V)
Lower Reference Voltage (V_{RB})	0V to (V_{RT} −0.5V)
V_{IN} Voltage Range	V_{RB} to V_{RT}

Converter Electrical Characteristics

The following specifications apply for V_A = V_{DR} = +3.0V_{DC}, V_{RT} = +1.9V, V_{RB} = 0.3V, C_L = 10 pF, f_{CLK} = 60 MHz at 50% duty cycle. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**: all other limits T_A = 25˚C (Notes 7, 8)

Symbol	Parameter	Conditions		Typical (Note 9)	Limits (Note 9)	Units (Limits)
DC ACCURACY						
INL	Integral Non-Linearity			+0.5 −0.2	**+1.9** **−1.35**	LSB (max) LSB (min)
DNL	Differential Non-Linearity			±0.25	**±0.90**	LSB (max)
	Missing Codes				**0**	(max)
FSE	Full Scale Error			3.0	**±13**	mV (max)
V_{OFF}	Zero Scale Offset Error			19	**27**	mV (max)
ANALOG INPUT AND REFERENCE CHARACTERISTICS						
V_{IN}	Input Voltage			1.6	**V_{RB}** **V_{RT}**	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 0.75V +0.5 Vrms	(CLK LOW)	3		pF
			(CLK HIGH)	4		pF
R_{IN}	R_{IN} Input Resistance			>1		MΩ
BW	Full Power Bandwidth			270		MHz
V_{RT}	Top Reference Voltage			1.9	V_A 0.5	V (max) V (min)
V_{RB}	Bottom Reference Voltage			0.3	V_{RT} − 0.5 0	V (max) V (min)
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		720	**590** **1070**	Ω (min) Ω (max)
I_{ref}	Reference Ladder Current	VRT to VRB		2.2	**1.5** **2.7**	mA mA
CLK, PD DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Logical High Input Voltage	V_{DR} = V_A = 3.6V			**2.0**	V (min)
V_{IL}	Logical Low Input Voltage	V_{DR} = V_A = 2.7V			**0.8**	V (max)
I_{IH}	Logical High Input Current	V_{IH} = V_{DR} = V_A = 3.6V		10		nA
I_{IL}	Logical Low Input Current	V_{IL} = 0V, V_{DR} = V_A = 2.7V		−50		nA
C_{IN}	Logic Input Capacitance			3		pF
DIGITAL OUTPUT CHARACTERISTICS						

Converter Electrical Characteristics (Continued)

The following specifications apply for $V_A = V_{DR} = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10$ pF, $f_{CLK} = 60$ MHz at 50% duty cycle. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits $T_A = 25^{\circ}C$ (Notes 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
V_{OH}	High Level Output Voltage	$V_A = V_{DR} = 2.7V$, $I_{OH} = -400$ µA	2.6	**2.4**	V (min)
V_{OL}	Low Level Output Voltage	$V_A = V_{DR} = 2.7V$, $I_{OL} = 1.0$ mA	0.4	**0.5**	V (max)
DYNAMIC PERFORMANCE					
ENOB	Effective Number of Bits	$f_{IN} = 10.1$ MHz, $V_{IN} =$ FS – 0.25 dB	7.6	**6.9**	Bits
		$f_{IN} = 29$ MHz, $V_{IN} =$ FS – 0.25 dB	7.4		Bits (min)
SINAD	Signal-to-Noise & Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} =$ FS – 0.25 dB	47.4	**43.3**	dB
		$f_{IN} = 29$ MHz, $V_{IN} =$ FS – 0.25 dB	46.1		dB (min)
SNR	Signal-to-Noise Ratio	$f_{IN} = 10.1$ MHz, $V_{IN} =$ FS – 0.25 dB	48	**44.5**	dB
		$f_{IN} = 29$ MHz, $V_{IN} =$ FS – 0.25 dB	47.2		dB (min)
SFDR	Spurious Free Dynamic Range	$f_{IN} = 10.1$ MHz, $V_{IN} =$ FS – 0.25 dB	59.1		dBc
		$f_{IN} = 29$ MHz, $V_{IN} =$ FS – 0.25 dB	54.5		dBc
THD	Total Harmonic Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} =$ FS – 0.25 dB	–56.9		dBc
		$f_{IN} = 29$ MHz, $V_{IN} =$ FS – 0.25 dB	–53.3		dBc
HD2	2nd Harmonic Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} =$ FS – 0.25 dB	-61.1		dBc
		$f_{IN} = 29$ MHz, $V_{IN} =$ FS – 0.25 dB	–54.9		dBc
HD3	3rd Harmonic Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} =$ FS – 0.25 dB	–64.2		dBc
		$f_{IN} = 29$ MHz, $V_{IN} =$ FS – 0.25 dB	–63.1		dBc
IMD	Intermodulation Distortion	$f_1 = 11$ MHz, $V_{IN} =$ FS – 6.25 dB $f_2 = 12$ MHz, $V_{IN} =$ FS – 6.25 dB	–55		dBc
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	DC Input	13	15.9	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} =$ FS – 3 dB	14		mA
DRI_D	Output Driver Supply Current	DC Input	0.04	0.2	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} =$ FS – 3 dB	4.2		mA
$I_A + DRI_D$	Total Operating Current	DC Input	13	16.1	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} =$ FS – 3 dB, PD = Low	18.2		
		CLK Low, PD = Hi	0.33		
PC	Power Consumption	DC Input	39	**48.3**	mW (max)
		$f_{IN} = 10$ MHz, $V_{IN} =$ FS – 3 dB, PD = Low	53		mW
		CLK Low, PD = Hi	0.3		mW
$PSRR_1$	Power Supply Rejection Ratio	FSE change with 2.7V to 3.3V change in V_A	–51		dB
$PSRR_2$	Power Supply Rejection Ratio	SNR with 200 mW at 1MHz on supply	45		dB
AC ELECTRICAL CHARACTERISTICS					
f_{C1}	Maximum Conversion Rate		80	**60**	MHz (min)
f_{C2}	Minimum Conversion Rate		10		MHz
t_{CL}	Minimum Clock Low Time		0.62		ns (min)
t_{CH}	Minimum Clock High Time		0.62		ns (min)
DC	Clock Duty Cycle		5 95		%(min) %(max)
t_{OH}	Output Hold Time	CLK to Data Invalid	5.2		ns
t_{OD}	Output Delay	CLK to Data Transition	7.1	**5.0**	ns (min)
				9.4	ns (max)
	Pipeline Delay (Latency)		5		Clock Cycles
t_{AD}	Sampling (Aperture) Delay	CLK Rise to Acquisition of Data	2.6		ns

Converter Electrical Characteristics (Continued)

The following specifications apply for $V_A = V_{DR} = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10$ pF, $f_{CLK} = 60$ MHz at 50% duty cycle. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits $T_A = 25^\circ C$ (Notes 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
DYNAMIC PERFORMANCE					
t_{AJ}	Aperture Jitter		2		ps rms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DR GND = 0V, unless otherwise specified.

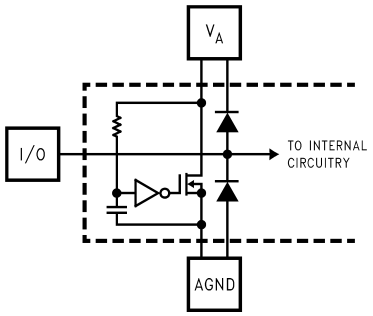
Note 3: When the input voltage at any pin exceeds the power supplies (that is, less than AGND or DR GND, or greater than V_A or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. In the 24-pin TSSOP, θ_{JA} is 92˚C/W, so P_DMAX = 1,358 mW at 25˚C and 706 mW at the maximum operating ambient temperature of 85˚C. Note that the power consumption of this device under normal operation will typically be about 49 mW (40 mW quiescent power + 4 mW reference ladder power + 5 mW to drive the output bus capacitance). The values for maximum power dissipation listed above will be reached only when the ADC08L060 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Note 6: See AN-450, “Surface Mounting Methods and Their Effect on Product Reliability”.

Note 7: The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_{DR} or below GND by more than 100 mV. For example, if V_A is $2.7V_{DC}$ the full-scale input voltage must be $\leq 2.8V_{DC}$ to ensure accurate conversions.



20041707

Note 8: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

Note 9: Typical figures are at $T_J = 25^\circ C$, and represent most likely parametric norms. Test limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

Note 10: I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by the load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent), $I_{DR} = V_{DR} (C_O \times f_O + C_1 \times f_1 + \ldots + C_{71} \times f_7)$ where V_{DR} is the output driver power supply voltage, C_n is the total capacitance on any given output pin, and f_n is the average frequency at which that pin is toggling.

Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the rise of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode t_{AD} after the clock goes high.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 60 MSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL-SCALE ERROR is a measure of how far the last code transition is from the ideal 1½ LSB below V_{RT} and is defined as:

$$V_{max} + 1.5\ LSB - V_{RT}$$

where V_{max} is the voltage at which the transition to the maximum (full scale) code occurs.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. Measured at 60 MSPS with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. it is defined as the ratio of the power in the second and thrid order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$(V_{RT} - V_{RB})/2^n$$

where "n" is the ADC resolution, which is 8 in the case of the ADC08L060.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC08L060, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the dc power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected and is here defined as

$$PSRR2 = 20Log\left(4\sqrt{10^{\frac{-SNR1}{10}} - 10^{\frac{-SNR0}{10}}}\right)$$

where SNR0 is the SNR measured with no noise or signal on the supply lines and SNR1 is the SNR measured with a 1 MHz, 200 mV_{P-P} signal riding upon the supply lines.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log\sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

ZERO SCALE OFFSET ERROR is the error in the input voltage required to cause the first code transition. It is defined as

$$V_{OFF} = V_{ZT} - V_{RB}$$

where V_{ZT} is the first code transition input voltage.

2nd HARMONIC DISTORTION (2nd HARM) is the difference, expressed in dB, between the rms power in the output fundamental frequency and the power in its 2nd harmonic at the output.

3rd HARMONIC DISTORTION (3rd HARM) is the difference, expressed in dB, between the rms power in the output fundamental frequency and the power in its 3rd harmonic at the output.

Timing Diagram

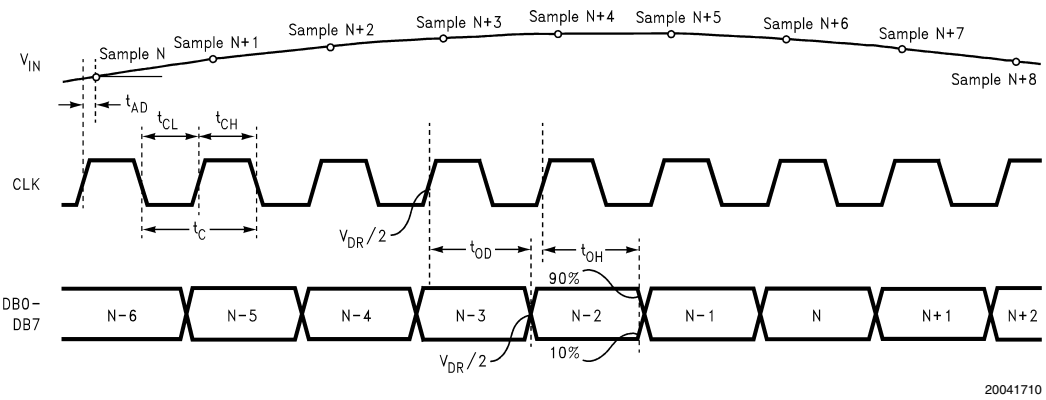
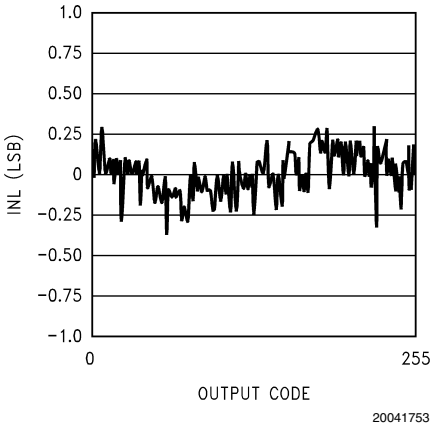


FIGURE 1. ADC08L060 Timing Diagram

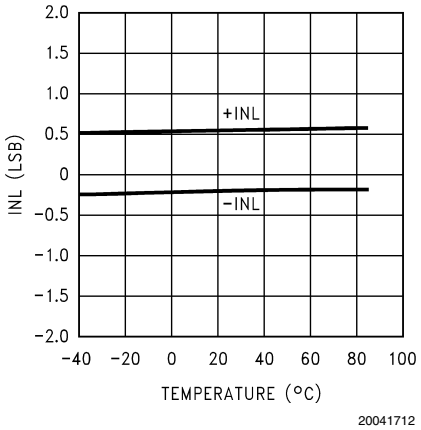
Typical Performance Characteristics

$V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

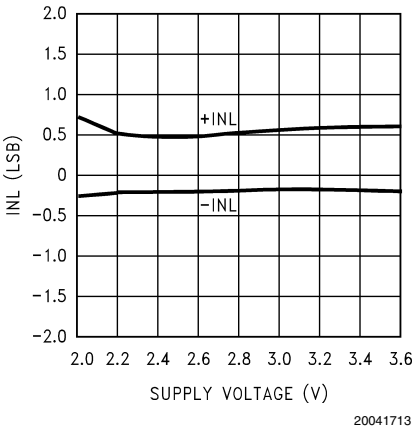
INL



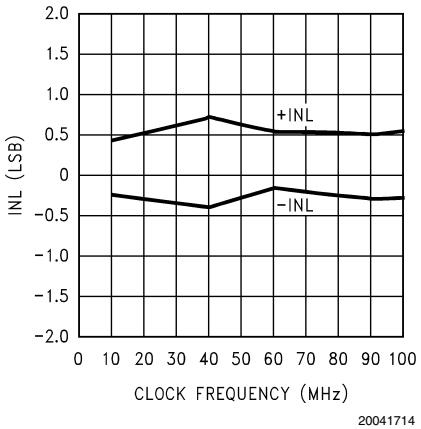
INL vs Temperature



INL vs Supply Voltage, V_A

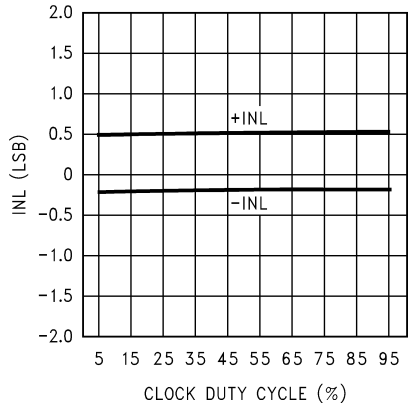


INL vs Sample Rate



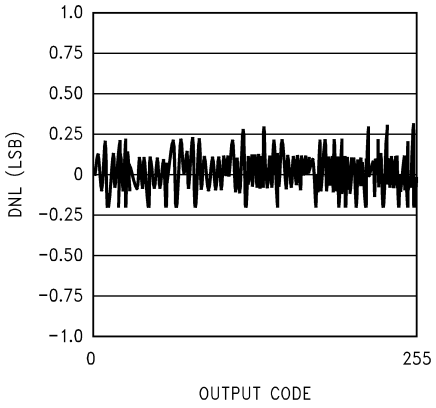
Typical Performance Characteristics $V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated (Continued)

INL vs Clock Duty Cycle



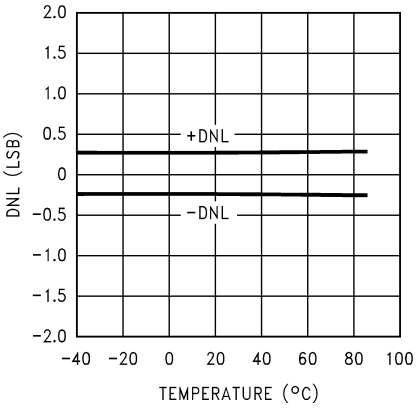
20041715

DNL



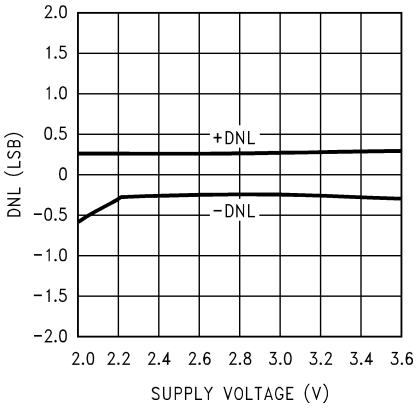
20041754

DNL vs Temperature



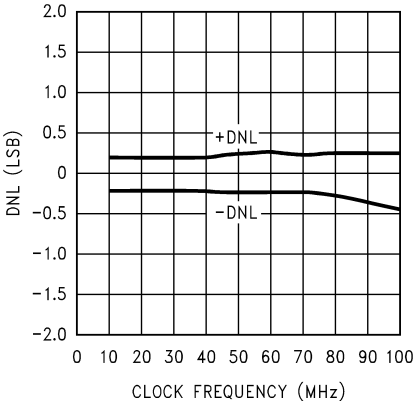
20041717

DNL vs Supply Voltage, V_A



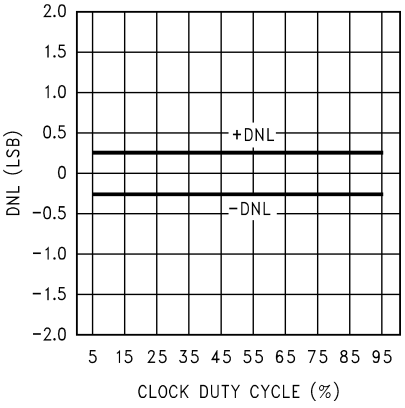
20041718

DNL vs Sample Rate



20041719

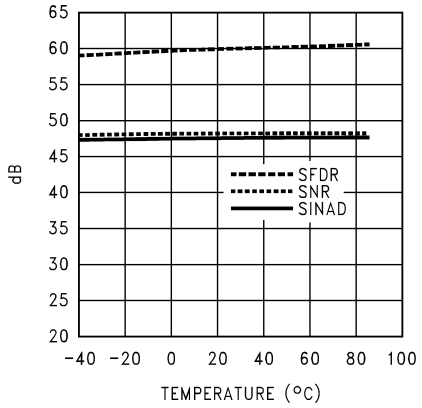
DNL vs Clock Duty Cycle



20041720

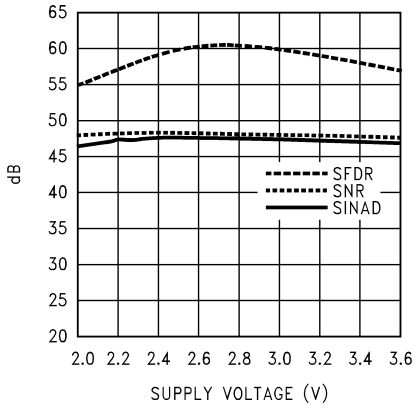
Typical Performance Characteristics $V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated (Continued)

SNR, SINAD and SFDR vs Temperature



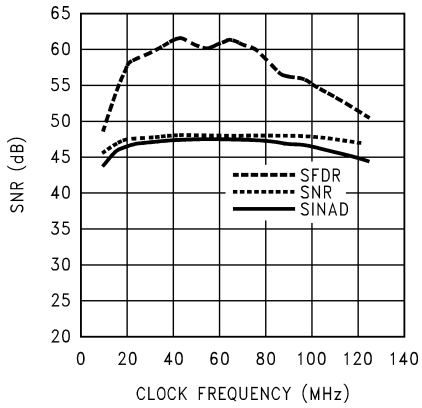
20041721

SNR, SINAD and SFDR vs Supply Voltage, V_A



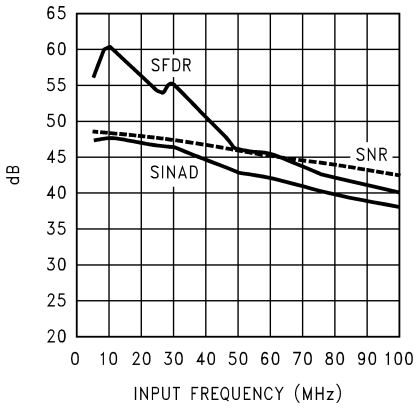
20041722

SNR, SINAD and SFDR vs Sample Rate



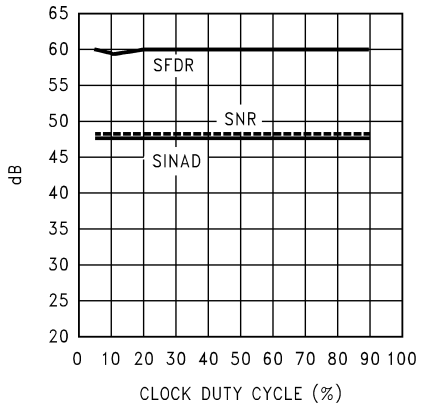
20041723

SNR, SINAD and SFDR vs Input Frequency



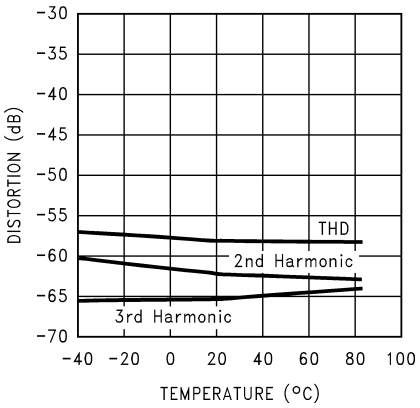
20041724

SNR, SINAD and SFDR vs Clock Duty Cycle



20041725

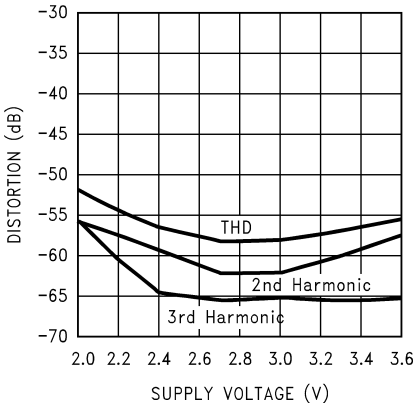
Distortion vs Temperature



20041726

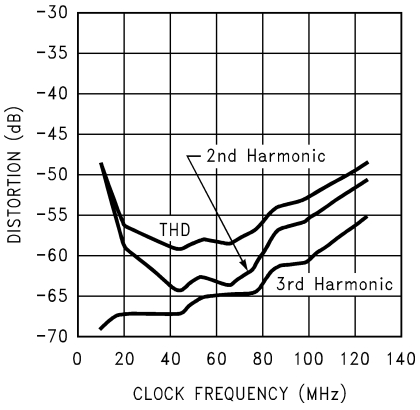
Typical Performance Characteristics $V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated (Continued)

Distortion vs Supply Voltage, V_A



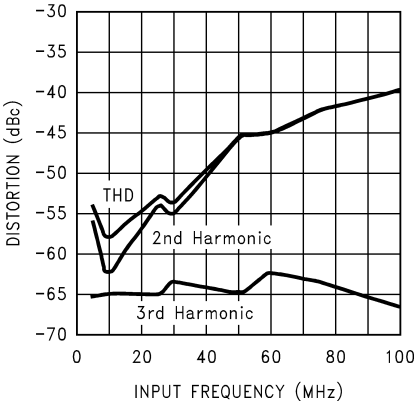
20041727

Distortion vs Sample Rate



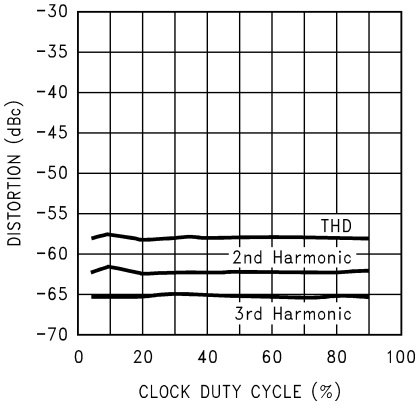
20041728

Distortion vs Input Frequency



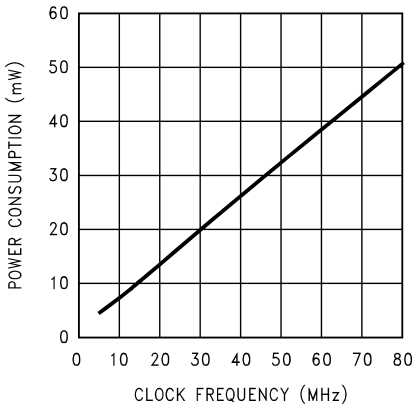
20041729

Distortion vs Clock Duty Cycle



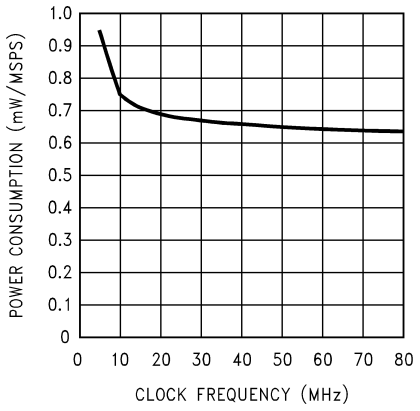
20041730

Power Consumption (Active) vs Sample Rate (f_{IN} = d.c.)



20041731

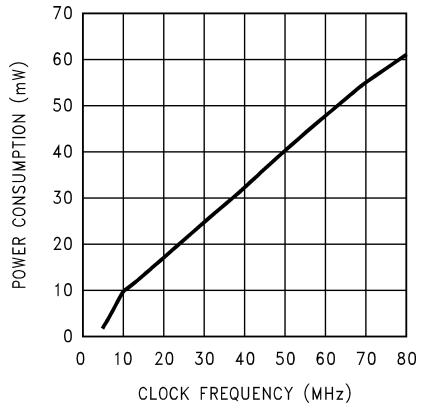
Power Consumption (Active) vs Sample Rate (f_{IN} = d.c.)



20041738

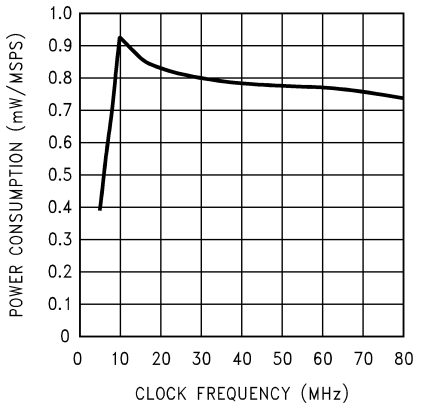
Typical Performance Characteristics $V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated (Continued)

Power Consumption (Active) vs Sample Rate (f_{IN} = 1 MHz)



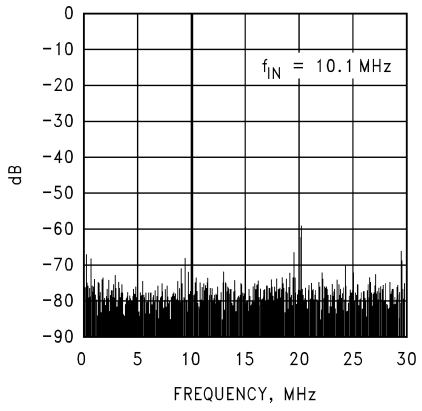
20041739

Power Consumption (Active) vs Sample Rate (f_{IN} = 1 MHz)



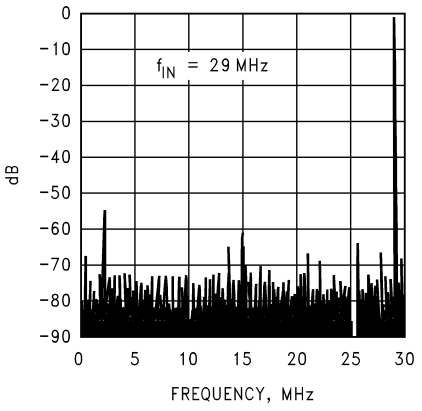
20041740

Spectral Response @ f_{IN} = 10 MHz



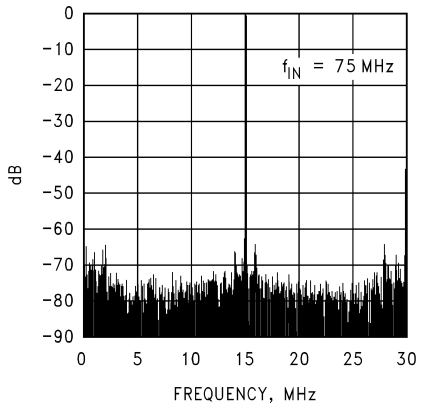
20041755

Spectral Response @ f_{IN} = 29 MHz



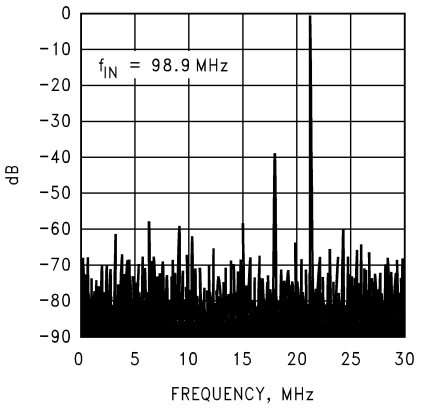
20041757

Spectral Response @ f_{IN} = 75 MHz



20041756

Spectral Response @ f_{IN} = 98.9 MHz



20041758

Functional Description

The ADC08L060 uses a unique architecture that achieves over 7 effective bits at input frequencies up to and beyond Nyquist.

The analog input signal that is within the voltage range set by V_{RT} and V_{RB} is digitized to eight bits. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RT} will cause the output word to consist of all ones.

Incorporating a switched capacitor bandgap, the ADC08L060 exhibits a power consumption that is proportional to frequency, limiting power consumption to what is needed at the clock rate that is used. This and its excellent performance over a wide range of clock frequencies makes it an ideal choice as a single ADC for many 8-bit needs.

Data is acquired at the rising edge of the clock and the digital equivalent of that data is available at the digital outputs 5 clock cycles plus t_{OD} later. The ADC08L060 will convert as long as an adequate clock signal is present at pin 24. The device is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the output pins hold the last conversion before the PD pin went high and the device consumes just 1 mW.

Applications Information

1.0 REFERENCE INPUTS

The reference inputs V_{RT} and V_{RB} are the top and bottom of the reference ladder, respectively. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in the Operating Ratings table (0.5V to (V_A – 0.3V) for V_{RT} and 0V to (V_{RT} – 0.5V) for V_{RB}). Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin to keep these voltages stable.

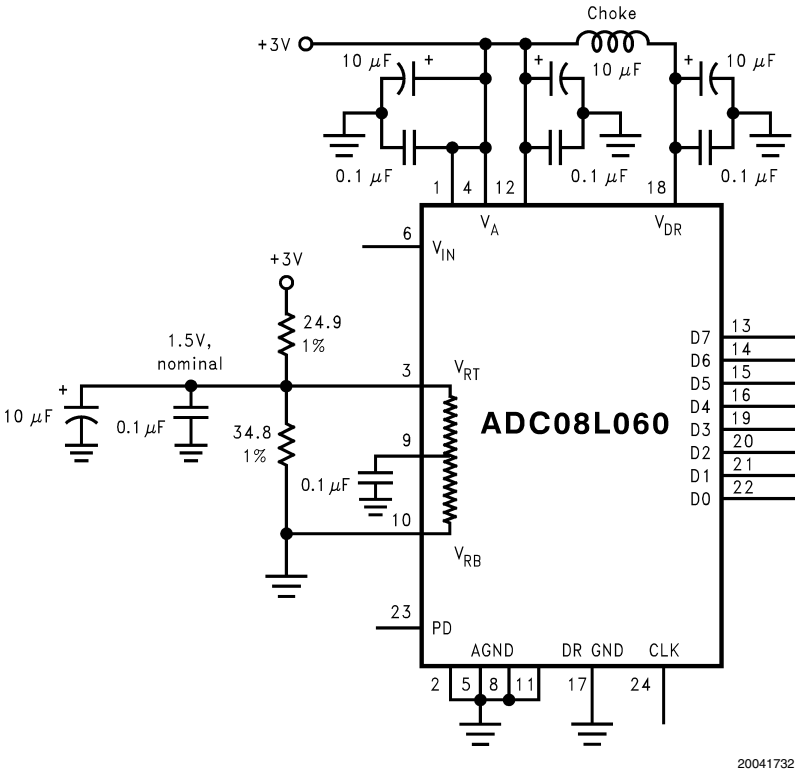


FIGURE 2. Simple, low component count reference biasing. Because of the ladder and external resistor tolerances, the reference voltage can vary too much for some applications.

The reference bias circuit of *Figure 2* is very simple and the performance is adequate for many applications. However, circuit tolerances will lead to a wide reference voltage range. Better reference stability can be achieved by driving the reference pins with low impedance sources.

The circuit of *Figure 3* will allow a more accurate setting of the reference voltages. The lower amplifier must have bipolar supplies as its output voltage must go negative to force V_{RB} to any voltage below the V_{BE} of the PNP transistor. Of course, the divider resistors at the amplifier input could be changed to suit your reference voltage needs, or the divider can be replaced with potentiometers for precise settings. The bottom of the ladder (V_{RB}) may simply be returned to ground if the minimum input signal excursion is 0V. Be sure that the driving source can source sufficient current into the V_{RT} pin and sink enough current from the V_{RB} pin to keep these pins stable.

The LMC662 amplifier shown was chosen for its low offset voltage and low cost. V_{RT} should always be at least 0.5V more positive than V_{RB} to minimize noise.

Applications Information (Continued)

The V_{RM} pin is the center of the reference ladder and should be bypassed to a quiet point in the analog ground plane with a 0.1 µF capacitor. DO NOT allow this pin to float.

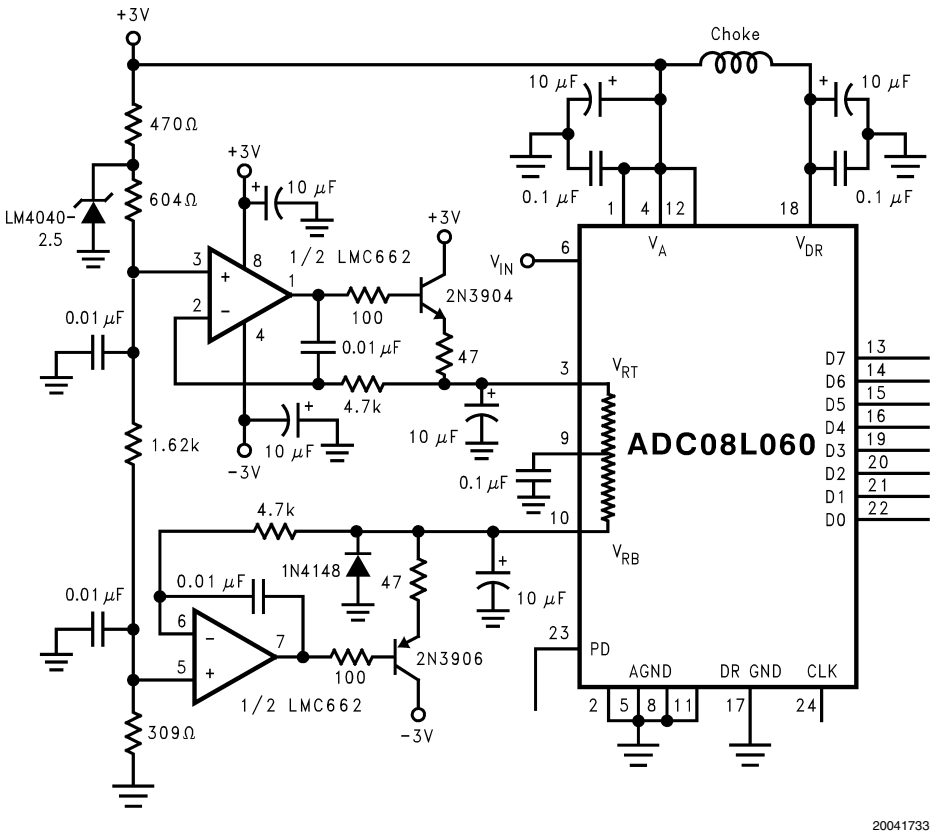


FIGURE 3. Driving the reference to force desired values requires driving with a low impedance source.

2.0 THE ANALOG INPUT

The analog input of the ADC08L060 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 3 pF when the clock is low, and 4 pF when the clock is high. Since a dynamic capacitance is more difficult to drive than is a fixed capacitance, choose an amplifier that can drive this type of load.

Figure 4 shows an example of an input circuit using the LMH6702. Any input amplifier should incorporate some gain as operational amplifiers exhibit better phase margin and transient response with gains above 2 or 3 than with unity gain. If an overall gain of less than 3 is required, attenuate the input and operate the amplifier at a higher gain, as shown in *Figure 4*.

The RC at the amplifier output filters the clock rate energy that comes out of the analog input due to the input sampling circuit. The optimum time constant for this circuit depends not only upon the amplifier and ADC, but also on the circuit layout and board material. A resistor value should be chosen between 10Ω and 47Ω and the capacitor value chose according to the formula

$$C = \frac{1}{2 \cdot \pi \cdot R \cdot f_{CLK}}$$

This will provide optimum SNR performance. Best THD performance is realized when the capacitor and resistor values are both zero. To optimize SINAD, reduce the capacitor value until SINAD performance is optimized. That is, until SNR = −THD. This value will usually be in the range of 20% to 65% of the value calculated with the above formula. An accurate calculation is not possible because of the board material and layout dependence.

The circuit of *Figure 4* has both gain and offset adjustments. If you eliminate these adjustments normal circuit tolerances may result in signal clipping unless care is exercised in the worst case analysis of component tolerances and the input signal excursion is appropriately limited to account for the worst case conditions.

Applications Information (Continued)

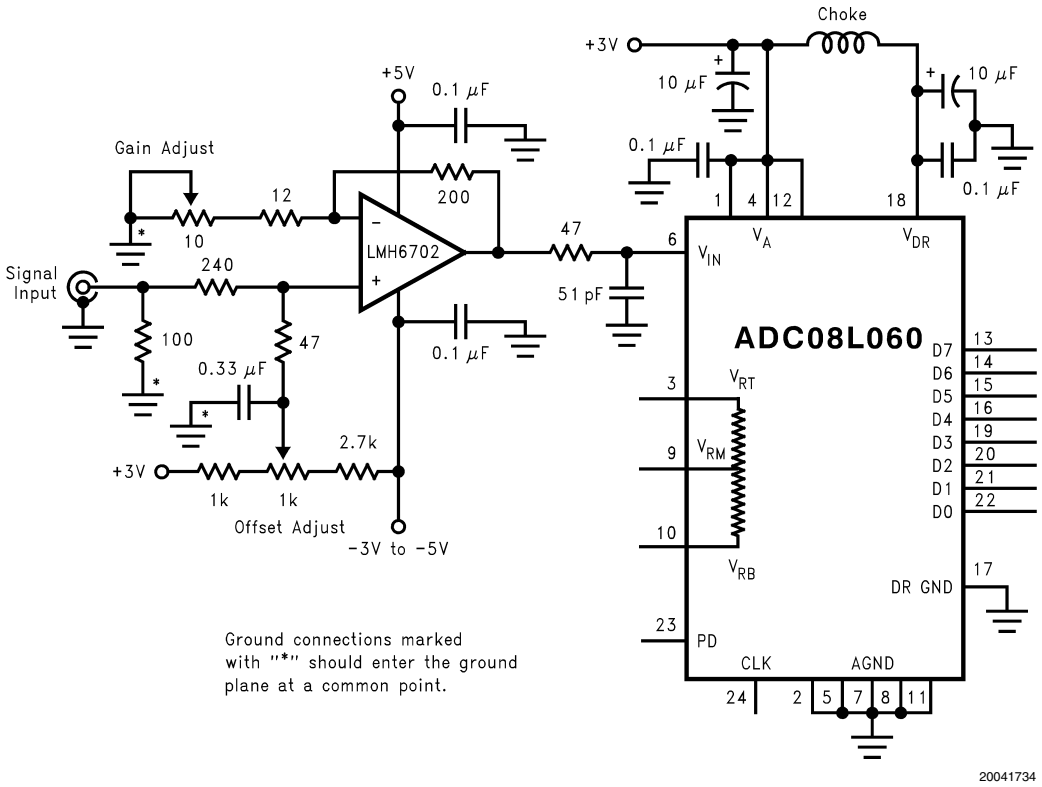


FIGURE 4. The input amplifier should incorporate some gain for best performance (see text).

3.0 POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 µF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 cm) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed within one centimeter of the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source is recommended for the V_A and V_{DR} supplies of the ADC08L060, these supply pins should be well isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A choke or 27Ω resistor is recommended between these supply lines with adequate bypass capacitors close to the supply pins.

As is the case with all high speed converters, the ADC08L060 should be assumed to have little power supply rejection. None of the supplies for the converter should be the supply that is used for other digital circuitry in any system with a lot of digital power being consumed. The ADC supplies should be the same supply used for other analog circuitry.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 300 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08L060 power pins.

4.0 THE DIGITAL INPUT PINS

The ADC08L060 has two digital input pins: The PD pin and the Clock pin.

4.1 The PD Pin

The Power Down (PD) pin, when high, puts the ADC08L060 into a low power mode where power consumption is reduced to 1.2 mW. Output data is valid and accurate about 1 millisecond after the PD pin is brought low.

The digital output pins retain the last conversion output code when either the clock is stopped or the PD pin is high.

4.2 The ADC08L060 Clock

Although the ADC08L060 is tested and its performance is guaranteed with a 60 MHz clock, it typically will function well with clock frequencies from 10 MHz to 80 MHz.

4.2.1 Clock Duty Cycle

The low and high times of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC08L060 is designed to maintain performance over a range of duty cycles. While it is specified and performance is quaranteed with a 50% clock duty cycle and 60 Msps, ADC08L060 performance is typically maintained with clock high and low times of 0.83 ns, corresponding to a clock duty cycle range of 5% to 95% with a 60 MHz clock. Note that minimum low and high times may not be simultaneously asserted.

Applications Information (Continued)

4.2.2 Clock Line Termination

The **CLOCK** line should be series terminated at the clock source in the characteristic impedance of that line. If the clock line is longer than

$$\frac{t_r}{6 \times t_{prop}}$$

where t_r is the clock rise time and t_{prop} is the propagation rate of the signal along the trace, the **CLOCK** pin should be a.c. terminated with a series RC to ground such that the resisitor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times L \times t_{prop}}{Z_o}$$

where "L" is the line length in inches and Z_o is the characteristic impedance of the clock line. Typical t_{PROP} is about 150 ps/inch on FR-4 board material. For FR-4 board material, the value of C becomes

$$C \geq \frac{6 \times 10^{-10} \times L}{Z_o}$$

This termination should be located as close as possible to, but within one centimeter of, the ADC08L060 clock pin.

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A combined analog and digital ground plane should be used.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise because of the skin effect. Total surface area is more important than is total ground plane volume. Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near a straight line between the ADC or any linear component and the power supply area as the resulting common return current path could cause fluctuation in the analog input "ground" return of the ADC.

To keep analog and digital (ground) return currents separate from each other (which minimizes noise coupling into the ADC input through the ground plane) use traces rather than a solid plane to route power to all components. Analog and digital power should be routed as far from each other as is practical. The analog power trace should also be routed away from digital areas of the board.

Noise performance is also enhanced by driving a single gate with each ADC output pin and locating the gate as close as possible to the ADC output. Inserting a 47Ω resistor in series with the ADC digital output pins will also help reduce ADC noise. Be sure to keep the resistors as close to the ADC output pins as possible. Eliminating ground plane copper beneath the ADC output lines can also help ADC noise performance, but could produce unacceptable radiation from the board.

Analog and digital circuitry should be kept well away from each other. Especially troublesome is high power digital components such as processors and large PLDs. Switch mode power supplies, including capacitive DC-DC converters, can cause noise problems with high speed ADCs. Keep such components well away from ADCs and low level analog signal areas. Such components should be located as close to the power supply as possible and should not be in the path of analog signal or power supply currents.

Digital circuits create substantial supply and ground current transients. The noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one that employs non-saturating transistor designs, or has low noise characteristics, like the 74LS and the 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74HC, 74F and 74AC(T) families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90˚ crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground plane.

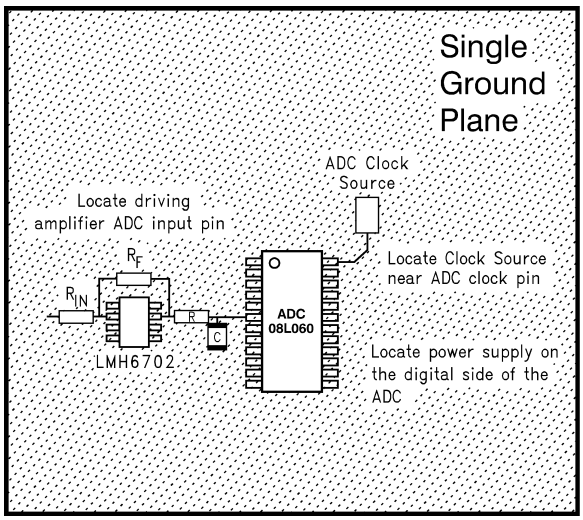


FIGURE 5. Layout Example

Figure 5 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed together away from any digital components.

6.0 DYNAMIC PERFORMANCE

The ADC08L060 is ac tested and its dynamic performance is guaranteed. To meet the published specifications, the clock source driving the CLK input should exhibit less than 10 ps

Applications Information (Continued)

(rms) of jitter. For best ac performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See *Figure 6*.

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path.

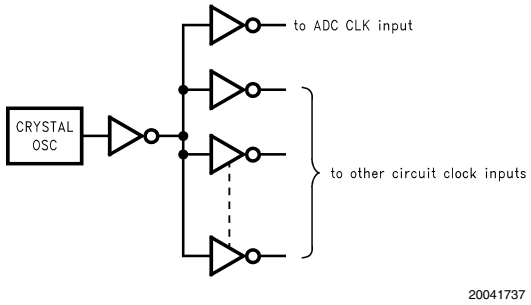


FIGURE 6. Isolating the ADC Clock from Digital Circuitry

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A 51Ω resistor in series with the offending digital input will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC08L060. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current is required from V_{DR} and DR GND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with a 74F541, for example) may be necessary if the data bus capacitance exceeds 5 pF. Dynamic performance can also be improved by adding 33Ω to 47Ω series resistors at each digital output, reducing the energy coupled back into the converter input pins.

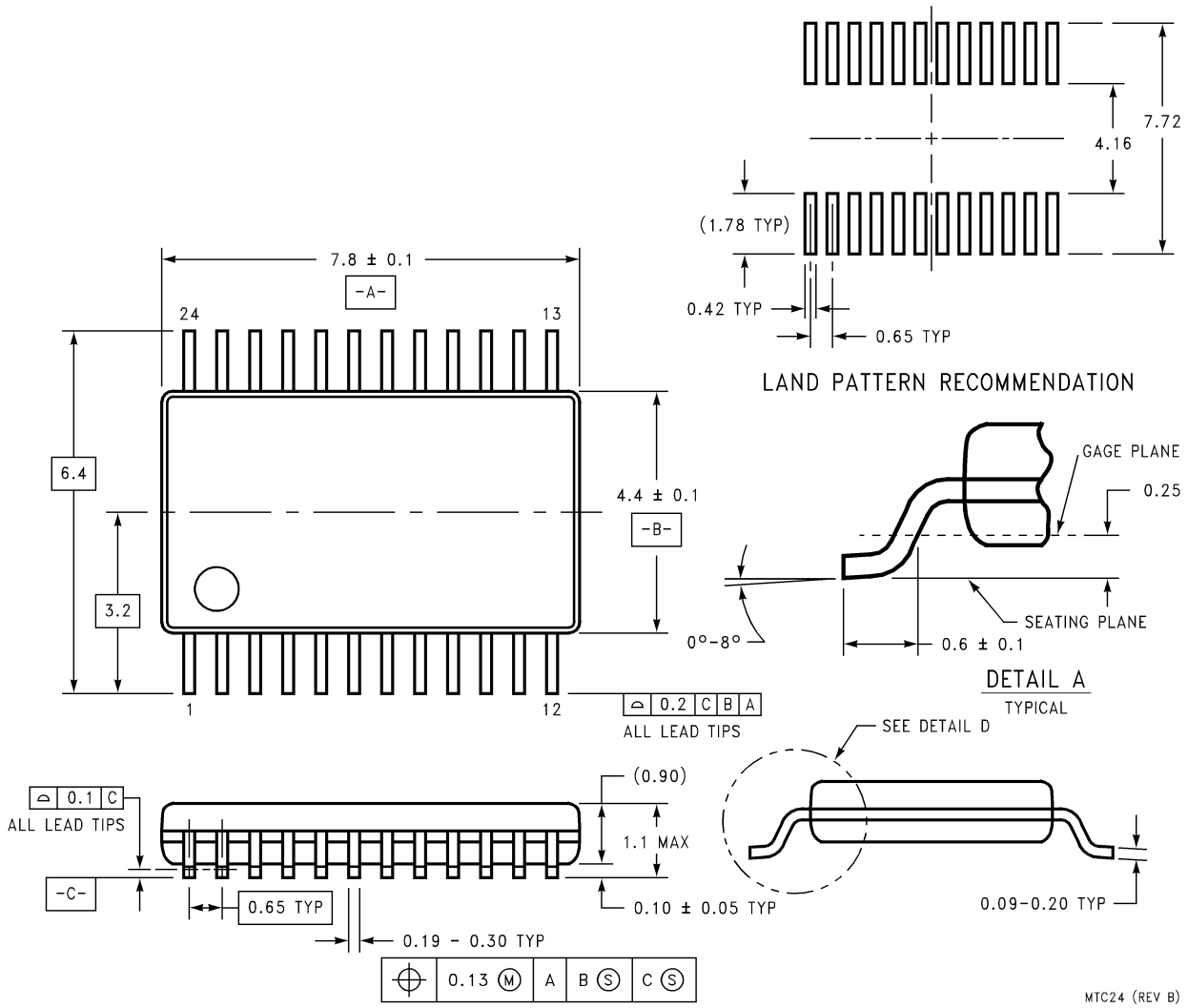
Using an inadequate amplifier to drive the analog input. As explained in Section 2.0, the capacitance seen at the input alternates between 3 pF and 4 pF with the clock. This dynamic capacitance is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device.

Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in Section 1.0, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. The use of simple gates with RC timing is generally inadequate as a clock source.

Physical Dimensions inches (millimeters)

unless otherwise noted



NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JECED REGISTRATION mo-153, VARIATION AD, DATED 7/93.

24-Lead Package TC
Order Number ADC08L060CIMT
NS Package Number MTC24

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.