Ultralow Distortion Current Feedback Differential ADC Driver

Data Sheet

ADA4927-1/ADA4927-2

FEATURES

- Extremely low harmonic distortion
  - −105 dBc HD2 at 10 MHz
  - −91 dBc HD2 at 70 MHz
  - −87 dBc HD2 at 100 MHz
  - −103 dBc HD3 at 10 MHz
  - −98 dBc HD3 at 70 MHz
  - −89 dBc HD3 at 100 MHz
- Better distortion at higher gains than VF amplifiers
- Low input voltage noise: 1.4 nV/√Hz
- High speed
  - −3 dB bandwidth of 2.3 GHz
  - 0.1 dB gain flatness: 150 MHz
  - Slew rate: 5000 V/µs, 25% to 75%
  - Fast 0.1% settling time: 10 ns
- Low input offset voltage: 0.3 mV typical
- Externally adjustable gain
- Stability and bandwidth controlled by feedback resistor
- Differential-to-differential or single-ended-to-differential operation
- Adjustable output common-mode voltage
- Wide supply operation: +5 V to ±5 V

APPLICATIONS

- ADC drivers
- Single-ended-to-differential converters
- IF and baseband gain blocks
- Differential buffers
- Differential line drivers

GENERAL DESCRIPTION

The ADA4927 is a low noise, ultralow distortion, high speed, current feedback differential amplifier that is an ideal choice for driving high performance ADCs with resolutions up to 16 bits from dc to 100 MHz. The output common-mode level can easily be matched to the required ADC input common-mode levels. The internal common-mode feedback loop provides exceptional output balance and suppression of even-order distortion products. Differential gain configurations are easily realized using an external feedback network comprising four resistors. The current feedback architecture provides loop gain that is nearly independent of closed-loop gain, achieving wide bandwidth, low distortion, and low noise at higher gains and lower power consumption than comparable voltage feedback amplifiers. The ADA4927 is fabricated using the Analog Devices, Inc., silicon-germanium complementary bipolar process, enabling very low levels of distortion with an input voltage noise of only 1.3 nV/√Hz.

FUNCTIONAL BLOCK DIAGRAMS

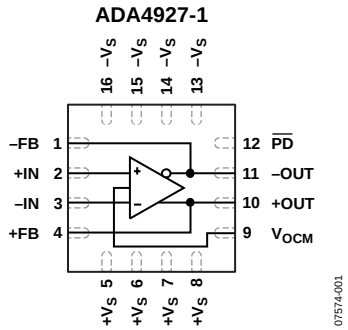


Figure 1.

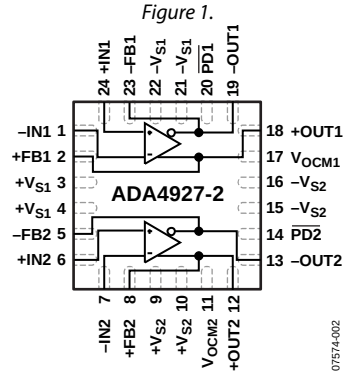


Figure 2.

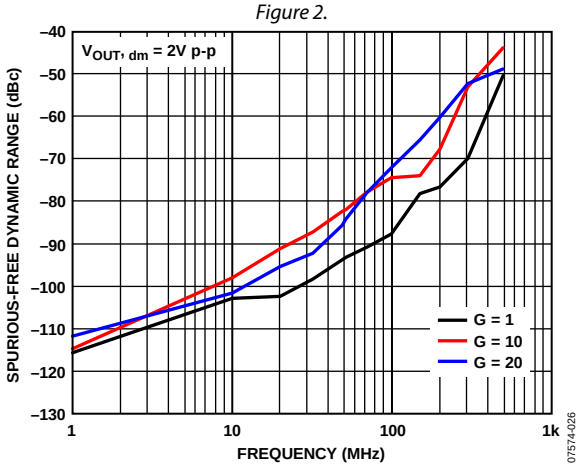


Figure 3. Spurious-Free Dynamic Range vs. Frequency at Various Gains

The low dc offset and excellent dynamic performance of the ADA4927 make it well suited for a wide variety of data acquisition and signal processing applications.

The ADA4927-1 is available in a Pb-free, 3 mm × 3 mm 16-lead LFCSP, and the ADA4927-2 is available in a Pb-free, 4 mm × 4 mm 24-lead LFCSP. The pinouts are optimized to facilitate printed circuit board (PCB) layout and to minimize distortion. They are specified to operate over the −40°C to +105°C temperature range.

Rev. B
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REVISION HISTORY

5/2016—Rev. A to Rev. 0

Changes to Figure 1 and Figure 2 ... 1
Changes to Figure 5 ... 8
Changes to Figure 6 ... 9
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25

8/2009—Rev. 0 to Rev. A

Changes to Ordering Guide ... 24

10/2008—Revision 0: Initial Version

SPECIFICATIONS

±5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = − 5 V, V_{OCM} = 0 V, R_F = 301 Ω, R_G = 301 Ω, R_T = 56.2 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 46 for signal definitions.

±D_{IN} to $V_{OUT, dm}$ Performance

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p		2300		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, dm}$ = 2.0 V p-p		1500		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 0.1 V p-p, ADA4927-1		150		MHz
	$V_{OUT, dm}$ = 0.1 V p-p, ADA4927-2		120		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V step, 25% to 75%		5000		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 2 V step		10		ns
Overdrive Recovery Time	V_{IN} = 0 V to 0.9 V step, G = 10		10		ns
NOISE/HARMONIC PERFORMANCE	See Figure 45 for distortion test circuit				
Second Harmonic	$V_{OUT, dm}$ = 2 V p-p, 10 MHz		−105		dBc
	$V_{OUT, dm}$ = 2 V p-p, 70 MHz		−91		dBc
	$V_{OUT, dm}$ = 2 V p-p, 100 MHz		−87		dBc
Third Harmonic	$V_{OUT, dm}$ = 2 V p-p, 10 MHz		−103		dBc
	$V_{OUT, dm}$ = 2 V p-p, 70 MHz		−98		dBc
	$V_{OUT, dm}$ = 2 V p-p, 100 MHz		−89		dBc
IMD	f_1 = 70 MHz, f_2 = 70.1 MHz, $V_{OUT, dm}$ = 2 V p-p		−94		dBc
	f_1 = 140 MHz, f_2 = 140.1 MHz, $V_{OUT, dm}$ = 2 V p-p		−85		dBc
Voltage Noise (RTI)	f = 100 kHz, G = 28		1.4		nV/√Hz
Input Current Noise	f = 100 kHz, G = 28		14		pA/√Hz
Crosstalk	f = 100 MHz, ADA4927-2		−75		dB
INPUT CHARACTERISTICS					
Offset Voltage	$V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−1.3	+0.3	+1.3	mV
	t_{MIN} to t_{MAX} variation		±1.5		µV/°C
Input Bias Current		−15	+0.5	+15	µA
	t_{MIN} to t_{MAX} variation		±0.1		µA/°C
Input Offset Current		−10.5	−0.6	+10.5	µA
Input Resistance	Differential		14		Ω
	Common mode		120		kΩ
Input Capacitance	Differential		0.5		pF
Input Common-Mode Voltage Range		−3.5		+3.5	V
Common-Mode Rejection Ratio (CMRR)	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V	−70	−93		dB
Open-Loop Transresistance	DC	120	185		kΩ
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, $R_F = R_G$ = 10 kΩ	−3.8		+3.8	V
Linear Output Current			65		mA p-p
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 1 V, 10 MHz, see Figure 44 for test circuit		−65		dB

V_{OCM} to $V_{OUT, cm}$ Performance

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
Small Signal −3 dB Bandwidth	$V_{OUT, cm}$ = 100 mV p-p		1300		MHz
Slew Rate	V_{IN} = −1.0 V to +1.0 V, 25% to 75%		1000		V/µs
Input Voltage Noise (RTI)	f = 100 kHz		15		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			±3.5		V
Input Resistance		3.8	5.0	7.5	kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$, $V_{DIN+} = V_{DIN-} = +V_S/2$	−10	−2	+5.2	mV
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	−70	−97		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.90	0.97	1.00	V/V

General Performance

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		11.0	V
Quiescent Current per Amplifier			20.0	22.1	mA
	t_{MIN} to t_{MAX} variation		±9.0		µA/°C
	Powered down			2.4	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$, ΔV_S = 1 V	−70	−89		dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		<1.8		V
	Enabled		>3.2		V
Turn-Off Time	To 0.1%		15		µs
Turn-On Time	To 0.1%		400		ns
$\overline{PD}$ Pin Bias Current per Amplifier					
Enabled	$\overline{PD}$ = 5 V	−2		+2	µA
Disabled	$\overline{PD}$ = 0 V	−110		−90	µA
OPERATING TEMPERATURE RANGE		−40		+105	°C

+5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, V_{OCM} = 2.5 V, R_F = 301 Ω, R_G = 301 Ω, R_T = 56.2 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 46 for signal definitions.

$\pm D_{IN}$ to $V_{OUT, dm}$ Performance

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p		2000		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, dm}$ = 2.0 V p-p		1300		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 0.1 V p-p, ADA4927-1		150		MHz
	$V_{OUT, dm}$ = 0.1 V p-p, ADA4927-2		110		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V step, 25% to 75%		4200		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 2 V step		10		ns
Overdrive Recovery Time	V_{IN} = 0 V to 0.15 V step, G = 10		10		ns
NOISE/HARMONIC PERFORMANCE	See Figure 45 for distortion test circuit				
Second Harmonic	$V_{OUT, dm}$ = 2 V p-p, 10 MHz		−104		dBc
	$V_{OUT, dm}$ = 2 V p-p, 70 MHz		−91		dBc
	$V_{OUT, dm}$ = 2 V p-p, 100 MHz		−86		dBc
Third Harmonic	$V_{OUT, dm}$ = 2 V p-p, 10 MHz		−95		dBc
	$V_{OUT, dm}$ = 2 V p-p, 70 MHz		−80		dBc
	$V_{OUT, dm}$ = 2 V p-p, 100 MHz		−76		dBc
IMD	f_1 = 70 MHz, f_2 = 70.1 MHz, $V_{OUT, dm}$ = 2 V p-p		−93		dBc
	f_1 = 140 MHz, f_2 = 140.1 MHz, $V_{OUT, dm}$ = 2 V p-p		−84		dBc
Voltage Noise (RTI)	f = 100 kHz, G = 28		1.4		nV/√Hz
Input Current Noise	f = 100 kHz, G = 28		19		pA/√Hz
Crosstalk	f = 100 MHz, ADA4927-2		−75		dB
INPUT CHARACTERISTICS					
Offset Voltage	$V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−1.3	+0.3	+1.3	mV
	t_{MIN} to t_{MAX} variation		±1.5		µV/°C
Input Bias Current		−30	−12	+4.0	µA
	t_{MIN} to t_{MAX} variation		±0.12		µA/°C
Input Offset Current		−10.5	−0.8	+10.5	µA
Input Resistance	Differential		14		Ω
	Common mode		120		kΩ
Input Capacitance	Differential		0.5		pF
Input Common-Mode Voltage Range		1.3		3.7	V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V	−70	−96		dB
Open-Loop Transresistance	DC	120	185		kΩ
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output	+1.0		+4.0	V
Linear Output Current			50		mA p-p
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 1 V, 10 MHz, see Figure 44 for test circuit		−65		dB

V_{OCM} to $V_{OUT, cm}$ Performance

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
Small signal −3 dB Bandwidth	$V_{OUT, cm}$ = 100 mV p-p		1300		MHz
Slew Rate	V_{IN} = 1.5 V to 3.5 V, 25% to 75%		1000		V/µs
Input Voltage Noise (RTI)	f = 100 kHz		15		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			1.5 to 3.5		V
Input Resistance		3.8	5.0	7.5	kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$, $V_{DIN+} = V_{DIN-} = +V_S/2$	−5.0	+2.0	+10	mV
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	−70	−100		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.90	0.97	1.00	V/V

General Performance

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		11.0	V
Quiescent Current per Amplifier			20	21.6	mA
	t_{MIN} to t_{MAX} variation		±7.0		µA/°C
	Powered down			0.6	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$, ΔV_S = 1 V	−70	−89		dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		<1.7		V
	Enabled		>3.0		V
Turn-Off Time			20		µs
Turn-On Time			500		ns
$\overline{PD}$ Pin Bias Current per Amplifier					
Enabled	$\overline{PD}$ = 5 V	−2		+2	µA
Disabled	$\overline{PD}$ = 0 V	−105		−95	µA
OPERATING TEMPERATURE RANGE		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 4
Input Currents +IN, –IN, $\overline{PD}$	±5 mA
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD 51-7.

Table 8.

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	87	°C/W
24-Lead LFCSP (Exposed Pad)	47	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4927 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes the properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4927. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/ exposed pad from metal traces, throughholes, ground, and power planes reduces θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the single 16-lead LFCSP (87°C/W) and the dual 24-lead LFCSP (47°C/W) on a JEDEC standard
4-layer board with the exposed pad soldered to a PCB pad that is connected to a solid plane.

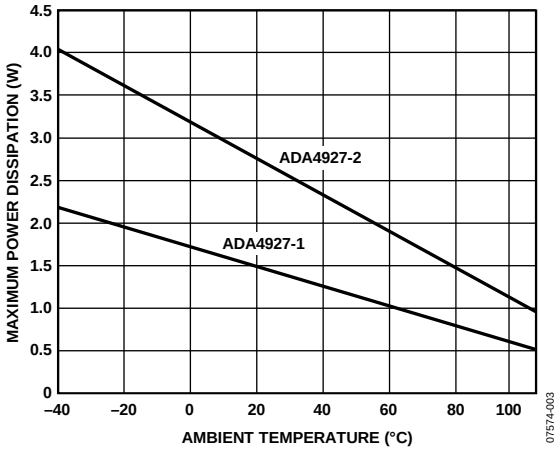


Figure 4. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

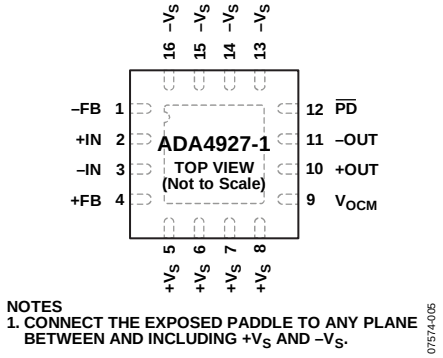


Figure 5. ADA4927-1 Pin Configuration

Table 9. ADA4927-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−FB	Negative Output for Feedback Component Connection
2	+IN	Positive Input Summing Node
3	−IN	Negative Input Summing Node
4	+FB	Positive Output for Feedback Component Connection
5 to 8	$+V_S$	Positive Supply Voltage
9	V_{OCM}	Output Common-Mode Voltage
10	+OUT	Positive Output for Load Connection
11	−OUT	Negative Output for Load Connection
12	$\overline{PD}$	Power-Down Pin
13 to 16	$-V_S$	Negative Supply Voltage
17 (EPAD)	Exposed Pad (EPAD)	Connect the exposed pad to any plane between and including $+V_S$ and $-V_S$.

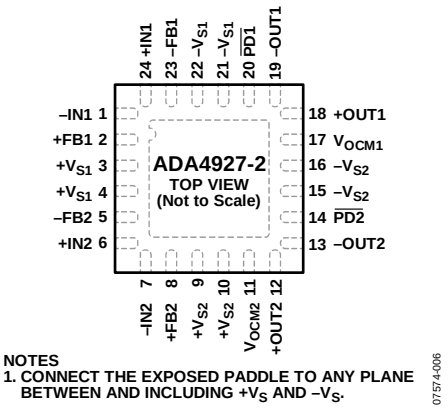


Figure 6. ADA4927-2 Pin Configuration

Table 10. ADA4927-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN1	Negative Input Summing Node 1
2	+FB1	Positive Output Feedback 1
3, 4	$+V_{S1}$	Positive Supply Voltage 1
5	−FB2	Negative Output Feedback 2
6	+IN2	Positive Input Summing Node 2
7	−IN2	Negative Input Summing Node 2
8	+FB2	Positive Output Feedback 2
9, 10	$+V_{S2}$	Positive Supply Voltage 2
11	V_{OCM2}	Output Common-Mode Voltage 2
12	+OUT2	Positive Output 2
13	−OUT2	Negative Output 2
14	$\overline{PD2}$	Power-Down Pin 2
15, 16	$-V_{S2}$	Negative Supply Voltage 2
17	V_{OCM1}	Output Common-Mode Voltage 1
18	+OUT1	Positive Output 1
19	−OUT1	Negative Output 1
20	$\overline{PD1}$	Power-Down Pin 1
21, 22	$-V_{S1}$	Negative Supply Voltage 1
23	−FB1	Negative Output Feedback 1
24	+IN1	Positive Input Summing Node 1
25 (EPAD)	Exposed Pad (EPAD)	Connect the exposed pad to any plane between and including $+V_S$ and $-V_S$.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, V_{OCM} = 0 V, R_G = 301 Ω, R_F = 301 Ω, R_T = 56.2 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. Refer to Figure 43 for basic test setup. Refer to Figure 46 for signal definitions.

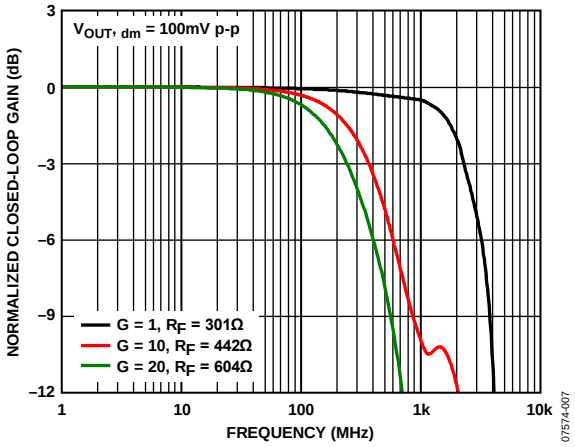


Figure 7. Small Signal Frequency Response for Various Gains

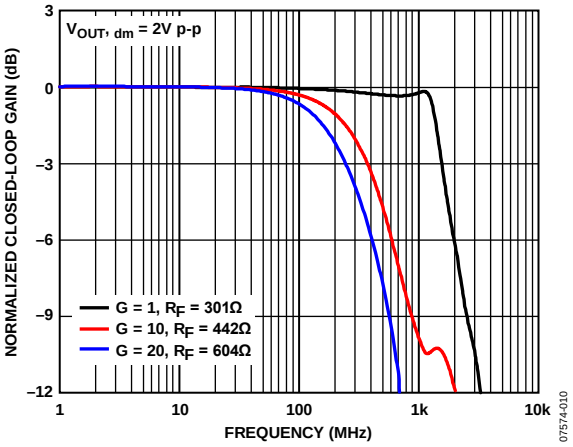


Figure 10. Large Signal Frequency Response for Various Gains

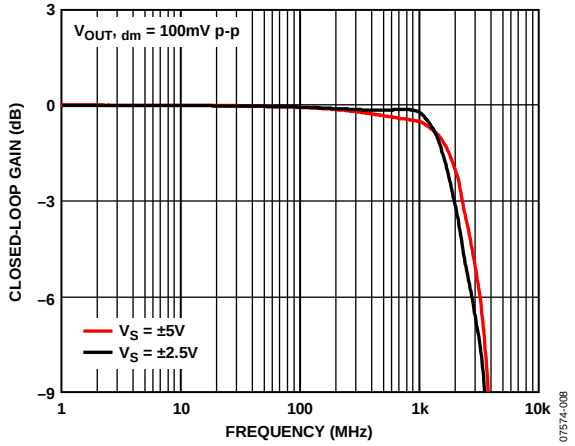


Figure 8. Small Signal Frequency Response for Various Supplies

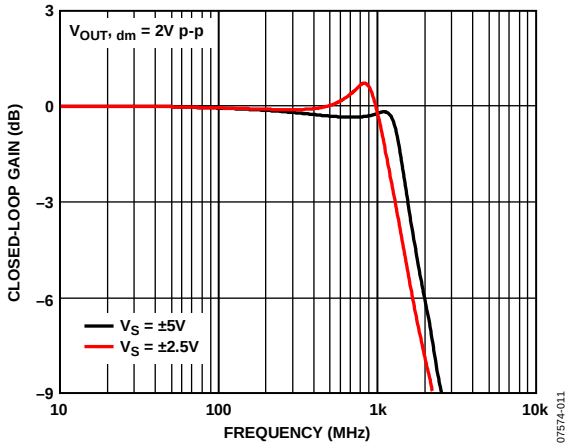


Figure 11. Large Signal Frequency Response for Various Supplies

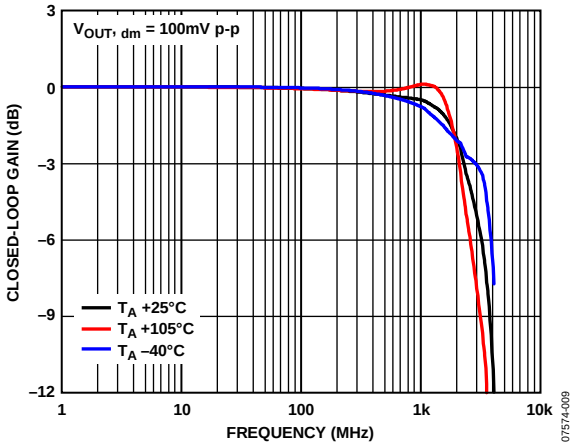


Figure 9. Small Signal Frequency Response for Various Temperatures

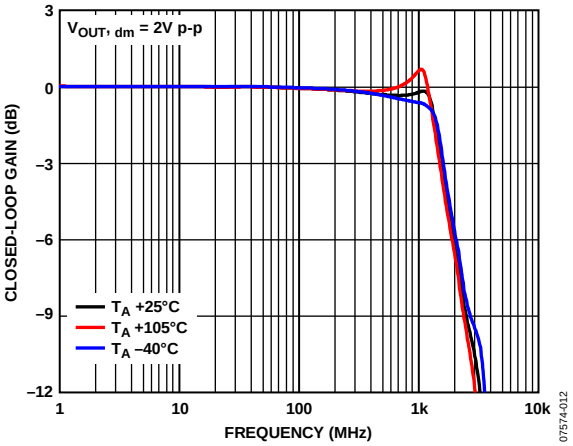


Figure 12. Large Signal Frequency Response for Various Temperatures

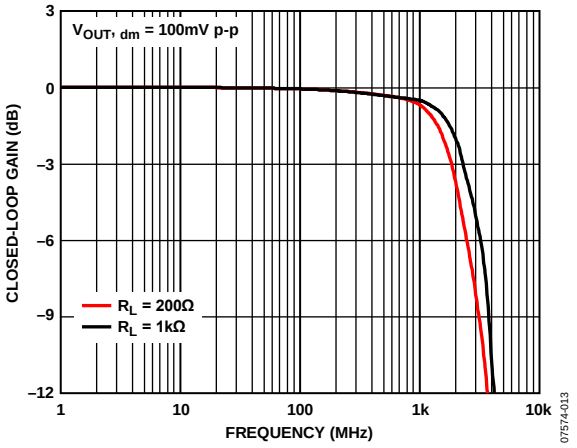


Figure 13. Small Signal Frequency Response for Various Loads

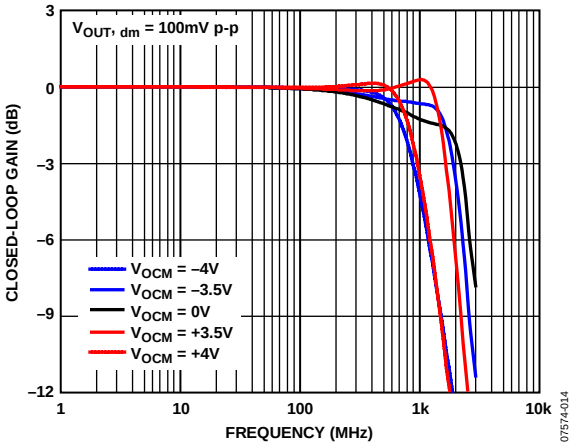


Figure 14. Small Signal Frequency Response at Various V_{OCM} Levels

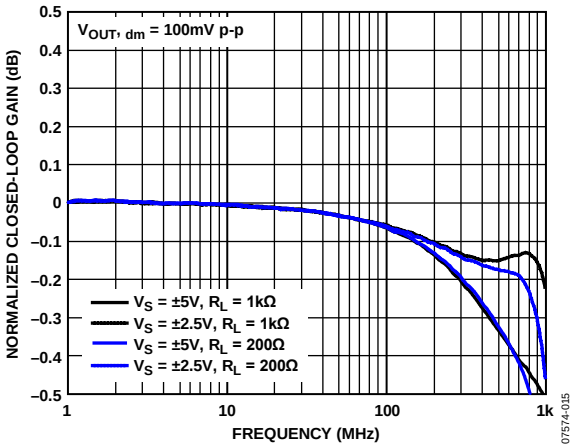


Figure 15. 0.1 dB Flatness Small Signal Frequency Response for Various Loads and Supplies

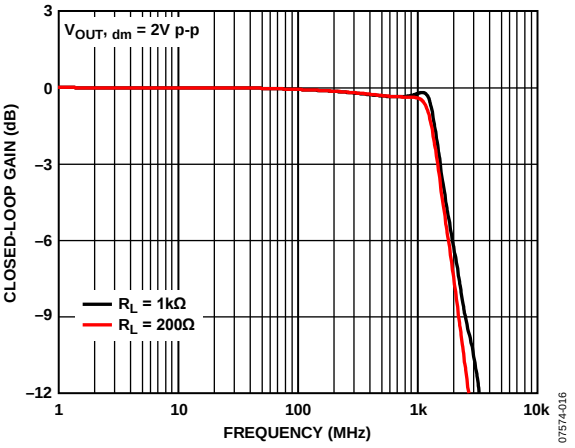


Figure 16. Large Signal Frequency Response for Various Loads

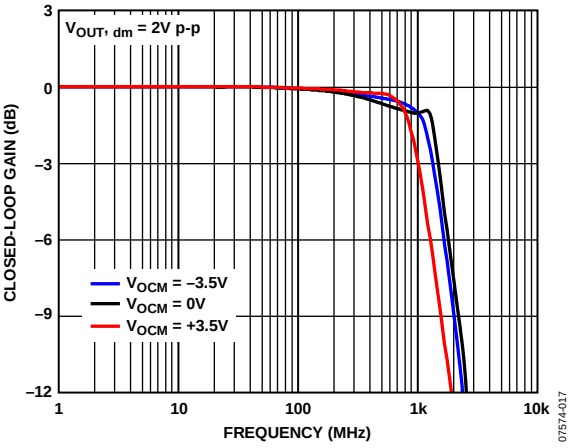


Figure 17. Large Signal Frequency Response at Various V_{OCM} Levels

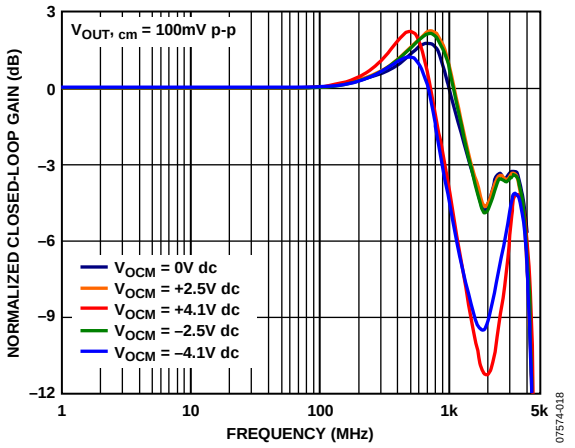


Figure 18. V_{OCM} Small Signal Frequency Response at Various DC Levels

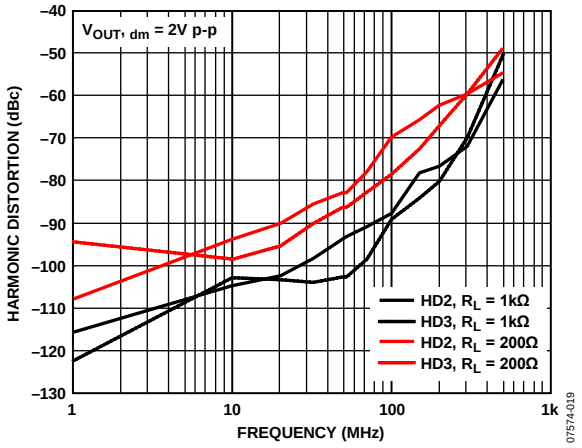


Figure 19. Harmonic Distortion vs. Frequency at Various Loads

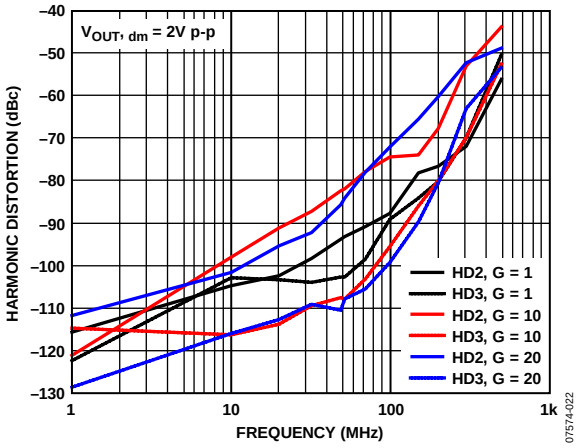


Figure 22. Harmonic Distortion vs. Frequency at Various Gains

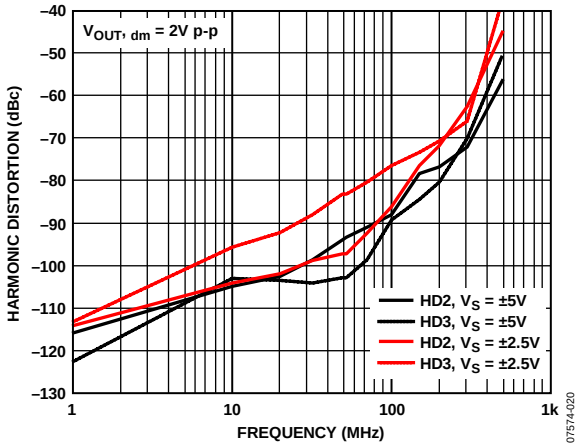


Figure 20. Harmonic Distortion vs. Frequency at Various Supplies

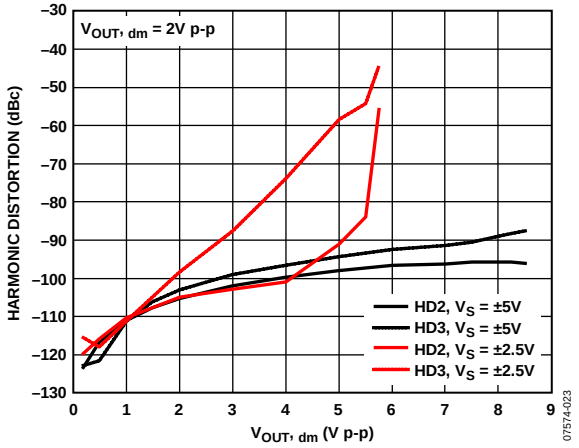


Figure 23. Harmonic Distortion vs. $V_{OUT, dm}$ and Supply Voltage, f = 10 MHz

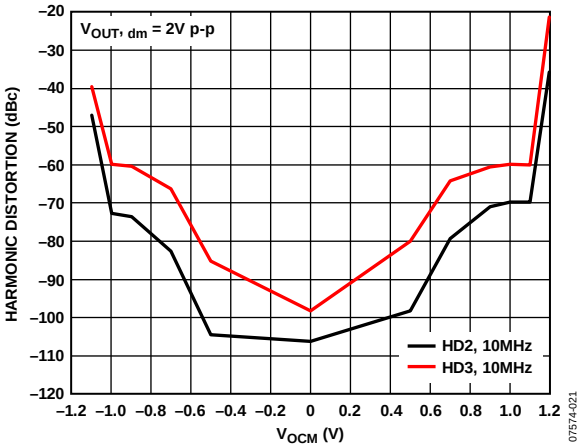


Figure 21. Harmonic Distortion vs. V_{OCM} at 10 MHz, ±2.5 V Supplies

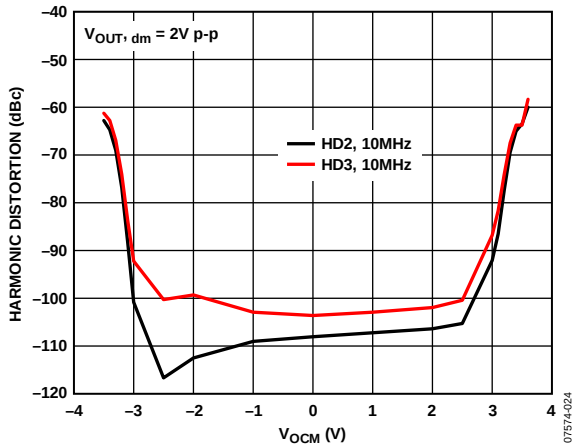


Figure 24. Harmonic Distortion vs. V_{OCM} at 10 MHz, ±5 V Supplies

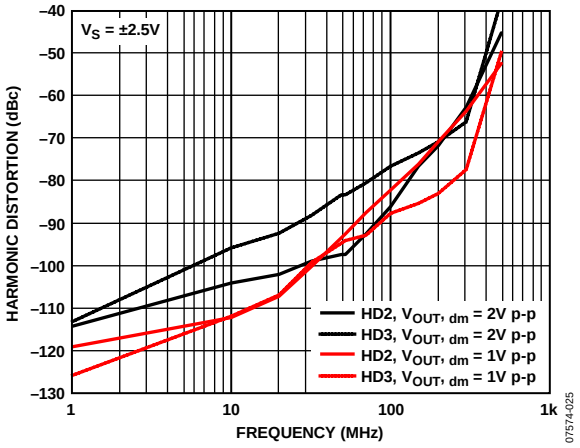


Figure 25. Harmonic Distortion vs. Frequency at Various $V_{OUT, dm}$

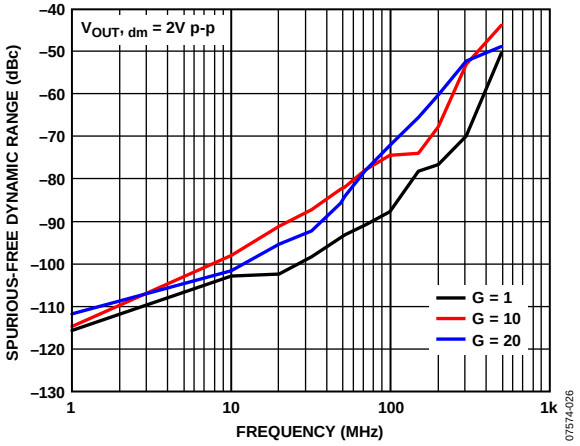


Figure 26. Spurious-Free Dynamic Range vs. Frequency at Various Gains

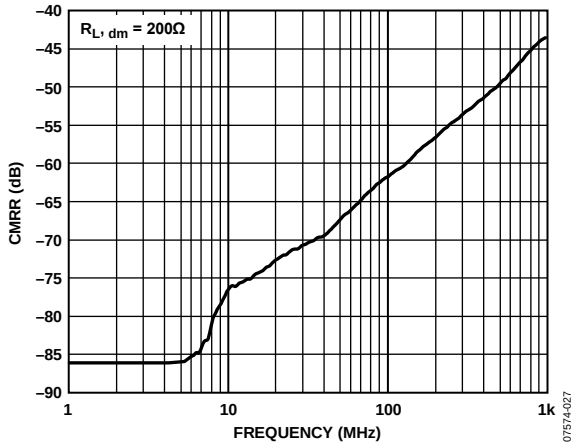


Figure 27. CMRR vs. Frequency

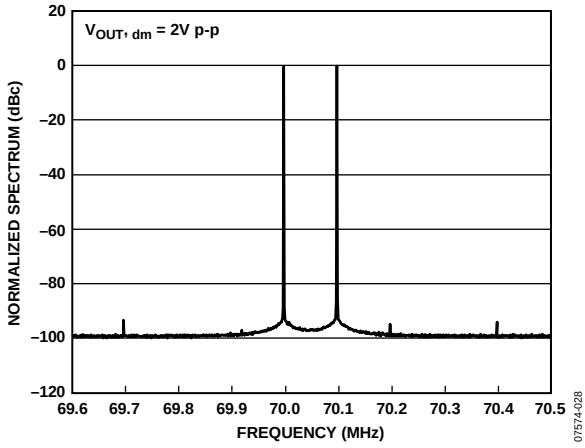


Figure 28. 70 MHz Intermodulation Distortion

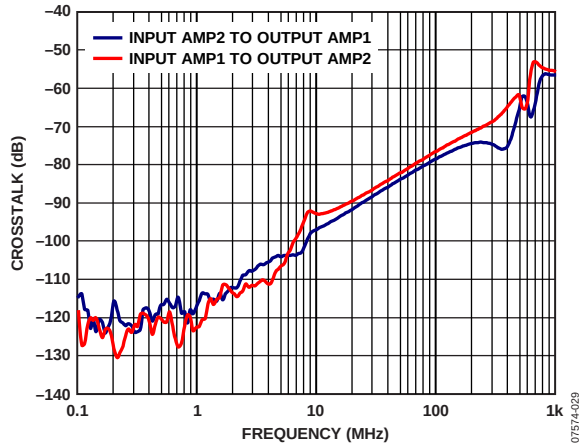


Figure 29. Crosstalk vs. Frequency for ADA4927-2

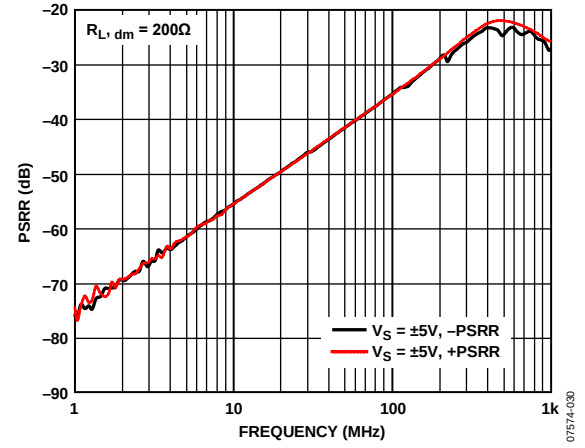


Figure 30. Power Supply Rejection Ratio vs. Frequency

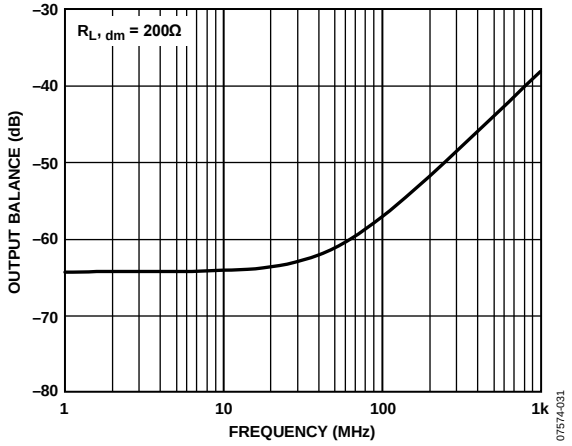


Figure 31. Output Balance vs. Frequency

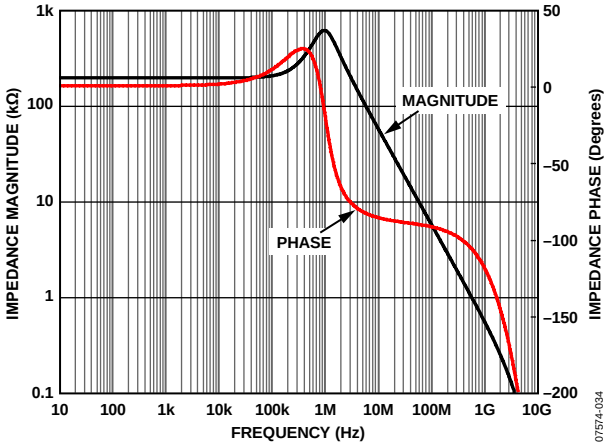


Figure 34. Open-Loop Transimpedance Magnitude and Phase vs. Frequency

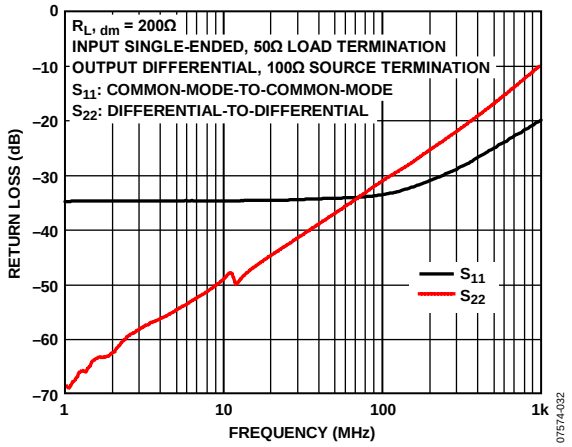


Figure 32. Return Loss (S_{11}, S_{12}) vs. Frequency

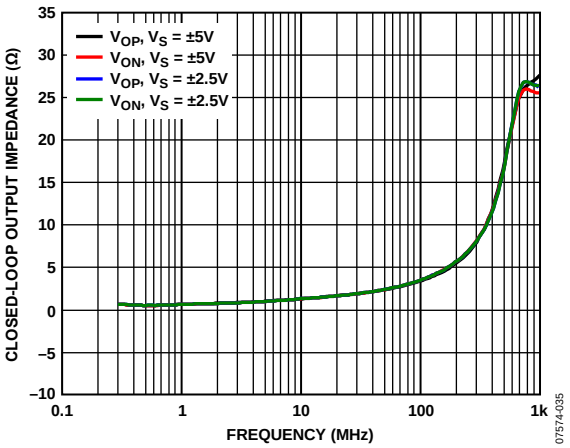


Figure 35. Closed-Loop Output Impedance Magnitude vs. Frequency at Various Supplies, G = 1

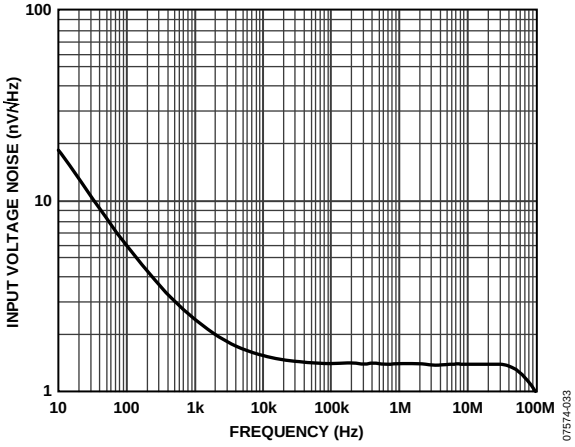


Figure 33. Voltage Noise Spectral Density, Referred to Input

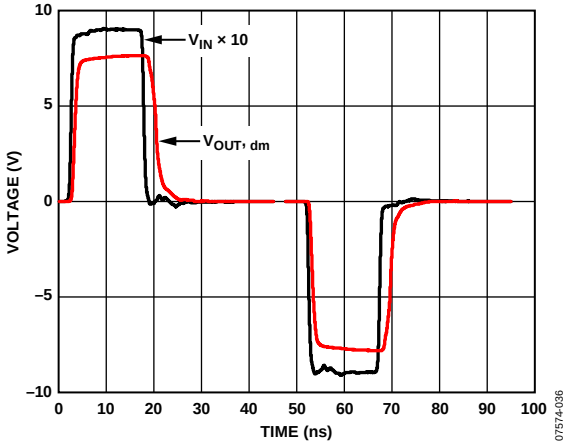


Figure 36. Overdrive Recovery, G = 10

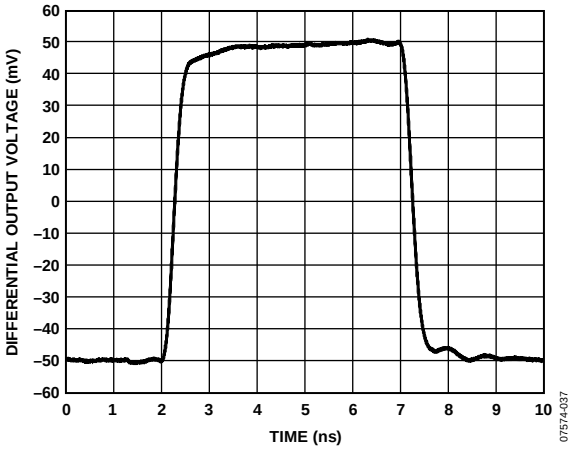


Figure 37. Small Signal Pulse Response

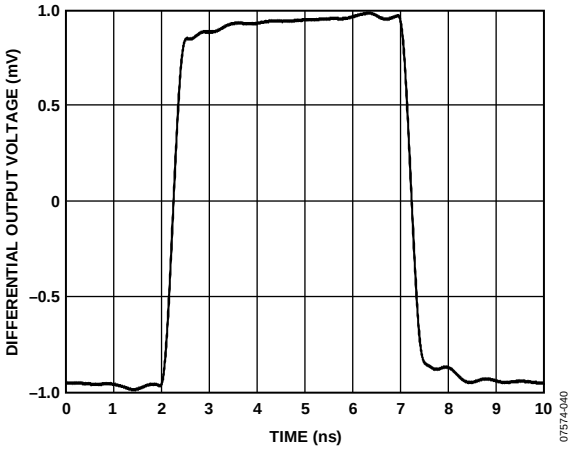


Figure 40. Large Signal Pulse Response

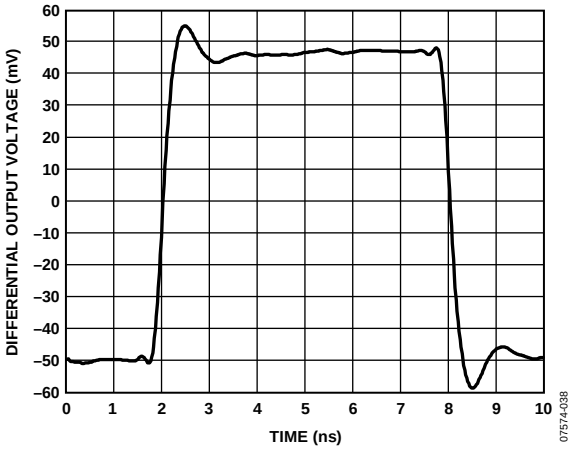


Figure 38. V_{OCM} Small Signal Pulse Response

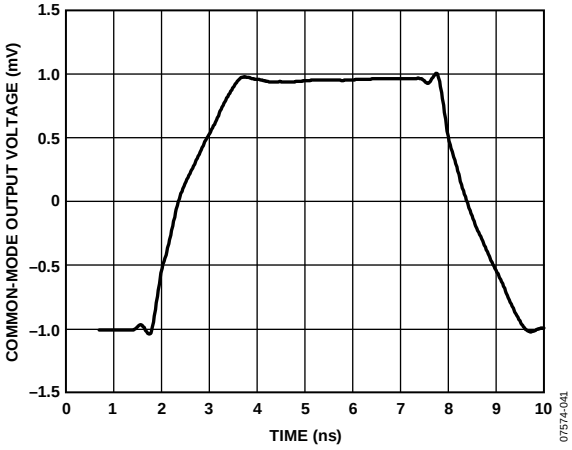


Figure 41. V_{OCM} Large Signal Pulse Response

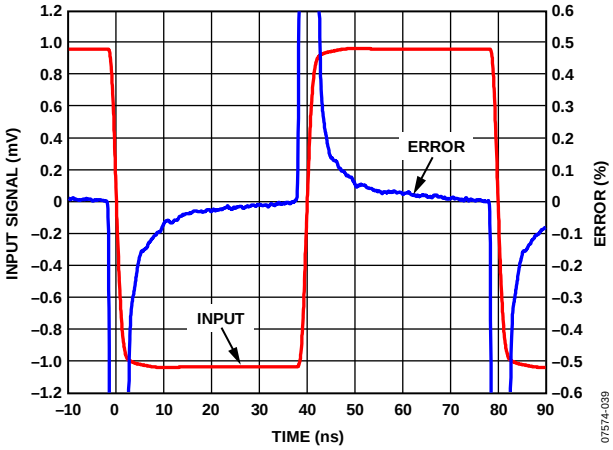


Figure 39. Settling Time

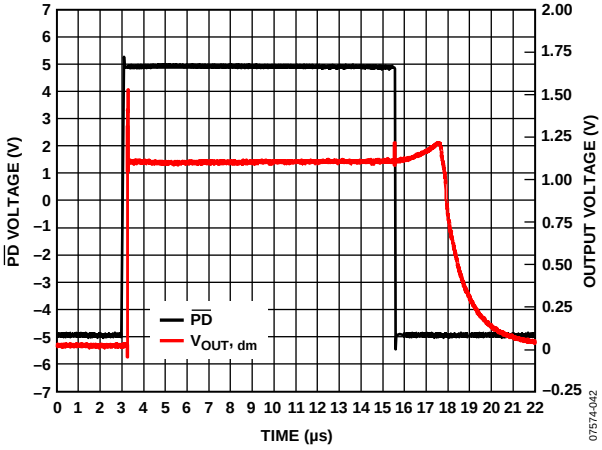


Figure 42. $\overline{PD}$ Response Time

TEST CIRCUITS

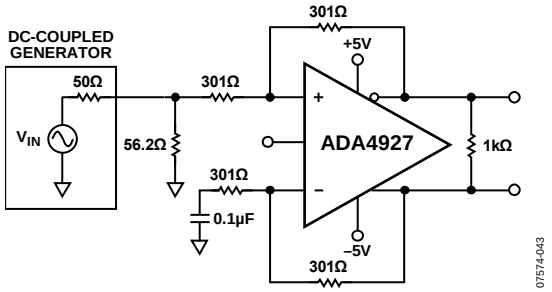


Figure 43. Equivalent Basic Test Circuit, G = 1

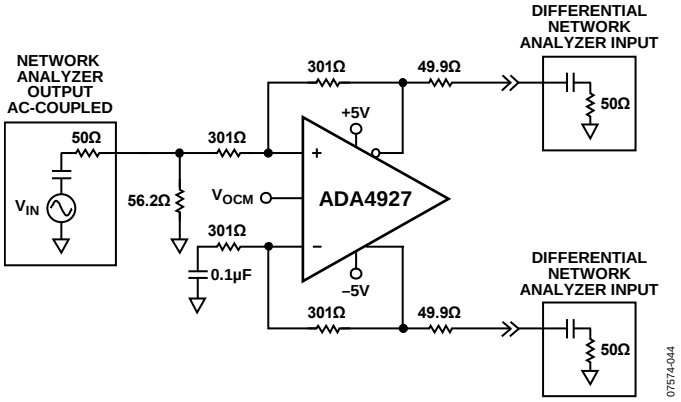


Figure 44. Test Circuit for Output Balance, CMRR

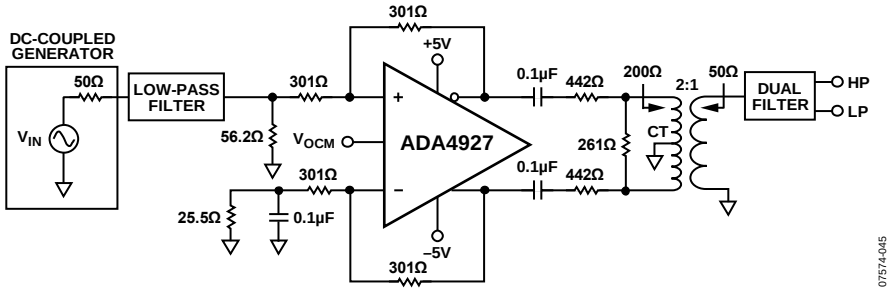


Figure 45. Test Circuit for Distortion Measurements

THEORY OF OPERATION

The ADA4927 differs from conventional operational amplifiers in that it has two outputs whose voltages move in opposite directions and an additional input, V_{OCM}. Moreover, the ADA4927 uses a current feedback architecture. Like a traditional current feedback operational amplifier, the ADA4927 relies on high open-loop trans-impedance, T(s), and negative current feedback to force the outputs to the desired voltages. The ADA4927 behaves much like a standard current feedback operational amplifier and facilitates single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Also, like a current feedback operational amplifier, the ADA4927 has low input impedance summing nodes, which are actually emitter-follower outputs. The ADA4927 outputs are low impedance, and the closed-loop output impedances are equal to the open-loop output impedances divided by a factor of 1 + loop gain. Because it uses current feedback, the ADA4927 manifests a nominally constant feed-back resistance, bandwidth product. In other words, the closed-loop bandwidth and stability of the ADA4927 depend primarily on the feedback resistor value. The closed-loop gain equations for typical configurations are the same as those of comparable voltage feedback differential amplifiers. The chief difference is that the ADA4927 dynamic performance depends on the feed-back resistor value rather than on the noise gain. Because of this, the elements used in the feedback loops must be resistive with values that ensure stability and sufficient bandwidth.

Two feedback loops are employed to control the differential and common-mode output voltages. The differential feedback loops use a current feedback architecture with external resistors and control only the differential output voltage. The common-mode feedback loop is internal, uses voltage feedback, and controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value within the specified limits. The output common-mode voltage is forced, by the internal common-mode loop, to be equal to the voltage applied to the V_{OCM} input.

The internal common-mode feedback loop produces outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. This results in differential outputs that are very close to the ideal of being identical in amplitude and are exactly 180° apart in phase.

DEFINITION OF TERMS

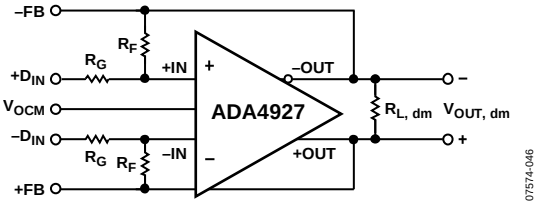


Figure 46. Circuit Definitions

Differential Voltage

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential-mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common ground reference. Similarly, the differential input voltage is defined as

$$V_{IN,\,dm} = (+D_{IN} - (-D_{IN}))$$

Common-Mode Voltage

Common-mode voltage refers to the average of two node voltages with respect to the local ground reference. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance

Output balance is a measure of how close the differential signals are to being equal in amplitude and opposite in phase. Output balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider midpoint with the magnitude of the differential signal (see Figure 44). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{\Delta V_{OUT,\,cm}}{\Delta V_{OUT,\,dm}} \right|$$

APPLICATIONS INFORMATION

ANALYZING AN APPLICATION CIRCUIT

The ADA4927 uses high open-loop transimpedance and negative current feedback to control the differential output voltage in such a way as to minimize the differential error currents. The differential error currents are defined as the currents that flow in and out of the differential inputs labeled +IN and −IN (see Figure 46). For most purposes, these currents can be assumed to be zero. The voltage between the +IN and −IN inputs is internally bootstrapped to 0 V; therefore, the voltages at the amplifier inputs are equal, and external analysis can be carried out in a similar fashion to that of voltage feedback amplifiers. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these principles, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

Using the approach previously described, the differential gain of the circuit in Figure 46 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This presumes that the input resistors (R_G) and feedback resistors (R_F) on each side are of equal value.

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4927 can be estimated using the noise model in Figure 47. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The output voltage due to v_{nIN} is obtained by multiplying v_{nIN} by the noise gain, G_N (defined in the G_N equation). The noise currents are uncorrelated with the same mean-square value, and each produces an output voltage that is equal to the noise current multiplied by the associated feedback resistance. The noise voltage density at the V_{OCM} pin is v_{nCM}. When the feedback networks have the same feedback factor, as in most cases, the output noise due to v_{nCM} is common mode. Each of the four resistors contributes $(4kTR_{xx})^{1/2}$. The noise from the feedback resistors appears directly at the output, and the noise from each gain resistor appears at the output multiplied by R_F/R_G. Table 11 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

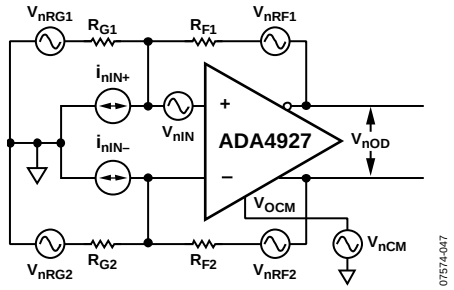


Figure 47. Noise Model

Table 11. Output Noise Voltage Density Calculations for Matched Feedback Networks

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Differential Output Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N(v_{nIN})$
Inverting Input	i_{nIN}	$i_{nIN} \times (R_{F2})$	1	$v_{nO2} = (i_{nIN})(R_{F2})$
Noninverting Input	i_{nIN}	$i_{nIN} \times (R_{F1})$	1	$v_{nO3} = (i_{nIN})(R_{F1})$
V_{OCM} Input	v_{nCM}	v_{nCM}	0	$v_{nO4} = 0$
Gain Resistor, R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	R_{F1}/R_{G1}	$v_{nO5} = (R_{F1}/R_{G1})(4kTR_{G1})^{1/2}$
Gain Resistor, R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	R_{F2}/R_{G2}	$v_{nO6} = (R_{F2}/R_{G2})(4kTR_{G2})^{1/2}$
Feedback Resistor, R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor, R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

Table 12. Differential Input, DC-Coupled

Nominal Gain (dB)	R_F (Ω)	R_G (Ω)	$R_{IN, dm}$ (Ω)	Differential Output Noise Density (nV/√Hz)
0	301	301	602	8.0
20	442	44.2	88.4	21.8
26	604	30.1	60.2	37.9

Table 13. Single-Ended Ground-Referenced Input, DC-Coupled, R_S = 50 Ω

Nominal Gain (dB)	R_F (Ω)	R_{G1} (Ω)	R_T (Ω)	$R_{IN, cm}$ (Ω)	R_{G2} (Ω)[1]	Differential Output Noise Density (nV/√Hz)
0	309	301	56.2	401	328	8.1
20	511	39.2	158	73.2	77.2	18.6
26	806	28	649	54.2	74.4	29.1

[1] RG2 = RG1 + (RS||RT).

Similar to the case of a conventional operational amplifier, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When the feedback factors are matched, $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, β1 = β2 = β, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to zero in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

Table 12 and Table 13 list several common gain settings, associated resistor values, input impedance, and output noise density for both balanced and unbalanced input configurations.

IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

The gain from the V_{OCM} pin to $V_{O, dm}$ is equal to

$$2(\beta1 - \beta2)/(\beta1 + \beta2)$$

When β1 = β2, this term goes to zero and there is no differential output voltage due to the voltage on the V_{OCM} input (including noise). The extreme case occurs when one loop is open and the other has 100% feedback; in this case, the gain from V_{OCM} input to $V_{O, dm}$ is either +2 or −2, depending on which loop is closed.

The feedback loops are nominally matched to within 1% in most applications, and the output noise and offsets due to the V_{OCM} input are negligible. If the loops are intentionally mismatched by a large amount, it is necessary to include the gain term from V_{OCM} to $V_{O, dm}$ and account for the extra noise. For example, if β1 = 0.5 and β2 = 0.25, the gain from V_{OCM} to $V_{O, dm}$ is 0.67. If the V_{OCM} pin is set to 2.5 V, a differential offset voltage is present at the output of (2.5 V)(0.67) = 1.67 V. The differential output noise contribution is (15 nV/√Hz)(0.67) = 10 nV/√Hz. Both of these results are undesirable in most applications; therefore, it is best to use nominally matched feedback factors.

Mismatched feedback networks also result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional operational amplifier.

As a practical summarization of the previous issues, resistors of 1% tolerance produce a worst-case input CMRR of approximately 40 dB, a worst-case differential-mode output offset of 25 mV due to a 2.5 V V_{OCM} input, negligible V_{OCM} noise contribution, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE FOR AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 48, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = R_G + R_G = 2 \times R_G$.

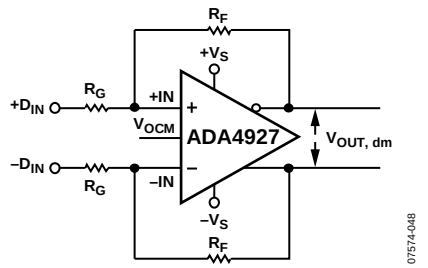


Figure 48. The ADA4927 Configured for Balanced (Differential) Inputs

For an unbalanced, single-ended input signal (see Figure 49), the input impedance is

$$R_{IN,SE} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

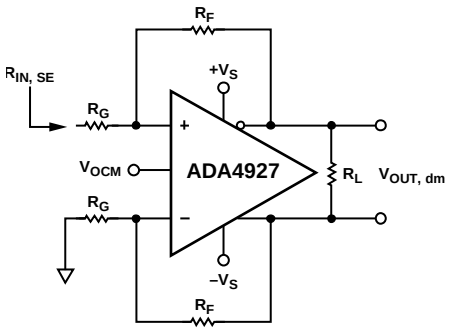


Figure 49. The ADA4927 with Unbalanced (Single-Ended) Input

The input impedance of the circuit is effectively higher than it would be for a conventional operational amplifier connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G. The common-mode voltage at the amplifier input terminals can be easily determined by noting that the voltage at the inverting input is equal to the noninverting output voltage divided down by the voltage divider formed by R_F and R_G in the lower loop. This voltage is present at both input terminals due to negative voltage feedback and is in phase with the input signal, thus reducing the effective voltage across R_G in the upper loop and partially bootstrapping R_G.

Terminating a Single-Ended Input

This section deals with how to properly terminate a single-ended input to the ADA4927 with a gain of 1, R_F = 348 Ω, and R_G = 348 Ω. An example using an input source with a terminated output voltage of 1 V p-p and a source resistance of 50 Ω illustrates the four simple steps that must be followed. Note that, because the terminated output voltage of the source is 1 V p-p, the open circuit output voltage of the source is 2 V p-p. The source shown in Figure 50 indicates this open-circuit voltage.

1. The input impedance must be calculated using the following formula:

$$R_{IN} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = \left(\frac{348}{1 - \frac{348}{2 \times (348 + 348)}} \right) = 464\Omega$$

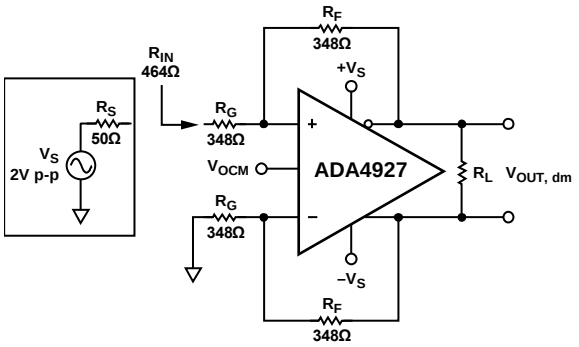


Figure 50. Calculating Single-Ended Input Impedance R_{IN}

2. To match the 50 Ω source resistance, the termination resistor, R_T, is calculated using $R_T||464\ \Omega = 50\ \Omega$. The closest standard 1% value for R_T is 56.2 Ω.

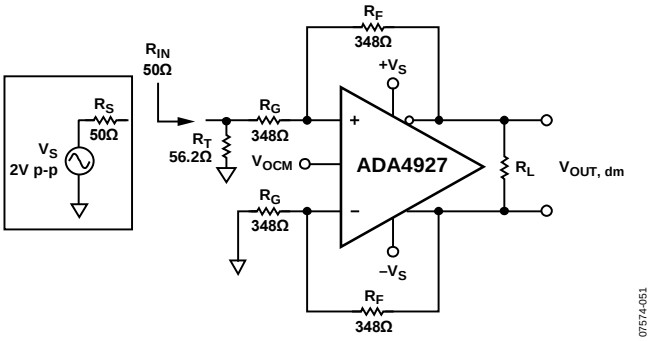


Figure 51. Adding Termination Resistor R_T

3. It can be seen from Figure 51 that the effective R_G in the upper feedback loop is now greater than the R_G in the lower loop due to the addition of the termination resistors. To compensate for the imbalance of the gain resistors, a correction resistor (R_{TS}) is added in series with R_G in the lower loop. R_{TS} is equal to the Thevenin equivalent of the source resistance R_S and the termination resistance R_T and is equal to $R_S||R_T$.

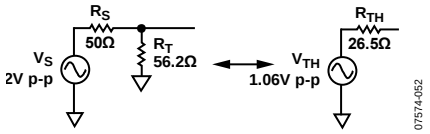


Figure 52. Calculating the Thevenin Equivalent

$R_{TS} = R_{TH} = R_S||R_T = 26.5\ \Omega$. Note that V_{TH} is greater than 1 V p-p, which was obtained with $R_T = 50\ \Omega$. The modified circuit with the Thevenin equivalent (closest 1% value used for R_{TH}) of the terminated source and R_{TS} in the lower feedback loop is shown in Figure 53.

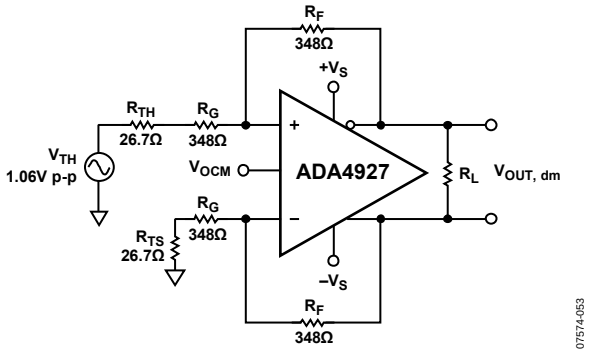


Figure 53. Thevenin Equivalent and Matched Gain Resistors

Figure 53 presents a tractable circuit with matched feedback loops that can be easily evaluated.

It is useful to point out two effects that occur with a terminated input. The first is that the value of R_G is increased in both loops, lowering the overall closed-loop gain. The second is that V_{TH} is a little larger than 1 V p-p, as it is when $R_T = 50\ \Omega$. These two effects have opposite impacts on the output voltage, and for large resistor values in the feedback loops (~1 kΩ), the effects essentially cancel each other out. For small R_F and R_G, or high gains, however, the diminished closed-loop gain is not canceled completely by the increased V_{TH}. This can be seen by evaluating Figure 53.

The desired differential output in this example is 1 V p-p because the terminated input signal is 1 V p-p and the closed-loop gain = 1. The actual differential output voltage, however, is equal to (1.06 V p-p)(348/374.7) = 0.984 V p-p. To obtain the desired output voltage of 1 V p-p, a final gain adjustment can be made by increasing R_F without modifying any of the input circuitry. This is discussed in Step 4.

4. The feedback resistor value is modified as a final gain adjustment to obtain the desired output voltage.
   To make the output voltage $V_{OUT} = 1$ V p-p, R_F must be calculated using the following formula:

$$R_F = \frac{(Desired\ V_{OUT,dm})(R_G + R_{TS})}{V_{TH}} = \frac{(1V\ p-p)(374.7\Omega)}{1.06V\ p-p} = 35$$

The closest standard 1% values to 353 Ω are 348 Ω and 357 Ω. Choosing 357 Ω for R_F gives a differential output voltage of 1.01 V p-p. The closed-loop bandwidth is diminished by a factor of approximately 348/357 from what it would be with $R_F = 348\ \Omega$ due to the inversely proportional relationship between R_F and closed-loop gain that is characteristic of current feedback amplifiers.

The final circuit is shown in Figure 54.

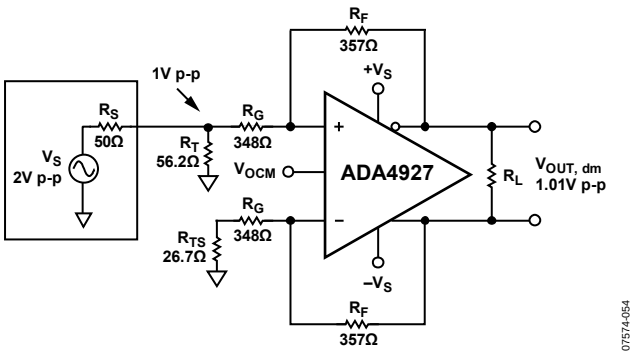


Figure 54. Terminated Single-Ended-to-Differential System with G = 1

INPUT COMMON-MODE VOLTAGE RANGE

The ADA4927 input common-mode range is centered between the two supply rails, in contrast to other ADC drivers with level-shifted input ranges, such as the ADA4937. The centered input common-mode range is best suited to ac-coupled, differential-to-differential, and dual supply applications.

For operation with ±5 V supplies, the input common-mode range at the summing nodes of the amplifier is specified as −3.5 V to +3.5 V and is specified as +1.3 V to +3.7 V with a single +5 V supply. To avoid nonlinearities, the voltage swing at the +IN and −IN terminals must be confined to these ranges.

INPUT AND OUTPUT CAPACITIVE AC COUPLING

Input ac coupling capacitors can be inserted between the source and R_G. This ac coupling blocks the flow of the dc common-mode feedback current and causes the ADA4927 dc input common-mode voltage to equal the dc output common-mode voltage. These ac coupling capacitors must be placed in both loops to keep the feedback factors matched.

Output ac coupling capacitors can be placed in series between each output and respective load. See Figure 58 for an example that uses input and output capacitive ac coupling.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4927 is internally biased with a voltage divider comprising two 10 kΩ resistors at a voltage approximately equal to the midsupply point, $[(+V_S) + (-V_S)]/2$. Because of this internal divider, the V_{OCM} pin sources and sinks current, depending on the externally applied voltage and associated source resistance. Relying on the internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where accurate control of the output common-mode level is required, it is recommended that an external source or resistor divider be used with source resistance less than 100 Ω. The output common-mode offset listed in the Specifications section presumes that the V_{OCM} input is driven by a low impedance voltage source.

It is also possible to connect the V_{OCM} input to a common-mode level (CML) output of an ADC; however, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 10 kΩ. If multiple ADA4927 devices share one ADC reference output, a buffer may be necessary to drive the parallel inputs.

POWER-DOWN

The power-down feature can reduce power consumption when a particular device is not in use and does not place the output in a high-Z state when asserted. The ADA4927 is generally enabled by pulling the power-down pin to the positive supply. See the Specifications tables for the specific voltages required to assert and deassert the power-down feature.

Power-Down in Cold Applications

The power-down feature should not be used in applications in which the ambient temperature falls below 0°C. Contact sales for information regarding applications that require the power-down feature to be used at ambient temperatures below 0°C.

LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4927 is sensitive to the PCB environment in which it operates. Realizing the superior performance requires attention to the details of high speed PCB design. This section shows a detailed example of how the ADA4927-1 was addressed.

The first requirement is a solid ground plane that covers as much of the board area around the ADA4927-1 as possible. However, clear the area near the feedback resistors (RF), gain resistors (RG), and the input summing nodes (Pin 2 and Pin 3) of all ground and power planes (see Figure 55). Clearing the ground and power planes minimizes any stray capacitance at these nodes and prevents peaking of the response of the amplifier at high frequencies. Whereas ideal current feedback amplifiers are insensitive to summing node capacitance, real-world amplifiers can exhibit peaking due to excessive summing node capacitance.

The thermal resistance, θ_{JA}, is specified for the device, including the exposed pad, soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD 51-7.

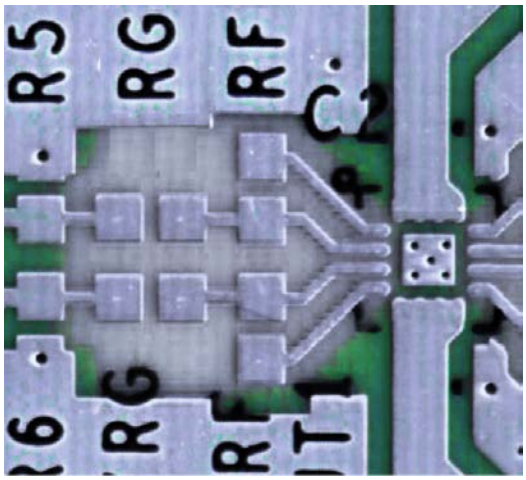


Figure 55. Ground and Power Plane Voiding in Vicinity of RF AND RG

Bypassed the power supply pins as close to the device as possible and directly to a nearby ground plane. Use high frequency ceramic chip capacitors. It is recommended that two parallel bypass capacitors (1000 pF and 0.1 µF) be used for each supply. The 1000 pF capacitor should be placed closer to the device. Further away, provide low frequency bulk bypassing, using 10 µF tantalum capacitors from each supply to ground.

Make signal routing short and direct to avoid parasitic effects. Wherever complementary signals exist, provide a symmetrical layout to maximize balanced performance. When routing differential signals over a long distance, place PCB traces close together, and twist any differential wiring such that the loop area is minimized. Doing this reduces radiated energy and makes the circuit less susceptible to interference.

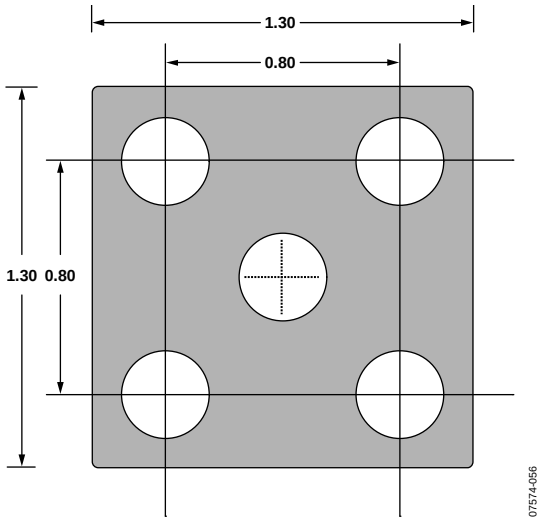


Figure 56. Recommended PCB Thermal Attach Pad Dimensions (Millimeters)

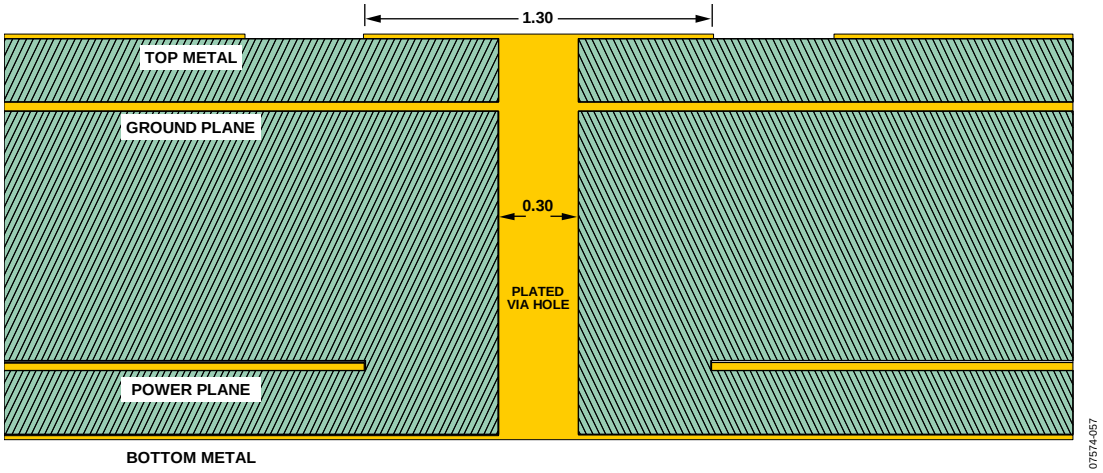


Figure 57. Cross-Section of 4-Layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in Millimeters)

HIGH PERFORMANCE ADC DRIVING

The ADA4927 is ideally suited for high gain, broadband ac-coupled and differential-to-differential applications on a single supply, though other applications are possible. Compared with voltage feedback amplifiers, the current feedback architecture provides superior distortion and bandwidth performance at high gains. This is because the ideal current feedback amplifier loop gain depends only on the feedback value and open-loop transimpedance, T(s).

The circuit in Figure 58 shows a front-end connection for an ADA4927 driving an AD9445, 14-bit, 105 MSPS ADC, with ac coupling on the ADA4927 input and output. (The AD9445 achieves optimum performance when driven differentially.) The ADA4927 eliminates the need for a transformer to drive the ADC and performs a single-ended-to-differential conversion and buffering of the driving signal.

The ADA4927 is configured with a single 5 V supply and gain of 10 for a single-ended input to differential output. The 158 Ω termination resistor, in parallel with the single-ended input impedance of approximately 73.2 Ω, provides a 50 Ω termination for the source. The additional 38.3 Ω at the inverting input closely matches the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input. Because of the high gain, a few iterations of the termination technique described in the Terminating a Single-Ended Input section are required. Two objectives of the design are to make R_F close to 500 Ω and obtain resistor values that are close to standard 1% values.

In this example, the signal generator has a 1 V p-p symmetric, ground-referenced bipolar output when terminated in 50 Ω.

The V_{OCM} pin of the ADA4927 is bypassed for noise reduction and left floating such that the internal divider sets the output common-mode voltage nominally at midsupply. Because the inputs are ac-coupled, no dc common-mode current flows in the feedback loops, and a nominal dc level of midsupply is present at the amplifier input terminals. Besides placing the amplifier inputs at their optimum levels, the ac coupling technique lightens the load on the amplifier and dissipates less power than applications with dc-coupled inputs.

The output of the amplifier is ac-coupled to the ADC through a second-order, low-pass filter with a cutoff frequency of 100 MHz. This reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

The AD9445 is configured for a 2 V p-p full-scale input by connecting the SENSE pin to AGND, as shown in Figure 58.

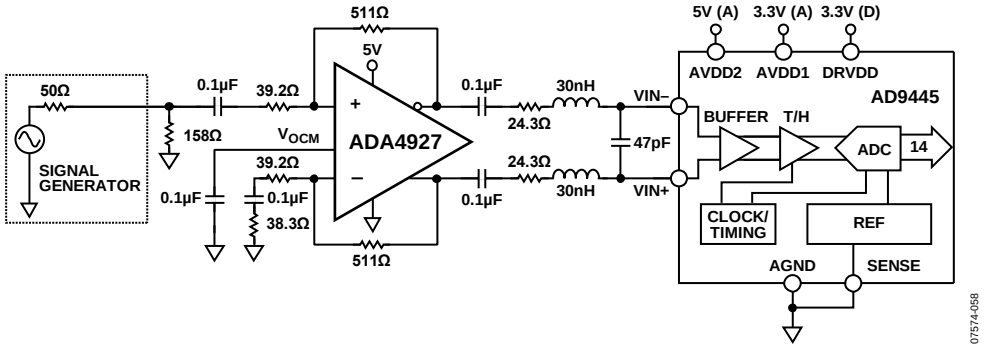


Figure 58. ADA4927 Driving an AD9445 ADC with AC-Coupled Input and Output

OUTLINE DIMENSIONS

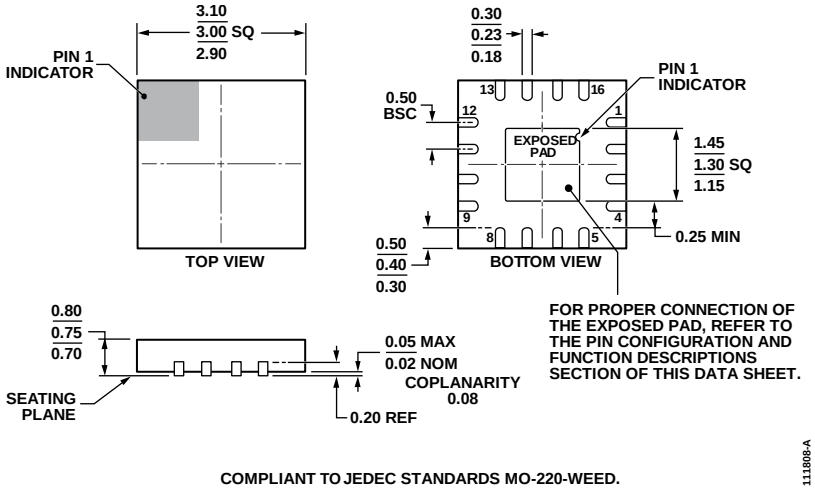


Figure 59. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-21)
Dimensions shown in millimeters

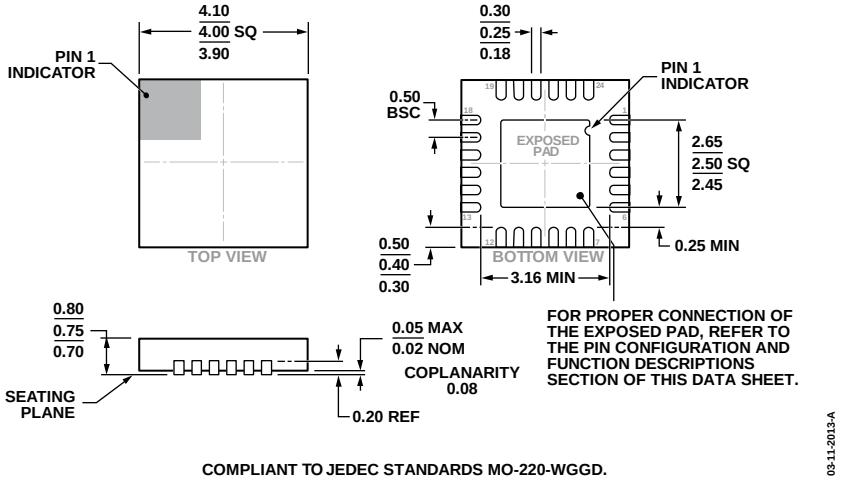


Figure 60. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4927-1YCPZ-R2	−40°C to +105°C	16-Lead LFCSP_VQ	CP-16-21	250	H1N
ADA4927-1YCPZ-RL	−40°C to +105°C	16-Lead LFCSP_VQ	CP-16-21	5,000	H1N
ADA4927-1YCPZ-R7	−40°C to +105°C	16-Lead LFCSP_VQ	CP-16-21	1,500	H1N
ADA4927-2YCPZ-R2	−40°C to +105°C	24-Lead LFCSP_VQ	CP-24-7	250	
ADA4927-2YCPZ-RL	−40°C to +105°C	24-Lead LFCSP_VQ	CP-24-7	5,000	
ADA4927-2YCPZ-R7	−40°C to +105°C	24-Lead LFCSP_VQ	CP-24-7	1,500	

[1] Z = RoHS Compliant Part.

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D07574-0-5/16(B)