

FEATURES

Low wideband noise

1 nV/ $\sqrt{\text{Hz}}$

2.8 pA/ $\sqrt{\text{Hz}}$

Low 1/f noise: 2.4 nV/ $\sqrt{\text{Hz}}$ at 10 Hz

Low distortion: -115 dBc at 100 kHz, $V_{\text{OUT}} = 2 \text{ V p-p}$

Low power: 3 mA per amplifier

Low input offset voltage: 0.5 mV maximum

High speed

-3 dB bandwidth: 230 MHz ($G = +1$)

Slew rate: 120 V/ μs

Settling time to 0.1%: 45 ns

Rail-to-rail output

Wide supply range: 3 V to 10 V

Disable feature

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)

Extended industrial temperature range (-55°C to +125°C)

Controlled manufacturing baseline

1 assembly/test site

1 fabrication site

Enhanced product change notification

Qualification data available on request

APPLICATIONS

Low noise preamplifier

Ultrasound amplifiers

PLL loop filters

High performance ADC drivers

DAC buffers

GENERAL DESCRIPTION

The ADA4897-1-EP/ADA4897-2-EP are unity-gain stable, low noise, rail-to-rail output, high speed voltage feedback amplifiers that have a quiescent current of 3 mA. With a 1/f noise of 2.4 nV/ $\sqrt{\text{Hz}}$ at 10 Hz and a spurious-free dynamic range of -80 dBc at 2 MHz, these amplifiers are ideal solutions in a variety of applications, including ultrasound, low noise preamplifiers, and drivers of high performance ADCs. The Analog Devices, Inc., proprietary next-generation SiGe bipolar process and innovative architecture enable such high performance amplifiers.

The ADA4897-1-EP/ADA4897-2-EP have 230 MHz bandwidth, 120 V/ μs slew rate, and settle to 0.1% in 45 ns. With a wide supply voltage range of 3 V to 10 V, the ADA4897-1-EP/ADA4897-2-EP are ideal candidates for systems that require high dynamic range, precision, low power, and high speed.

The ADA4897-1-EP is available in 6-lead SOT-23 package and the ADA4897-2-EP is available in a 10-lead MSOP package. The ADA4897-1-EP/ADA4897-2-EP operate over the extended industrial temperature range of -55°C to +125°C. Additional application and technical information can be found in the ADA4897-1/ADA4897-2 data sheet.

FUNCTIONAL BLOCK DIAGRAM

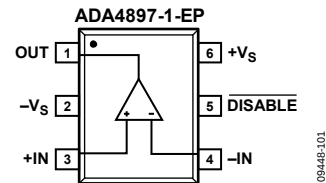


Figure 1. 6-Lead SOT-23 (ADA4897-1-EP)

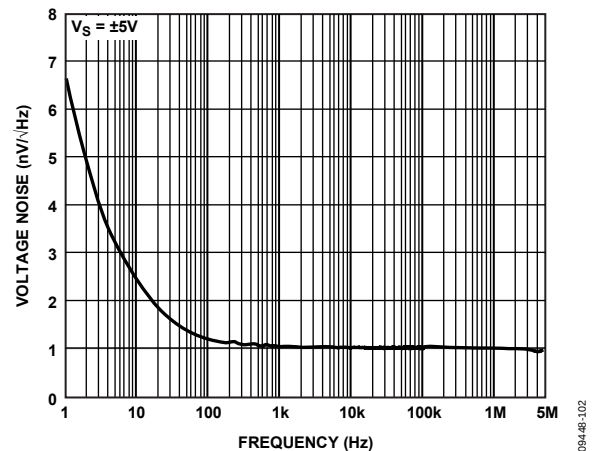


Figure 2. Voltage Noise vs. Frequency

Table 1. Other Low Noise Amplifiers

Part No.	V_N (nV/ $\sqrt{\text{Hz}}$)		BW (MHz)	Supply Voltage (V)
	At 1 kHz	At 100 kHz		
AD797	0.9	0.9	8	10 to 30
AD8021	5	2.1	490	5 to 24
AD8099	3	0.95	510	5 to 12
AD8045	6	3	1000	3.3 to 12
ADA4899-1	1.4	1	600	5 to 12
ADA4898-1/ ADA4898-2	0.9	0.9	65	10 to 32

Table 2. Complementary ADCs

Part No.	Bits	Speed (MSPS)	Power (mW)
AD7944	14	2.5	15.5
AD7985	16	2.5	15.5
AD7986	18	2	15

TABLE OF CONTENTS

Features	1	+3 V Supply	6
Enhanced Product Features	1	Absolute Maximum Ratings	8
Applications	1	Thermal Resistance	8
General Description	1	Maximum Power Dissipation	8
Functional Block Diagram	1	ESD Caution.....	8
Revision History	2	Pin Configurations and Function Descriptions	9
Specifications.....	3	Typical Performance Characteristics	10
±5 V Supply	3	Outline Dimensions	12
+5 V Supply	4	Ordering Guide	12

REVISION HISTORY

2/13—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

$T_A = 25^\circ\text{C}$, $G = +1$, $R_L = 1\text{ k}\Omega$ to ground, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$G = +1$, $V_{OUT} = 0.02\text{ V p-p}$		230		MHz
	$G = +1$, $V_{OUT} = 2\text{ V p-p}$		30		MHz
	$G = +2$, $V_{OUT} = 0.02\text{ V p-p}$		90		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_{OUT} = 2\text{ V p-p}$, $R_L = 100\ \Omega$		7		MHz
Slew Rate	$G = +2$, $V_{OUT} = 6\text{ V step}$		120		V/ μs
Settling Time to 0.1%	$G = +2$, $V_{OUT} = 2\text{ V step}$		45		ns
Settling Time to 0.01%	$G = +2$, $V_{OUT} = 2\text{ V step}$		90		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	$V_{OUT} = 2\text{ V p-p}$				
	$f_C = 100\text{ kHz}$		–115		dBc
	$f_C = 1\text{ MHz}$		–93		dBc
	$f_C = 2\text{ MHz}$		–80		dBc
	$f_C = 5\text{ MHz}$		–61		dBc
Input Voltage Noise	$f = 10\text{ Hz}$		2.4		nV/ $\sqrt{\text{Hz}}$
	$f = 100\text{ kHz}$		1		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 10\text{ Hz}$		11		pA/ $\sqrt{\text{Hz}}$
	$f = 100\text{ kHz}$		2.8		pA/ $\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz Noise	$G = +101$, $R_F = 1\text{ k}\Omega$, $R_G = 10\ \Omega$		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		–500	–28	+500	μV
Input Offset Voltage Drift			0.2		$\mu\text{V}/^\circ\text{C}$
Input Bias Current		–17	–11	–4	μA
Input Bias Current Drift			3		nA/ $^\circ\text{C}$
Input Bias Offset Current		–0.6	–0.02	+0.6	μA
Open-Loop Gain	$V_{OUT} = -4\text{ V to }+4\text{ V}$	100	110		dB
INPUT CHARACTERISTICS					
Input Resistance					
	Common-Mode		10		M Ω
Differential			10		k Ω
Input Capacitance					
	Common-Mode		3		pF
Differential			11		pF
Input Common-Mode Voltage Range			–4.9 to +4.1		V
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = -2\text{ V to }+2\text{ V}$	–92	–120		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	$V_{IN} = \pm 5\text{ V}$, $G = +2$		81		ns
Output Voltage Swing					
	Positive	$R_L = 1\text{ k}\Omega$	4.85	4.96	V
Negative	$R_L = 100\ \Omega$	4.5	4.73		V
	$R_L = 1\text{ k}\Omega$	–4.85	–4.97		V
Output Current	$R_L = 100\ \Omega$	–4.5	–4.84		V
	SFDR = –45 dBc		80		mA
Short-Circuit Current	Sinking/sourcing		135		mA
Capacitive Load Drive	30% overshoot, $G = +2$		39		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier	$\overline{\text{DISABLE}} = -5 \text{ V}$	2.8	3.0	3.2	mA
Power Supply Rejection Ratio (PSRR)			0.13	0.25	mA
Positive	$+V_S = 4 \text{ V to } 6 \text{ V}, -V_S = -5 \text{ V}$	-96	-125		dB
Negative	$+V_S = 5 \text{ V}, -V_S = -4 \text{ V to } -6 \text{ V}$	-96	-121		dB
DISABLE PIN					
$\overline{\text{DISABLE}}$ Voltage	Enabled		$> +V_S - 0.5$		V
	Disabled		$< +V_S - 2$		V
Input Current					
Enabled	$\overline{\text{DISABLE}} = +5 \text{ V}$		-1.2		μA
Disabled	$\overline{\text{DISABLE}} = -5 \text{ V}$		-40		μA
Switching Speed					
Enabled			0.25		μs
Disabled			12		μs

+5 V SUPPLY

$T_A = 25^\circ\text{C}$, $G = +1$, $R_L = 1 \text{ k}\Omega$ to midsupply, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +1, V_{\text{OUT}} = 0.02 \text{ V p-p}$		230		MHz
	$G = +1, V_{\text{OUT}} = 2 \text{ V p-p}$		30		MHz
	$G = +2, V_{\text{OUT}} = 0.02 \text{ V p-p}$		90		MHz
Bandwidth for 0.1 dB Flatness	$G = +2, V_{\text{OUT}} = 2 \text{ V p-p}, R_L = 100 \Omega$		7		MHz
Slew Rate	$G = +2, V_{\text{OUT}} = 3 \text{ V step}$		100		V/ μs
Settling Time to 0.1%	$G = +2, V_{\text{OUT}} = 2 \text{ V step}$		45		ns
Settling Time to 0.01%	$G = +2, V_{\text{OUT}} = 2 \text{ V step}$		95		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	$V_{\text{OUT}} = 2 \text{ V p-p}$				
	$f_C = 100 \text{ kHz}$		-115		dBc
	$f_C = 1 \text{ MHz}$		-93		dBc
	$f_C = 2 \text{ MHz}$		-80		dBc
	$f_C = 5 \text{ MHz}$		-61		dBc
Input Voltage Noise	$f = 10 \text{ Hz}$		2.4		nV/ $\sqrt{\text{Hz}}$
	$f = 100 \text{ kHz}$		1		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 10 \text{ Hz}$		11		pA/ $\sqrt{\text{Hz}}$
	$f = 100 \text{ kHz}$		2.8		pA/ $\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz Noise	$G = +101, R_F = 1 \text{ k}\Omega, R_G = 10 \Omega$		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		-500	-30	+500	μV
Input Offset Voltage Drift			0.2		$\mu\text{V}/^\circ\text{C}$
Input Bias Current		-17	-11	-4	μA
Input Bias Current Drift			3		nA/ $^\circ\text{C}$
Input Bias Offset Current		-0.6	-0.02	+0.6	μA
Open-Loop Gain	$V_{\text{OUT}} = 0.5 \text{ V to } 4.5 \text{ V}$	97	110		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance					
Common-Mode			10		M Ω
Differential			10		k Ω
Input Capacitance					
Common-Mode			3		pF
Differential			11		pF
Input Common-Mode Voltage Range			0.1 to 4.1		V
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = 1\text{ V to }4\text{ V}$	-91	-118		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	$V_{IN} = 0\text{ V to }5\text{ V}, G = +2$		96		ns
Output Voltage Swing					
Positive	$R_L = 1\text{ k}\Omega$	4.85	4.98		V
	$R_L = 100\text{ }\Omega$	4.8	4.88		V
Negative	$R_L = 1\text{ k}\Omega$	0.15	0.014		V
	$R_L = 100\text{ }\Omega$	0.2	0.08		V
Output Current	SFDR = -45 dBc		70		mA
Short-Circuit Current	Sinking/sourcing		125		mA
Capacitive Load Drive	30% overshoot, $G = +2$		39		pF
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.6	2.8	2.9	mA
	$\overline{\text{DISABLE}} = 0\text{ V}$		0.05	0.18	mA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S = 4.5\text{ V to }5.5\text{ V}, -V_S = 0\text{ V}$	-96	-123		dB
Negative	$+V_S = 5\text{ V}, -V_S = -0.5\text{ V to }+0.5\text{ V}$	-96	-121		dB
DISABLE PIN					
$\overline{\text{DISABLE}}$ Voltage	Enabled		$>+V_S - 0.5$		V
	Disabled		$<+V_S - 2$		V
Input Current					
Enabled	$\overline{\text{DISABLE}} = +5\text{ V}$		-1.2		μA
Disabled	$\overline{\text{DISABLE}} = 0\text{ V}$		-20		μA
Switching Speed					
Enabled			0.25		μs
Disabled			12		μs

+3 V SUPPLY

$T_A = 25^\circ\text{C}$, $G = +1$, $R_L = 1\text{ k}\Omega$ to midsupply, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$G = +1$, $V_{OUT} = 0.02\text{ V p-p}$		230		MHz
	$G = -1$, $V_{OUT} = 1\text{ V p-p}$		45		MHz
	$G = +2$, $V_{OUT} = 0.02\text{ V p-p}$		90		MHz
	$G = +2$, $V_{OUT} = 2\text{ V p-p}$, $R_L = 100\ \Omega$		7		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_{OUT} = 1\text{ V step}$		85		V/ μs
Slew Rate	$G = +2$, $V_{OUT} = 2\text{ V step}$		45		ns
Settling Time to 0.1%	$G = +2$, $V_{OUT} = 2\text{ V step}$		96		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	$f_C = 100\text{ kHz}$, $V_{OUT} = 2\text{ V p-p}$, $G = +2$		–105		dBc
	$f_C = 1\text{ MHz}$, $V_{OUT} = 1\text{ V p-p}$, $G = -1$		–84		dBc
	$f_C = 2\text{ MHz}$, $V_{OUT} = 1\text{ V p-p}$, $G = -1$		–77		dBc
	$f_C = 5\text{ MHz}$, $V_{OUT} = 1\text{ V p-p}$, $G = -1$		–60		dBc
Input Voltage Noise	$f = 10\text{ Hz}$		2.3		nV/ $\sqrt{\text{Hz}}$
	$f = 100\text{ kHz}$		1		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 10\text{ Hz}$		11		pA/ $\sqrt{\text{Hz}}$
	$f = 100\text{ kHz}$		2.8		pA/ $\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz Noise	$G = +101$, $R_F = 1\text{ k}\Omega$, $R_G = 10\ \Omega$		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		–500	–30	+500	μV
Input Offset Voltage Drift			0.2		$\mu\text{V}/^\circ\text{C}$
Input Bias Current		–17	–11	–4	μA
Input Bias Current Drift			3		nA/ $^\circ\text{C}$
Input Bias Offset Current		–0.6	–0.02	+0.6	μA
Open-Loop Gain	$V_{OUT} = 0.5\text{ V to }2.5\text{ V}$	95	108		dB
INPUT CHARACTERISTICS					
Input Resistance			10		M Ω
			10		k Ω
Input Capacitance			3		pF
			11		pF
Input Common-Mode Voltage Range			0.1 to 2.1		V
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = 1.1\text{ V to }1.9\text{ V}$	–90	–124		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	$V_{IN} = 0\text{ V to }3\text{ V}$, $G = +2$		83		ns
Output Voltage Swing					
	Positive				
	$R_L = 1\text{ k}\Omega$	2.85	2.97		V
	$R_L = 100\ \Omega$	2.8	2.92		V
Negative	$R_L = 1\text{ k}\Omega$	0.15	0.01		V
	$R_L = 100\ \Omega$	0.2	0.05		V
Output Current	SFDR = –45 dBc		60		mA
Short-Circuit Current	Sinking/sourcing		120		mA
Capacitive Load Drive	30% overshoot, $G = +2$		39		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.5	2.7	2.9	mA
	$\overline{\text{DISABLE}} = 0\text{ V}$		0.035	0.15	mA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S = 2.7\text{ V to } 3.7\text{ V}, -V_S = 0\text{ V}$	-96	-121		dB
Negative	$+V_S = 3\text{ V}, -V_S = -0.3\text{ V to } +0.7\text{ V}$	-96	-120		dB
DISABLE PIN					
$\overline{\text{DISABLE}}$ Voltage	Enabled		$>+V_S - 0.5$		V
	Disabled		$<-V_S + 2$		V
Input Current					
Enabled	$\overline{\text{DISABLE}} = +3\text{ V}$		-1.2		μA
Disabled	$\overline{\text{DISABLE}} = 0\text{ V}$		-15		μA
Switching Speed					
Enabled			0.25		μs
Disabled			12		μs

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S - 0.7\text{ V}$ to $+V_S + 0.7\text{ V}$
Differential Input Voltage	$\pm 0.7\text{ V}$
Storage Temperature Range	-65°C to $+125^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 7 lists the θ_{JA} for the [ADA4897-1-EP/ADA4897-2-EP](#).

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead Single SOT-23 (ADA4897-1-EP)	150	$^\circ\text{C}/\text{W}$
10-Lead Dual MSOP (ADA4897-2-EP)	210	$^\circ\text{C}/\text{W}$

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the [ADA4897-1-EP/ADA4897-2-EP](#) is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C , which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the [ADA4897-1-EP/ADA4897-2-EP](#). Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the [ADA4897-1-EP/ADA4897-2-EP](#) drive at the output.

The quiescent power dissipation is the voltage between the supply pins ($\pm V_S$) multiplied by the quiescent current (I_S).

$$P_D = \text{Quiescent Power} + (\text{Total Drive Power} - \text{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L} \right) - \frac{V_{OUT}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA} . Also, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduces θ_{JA} .

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

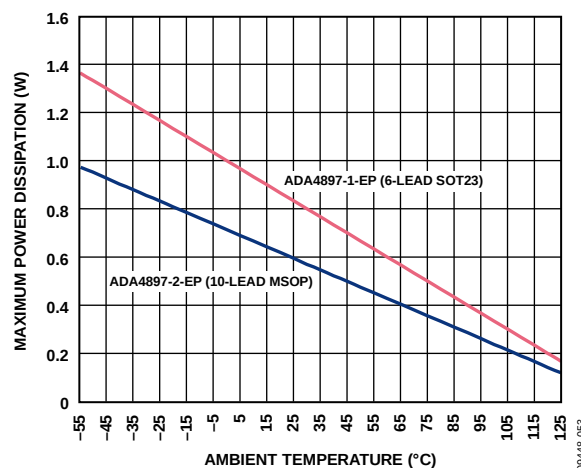


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

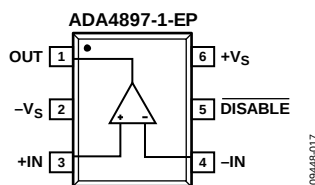


Figure 4. 6-Lead SOT-23 Pin Configuration

Table 8. [ADA4897-1-EP](#) Pin Function Descriptions

Pin No.	Mnemonic	Description
4	-IN	Inverting Input.
3	+IN	Noninverting Input.
2	-Vs	Negative Supply.
1	OUT	Output.
6	+Vs	Positive Supply.
5	DISABLE	Disable.

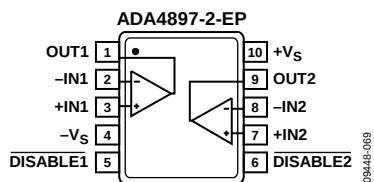


Figure 5. 10-Lead MSOP Pin Configuration

Table 9. [ADA4897-2-EP](#) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT1	Output 1.
2	-IN1	Inverting Input 1.
3	+IN1	Noninverting Input 1.
4	-Vs	Negative Supply.
5	DISABLE1	Disable 1.
6	DISABLE2	Disable 2.
7	+IN2	Noninverting Input 2.
8	-IN2	Inverting Input 2.
9	OUT2	Output 2.
10	+Vs	Positive Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

$R_L = 1\text{ k}\Omega$, unless otherwise noted. When $G = +1$, $R_F = 0\text{ }\Omega$; otherwise, $R_F = 249\text{ }\Omega$.

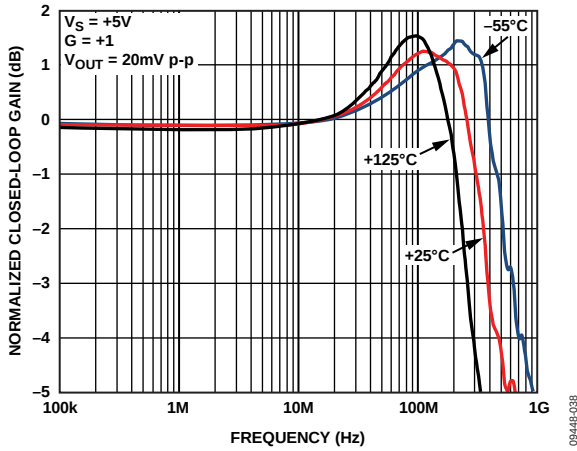


Figure 6. Small Signal Frequency Response vs. Temperature

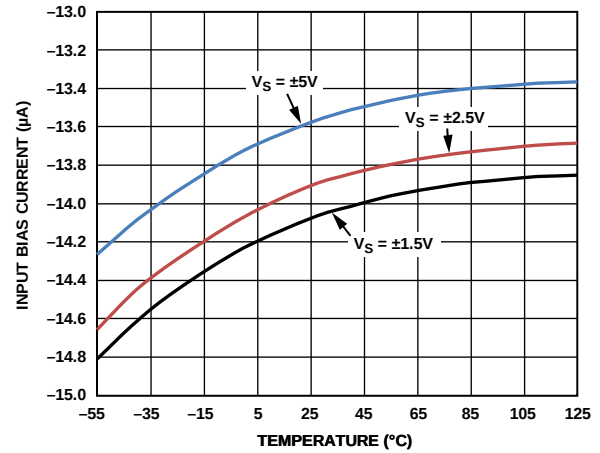


Figure 9. Input Bias Current vs. Temperature for Various Supplies

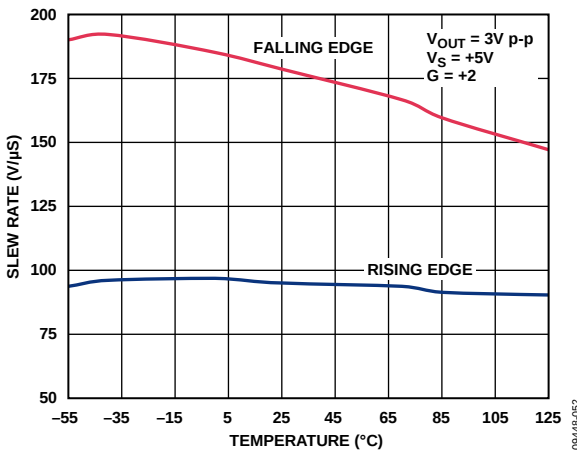


Figure 7. Slew Rate vs. Temperature

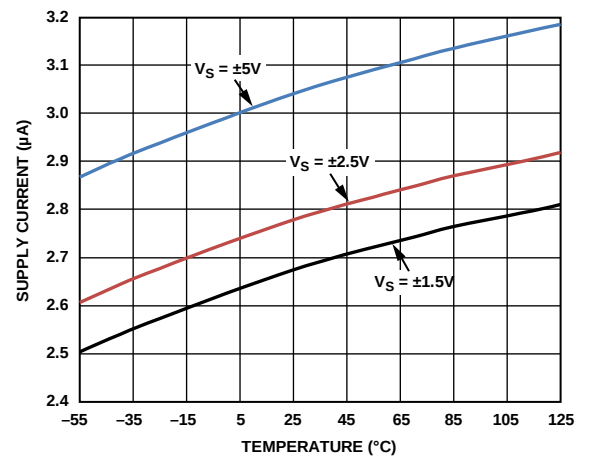


Figure 10. Supply Current vs. Temperature for Various Supplies

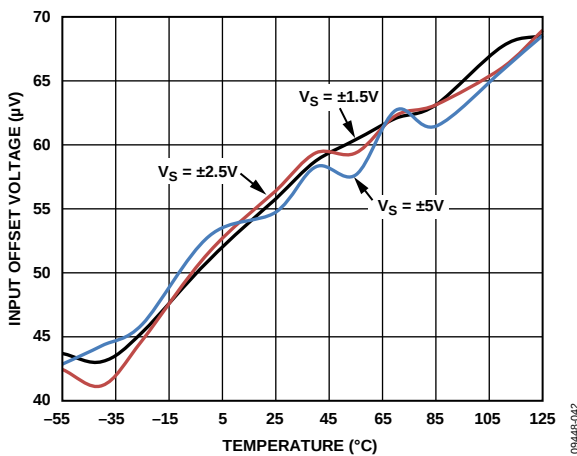


Figure 8. Input Offset Voltage vs. Temperature for Various Supplies

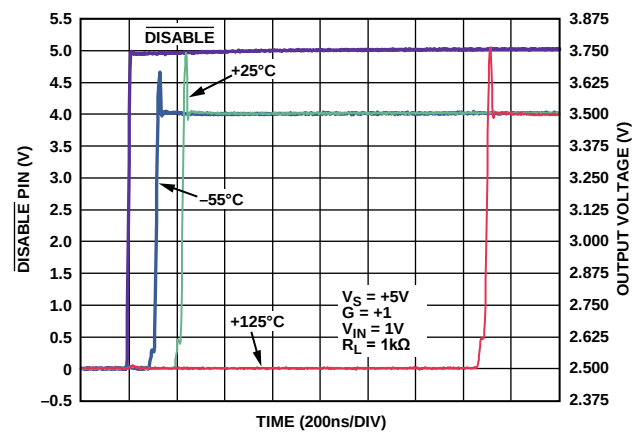


Figure 11. Turn-On Time vs. Temperature

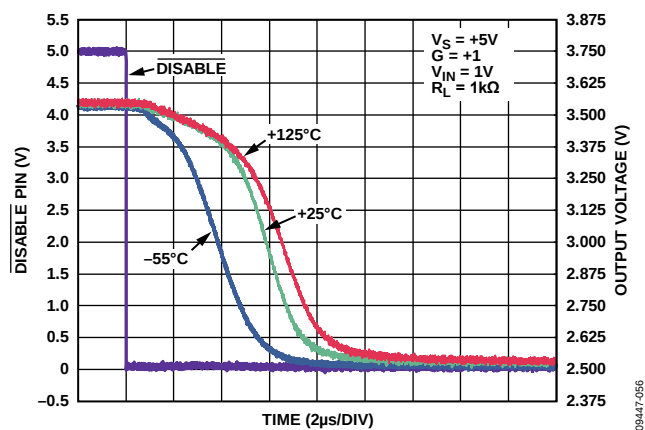
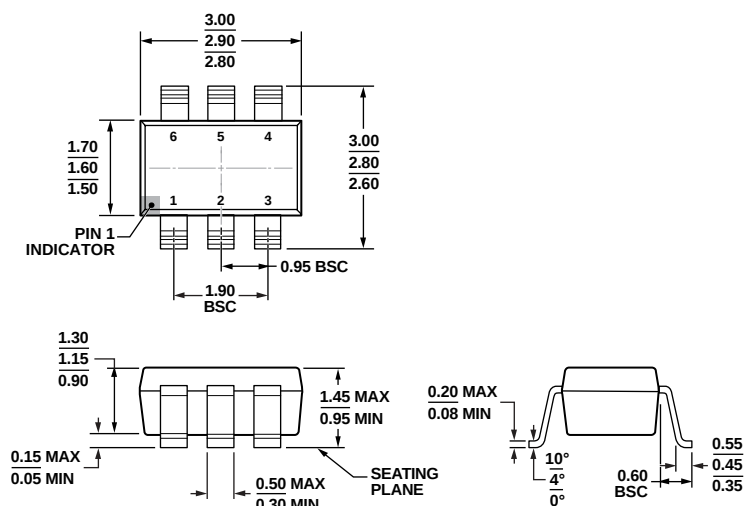


Figure 12. Turn-Off Time vs. Temperature

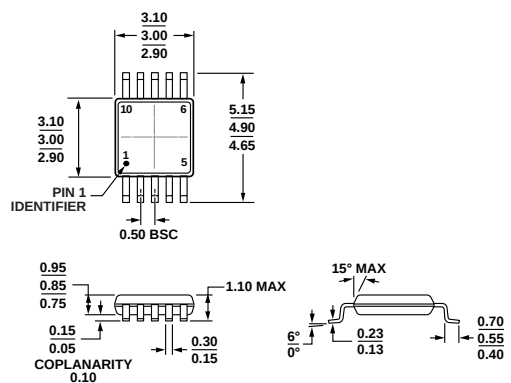
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 13. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 14. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4897-1SRJZ-EPR7	–55°C to +125°C	6-Lead SOT-23	RJ-6	3,000	H2L
ADA4897-1ARJ-EBZ		Evaluation Board for the 6-Lead SOT-23			
ADA4897-2TRMZ-EP	–55°C to +125°C	10-Lead MSOP	RM-10	50	H3E
ADA4897-2ARM-EBZ		Evaluation Board for the 10-Lead MSOP			

¹ Z = RoHS Compliant Part.