Low Cost CMOS, High Speed, Rail-to-Rail Amplifiers

ADA4891-1/ADA4891-2/ADA4891-3/ADA4891-4

FEATURES

- **High speed and fast settling**
  - **−3 dB bandwidth: 220 MHz (G = +1)**
  - **Slew rate: 170 V/µs**
  - **Settling time to 0.1%: 28 ns**
- **Video specifications (G = +2, R_L = 150 Ω)**
  - **0.1 dB gain flatness: 25 MHz**
  - **Differential gain error: 0.05%**
  - **Differential phase error: 0.25°**
- **Single-supply operation**
  - **Wide supply range: 2.7 V to 5.5 V**
  - **Output swings to within 50 mV of supply rails**
- **Low distortion: 79 dBc SFDR at 1 MHz**
- **Linear output current: 125 mA at −40 dBc**
- **Low power: 4.4 mA per amplifier**

APPLICATIONS

- **Imaging**
- **Consumer video**
- **Active filters**
- **Coaxial cable drivers**
- **Clock buffers**
- **Photodiode preamp**
- **Contact image sensor and buffers**

GENERAL DESCRIPTION

The ADA4891-1 (single), ADA4891-2 (dual), ADA4891-3 (triple), and ADA4891-4 (quad) are CMOS, high speed amplifiers that offer high performance at a low cost. The amplifiers feature true single-supply capability, with an input voltage range that extends 300 mV below the negative rail.

In spite of their low cost, the ADA4891 family provides high performance and versatility. The rail-to-rail output stage enables the output to swing to within 50 mV of each rail, enabling maximum dynamic range.

The ADA4891 family of amplifiers is ideal for imaging applications, such as consumer video, CCD buffers, and contact image sensor and buffers. Low distortion and fast settling time also make them ideal for active filter applications.

The ADA4891-1/ADA4891-2/ADA4891-3/ADA4891-4 are available in a wide variety of packages. The ADA4891-1 is available in 8-lead SOIC and 5-lead SOT-23 packages. The ADA4891-2 is available in 8-lead SOIC and 8-lead MSOP packages. The ADA4891-3 and ADA4891-4 are available in 14-lead SOIC and 14-lead TSSOP packages. The amplifiers are specified to operate over the extended temperature range of −40°C to +125°C.

CONNECTION DIAGRAMS

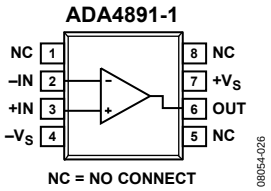


Figure 1. 8-Lead SOIC_N (R-8)

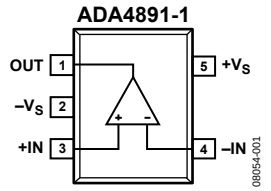


Figure 2. 5-Lead SOT-23 (RJ-5)

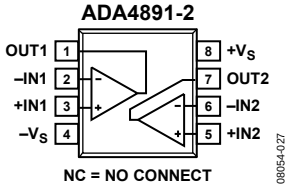


Figure 3. 8-Lead SOIC_N (R-8) and 8-Lead MSOP (RM-8)

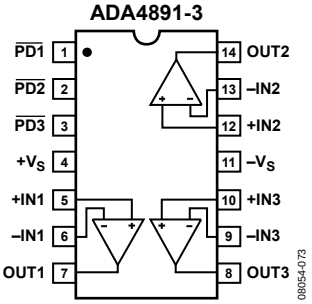


Figure 4. 14-Lead SOIC_N (R-14) and 14-Lead TSSOP (RU-14)

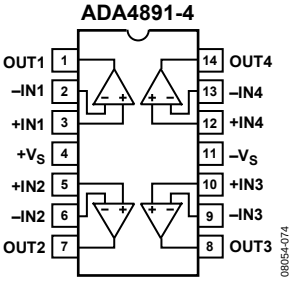


Figure 5. 14-Lead SOIC_N (R-14) and 14-Lead TSSOP (RU-14)

Rev. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2010 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

7/10—Rev. A to Rev. B

Added ADA4891-3 and ADA4891-4 ... Universal
Added 14-Lead SOIC and 14-Lead TSSOP Packages ... Universal
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6/10—Rev. 0 to Rev. A

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Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

2/10—Revision 0: Initial Version

SPECIFICATIONS

5 V OPERATION

T_A = 25°C, V_S = 5 V, R_L = 1 kΩ to 2.5 V, unless otherwise noted. All specifications are for the ADA4891-1, ADA4891-2, ADA4891-3, and ADA4891-4, unless otherwise noted. For the ADA4891-1 and ADA4891-2, R_F = 604 Ω; for the ADA4891-3 and ADA4891-4, R_F = 453 Ω, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small-Signal Bandwidth	ADA4891-1/ADA4891-2, G = +1, V_O = 0.2 V p-p		240		MHz
	ADA4891-3/ADA4891-4, G = +1, V_O = 0.2 V p-p		220		MHz
	ADA4891-1/ADA4891-2, G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V		90		MHz
	ADA4891-3/ADA4891-4, G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V		96		MHz
Bandwidth for 0.1 dB Gain Flatness	ADA4891-1/ADA4891-2, G = +2, V_O = 2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 604 Ω		25		MHz
	ADA4891-3/ADA4891-4, G = +2, V_O = 2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 374 Ω		25		MHz
Slew Rate, t_R/t_F	G = +2, V_O = 2 V step, 10% to 90%		170/210		V/µs
−3 dB Large-Signal Frequency Response	G = +2, V_O = 2 V p-p, R_L = 150 Ω		40		MHz
Settling Time to 0.1%	G = +2, V_O = 2 V step		28		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3	f_C = 1 MHz, V_O = 2 V p-p, G = +1		−79/−93		dBc
	f_C = 1 MHz, V_O = 2 V p-p, G = −1		−75/−91		dBc
Input Voltage Noise	f = 1 MHz		9		nV/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.05		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.25		Degrees
All-Hostile Crosstalk	f = 5 MHz, G = +2, V_O = 2 V p-p		−80		dB
DC PERFORMANCE					
Input Offset Voltage			±2.5	±10	mV
	T_{MIN} to T_{MAX}		±3.1		mV
Offset Drift			6		µV/°C
Input Bias Current		−50	+2	+50	pA
Open-Loop Gain	R_L = 1 kΩ to 2.5 V	77	83		dB
	R_L = 150 Ω to 2.5 V		71		dB
INPUT CHARACTERISTICS					
Input Resistance			5		GΩ
Input Capacitance			3.2		pF
Input Common-Mode Voltage Range			$-V_S$ − 0.3 to $+V_S$ − 0.8		V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to 3.0 V		88		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ to 2.5 V		0.01 to 4.98		V
	R_L = 150 Ω to 2.5 V		0.08 to 4.90		V
Output Current	1% THD with 1 MHz, V_O = 2 V p-p		125		mA
Short-Circuit Current					
Sourcing			205		mA
Sinking			307		mA
POWER-DOWN PINS ($\overline{PD1}$, $\overline{PD2}$, $\overline{PD3}$)	ADA4891-3 only				
Threshold Voltage, V_{TH}			2.4		V
Bias Current	Part enabled		65		nA
	Part powered down		−22		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Turn-On Time	Part enabled, output rises to 90% of final value		166		ns
Turn-Off Time	Part powered down, output falls to 10% of final value		49		ns
POWER SUPPLY					
Operating Range		2.7		5.5	V
Quiescent Current per Amplifier			4.4		mA
Supply Current When Powered Down	ADA4891-3 only		0.8		mA
Power Supply Rejection Ratio (PSRR)					
Positive PSRR	$+V_S$ = 5 V to 5.25 V, $-V_S$ = 0 V		65		dB
Negative PSRR	$+V_S$ = 5 V, $-V_S$ = −0.25 V to 0 V		63		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

3 V OPERATION

T_A = 25°C, V_S = 3 V, R_L = 1 kΩ to 1.5 V, unless otherwise noted. All specifications are for the ADA4891-1, ADA4891-2, ADA4891-3, and ADA4891-4, unless otherwise noted. For the ADA4891-1 and ADA4891-2, R_F = 604 Ω; for the ADA4891-3 and ADA4891-4, R_F = 453 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small-Signal Bandwidth	ADA4891-1/ADA4891-2, G = +1, V_O = 0.2 V p-p		190		MHz
	ADA4891-3/ADA4891-4, G = +1, V_O = 0.2 V p-p		175		MHz
	ADA4891-1/ADA4891-2, G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 1.5 V		75		MHz
	ADA4891-3/ADA4891-4, G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 1.5 V		80		MHz
Bandwidth for 0.1 dB Gain Flatness	ADA4891-1/ADA4891-2, G = +2, V_O = 2 V p-p, R_L = 150 Ω to 1.5 V, R_F = 604 Ω		18		MHz
	ADA4891-3/ADA4891-4, G = +2, V_O = 2 V p-p, R_L = 150 Ω to 1.5 V, R_F = 374 Ω		18		MHz
Slew Rate, t_R/t_F	G = +2, V_O = 2 V step, 10% to 90%		140/230		V/µs
−3 dB Large-Signal Frequency Response	G = +2, V_O = 2 V p-p, R_L = 150 Ω		40		MHz
Settling Time to 0.1%	G = +2, V_O = 2 V step		30		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3	f_C = 1 MHz, V_O = 2 V p-p, G = −1		−70/−89		dBc
Input Voltage Noise	f = 1 MHz		9		nV/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 0.5 V, $+V_S$ = 2 V, $-V_S$ = −1 V		0.23		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 0.5 V, $+V_S$ = 2 V, $-V_S$ = −1 V		0.77		Degrees
All-Hostile Crosstalk	f = 5 MHz, G = +2		−80		dB
DC PERFORMANCE					
Input Offset Voltage			±2.5	±10	mV
	T_{MIN} to T_{MAX}		±3.1		mV
Offset Drift			6		µV/°C
Input Bias Current		−50	+2	+50	pA
Open-Loop Gain	R_L = 1 kΩ to 1.5 V	72	76		dB
	R_L = 150 Ω to 1.5 V		65		dB
INPUT CHARACTERISTICS					
Input Resistance			5		GΩ
Input Capacitance			3.2		pF
Input Common-Mode Voltage Range			$-V_S$ − 0.3 to $+V_S$ − 0.8		V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to 1.5 V		87		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ to 1.5 V		0.01 to 2.98		V
	R_L = 150 Ω to 1.5 V		0.07 to 2.87		V
Output Current	1% THD with 1 MHz, V_O = 2 V p-p		37		mA
Short-Circuit Current					
Sourcing			80		mA
Sinking			163		mA
POWER-DOWN PINS ($\overline{PD1}$, $\overline{PD2}$, $\overline{PD3}$)	ADA4891-3 only				
Threshold Voltage, V_{TH}			1.3		V
Bias Current	Part enabled		48		nA
	Part powered down		−13		µA
Turn-On Time	Part enabled, output rises to 90% of final value		185		ns
Turn-Off Time	Part powered down, output falls to 10% of final value		58		ns
POWER SUPPLY					
Operating Range		2.7		5.5	V
Quiescent Current per Amplifier			3.5		mA
Supply Current When Powered Down	ADA4891-3 only		0.73		mA
Power Supply Rejection Ratio (PSRR)					
Positive PSRR	$+V_S$ = 3 V to 3.15 V, $-V_S$ = 0 V		76		dB
Negative PSRR	$+V_S$ = 3 V, $-V_S$ = −0.15 V to 0 V		72		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage (Common Mode)	$-V_S - 0.5$ V to $+V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4891-1/ADA4891-2/ADA4891-3/ADA4891-4 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

The still-air thermal properties of the package (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) can be used to determine the junction temperature of the die.

The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. It can be calculated by

$$P_D = (V_T \times I_S) + (V_S - V_{OUT}) \times (V_{OUT}/R_L) \quad (2)$$

where:
V_T is the total supply rail.
I_S is the quiescent current.
V_S is the positive supply rail.
V_{OUT} is the output of the amplifier.
R_L is the output load of the amplifier.

To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 6. These curves are derived by setting $T_J = 150°C$ in Equation 1. Figure 6 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard 4-layer board.

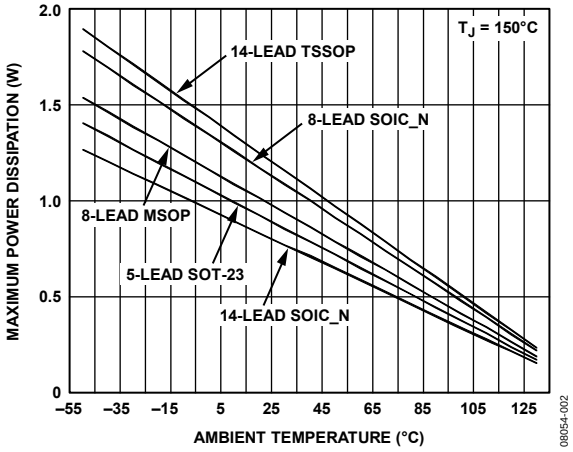


Figure 6. Maximum Power Dissipation vs. Ambient Temperature

Table 4 lists the thermal resistance (θ_{JA}) for each ADA4891-1/ADA4891-2/ADA4891-3/ADA4891-4 package.

Table 4.

Package Type	θ_{JA}	Unit
5-Lead SOT-23	146	°C/W
8-Lead SOIC_N	115	°C/W
8-Lead MSOP	133	°C/W
14-Lead SOIC_N	162	°C/W
14-Lead TSSOP	108	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, all plots are characterized for the ADA4891-1, ADA4891-2, ADA4891-3, and ADA4891-4. For the ADA4891-1 and ADA4891-2, the typical R_F value is 604 Ω. For the ADA4891-3 and ADA4891-4, the typical R_F value is 453 Ω.

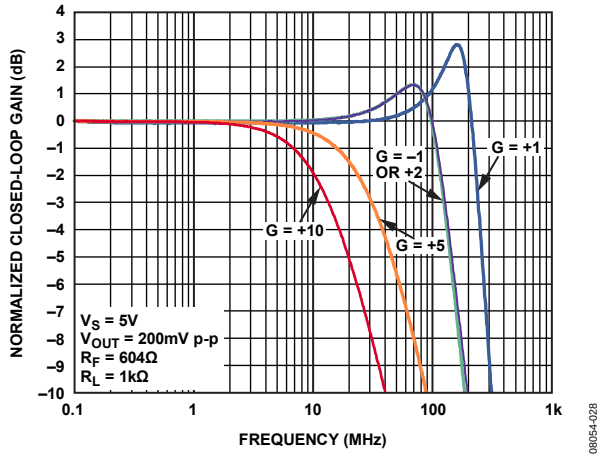


Figure 7. Small-Signal Frequency Response vs. Gain, V_S = 5 V, ADA4891-1/ADA4891-2

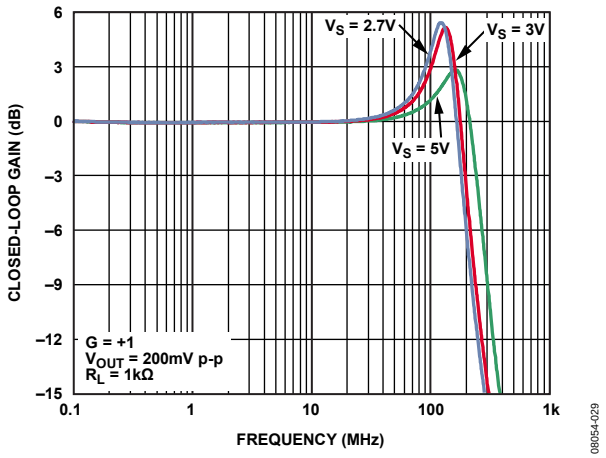


Figure 8. Small-Signal Frequency Response vs. Supply Voltage, ADA4891-1/ADA4891-2

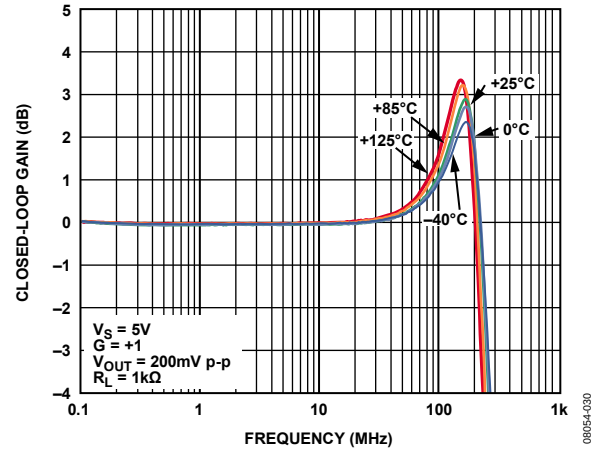


Figure 9. Small-Signal Frequency Response vs. Temperature, V_S = 5 V, ADA4891-1/ADA4891-2

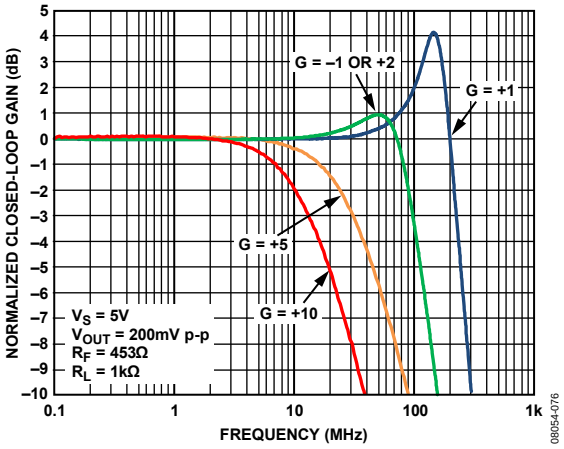


Figure 10. Small-Signal Frequency Response vs. Gain, V_S = 5 V, ADA4891-3/ADA4891-4

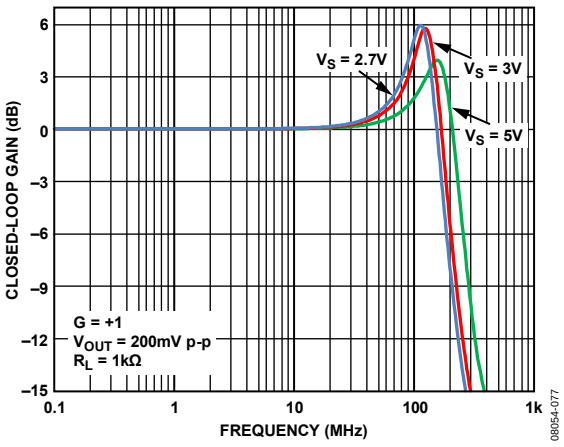


Figure 11. Small-Signal Frequency Response vs. Supply Voltage, ADA4891-3/ADA4891-4

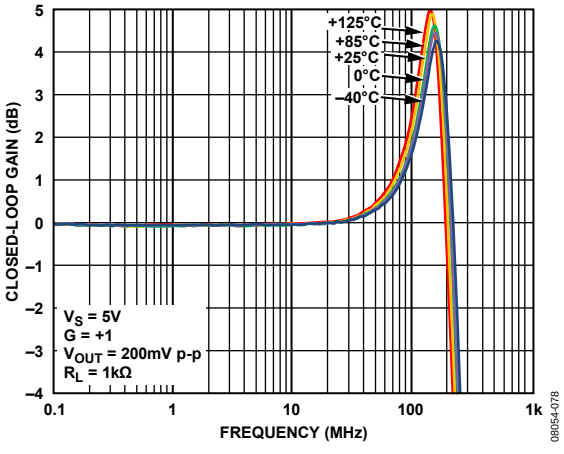


Figure 12. Small-Signal Frequency Response vs. Temperature, V_S = 5 V, ADA4891-3/ADA4891-4

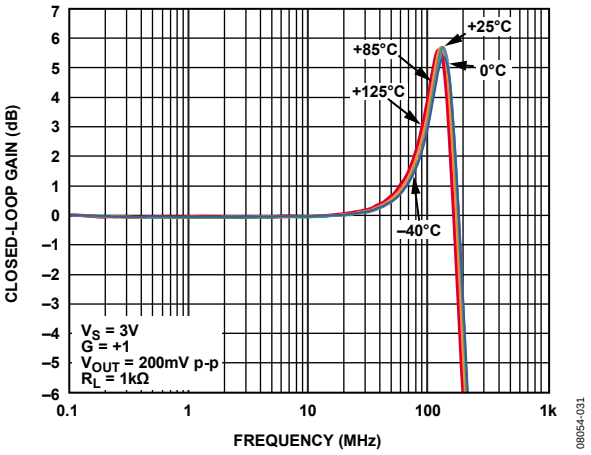


Figure 13. Small-Signal Frequency Response vs. Temperature, V_S = 3 V, ADA4891-1/ADA4891-2

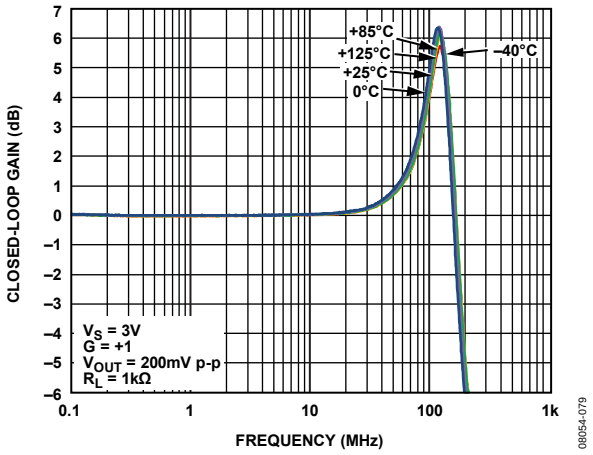


Figure 16. Small-Signal Frequency Response vs. Temperature, V_S = 3 V, ADA4891-3/ADA4891-4

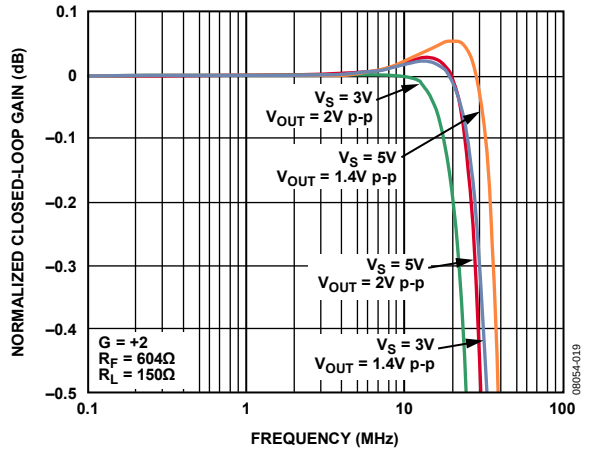


Figure 14. 0.1 dB Gain Flatness vs. Supply Voltage, G = +2, ADA4891-1/ADA4891-2

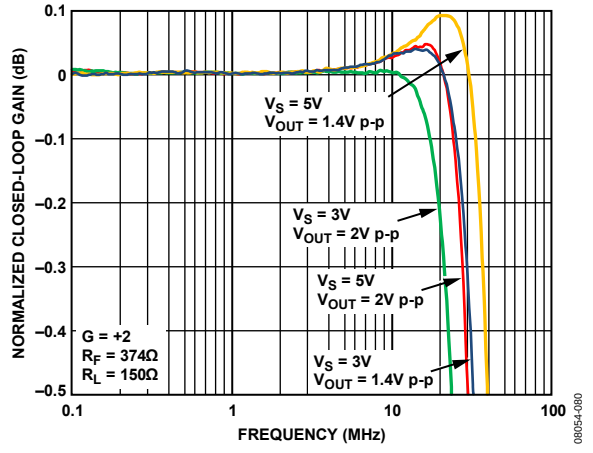


Figure 17. 0.1 dB Gain Flatness vs. Supply Voltage, G = +2, ADA4891-3/ADA4891-4

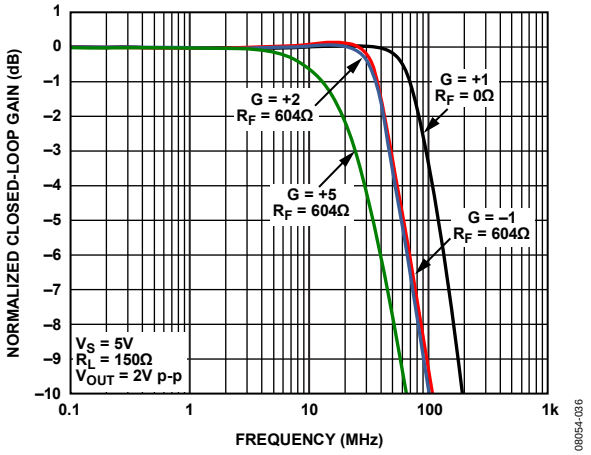


Figure 15. Large-Signal Frequency Response vs. Gain, V_S = 5 V, ADA4891-1/ADA4891-2

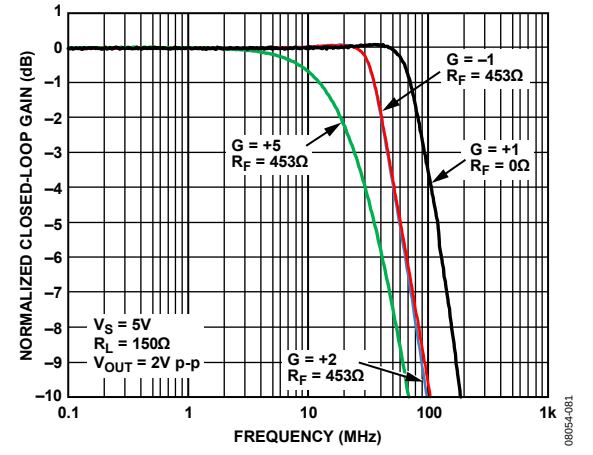


Figure 18. Large-Signal Frequency Response vs. Gain, V_S = 5 V, ADA4891-3/ADA4891-4

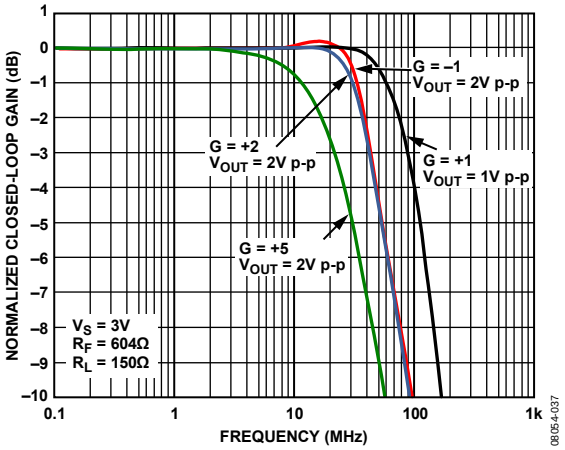


Figure 19. Large-Signal Frequency Response vs. Gain, V_S = 3 V, ADA4891-1/ADA4891-2

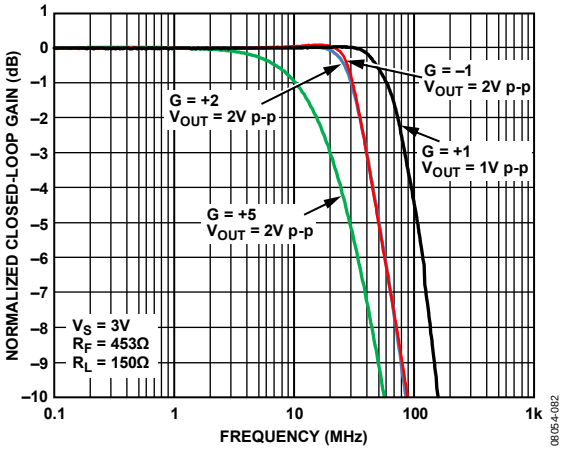


Figure 22. Large-Signal Frequency Response vs. Gain, V_S = 3 V, ADA4891-3/ADA4891-4

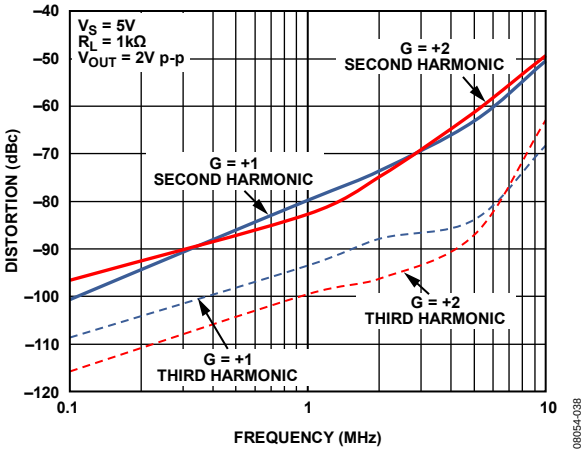


Figure 20. Harmonic Distortion (HD2, HD3) vs. Frequency, V_S = 5 V

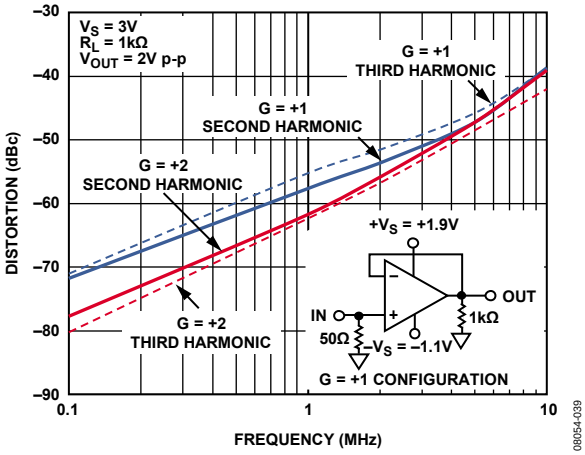


Figure 23. Harmonic Distortion (HD2, HD3) vs. Frequency, V_S = 3 V

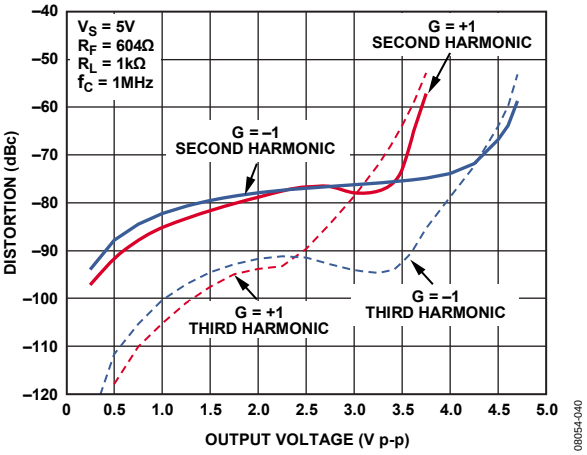


Figure 21. Harmonic Distortion (HD2, HD3) vs. Output Voltage, V_S = 5 V

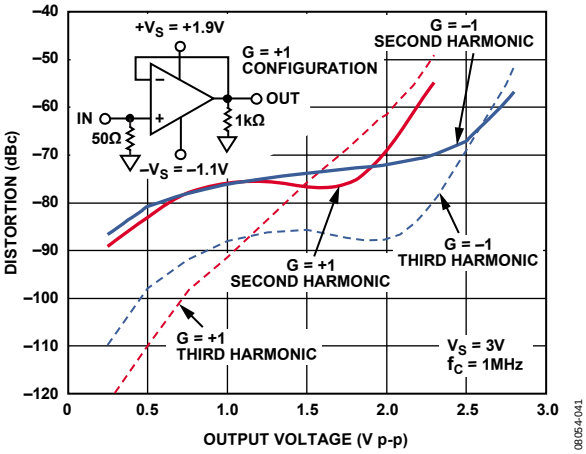


Figure 24. Harmonic Distortion (HD2, HD3) vs. Output Voltage, V_S = 3 V

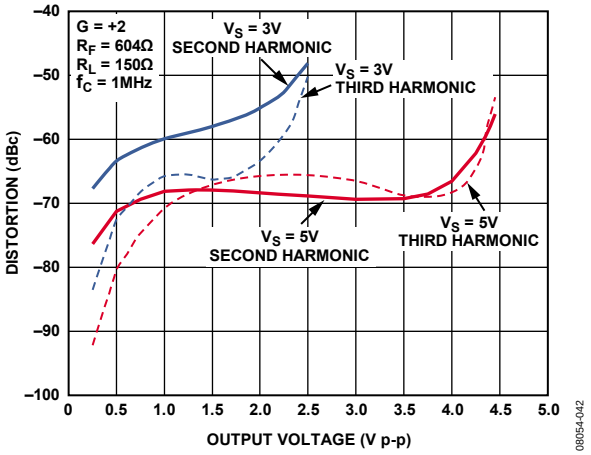


Figure 25. Harmonic Distortion (HD2, HD3) vs. Output Voltage, G = +2

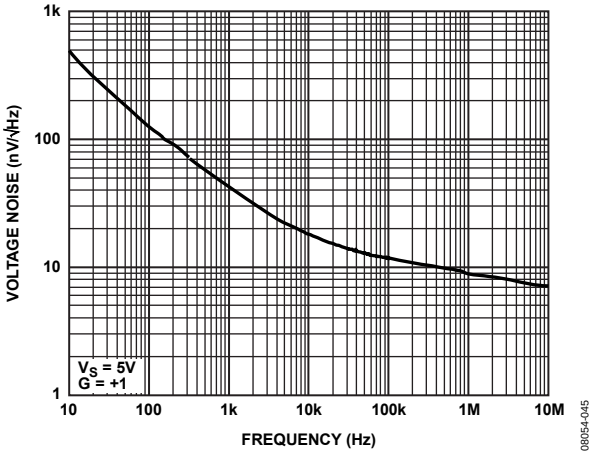


Figure 28. Input Voltage Noise vs. Frequency

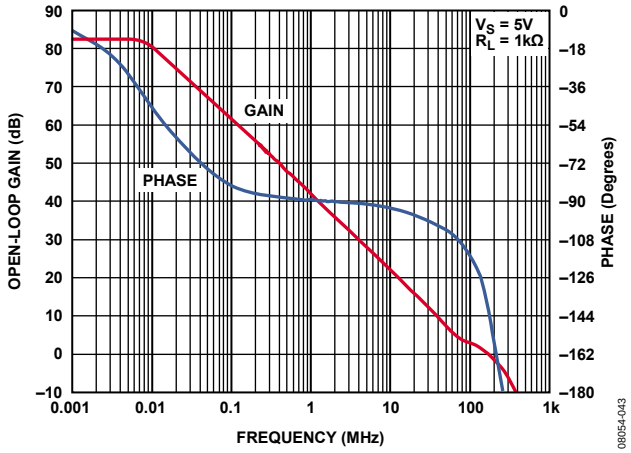


Figure 26. Open-Loop Gain and Phase vs. Frequency

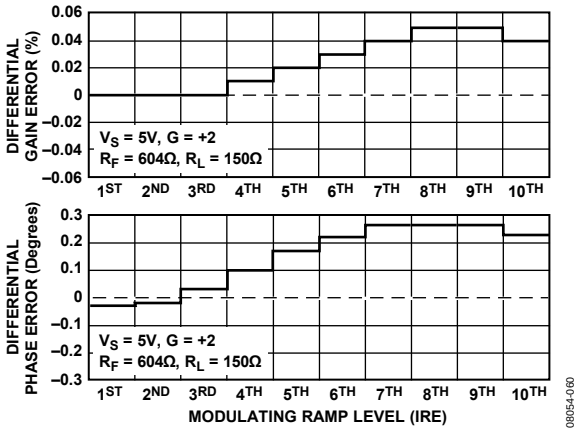


Figure 29. Differential Gain and Phase Errors

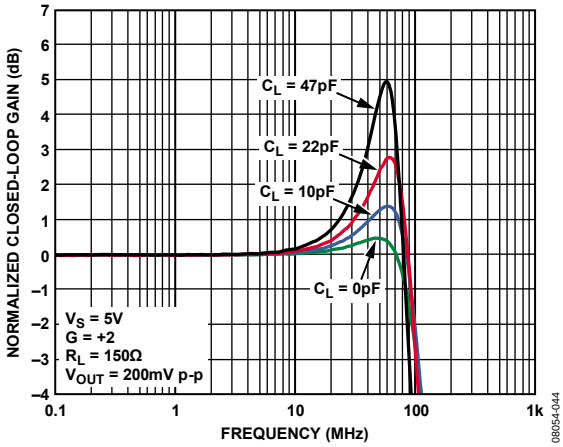


Figure 27. Small-Signal Frequency Response vs. C_L, ADA4891-1/ADA4891-2

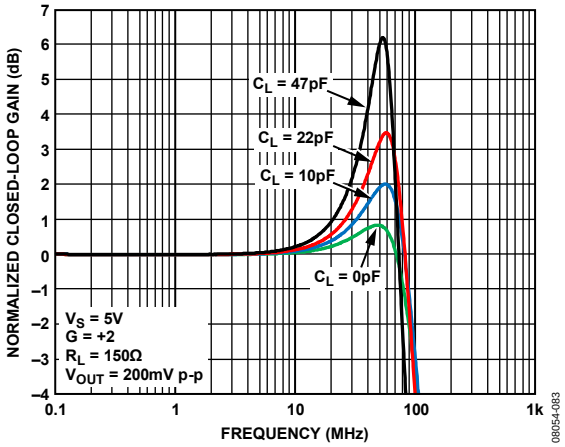


Figure 30. Small-Signal Frequency Response vs. C_L, ADA4891-3/ADA4891-4

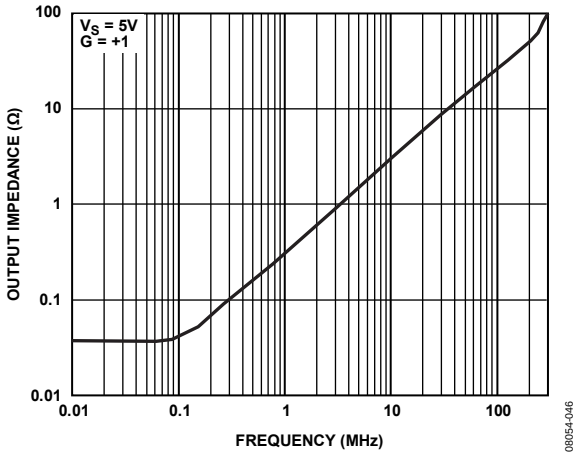


Figure 31. Closed-Loop Output Impedance vs. Frequency, Part Enabled

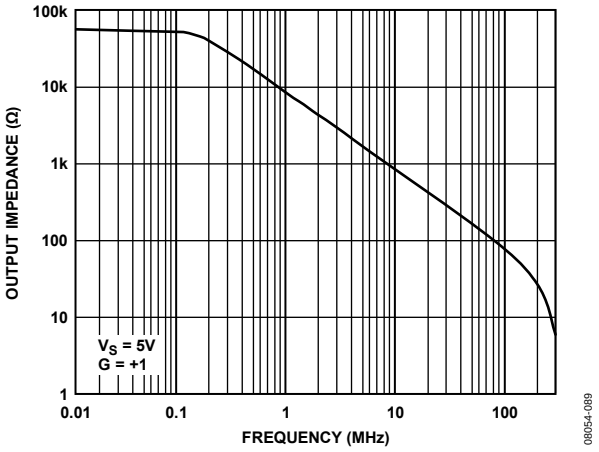


Figure 34. Closed-Loop Output Impedance vs. Frequency, Part Disabled (ADA4891-3 Only)

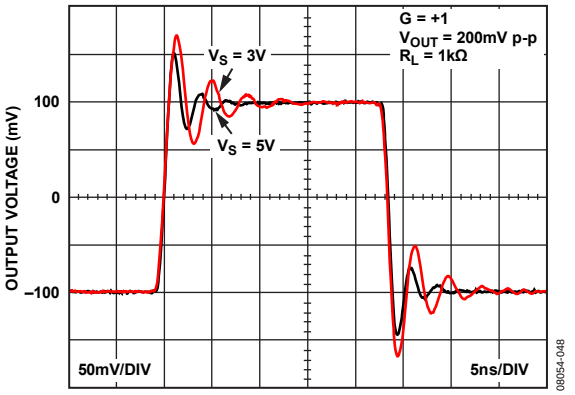


Figure 32. Small-Signal Step Response, G = +1

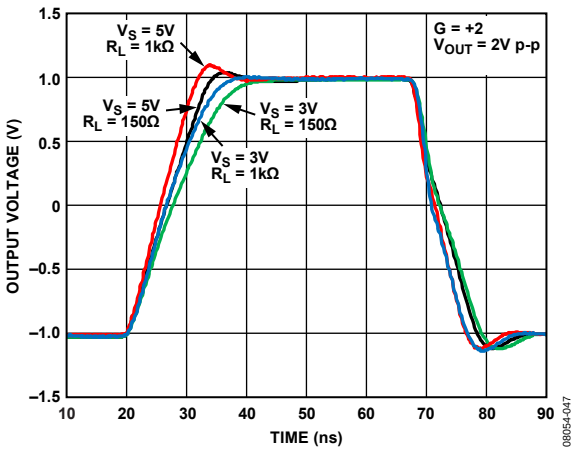


Figure 35. Large-Signal Step Response, G = +2

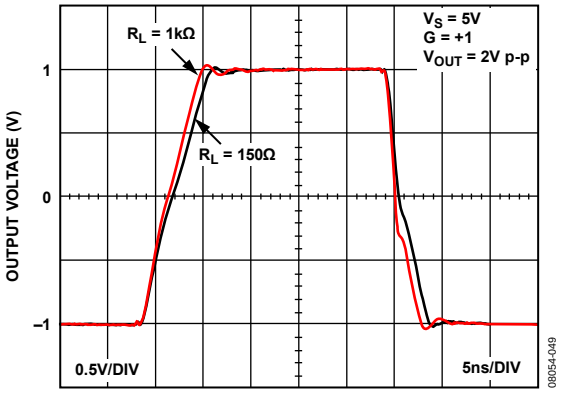


Figure 33. Large-Signal Step Response, V_S = 5 V, G = +1

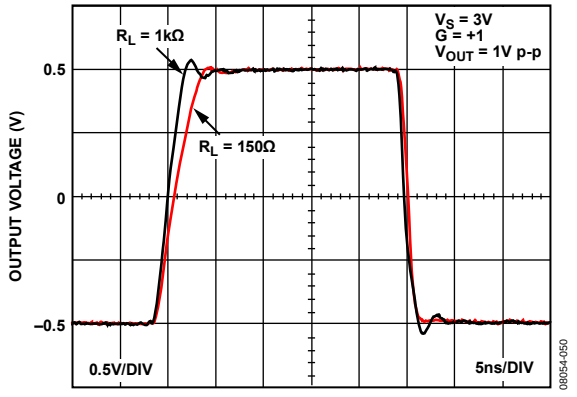


Figure 36. Large-Signal Step Response, V_S = 3 V, G = +1

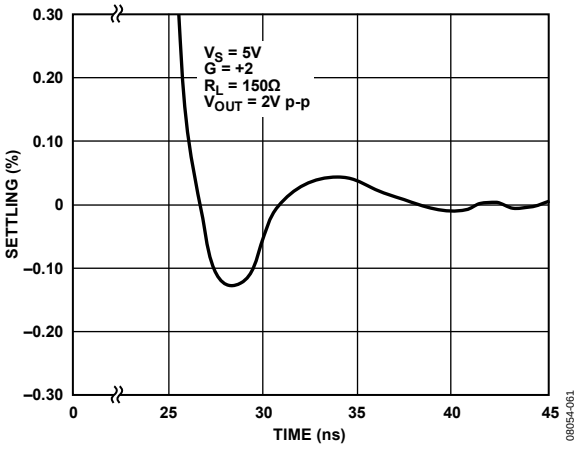


Figure 37. Short-Term Settling Time to 0.1%

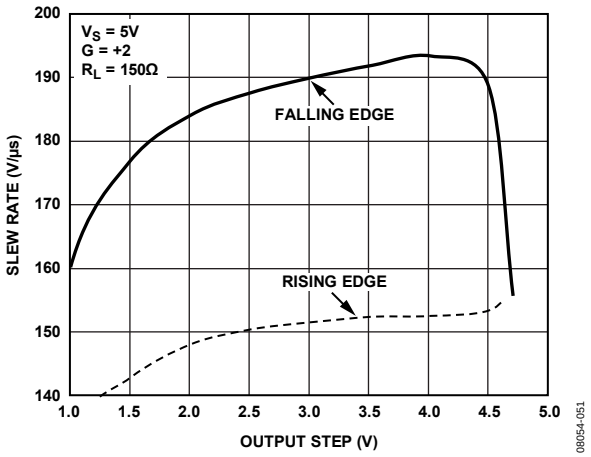


Figure 40. Slew Rate vs. Output Step

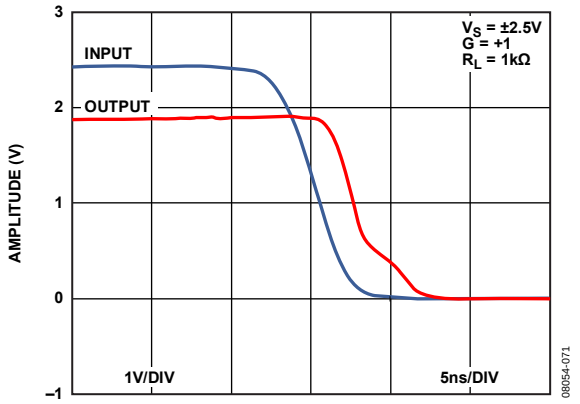


Figure 38. Input Overdrive Recovery from Positive Rail

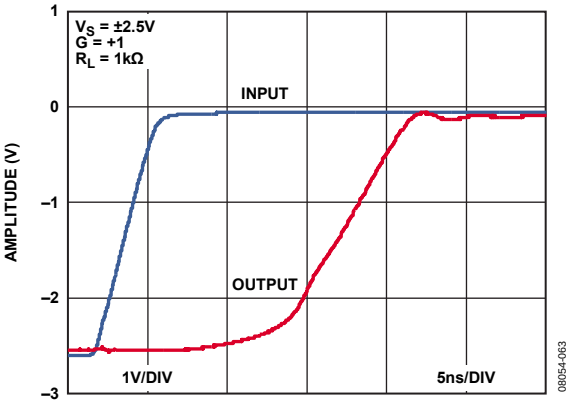


Figure 41. Input Overdrive Recovery from Negative Rail

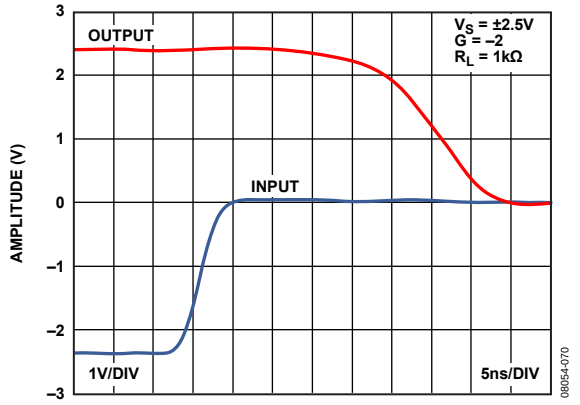


Figure 39. Output Overdrive Recovery from Positive Rail

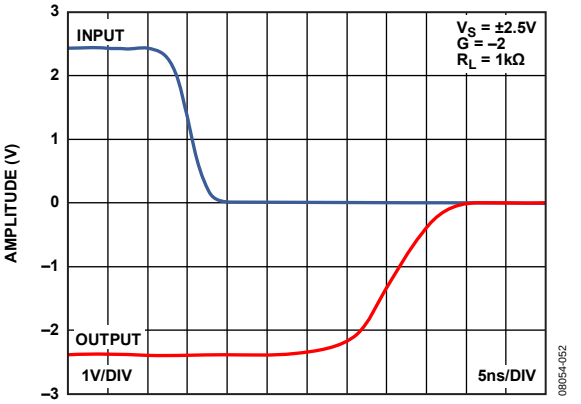


Figure 42. Output Overdrive Recovery from Negative Rail

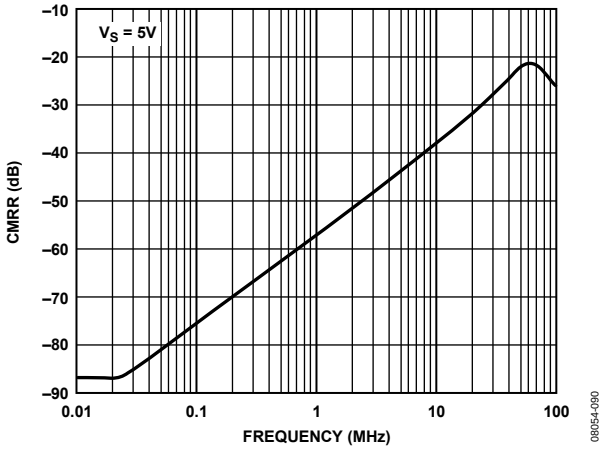


Figure 43. CMRR vs. Frequency

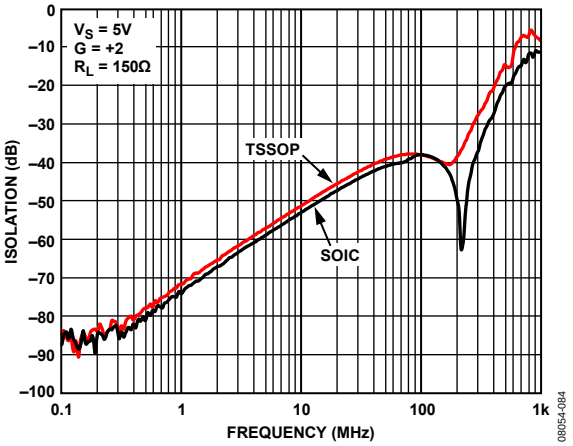


Figure 46. Forward Isolation vs. Frequency (ADA4891-3 Only)

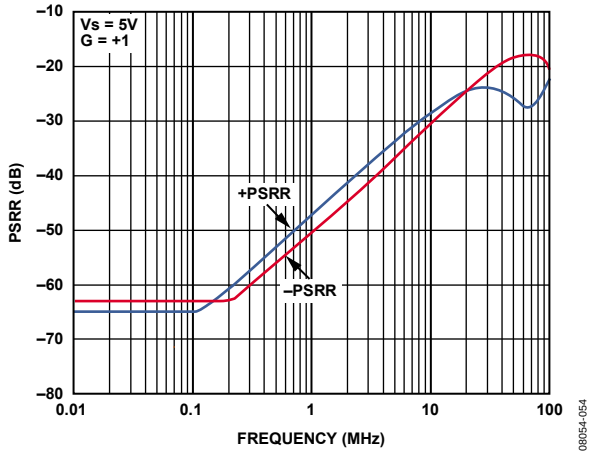


Figure 44. PSRR vs. Frequency

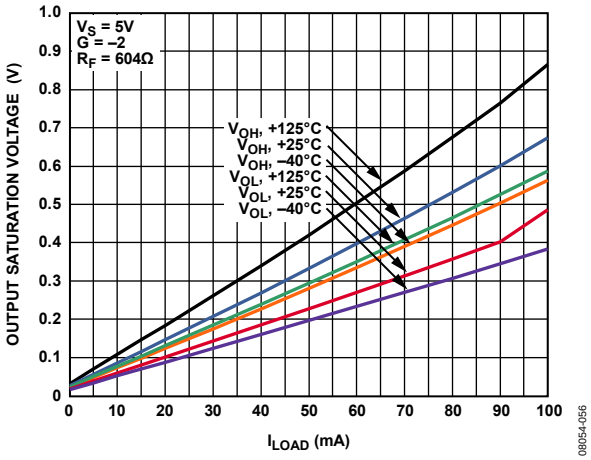


Figure 47. Output Saturation Voltage vs. Load Current and Temperature

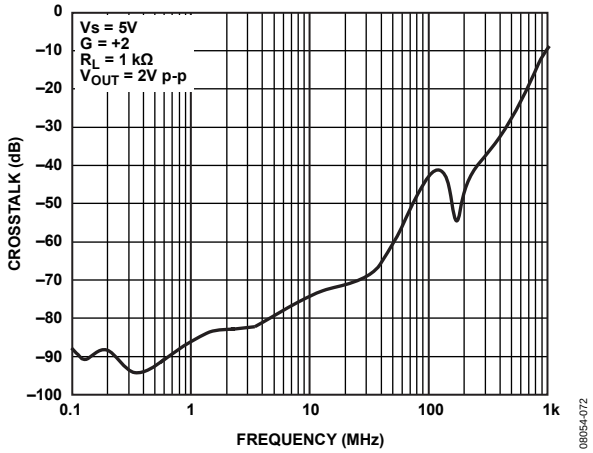


Figure 45. All-Hostile Crosstalk (Output-to-Output) vs. Frequency

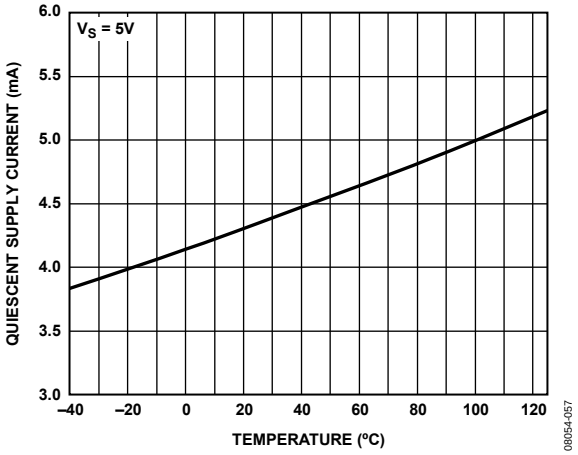


Figure 48. Supply Current per Amplifier vs. Temperature

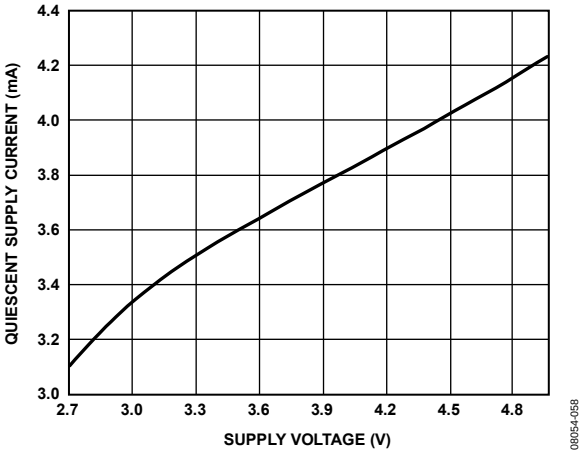


Figure 49. Supply Current per Amplifier vs. Supply Voltage

APPLICATIONS INFORMATION

USING THE ADA4891

Understanding the subtleties of the ADA4891 family of amplifiers provides insight into how to extract the peak performance from the device. The following sections describe the effect of gain, component values, and parasitics on the performance of the ADA4891. The wideband, noninverting gain configuration of the ADA4891 is shown in Figure 50; the wideband, inverting gain configuration of the ADA4891 is shown in Figure 51.

WIDEBAND, NONINVERTING GAIN OPERATION

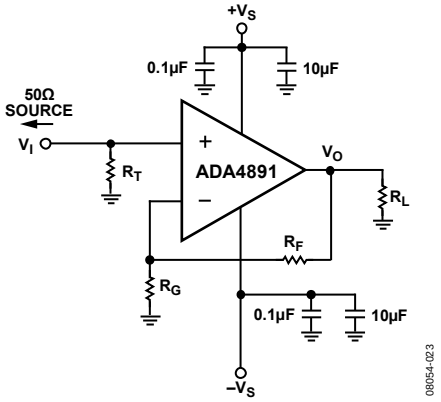


Figure 50. Noninverting Gain Configuration

In Figure 50, R_F and R_G denote the feedback and gain resistors, respectively. Together, R_F and R_G determine the noise gain of the amplifier. The value of R_F defines the 0.1 dB bandwidth (for more information, see the Effect of R_F on 0.1 dB Gain Flatness section). Typical R_F values range from 549 Ω to 698 Ω for the ADA4891-1/ADA4891-2. Typical R_F values range from 301 Ω to 453 Ω for the ADA4891-3/ADA4891-4.

In a controlled impedance signal path, R_T is used as the input termination resistor designed to match the input source impedance. Note that R_T is not required for normal operation. R_T is generally set to match the input source impedance.

WIDEBAND, INVERTING GAIN OPERATION

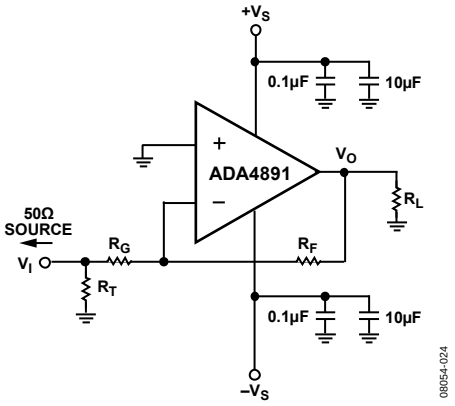


Figure 51. Inverting Gain Configuration

Figure 51 shows the inverting gain configuration. For the inverting gain configuration, set the parallel combination of R_T and R_G to match the input source impedance.

Note that a bias current cancellation resistor is not required in the noninverting input of the amplifier because the input bias current of the ADA4891 is very low (less than 2 pA). Therefore, the dc errors caused by the bias current are negligible.

For both noninverting and inverting gain configurations, it is often useful to increase the R_F value to decrease the load on the output. Increasing the R_F value improves harmonic distortion at the expense of reducing the 0.1 dB bandwidth of the amplifier. This effect is discussed further in the Effect of R_F on 0.1 dB Gain Flatness section.

RECOMMENDED VALUES

Table 5 and Table 6 provide a quick reference for various configurations and show the effect of gain on the −3 dB small-signal bandwidth, slew rate, and peaking of the ADA4891-1/ADA4891-2/ADA4891-3/ADA4891-4. Note that as the gain increases, the small-signal bandwidth decreases, as is expected from the gain bandwidth product relationship. In addition, the phase margin improves with higher gains, and the amplifier becomes more stable. As a result, the peaking in the frequency response is reduced (see Figure 7 and Figure 10).

Table 5. Recommended Component Values and Effect of Gain on ADA4891-1/ADA4891-2 Performance (R_L = 1 kΩ)

	Feedback Network Values		−3 dB Small-Signal Bandwidth (MHz)	Slew Rate (V/µs)		
Gain	R_F (Ω)	R_G (Ω)	V_{OUT} = 200 mV p-p	t_R	t_F	Peaking (dB)
−1	604	604	118	188	192	1.3
+1	0	Open	240	154	263	2.6
+2	604	604	120	170	210	1.4
+5	604	151	32.5	149	154	0
+10	604	67.1	12.7	71	72	0

Table 6. Recommended Component Values and Effect of Gain on ADA4891-3/ADA4891-4 Performance (R_L = 1 kΩ)

	Feedback Network Values		−3 dB Small-Signal Bandwidth (MHz)	Slew Rate (V/µs)		
Gain	R_F (Ω)	R_G (Ω)	V_{OUT} = 200 mV p-p	t_R	t_F	Peaking (dB)
−1	453	453	97	186	194	0.9
+1	0	Open	220	151	262	4.1
+2	453	453	97	181	223	0.9
+5	453	90.6	31	112	120	0
+10	453	45.3	13	68	67	0

EFFECT OF R_F ON 0.1 dB GAIN FLATNESS

Gain flatness is an important specification in video applications. It represents the maximum allowable deviation in the signal amplitude within the pass band. Tests have revealed that the human eye is unable to distinguish brightness variations of less than 1%, which translates into a 0.1 dB signal drop within the pass band or, put simply, 0.1 dB gain flatness.

The PCB layout configuration and bond pads of the chip often contribute to stray capacitance. The stray capacitance at the inverting input forms a pole with the feedback and gain resistors. This additional pole adds phase shift and reduces phase margin in the closed-loop phase response, causing instability in the amplifier and peaking in the frequency response.

Figure 52 and Figure 53 show the effect of using various values for Feedback Resistor R_F on the 0.1 dB gain flatness of the parts. Figure 52 shows the effect for the ADA4891-1/ADA4891-2. Figure 53 show the effect for the ADA4891-3/ADA4891-4. Note that a larger R_F value causes more peaking because the additional pole formed by R_F and the input stray capacitance shifts down in frequency and interacts significantly with the internal poles of the amplifier.

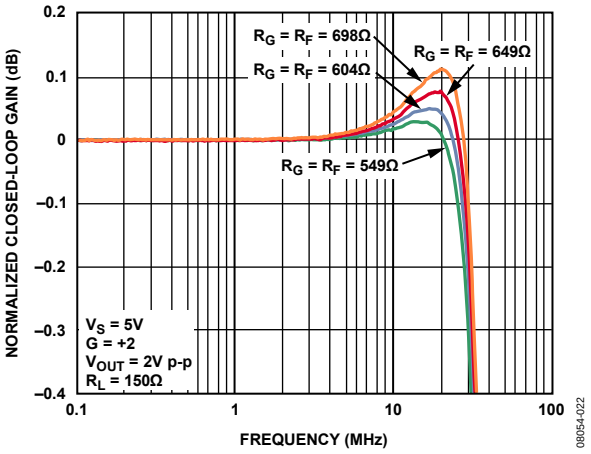


Figure 52. 0.1 dB Gain Flatness, Noninverting Gain Configuration, ADA4891-1/ADA4891-2

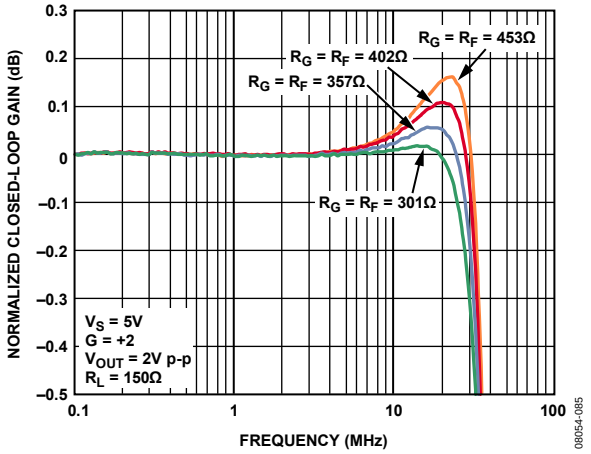


Figure 53. 0.1 dB Gain Flatness, Noninverting Gain Configuration, ADA4891-3/ADA4891-4

To obtain the desired 0.1 dB bandwidth, adjust the feedback resistor, R_F, as shown in Figure 52 and Figure 53. If R_F cannot be adjusted, a small capacitor can be placed in parallel with R_F to reduce peaking.

The feedback capacitor, C_F, forms a zero with the feedback resistor, which cancels out the pole formed by the input stray capacitance and the gain and feedback resistors. For a first pass in determining the C_F value, use the following equation:

$$R_G \times C_S = R_F \times C_F$$

where:
R_G is the gain resistor.
C_S is the input stray capacitance.
R_F is the feedback resistor.
C_F is the feedback capacitor.

Using this equation, the original closed-loop frequency response of the amplifier is restored, as if there is no stray input capacitance. Most often, however, the value of C_F is determined empirically.

Figure 54 shows the effect of using various values for the feedback capacitor to reduce peaking. In this case, the ADA4891-1/ADA4891-2 are used for demonstration purposes and R_F = R_G = 604 Ω. The input stray capacitance, together with the board parasitics, is approximately 2 pF.

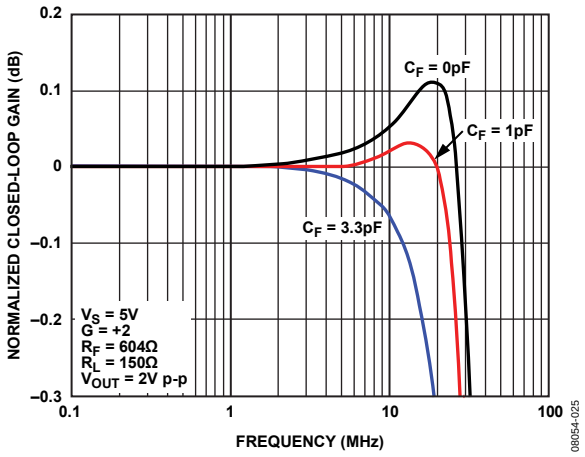


Figure 54. 0.1 dB Gain Flatness vs. C_F, V_S = 5 V, ADA4891-1/ADA4891-2

DRIVING CAPACITIVE LOADS

A highly capacitive load reacts with the output impedance of the amplifiers, causing a loss of phase margin and subsequent peaking or even oscillation. The ADA4891-1/ADA4891-2 are used to demonstrate this effect (see Figure 55 and Figure 56).

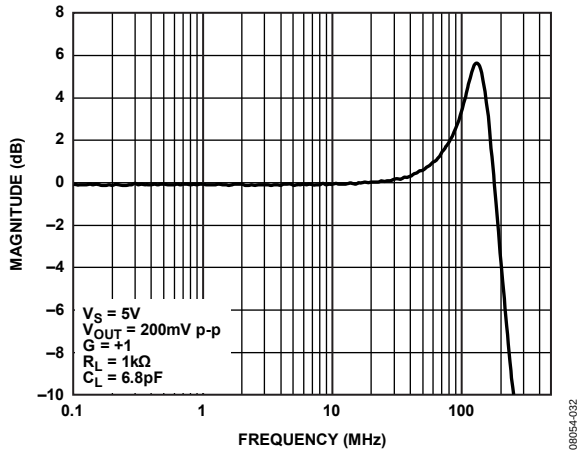


Figure 55. Closed-Loop Frequency Response, C_L = 6.8 pF, ADA4891-1/ADA4891-2

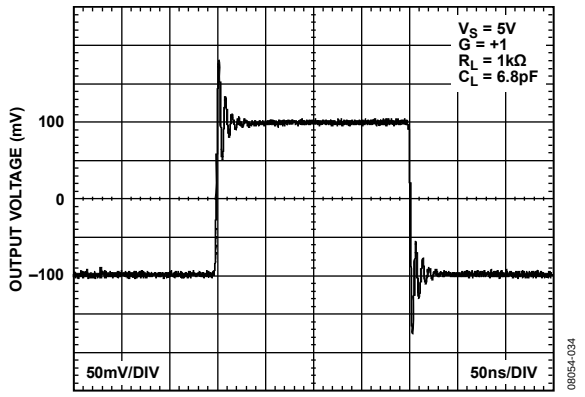


Figure 56. 200 mV Step Response, C_L = 6.8 pF, ADA4891-1/ADA4891-2

These four methods minimize the output capacitive loading effect.

- Reducing the output resistive load. This pushes the pole further away and, therefore, improves the phase margin.
- Increasing the phase margin with higher noise gains. As the closed-loop gain is increased, the larger phase margin allows for large capacitive loads with less peaking.
- Adding a parallel capacitor (C_F) with R_F, from −IN to the output. This adds a zero in the closed-loop frequency response, which tends to cancel out the pole formed by the capacitive load and the output impedance of the amplifier. See the Effect of R_F on 0.1 dB Gain Flatness section for more information.
- Placing a small value resistor (R_S) in series with the output to isolate the load capacitor from the output stage of the amplifier.

Figure 57 shows the effect of using a snub resistor (R_S) on reducing the peaking in the worst-case frequency response (gain of +1). Using R_S = 100 Ω reduces the peaking by 3 dB, with the trade-off that the closed-loop gain is reduced by 0.9 dB due to attenuation at the output. R_S can be adjusted from 0 Ω to 100 Ω to maintain an acceptable level of peaking and closed-loop gain, as shown in Figure 57.

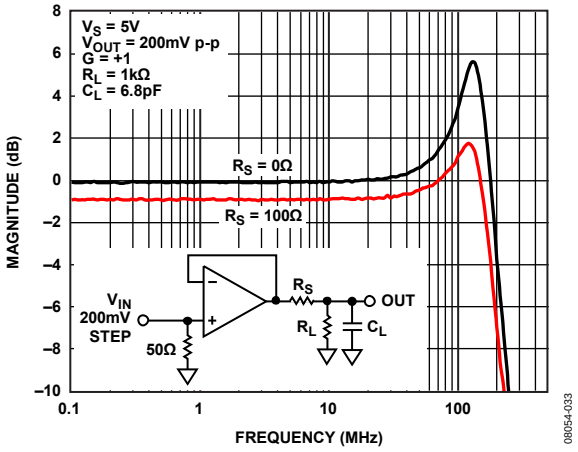


Figure 57. Closed-Loop Frequency Response with Snub Resistor, C_L = 6.8 pF

Figure 58 shows that the transient response is also much improved by the snub resistor (R_S = 100 Ω) compared to that of Figure 56.

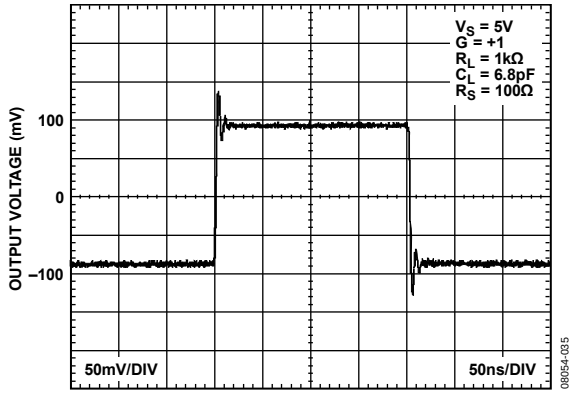


Figure 58. 200 mV Step Response, C_L = 6.8 pF, R_S = 100 Ω

TERMINATING UNUSED AMPLIFIERS

Terminating unused amplifiers in a multiamplifier package is an important step in ensuring proper operation of the functional amplifier. Unterminated amplifiers can oscillate and draw excessive power. The recommended procedure for terminating unused amplifiers is to connect any unused amplifiers in a unity-gain configuration and to connect the noninverting input to midsupply voltage. With symmetrical bipolar power supplies, this means connecting the noninverting input to ground, as shown in Figure 59.

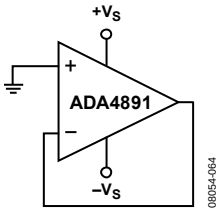


Figure 59. Terminating Unused Amplifier with Symmetrical Bipolar Power Supplies

In single power supply applications, a synthetic midsupply source must be created. This can be accomplished with a simple resistive voltage divider. Figure 60 shows the proper connection for terminating an unused amplifier in a single-supply configuration.

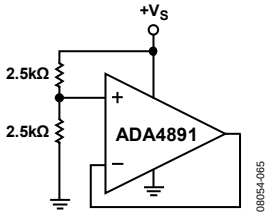


Figure 60. Terminating Unused Amplifier with Single Power Supply

DISABLE FEATURE (ADA4891-3 ONLY)

The ADA4891-3 includes a power-down feature that can be used to save power when an amplifier is not in use. When an amplifier is powered down, its output goes to a high impedance state. The output impedance decreases as frequency increases; this effect can be observed in Figure 34. With the power-down function, a forward isolation of −40 dB can be achieved at 50 MHz. Figure 46 shows the forward isolation vs. frequency data. The power-down feature is asserted by pulling the $\overline{PD1}$, $\overline{PD2}$, or $\overline{PD3}$ pin low.

Table 7 summarizes the operation of the power-down feature.

Table 7. Disable Function

Power-Down Pin Connection ($\overline{PDx}$)	Amplifier Status
>V_{TH} or floating	Enabled
<V_{TH}	Disabled

SINGLE-SUPPLY OPERATION

The ADA4891 can also be operated from a single power supply. Figure 61 shows the ADA4891-3 configured as a single 5 V supply video driver.

- The input signal is ac-coupled into the amplifier via Capacitor C1.
- Resistor R2 and Resistor R4 establish the input midsupply reference for the amplifier.
- Capacitor C5 prevents constant current from being drawn through the gain set resistor (R_G) and enables the ADA4891-3 at dc to provide unity gain to the input midsupply voltage, thereby establishing the output voltage at midsupply.
- Capacitor C6 is the output coupling capacitor.

The large-signal frequency response obtained with single-supply operation is identical to the bipolar supply operation (Figure 18 shows the large-signal frequency response).

Four pairs of low frequency poles are formed by R2/2 and C2, R3 and C1, R_G and C5, and R_L and C6. With this configuration, the −3 dB cutoff frequency at low frequency is 12 Hz. The values of C1, C2, C5, and C6 can be adjusted to change the low frequency −3 dB cutoff point to suit individual design needs.

For more information about single-supply operation of op amps, see the Analog Dialogue article "Avoiding Op Amp Instability Problems in Single-Supply Applications" (Volume 35, Number 2) at www.analog.com.

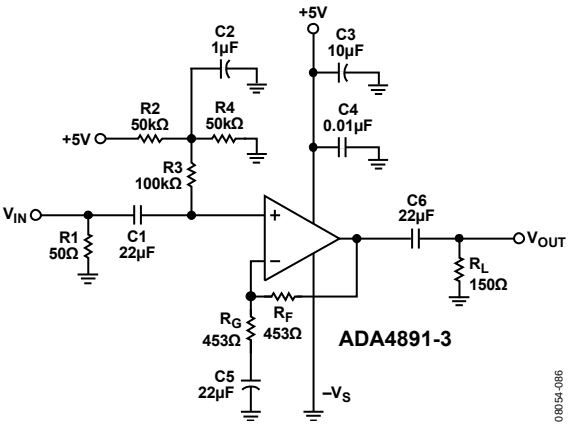


Figure 61. Single-Supply Video Driver Schematic

VIDEO RECONSTRUCTION FILTER

A common application for active filters is at the output of video digital-to-analog converters (DACs)/encoders. The filter, or more appropriately, the video reconstruction filter, is used at the output of a video DAC/encoder to eliminate the multiple images that are created during the sampling process within the DAC. For portable video applications, the ADA4891 is an ideal choice due to its lower power requirements and high performance.

For active filters, a good rule of thumb is that the −3 dB bandwidth of the amplifiers be at least 10 times higher than the corner frequency of the filter. This ensures that no initial roll-off is introduced by the amplifier and that the pass band is flat until the cutoff frequency.

An example of a 15 MHz, 3-pole, Sallen-Key, low-pass video reconstruction filter is shown in Figure 62. This circuit features a gain of +2, a 0.1 dB bandwidth of 7.3 MHz, and over 17 dB attenuation at 29.7 MHz (see Figure 63). The filter has three poles: two poles are active, with a third passive pole (R6 and C4) placed at the output. C3 improves the filter roll-off. R6, R7, and R8 make up the video load of 150 Ω. Components R6, C4, R7, R8, and the input termination of the network analyzer form a 6 dB attenuator; therefore, the reference level is roughly 0 dB, as shown in Figure 63.

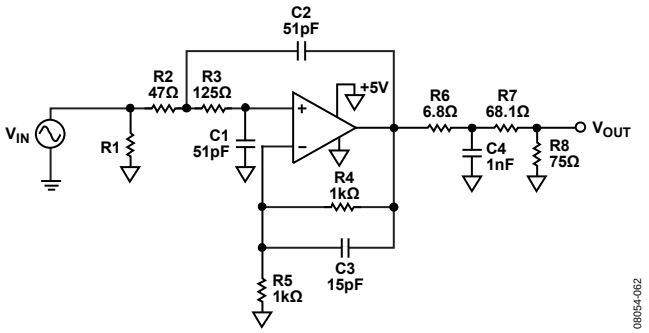


Figure 62. 15 MHz Video Reconstruction Filter Schematic

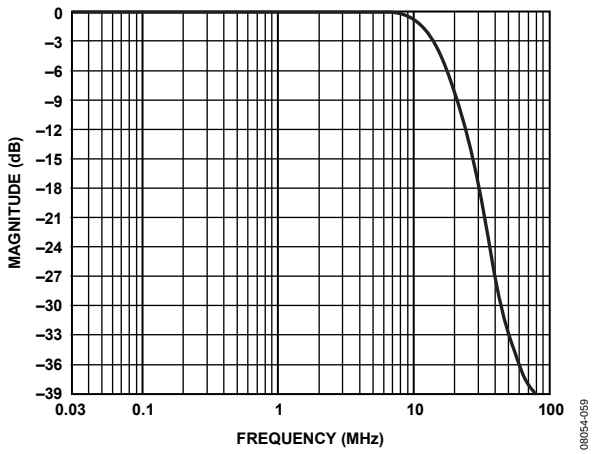


Figure 63. Video Reconstruction Filter Frequency Performance

MULTIPLEXER

The ADA4891-3 has a disable pin used to power down the amplifier to save power or to create a mux circuit. If two or more ADA4891-3 outputs are connected together and only one output is enabled, then only the signal of the enabled amplifier appears at the output. This configuration is used to select from various input signal sources. Additionally, the same input signal is applied to different gain stages, or differently tuned filters, to make a gain-step amplifier or a selectable frequency amplifier.

Figure 64 shows a schematic of two ADA4891-3 devices used to create a mux that selects between two inputs. One input is a 1 V p-p, 3 MHz sine wave; the other input is a 2 V p-p, 1 MHz sine wave.

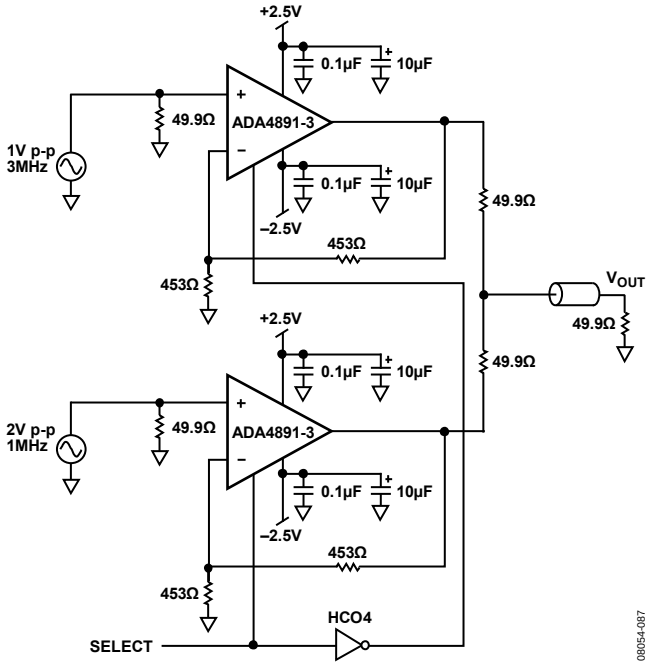


Figure 64. Two-to-One Multiplexer Using Two ADA4861-3 Devices

The select signal and the output waveforms for this circuit are shown in Figure 65.

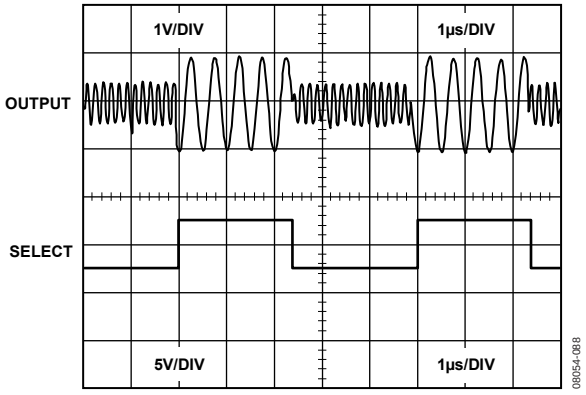


Figure 65. ADA4861-3 Mux Output

LAYOUT, GROUNDING, AND BYPASSING

POWER SUPPLY BYPASSING

Power supply pins are additional op amp inputs, and care must be taken so that a noise-free, stable dc voltage is applied. The purpose of bypass capacitors is to create a low impedance path from the supply to ground over a range of frequencies, thereby shunting or filtering the majority of the noise to ground. Bypassing is also critical for stability, frequency response, distortion, and PSRR performance.

If traces are used between components and the package, chip capacitors of 0.1 µF (X7R or NPO) are critical and should be placed as close as possible to the amplifier package. The 0508 case size for such a capacitor is recommended because it offers low series inductance and excellent high frequency performance. Larger chip capacitors, such as 0.1 µF capacitors, can be shared among a few closely spaced active components in the same signal path. A 10 µF tantalum capacitor is less critical for high frequency bypassing, but it provides additional bypassing for lower frequencies.

GROUNDING

When possible, ground and power planes should be used. Ground and power planes reduce the resistance and inductance of the power supply feeds and ground returns. If multiple planes are used, they should be stitched together with multiple vias. The returns for the input, output terminations, bypass capacitors, and R_G should all be kept as close to the ADA4891 as possible. Ground vias should be placed at the side or at the very end of the component mounting pads to provide a solid ground return. The output load ground and the bypass capacitor grounds should be returned to a common point on the ground plane to minimize parasitic inductance and to help improve distortion performance.

INPUT AND OUTPUT CAPACITANCE

Parasitic capacitance can cause peaking and instability and, therefore, should be minimized to ensure stable operation.

High speed amplifiers are sensitive to parasitic capacitance between the inputs and ground. A few picofarads of capacitance reduce the input impedance at high frequencies, in turn increasing the gain of the amplifier and causing peaking of the frequency response or even oscillations, if severe enough. It is recommended that the external passive components that are connected to the input pins be placed as close as possible to the inputs to avoid parasitic capacitance.

In addition, the ground and power planes under the pins of the ADA4891 should be cleared of copper to prevent parasitic capacitance between the input and output pins to ground. This is because a single mounting pad on a SOIC footprint can add as much as 0.2 pF of capacitance to ground if the ground or power plane is not cleared under the ADA4891 pins. In fact, the ground and power planes should be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling between the inputs and outputs and to avoid any positive feedback, the input and output signal traces should not be parallel. In addition, the input traces should not be close to each other. A minimum of 7 mils between the two inputs is recommended.

LEAKAGE CURRENTS

In extremely low input bias current amplifier applications, stray leakage current paths must be kept to a minimum. Any voltage differential between the amplifier inputs and nearby traces sets up a leakage path through the PCB. Consider a 1 V signal and 100 GΩ to ground present at the input of the amplifier. The resultant leakage current is 10 pA; this is 5× the typical input bias current of the amplifier. Poor PCB layout, contamination, and the board material can create large leakage currents. Common contaminants on boards are skin oils, moisture, solder flux, and cleaning agents. Therefore, it is imperative that the board be thoroughly cleaned and that the board surface be free of contaminants to take full advantage of the low input bias currents of the ADA4891.

To significantly reduce leakage paths, a guard ring/shield should be used around the inputs. The guard ring circles the input pins and is driven to the same potential as the input signal, thereby reducing the potential difference between pins. For the guard ring to be completely effective, it must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above and below, using a multilayer board (see Figure 66).

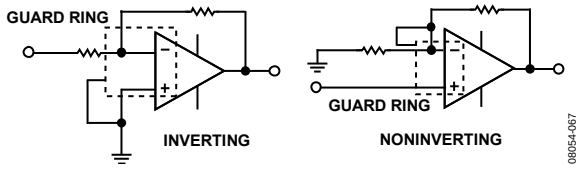


Figure 66. Guard Ring Configurations

The 5-lead SOT-23 package for the ADA4891-1 presents a challenge in keeping the leakage paths to a minimum. The pin spacing is very tight, so extra care must be used when constructing the guard ring (see Figure 67 for the recommended guard ring construction).

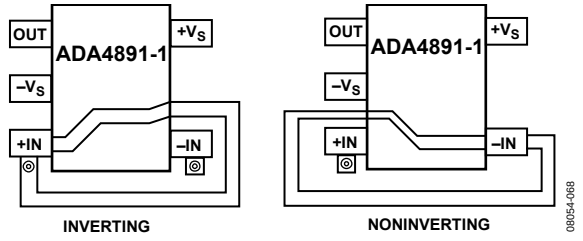
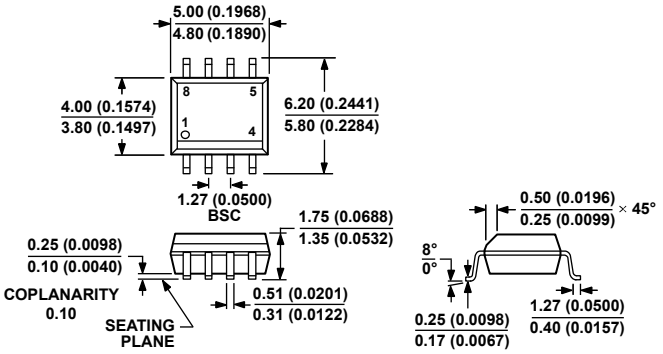


Figure 67. Guard Ring Layout, 5-Lead SOT-23

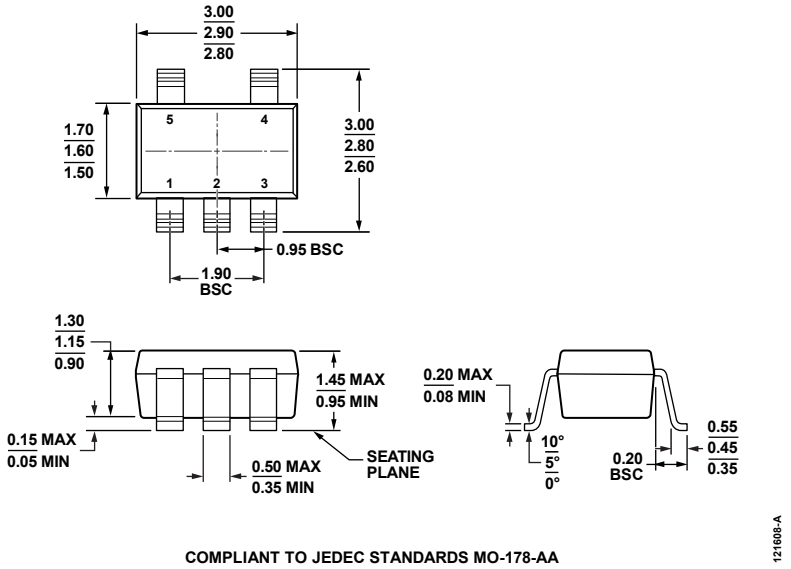
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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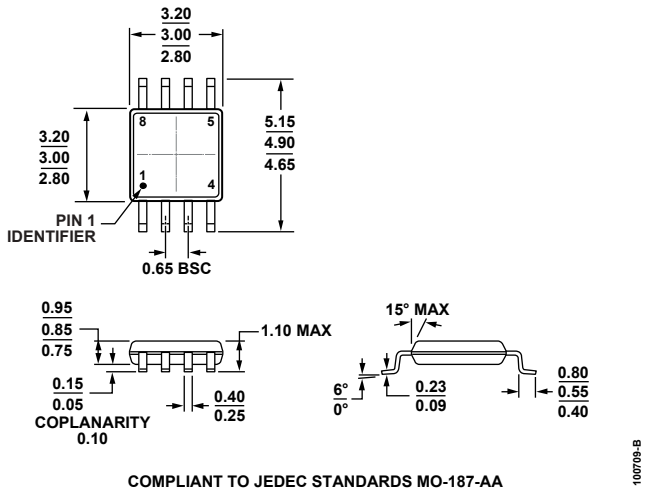
Figure 68. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-178-AA

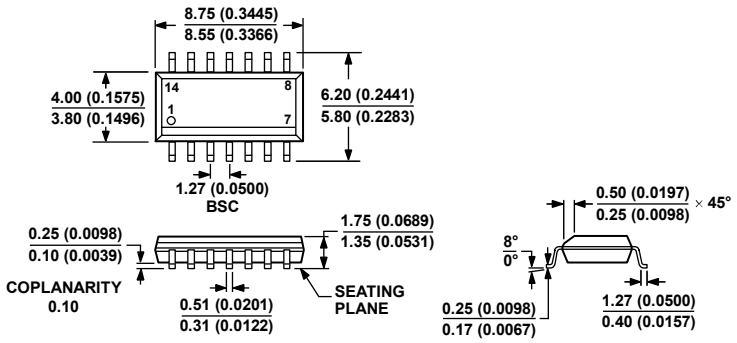
121608-A

Figure 69. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters



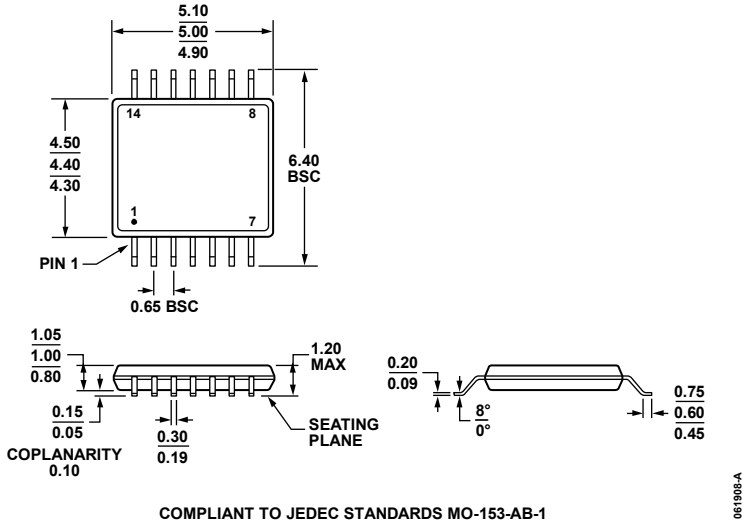
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 70. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



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Figure 71. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 72. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4891-1ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4891-1ARZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
ADA4891-1ARZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
ADA4891-1ARJZ-R7	−40°C to +125°C	5-Lead SOT-23, 7" Tape and Reel	RJ-5	H1W
ADA4891-1ARJZ-RL	−40°C to +125°C	5-Lead SOT-23, 13" Tape and Reel	RJ-5	H1W
ADA4891-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4891-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
ADA4891-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
ADA4891-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	H1U
ADA4891-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	H1U
ADA4891-2ARMZ-R7	−40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	H1U
ADA4891-3ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	
ADA4891-3ARUZ-R7	−40°C to +125°C	14-Lead TSSOP, 7" Tape and Reel	RU-14	
ADA4891-3ARUZ-RL	−40°C to +125°C	14-Lead TSSOP, 13" Tape and Reel	RU-14	
ADA4891-3ARZ	−40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4891-3ARZ-R7	−40°C to +125°C	14-Lead SOIC_N, 7" Tape and Reel	R-14	
ADA4891-3ARZ-RL	−40°C to +125°C	14-Lead SOIC_N, 13" Tape and Reel	R-14	
ADA4891-4ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	
ADA4891-4ARUZ-R7	−40°C to +125°C	14-Lead TSSOP, 7" Tape and Reel	RU-14	
ADA4891-4ARUZ-RL	−40°C to +125°C	14-Lead TSSOP, 13" Tape and Reel	RU-14	
ADA4891-4ARZ	−40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4891-4ARZ-R7	−40°C to +125°C	14-Lead SOIC_N, 7" Tape and Reel	R-14	
ADA4891-4ARZ-RL	−40°C to +125°C	14-Lead SOIC_N, 13" Tape and Reel	R-14	
ADA4891-1AR-EBZ		Evaluation Board for 8-Lead SOIC_N		
ADA4891-1ARJ-EBZ		Evaluation Board for 5-Lead SOT-23		
ADA4891-2AR-EBZ		Evaluation Board for 8-Lead SOIC_N		
ADA4891-2ARM-EBZ		Evaluation Board for 8-Lead MSOP		
ADA4891-3AR-EBZ		Evaluation Board for 14-Lead SOIC_N		
ADA4891-3ARU-EBZ		Evaluation Board for 14-Lead TSSOP		
ADA4891-4AR-EBZ		Evaluation Board for 14-Lead SOIC_N		
ADA4891-4ARU-EBZ		Evaluation Board for 14-Lead TSSOP		

[1] Z = RoHS Compliant Part.

NOTES

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