18 V, 725 µA, 4 MHz CMOS RRIO Operational Amplifier

Data Sheet

ADA4666-2

FEATURES

- Low power at high voltage (18 V): 725 µA maximum
- Low offset voltage:
  - 2.2 mV maximum over entire common-mode range
- Low input bias current: 15 pA maximum
- Gain bandwidth product: 4 MHz typical at A_V = 100
- Unity-gain crossover: 4 MHz typical
- −3 dB closed-loop bandwidth: 2.1 MHz typical
- Single-supply operation: 3 V to 18 V
- Dual-supply operation: ±1.5 V to ±9 V
- Unity-gain stable

APPLICATIONS

- Current shunt monitors
- Active filters
- Portable medical equipment
- Buffer/level shifting
- High impedance sensor interfaces
- Battery powered instrumentation

GENERAL DESCRIPTION

The ADA4666-2 is a dual, rail-to-rail input/output amplifier optimized for low power, high bandwidth, and wide operating supply voltage range applications.

The ADA4666-2 performance is guaranteed at 3.0 V, 10 V, and 18 V power supply voltages. It is an excellent selection for applications that use single-ended supplies of 3.3 V, 5 V, 10 V, 12 V, and 15 V, and dual supplies of ±2.5 V, ±3.3 V, and ±5 V.

The ADA4666-2 is specified over the extended industrial temperature range (−40°C to +125°C) and is available in 8-lead MSOP and 8-lead LFCSP (3 mm × 3 mm) packages.

PIN CONNECTION DIAGRAMS

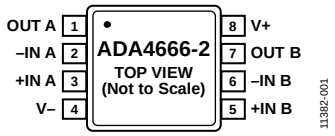


Figure 1. 8-Lead MSOP

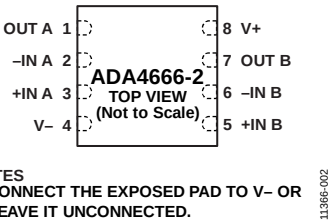


Figure 2. 8-Lead LFCSP

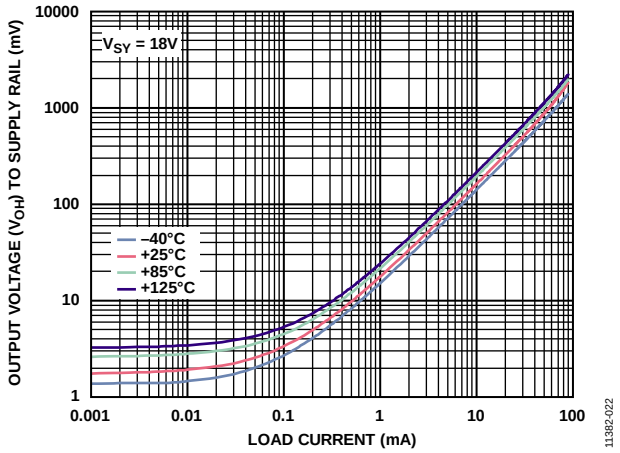


Figure 3. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

Table 1. Precision Low Power Op Amps (<1 mA)

Supply Voltage	5 V	12 V to 16 V	30 V
Single	ADA4505-1	OP196	OP777
	AD8500		
Dual	ADA4505-2	AD8657	ADA4096-2
	AD8502	OP296	OP727
	AD8506	ADA4661-2	AD8682
	AD8546	ADA4666-2	AD8622
Quad	ADA4505-4	AD8659	ADA4096-4
	AD8504	OP496	OP747
	AD8508		AD8684
	AD8548		AD8624

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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REVISION HISTORY

7/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—18 V OPERATION

V_{SY} = 18 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.5	2.2	mV
		V_{CM} = 0 V to 18 V			2.2	mV
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C			3.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.6	3.1	µV/°C
Input Bias Current	I_B			0.5	15	pA
		−40°C ≤ T_A ≤ +85°C			100	pA
		−40°C ≤ T_A ≤ +125°C			900	pA
Input Offset Current	I_{OS}				11	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
		−40°C ≤ T_A ≤ +125°C			300	pA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 18 V	80	95		dB
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C	77			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 17.5 V	120	147		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Input Resistance						
Differential Mode	R_{INDM}			>10		GΩ
Common Mode	R_{INCM}			>10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			8.5		pF
Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	17.95	17.97		V
		−40°C ≤ T_A ≤ +125°C	17.94			V
		R_L = 1 kΩ to V_{CM}	17.6	17.79		V
		−40°C ≤ T_A ≤ +125°C	17.58			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		14	25	mV
		−40°C ≤ T_A ≤ +125°C			40	mV
		R_L = 1 kΩ to V_{CM}		120	200	mV
		−40°C ≤ T_A ≤ +125°C			300	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		40		mA
Short-Circuit Current	I_{SC}	Pulse width = 10 ms; refer to the Maximum Power Dissipation section		±220		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		0.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		630	725	µA
		−40°C ≤ T_A ≤ +125°C			975	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_S = 1 kΩ, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		4		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2.1		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		60		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		1.3		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Channel Separation	CS	V_{IN} = 17.9 V p-p, f = 10 kHz, R_L = 10 kΩ		80		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV peak (200 mV p-p)				
f = 400 MHz				34		dB
f = 900 MHz				42		dB
f = 1800 MHz				50		dB
f = 2400 MHz				60		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	A_V = 1, V_{IN} = 5.4 V rms at 1 kHz				
Bandwidth = 80 kHz				0.0004		%
Bandwidth = 500 kHz				0.0008		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		360		fA/√Hz

ELECTRICAL CHARACTERISTICS—10 V OPERATION

V_{SY} = 10 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				2.2	mV
		V_{CM} = 0 V to 10 V			2.2	mV
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C			3.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.6	3.1	µV/°C
Input Bias Current	I_B			0.25	15	pA
		−40°C ≤ T_A ≤ +85°C			80	pA
		−40°C ≤ T_A ≤ +125°C			750	pA
Input Offset Current	I_{OS}				11	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
		−40°C ≤ T_A ≤ +125°C			270	pA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 10 V	75	90		dB
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C	72			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 9.5 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Input Resistance						
Differential Mode	R_{INDM}			>10		GΩ
Common Mode	R_{INCM}			>10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			8.5		pF
Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	9.96	9.98		V
		−40°C ≤ T_A ≤ +125°C	9.96			V
		R_L = 1 kΩ to VCM	9.7	9.88		V
		−40°C ≤ T_A ≤ +125°C	9.7			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		10	15	mV
		−40°C ≤ T_A ≤ +125°C			30	mV
		R_L = 1 kΩ to V_{CM}		77	110	mV
		−40°C ≤ T_A ≤ +125°C			200	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		40		mA
Short-Circuit Current	I_{SC}	Pulse width = 10 ms; refer to the Maximum Power Dissipation section		±220		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		0.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		620	725	µA
		−40°C ≤ T_A ≤ +125°C			975	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_S = 1 kΩ, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.8		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		4		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2.1		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		60		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		1.3		µs
Channel Separation	CS	V_{IN} = 9.9 V p-p, f = 10 kHz, R_L = 10 kΩ		85		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV peak (200 mV p-p)				
f = 400 MHz				34		dB
f = 900 MHz				42		dB
f = 1800 MHz				50		dB
f = 2400 MHz				60		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	A_V = 1, V_{IN} =2.2 V rms at 1 kHz				
Bandwidth = 80 kHz				0.0004		%
Bandwidth = 500 kHz				0.0008		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		360		fA/√Hz

ELECTRICAL CHARACTERISTICS—3.0 V OPERATION

V_{SY} = 3.0 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.5	2.2	mV
		V_{CM} = 0 V to 3.0 V			2.2	mV
		V_{CM} = 0 V to 3.0 V; −40°C ≤ T_A ≤ +125°C			3.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.6	3.1	µV/°C
Input Bias Current	I_B			0.15	8	pA
		−40°C ≤ T_A ≤ +85°C			45	pA
		−40°C ≤ T_A ≤ +125°C			650	pA
Input Offset Current	I_{OS}				11	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
		−40°C ≤ T_A ≤ +125°C			27	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3.0 V	64	80		dB
		V_{CM} = 0 V to 3.0 V; −40°C ≤ T_A ≤ +125°C	61			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 2.5 V	105	130		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Input Resistance						
Differential Mode	R_{INDM}			>10		GΩ
Common Mode	R_{INCM}			>10		GΩ
Input Capacitance,						
Differential Mode	C_{INDM}			8.5		pF
Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.98	2.99		V
		−40°C ≤ T_A ≤ +125°C	2.98			V
		R_L = 1 kΩ to V_{CM}	2.9	2.96		V
		−40°C ≤ T_A ≤ +125°C	2.9			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		4	8	mV
		−40°C ≤ T_A ≤ +125°C			15	mV
		R_L = 1 kΩ to V_{CM}		25	40	mV
		−40°C ≤ T_A ≤ +125°C			65	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		40		mA
Short-Circuit Current	I_{SC}	Pulse width = 10 ms; refer to the Maximum Power Dissipation section		±220		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		0.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		615	725	µA
		−40°C ≤ T_A ≤ +125°C			975	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_S = 1 kΩ, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.7		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		4		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.7		MHz
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		1.3		µs
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		60		Degrees
Channel Separation	CS	V_{IN} = 2.9 V p-p, f = 10 kHz, R_L = 10 kΩ		90		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV peak (200 mV p-p)				
f = 400 MHz				34		dB
f = 900 MHz				42		dB
f = 1800 MHz				50		dB
f = 2400 MHz				60		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	A_V = 1, V_{IN} = 0.44 V rms at 1 kHz				
Bandwidth = 80 kHz				0.002		%
Bandwidth = 500 kHz				0.003		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		360		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage	(V–) – 300 mV to (V+) + 300 mV
Input Current[1]	±10 mA
Differential Input Voltage	Limited by maximum input current
Output Short-Circuit Duration to GND	Refer to the Maximum Power Dissipation section
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
Junction	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD	4 kV
Human Body Model[2]	
Machine Model[3]	400 V
Field-Induced Charged-Device Model (FICDM)[4]	1.25 kV

[1] The input pins have clamp diodes to the power supply pins and to each other. Limit the input current to 10 mA or less when input signals exceed the power supply rail by 0.3 V.
[2] Applicable standard: MIL-STD-883, Method 3015.7.
[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).
[4] Applicable Standard JESD22-C101C (ESD FICDM standard of JEDEC).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer JEDEC board. The exposed pad of the LFCSP package is soldered to the board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	142	45	°C/W
8-Lead LFCSP	83.5	48.5[1]	°C/W

[1] θ_{JC} is measured on the top surface of the package.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

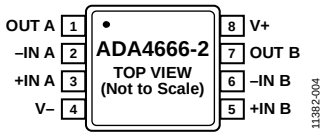


Figure 4. Pin Configuration, 8-Lead MSOP

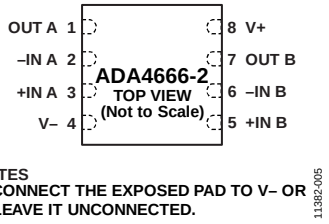


Figure 5. Pin Configuration, 8-Lead LFCSP

Table 7. Pin Function Descriptions

Pin No.[1]			
8-Lead MSOP	**8-Lead LFCSP**	**Mnemonic**	**Description**
1	1	OUT A	Output, Channel A.
2	2	–IN A	Negative Input, Channel A.
3	3	+IN A	Positive Input, Channel A.
4	4	V–	Negative Supply Voltage.
5	5	+IN B	Positive Input, Channel B.
6	6	–IN B	Negative Input, Channel B.
7	7	OUT B	Output, Channel B.
8	8	V+	Positive Supply Voltage.
N/A	9[2]	EPAD	Exposed Pad. For the 8-lead LFCSP only, connect the exposed pad to V– or leave it unconnected.

[1] N/A means not applicable.
[2] The exposed pad is not shown in the pin configuration diagram, Figure 5.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

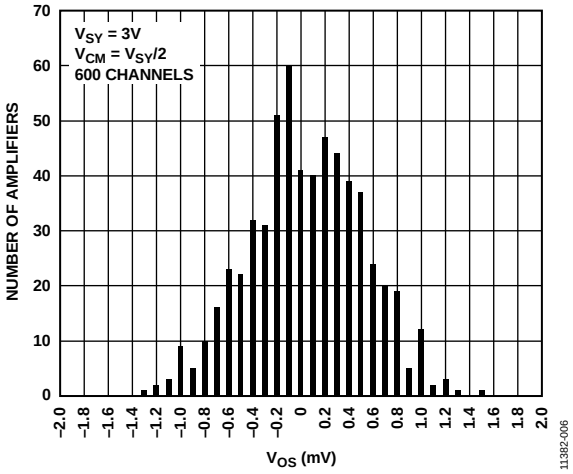


Figure 6. Input Offset Voltage Distribution

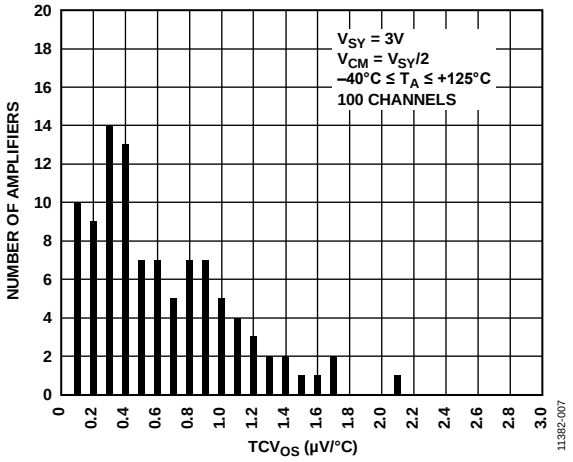


Figure 7. Input Offset Voltage Drift Distribution

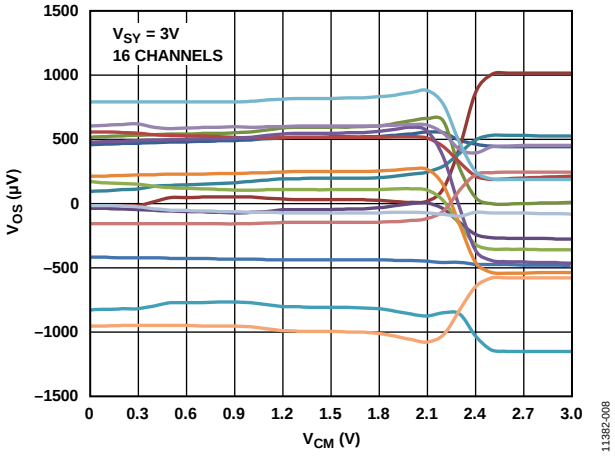


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

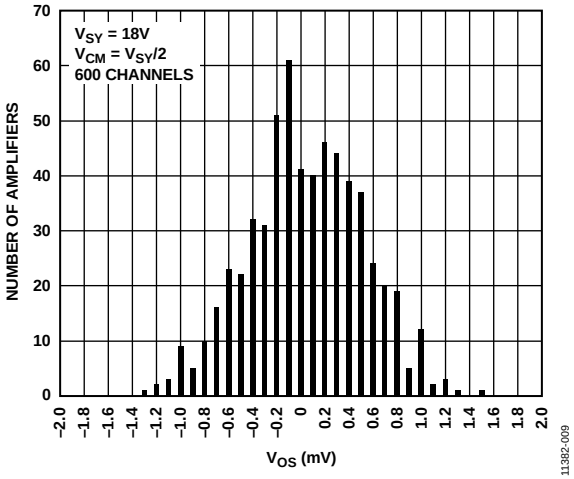


Figure 9. Input Offset Voltage Distribution

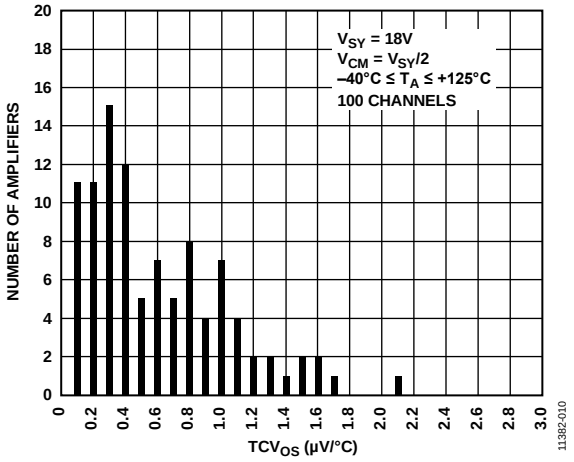


Figure 10. Input Offset Voltage Drift Distribution

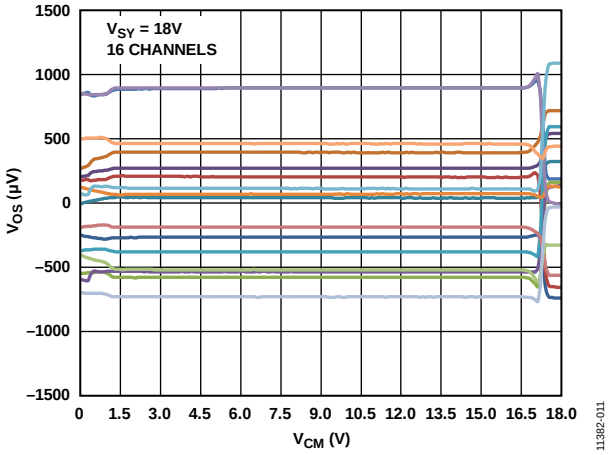


Figure 11. Input Offset Voltage vs. Common-Mode Voltage

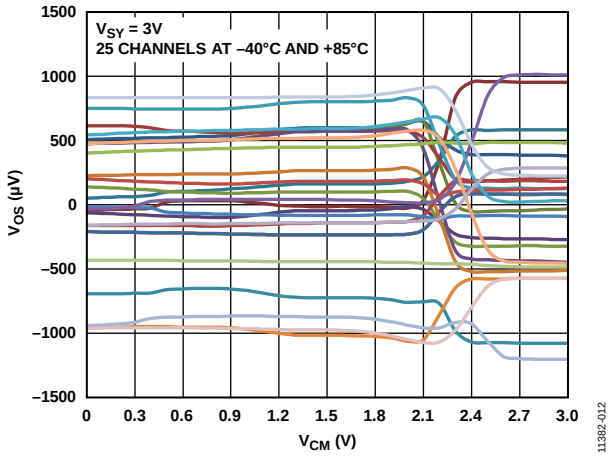


Figure 12. Input Offset Voltage vs. Common-Mode Voltage

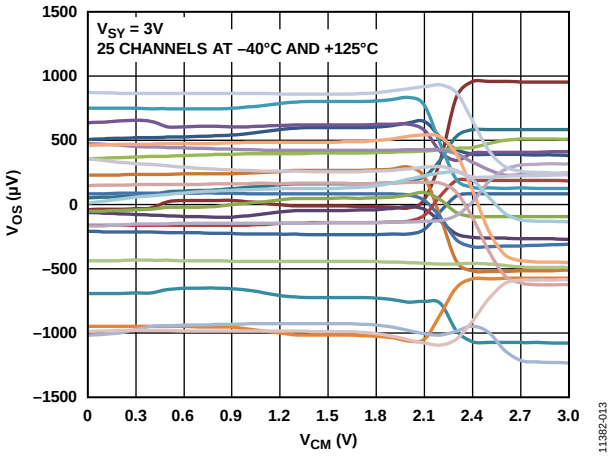


Figure 13. Input Offset Voltage vs. Common-Mode Voltage

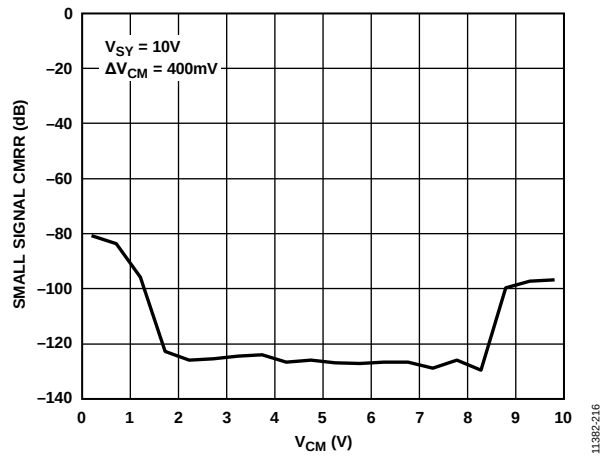


Figure 14. Small Signal CMRR vs. Common-Mode Voltage

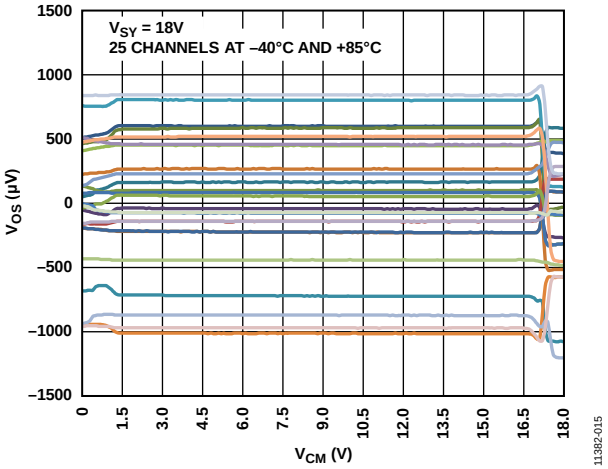


Figure 15. Input Offset Voltage vs. Common-Mode Voltage

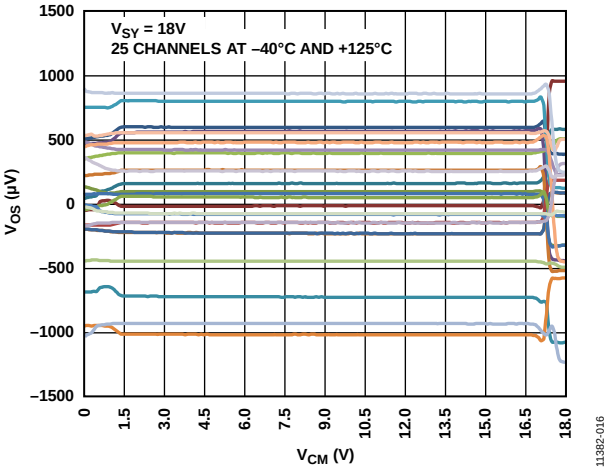


Figure 16. Input Offset Voltage vs. Common-Mode Voltage

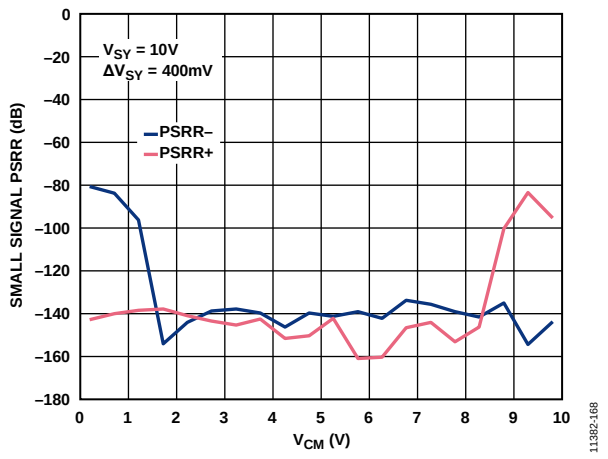


Figure 17. Small Signal PSRR vs. Common-Mode Voltage

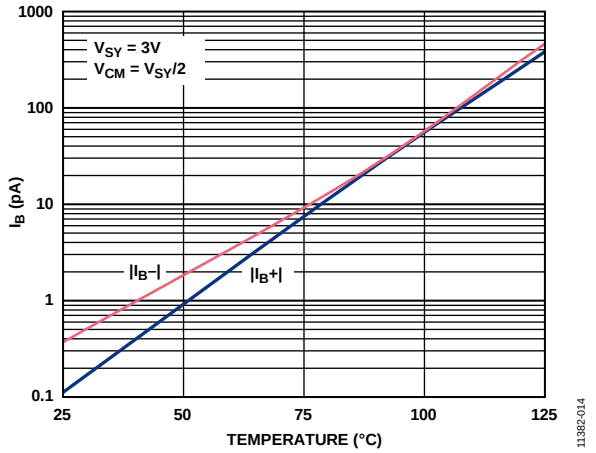


Figure 18. Input Bias Current vs. Temperature

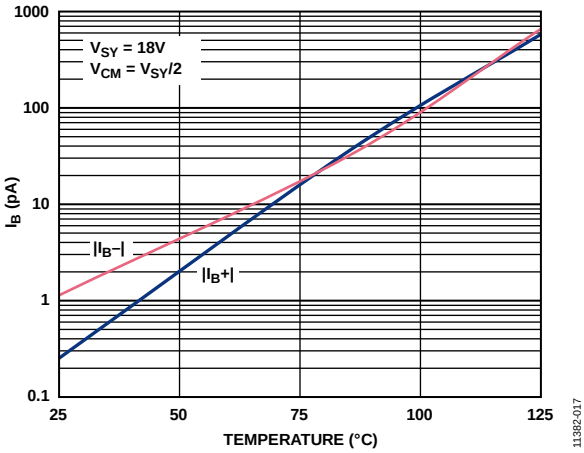


Figure 21. Input Bias Current vs. Temperature

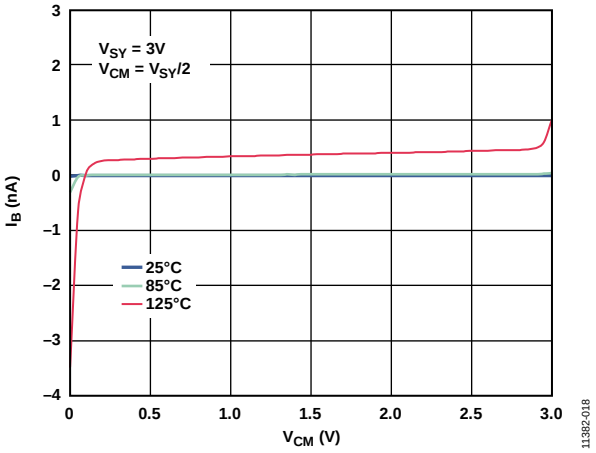


Figure 19. Input Bias Current vs. Common-Mode Voltage

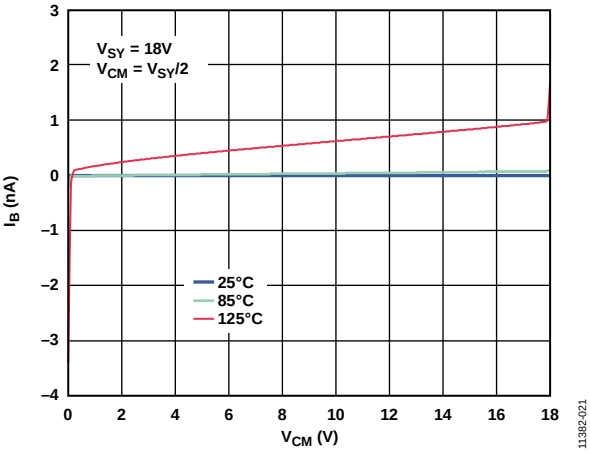


Figure 22. Input Bias Current vs. Common-Mode Voltage

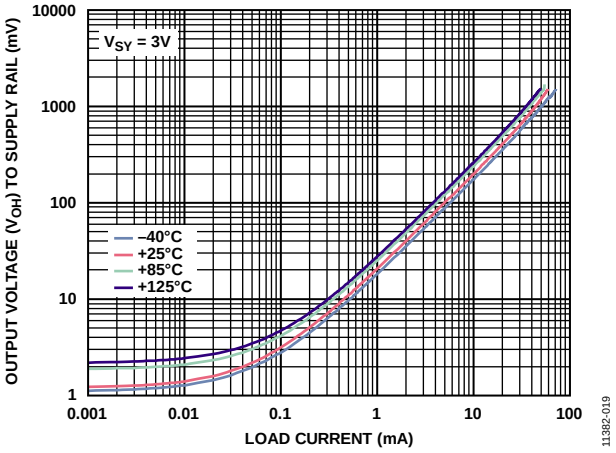


Figure 20. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

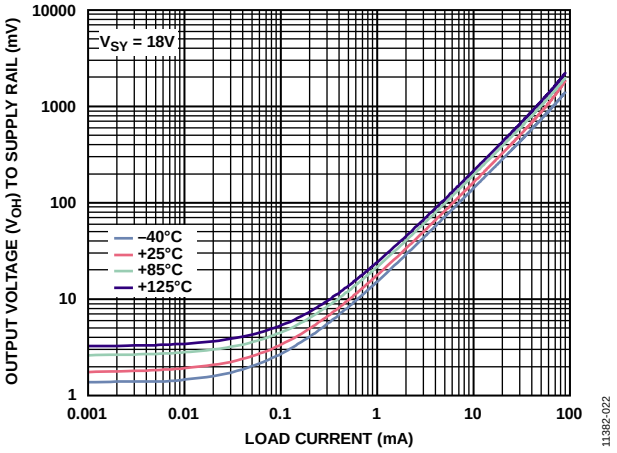


Figure 23. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

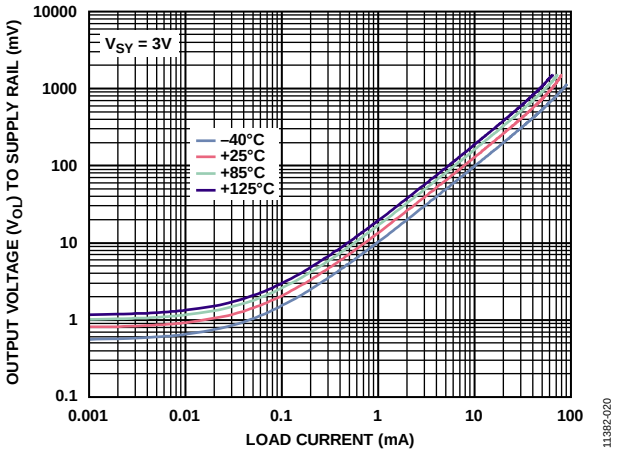


Figure 24. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

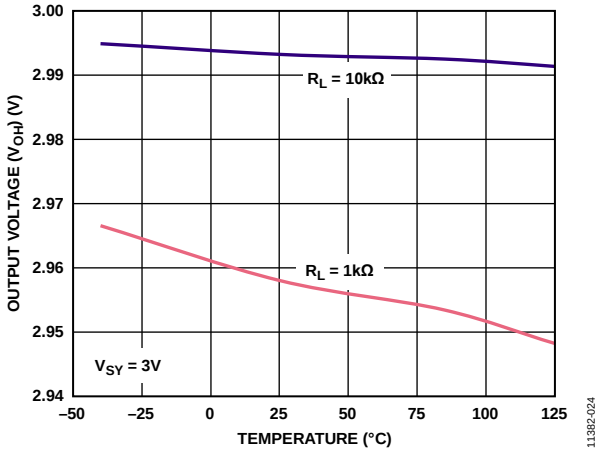


Figure 25. Output Voltage (V_{OH}) vs. Temperature

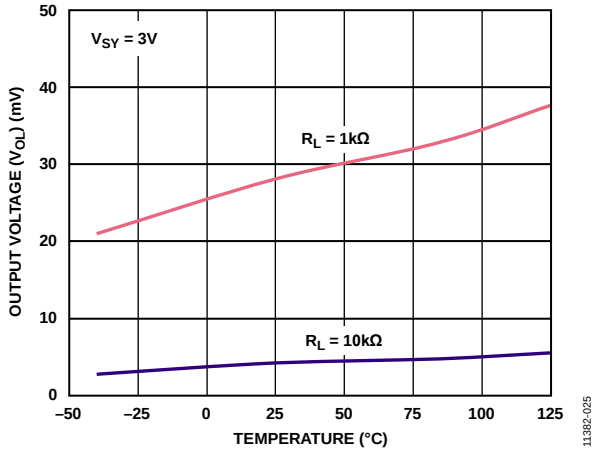


Figure 26. Output Voltage (V_{OL}) vs. Temperature

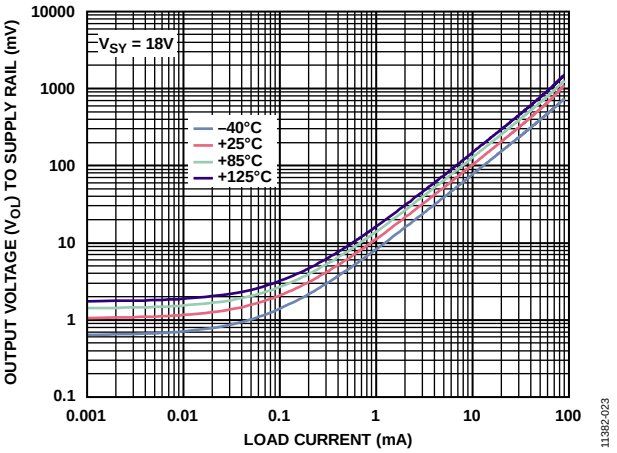


Figure 27. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

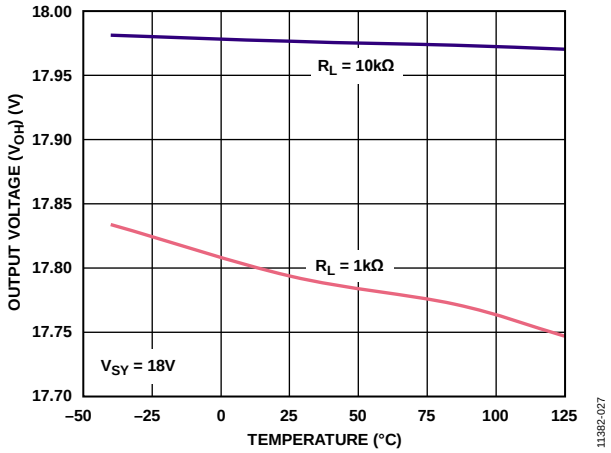


Figure 28. Output Voltage (V_{OH}) vs. Temperature

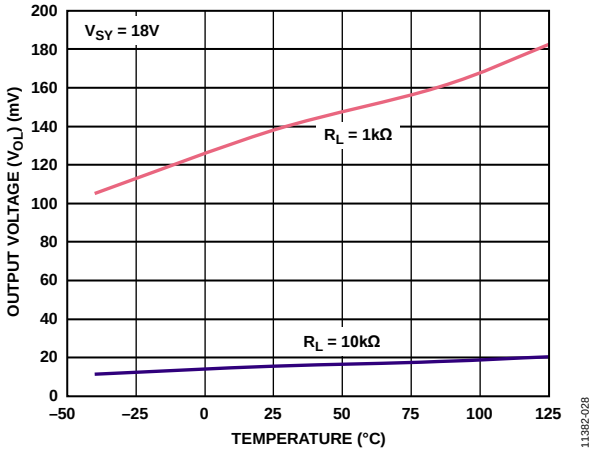


Figure 29. Output Voltage (V_{OL}) vs. Temperature

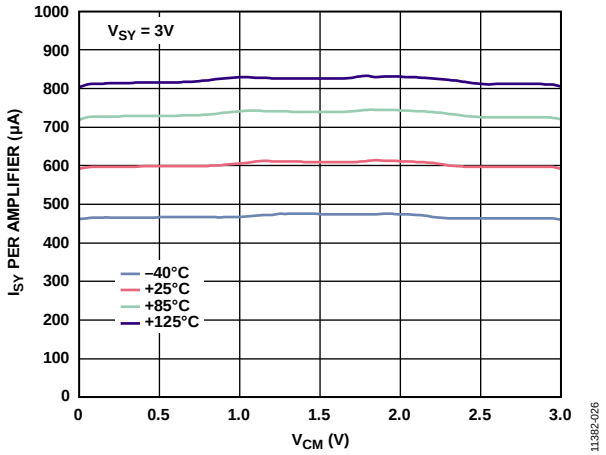


Figure 30. Supply Current vs. Common-Mode Voltage

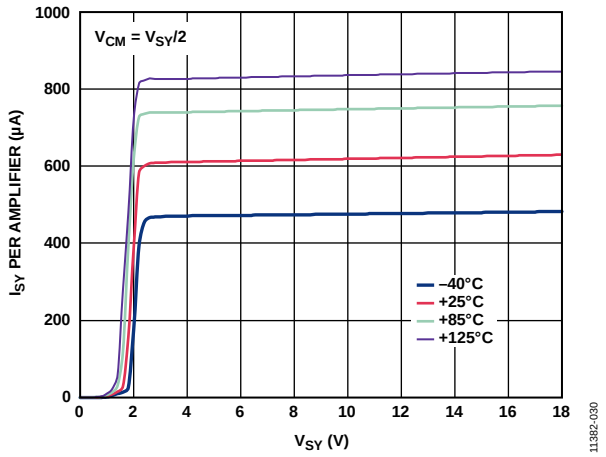


Figure 31. Supply Current vs. Supply Voltage

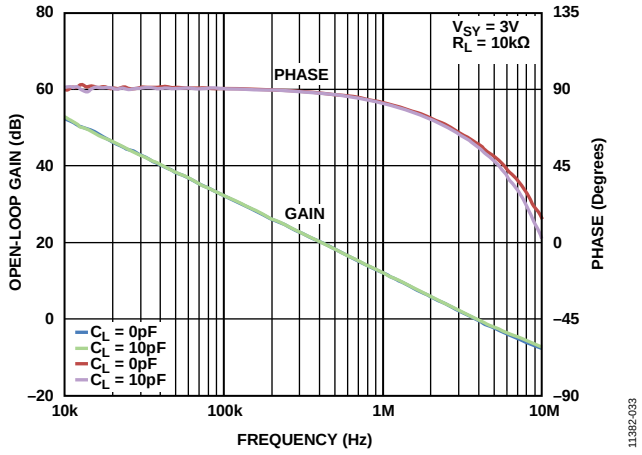


Figure 32. Open-Loop Gain and Phase vs. Frequency

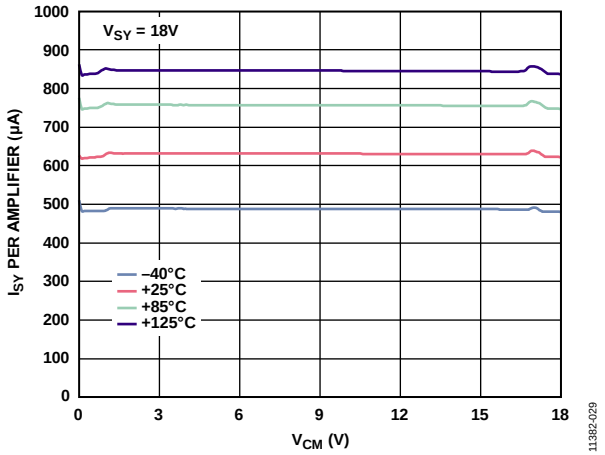


Figure 33. Supply Current vs. Common-Mode Voltage

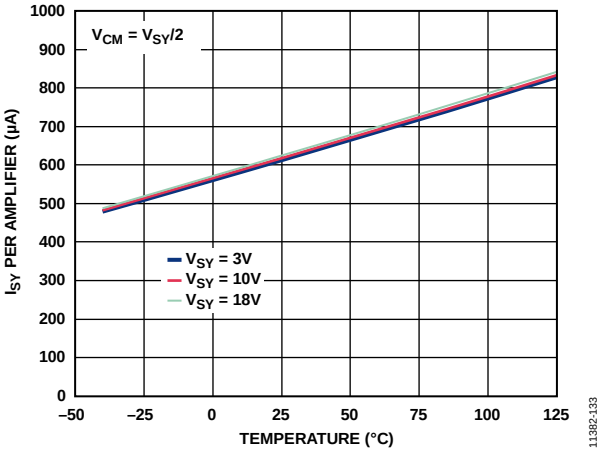


Figure 34. Supply Current vs. Temperature

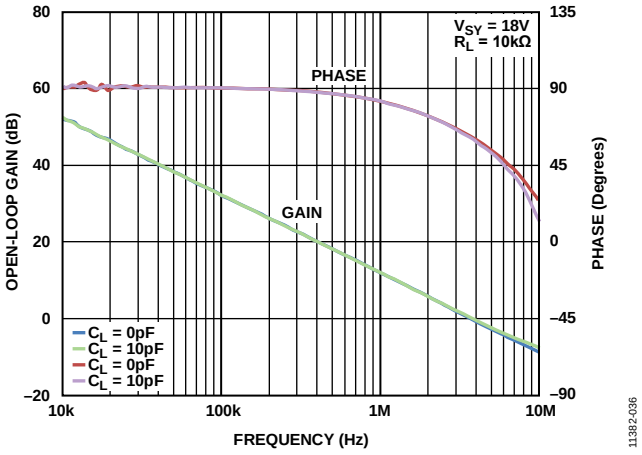


Figure 35. Open-Loop Gain and Phase vs. Frequency

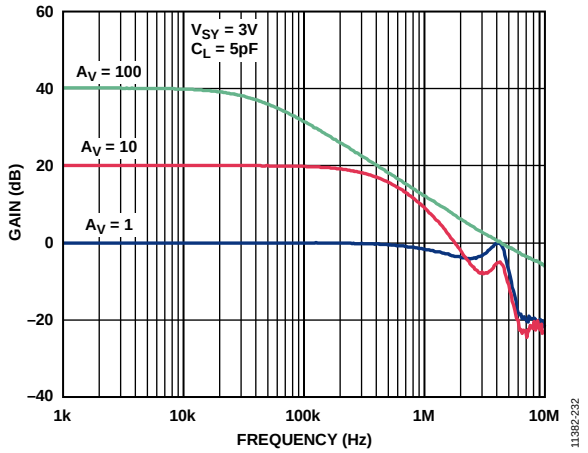


Figure 36. Closed-Loop Gain vs. Frequency

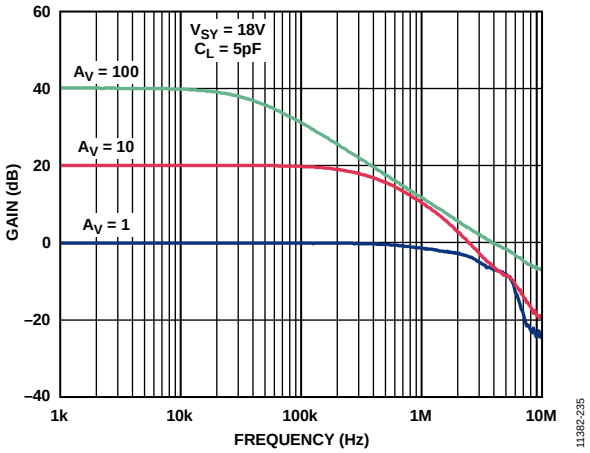


Figure 39. Closed-Loop Gain vs. Frequency

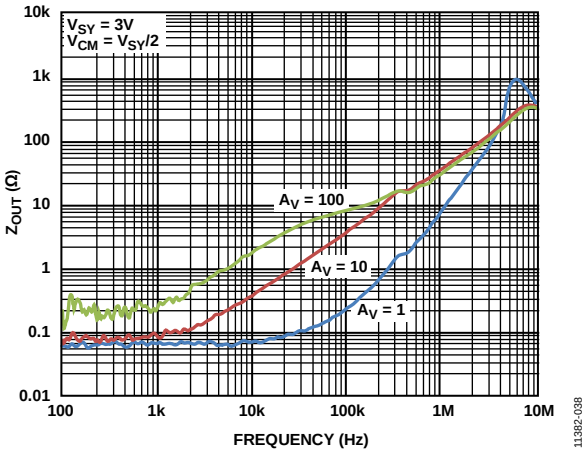


Figure 37. Output Impedance vs. Frequency

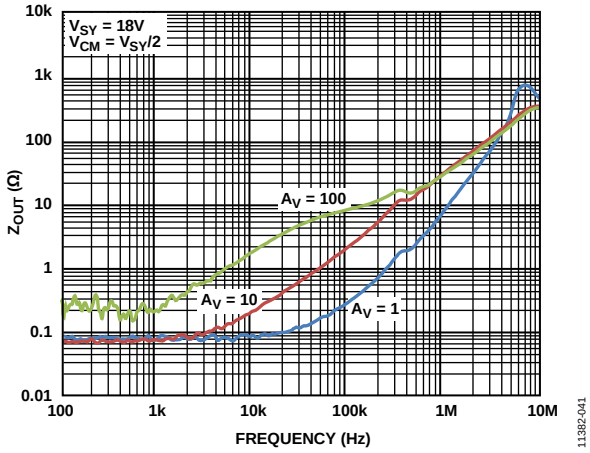


Figure 40. Output Impedance vs. Frequency

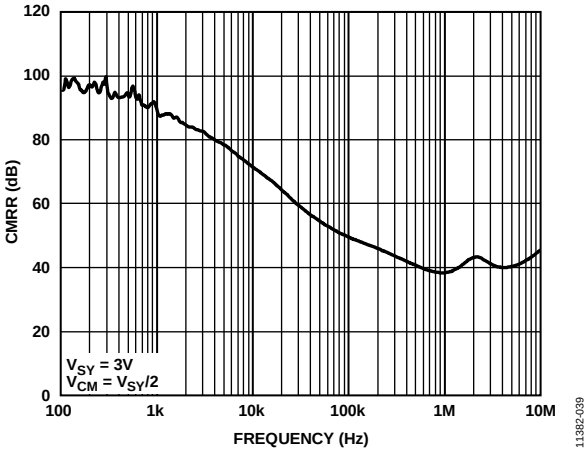


Figure 38. CMRR vs. Frequency

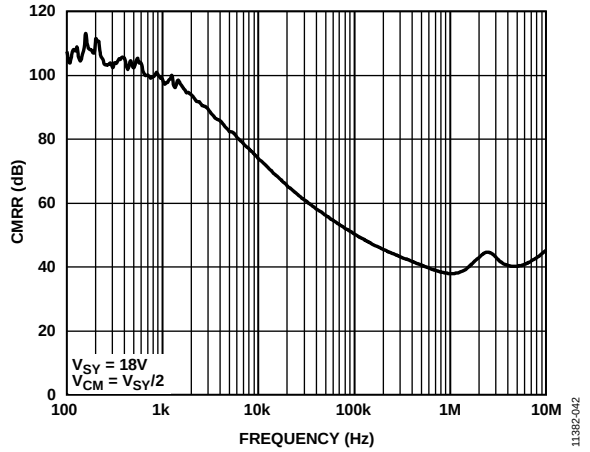


Figure 41. CMRR vs. Frequency

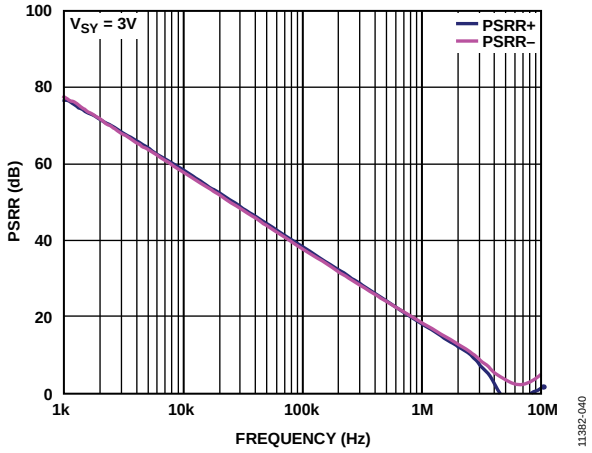


Figure 42. PSRR vs. Frequency

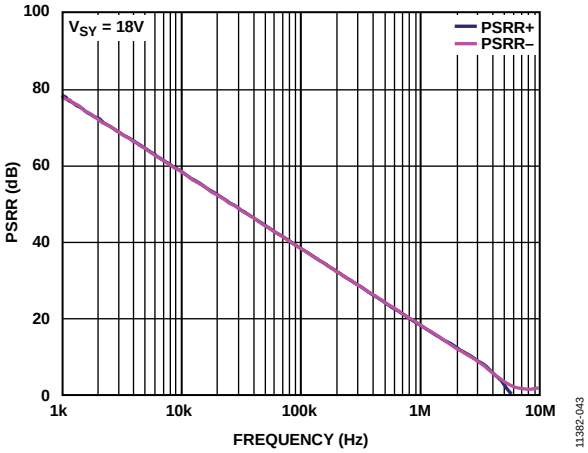


Figure 45. PSRR vs. Frequency

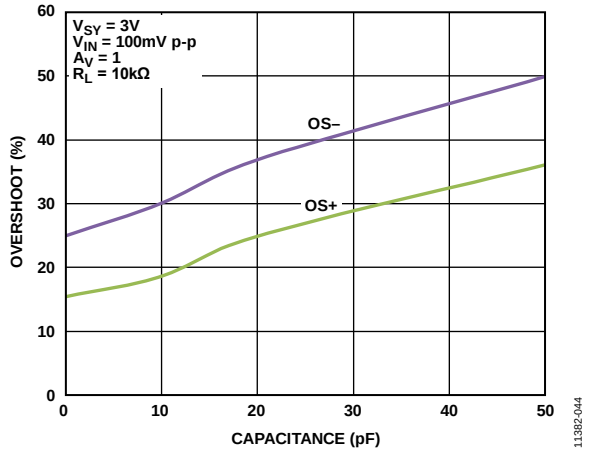


Figure 43. Small Signal Overshoot vs. Load Capacitance

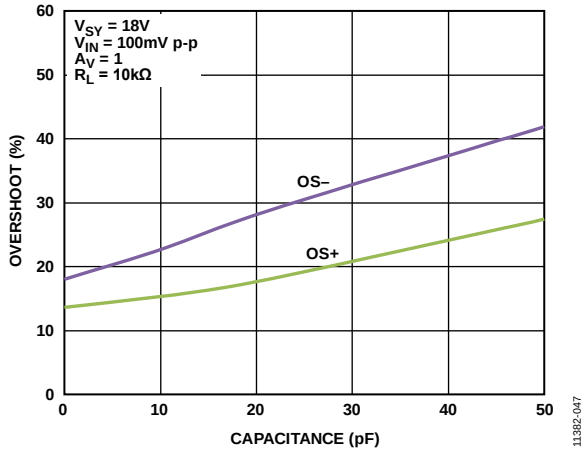


Figure 46. Small Signal Overshoot vs. Load Capacitance

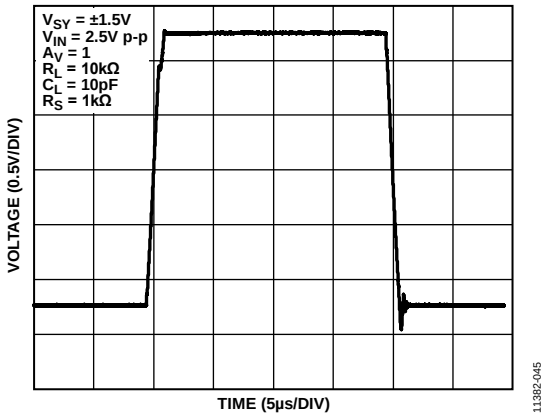


Figure 44. Large Signal Transient Response

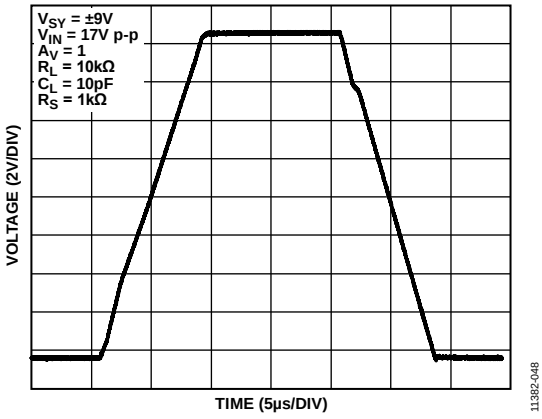


Figure 47. Large Signal Transient Response

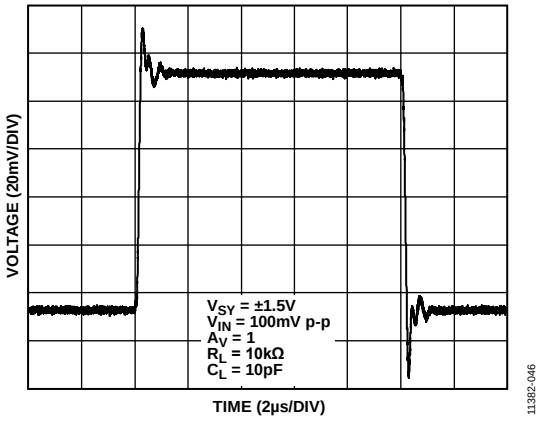


Figure 48. Small Signal Transient Response

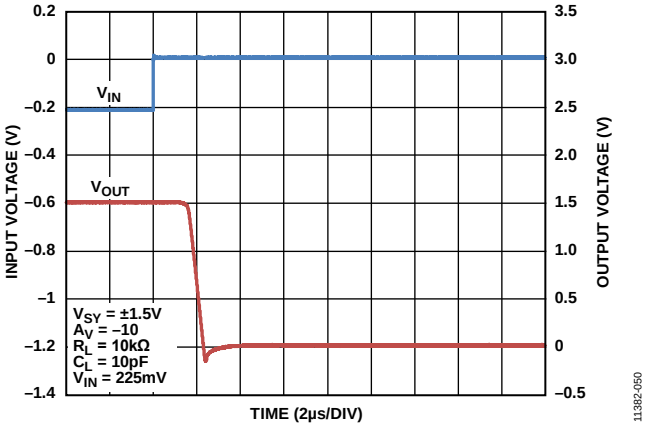


Figure 49. Positive Overload Recovery

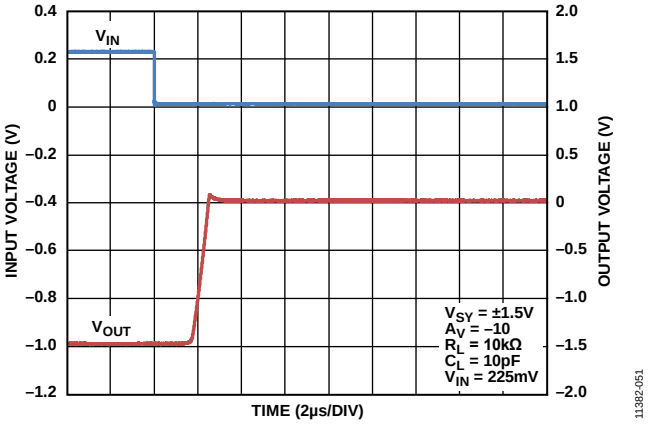


Figure 50. Negative Overload Recovery

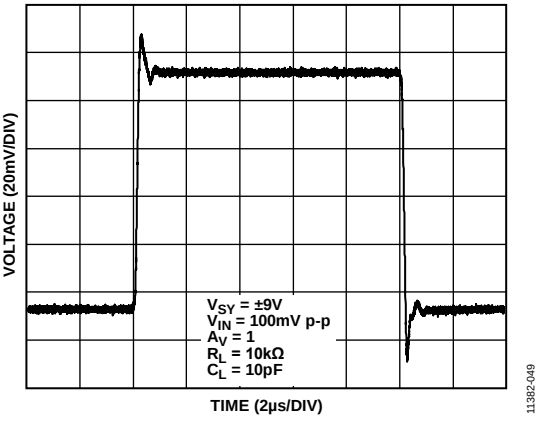


Figure 51. Small Signal Transient Response

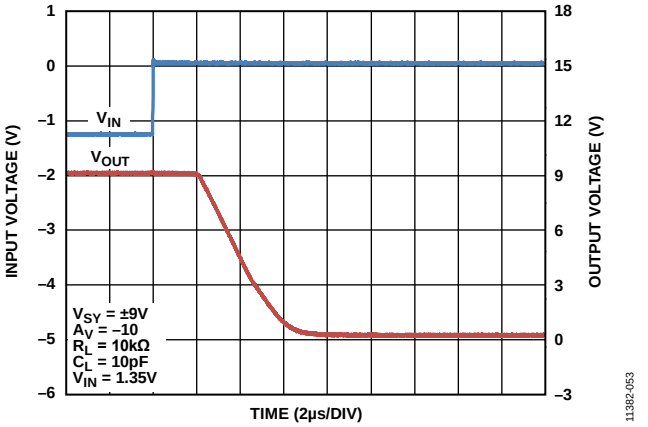


Figure 52. Positive Overload Recovery

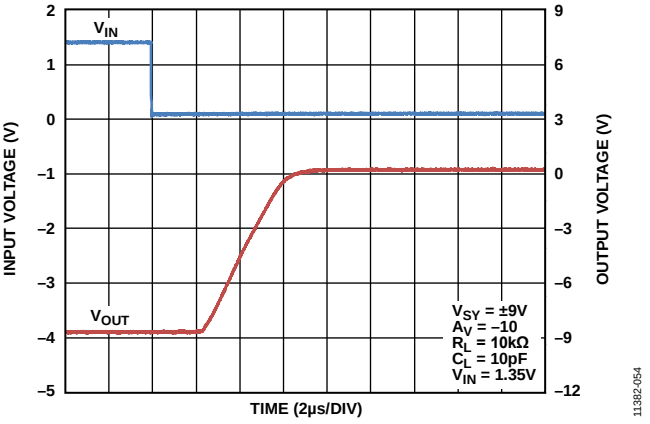


Figure 53. Negative Overload Recovery

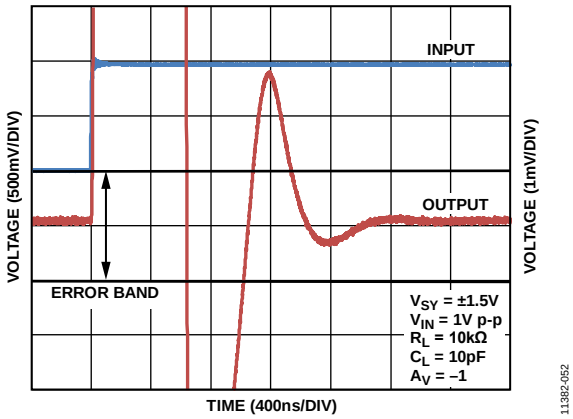


Figure 54. Positive Settling Time to 0.1%

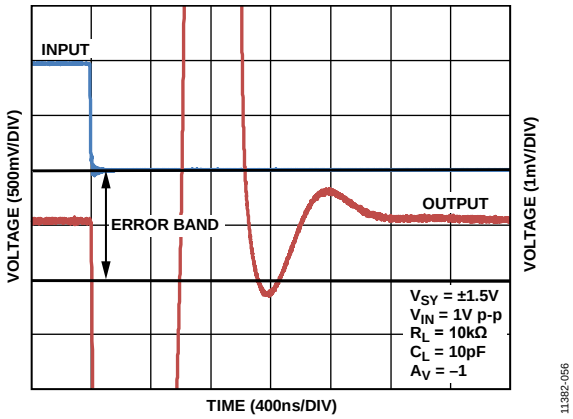


Figure 55. Negative Settling Time to 0.1%

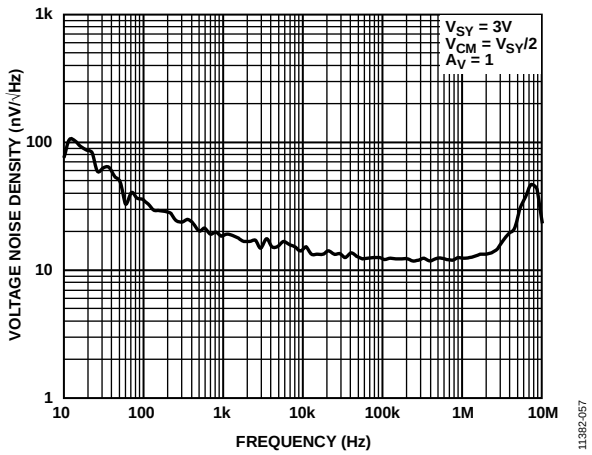


Figure 56. Voltage Noise Density vs. Frequency

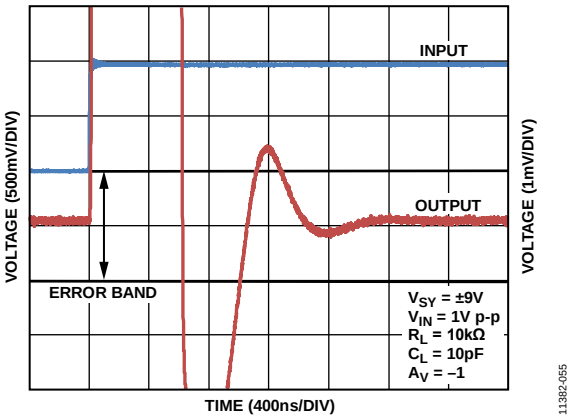


Figure 57. Positive Settling Time to 0.1%

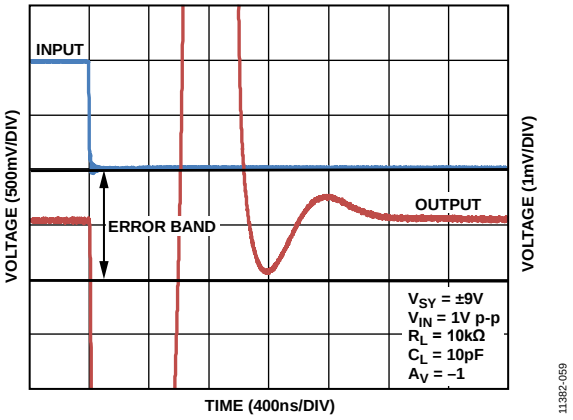


Figure 58. Negative Settling Time to 0.1%

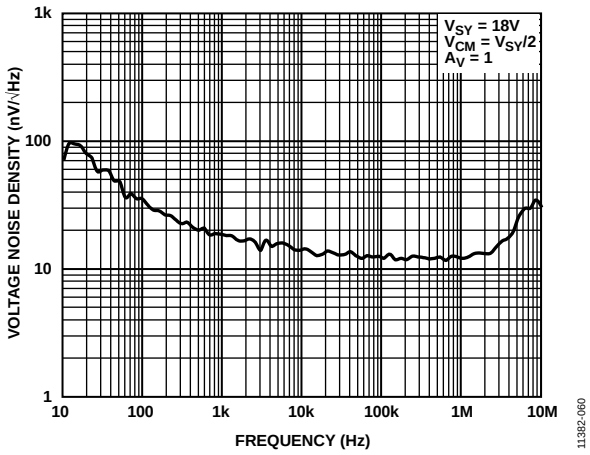


Figure 59. Voltage Noise Density vs. Frequency

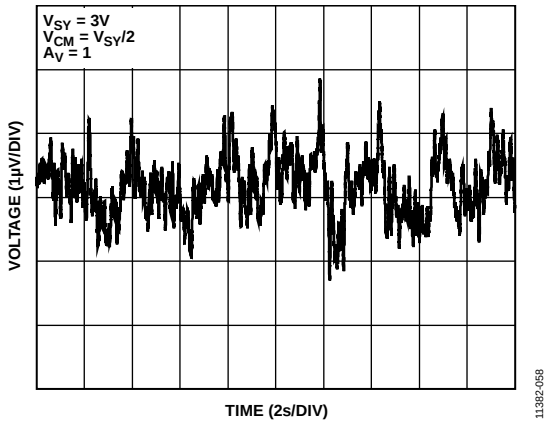


Figure 60. 0.1 Hz to 10 Hz Noise

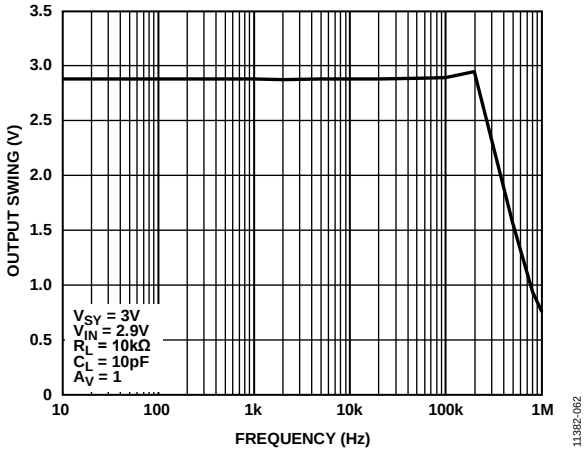


Figure 61. Output Swing vs. Frequency

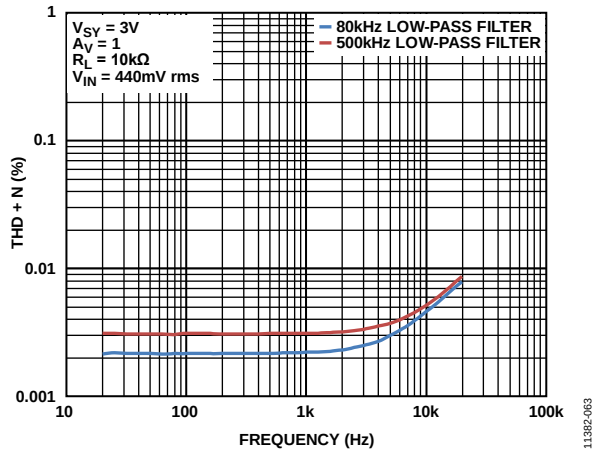


Figure 62. THD + N vs. Frequency

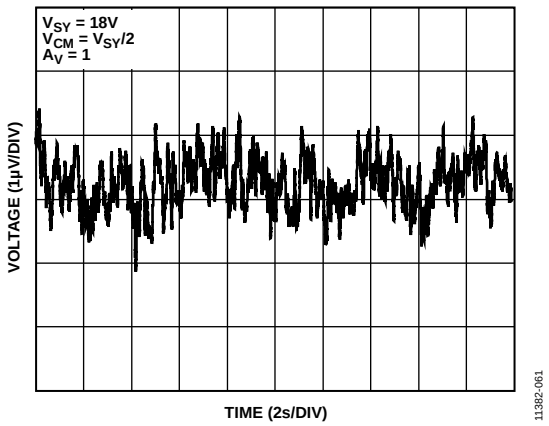


Figure 63. 0.1 Hz to 10 Hz Noise

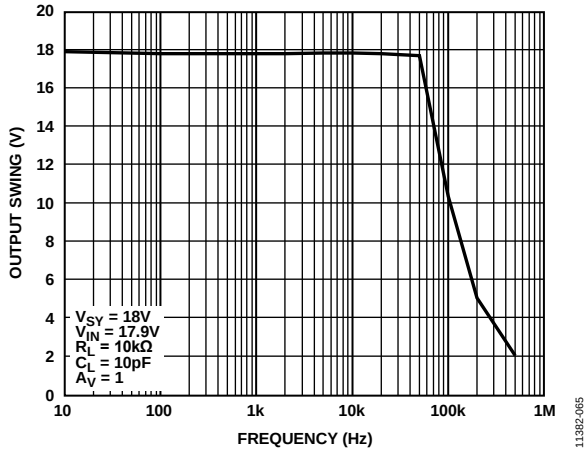


Figure 64. Output Swing vs. Frequency

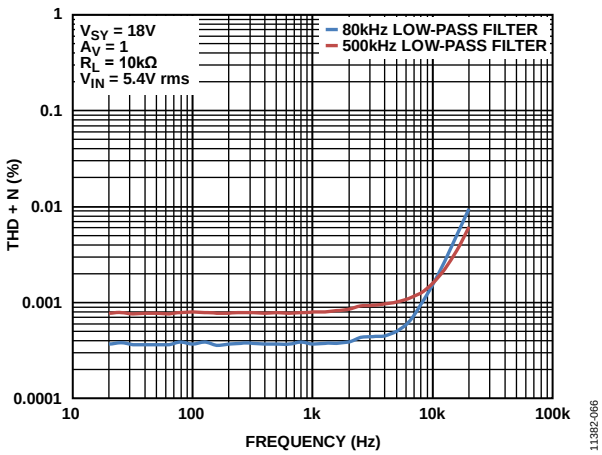


Figure 65. THD + N vs. Frequency

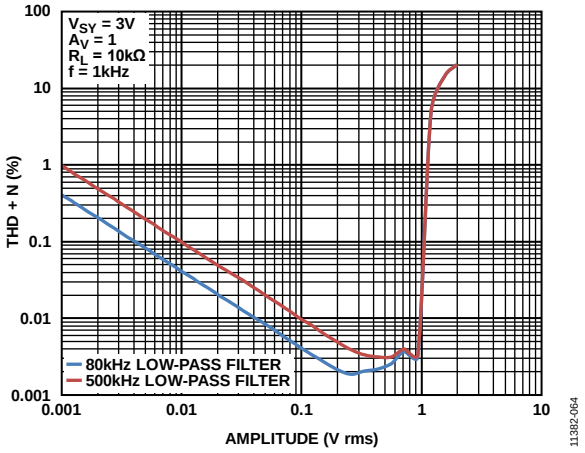


Figure 66. THD + N vs. Amplitude

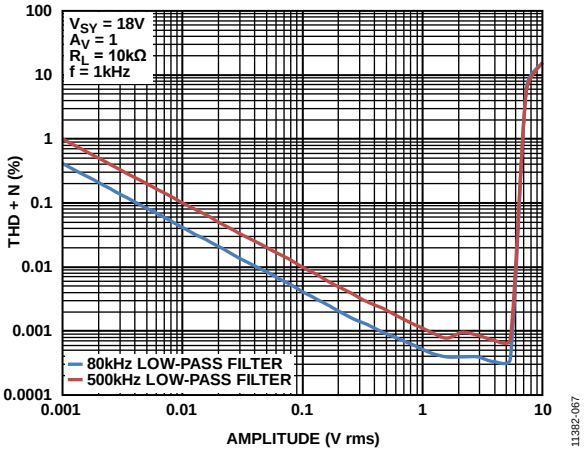


Figure 68. THD + N vs. Amplitude

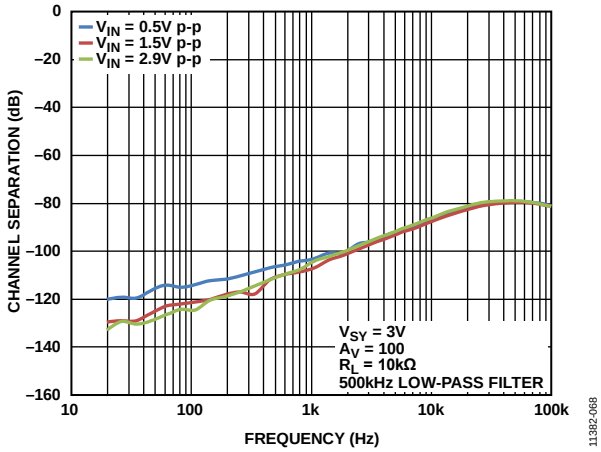


Figure 67. Channel Separation vs. Frequency

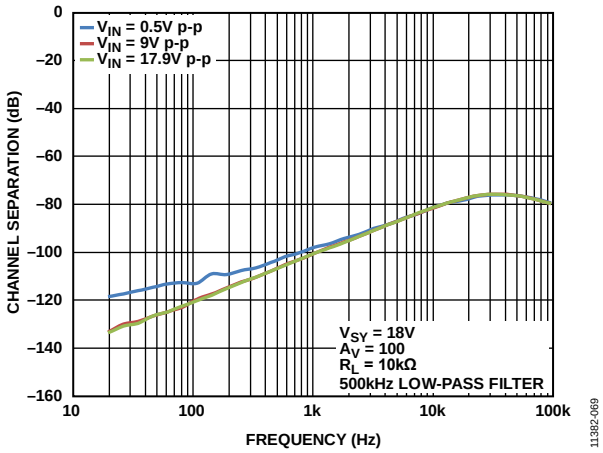


Figure 69. Channel Separation vs. Frequency

APPLICATIONS INFORMATION

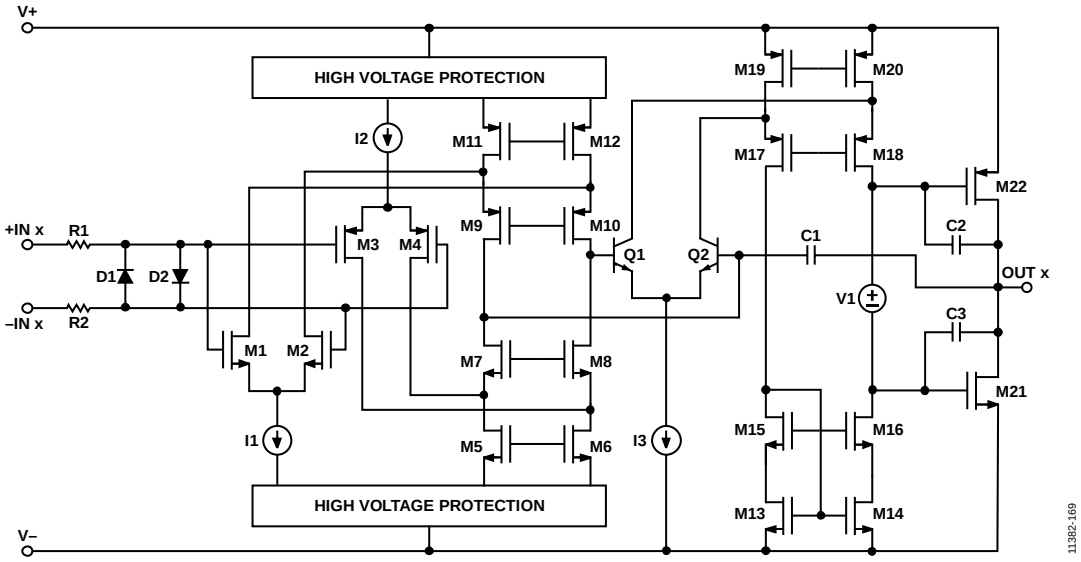


Figure 70. Simplified Schematic

The ADA4666-2 is a low power, rail-to-rail input and output, CMOS amplifier that operates over a wide supply voltage range of 3 V to 18 V. To achieve a rail-to-rail input and output range with very low supply current, the ADA4666-2 uses unique input and output stages.

INPUT STAGE

Figure 70 shows the simplified schematic of the ADA4666-2. The amplifier uses a three-stage architecture with a fully differential input stage to achieve excellent dc performance specifications.

The input stage comprises two differential transistor pairs—a NMOS pair (M1, M2), a PMOS pair (M3, M4)—and folded-cascode transistors (M5 to M12). The input common-mode voltage determines which differential pair is active. The PMOS differential pair is active for most of the input common-mode range. The NMOS pair is required for input voltages up to and including the upper supply rail. This topology allows the amplifier to maintain a wide dynamic input voltage range and maximize signal swing to both supply rails.

The proprietary high voltage protection circuitry in the ADA4666-2 minimizes the common-mode voltage changes seen by the amplifier input stage for most of the input common-mode range. This results in the amplifier having excellent disturbance rejection when operating in this preferred common-mode range. The performance benefits of operating within this preferred range are shown in the PSRR vs. V_{CM} (see Figure 17), CMRR vs. V_{CM} (see Figure 14) and V_{OS} vs. V_{CM} graphs (see Figure 8, Figure 11, Figure 12, Figure 13, Figure 15, and Figure 16). The CMRR performance benefits of the reduced common-mode range are guaranteed at final test and shown in the electrical characteristics (see Table 2 to Table 4).

For most of the input common-mode voltage range, the PMOS differential pair is active. When the input common-mode voltage is within a few volts of the power supplies, the input transistors are exposed to these voltage changes. As the common-mode voltage approaches the positive power supply, the active differential pair changes from the PMOS pair to the NMOS pair. Differential pairs commonly exhibit different offset voltages. The handoff of control from one differential pair to the other creates a step like characteristic that is visible in the V_{OS} vs. V_{CM} graphs (see Figure 8, Figure 11, Figure 12, Figure 13, Figure 15, and Figure 16). This characteristic is inherent in all rail-to-rail input amplifiers that use the dual differential pair topology.

Additional steps in the V_{OS} vs. V_{CM} graphs are visible as the common-mode voltage approaches the negative power supply. These changes are a result of the load transistors (M5, M6) running out of headroom. As the load transistors are forced into the triode region of operation, the mismatch of their drain impedance becomes a significant portion of the amplifier offset. This effect can also be seen in the V_{OS} vs. V_{CM} graphs (see Figure 8, Figure 11, Figure 12, Figure 13, Figure 15, and Figure 16).

Current Source I2 drives the PMOS transistor pair. As the input common-mode voltage approaches the upper power supply, this current is reduced to zero. At the same time, a replica current source, I1, is increased from zero to enable the NMOS transistor pair.

The ADA4666-2 achieves its high performance specifications by using low voltage MOS devices for its differential inputs. These low voltage MOS devices offer excellent noise and bandwidth per unit of current. The input stage is isolated from the high system voltages with proprietary protection circuitry. This regulation circuitry protects the input devices from the high supply voltages at which the amplifier can operate.

The input devices are also protected from large differential input voltages by clamp diodes (D1 and D2). These diodes are buffered from the inputs with two 120 Ω resistors (R1 and R2). The diodes conduct significant current whenever the differential voltage exceeds approximately 600 mV; in this condition, the differential input resistance falls to 240 Ω. It is possible for a significant amount of current to flow through these protection diodes. The user must ensure that current flowing into the input pins is limited to the absolute maximum of 10 mA.

GAIN STAGE

The second stage of the amplifier is composed of an NPN differential pair (Q1,Q2) and folded cascode transistors (M13 to M20). The amplifier features nested Miller compensation (C1 to C3).

OUTPUT STAGE

The ADA4666-2 features a complementary output stage consisting of the M21 and M22 transistors. These transistors are configured in a Class AB topology and are biased by the voltage source, V1. This topology allows the output voltage to go within millivolts of the supply rails, achieving a rail-to-rail output swing. The output voltage is limited by the output impedance of the transistors, which are low R_{ON} MOS devices. The output voltage swing is a function of the load current and can be estimated using the output voltage to the supply rail vs. load current graphs (see Figure 20, Figure 23, Figure 24, and Figure 27). The high voltage and high current capability of the ADA4666-2 output stage requires the user to ensure that it operates within the thermal safe operating area (see the Maximum Power Dissipation section).

MAXIMUM POWER DISSIPATION

The ADA4666-2 is capable of driving an output current up to 220 mA. However, the usable output load current drive is limited to the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the ADA4666-2 is 150°C (see Table 5). The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated by the output stage transistor. It can be calculated as follows:

$$P_D = (V_{SY} \times I_{SY}) + (V_{SY} - V_{OUT}) \times I_{LOAD}$$

where:
V_{SY} is the power supply rail.
I_{SY} is the quiescent current.
V_{OUT} is the output of the amplifier.
I_{LOAD} is the output load.

Do not exceed the maximum junction temperature for the device, 150°C. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device. To ensure proper operation, it is necessary to observe the maximum power derating curves. Figure 71 shows the maximum safe power dissipation in the package vs. the ambient temperature on a standard 4-layer JEDEC board. The exposed pad of the LFCSP package is soldered to the board.

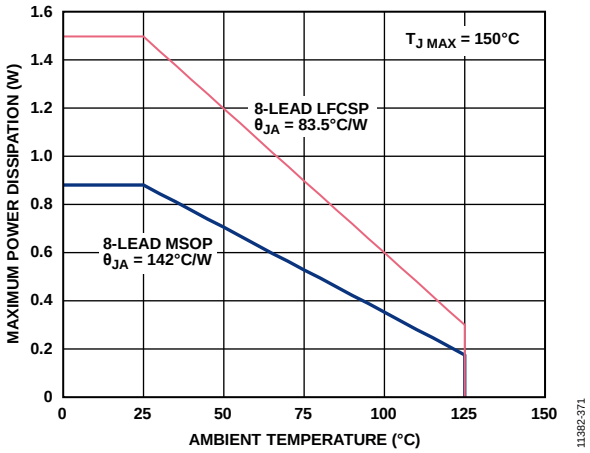


Figure 71. Maximum Power Dissipation vs. Ambient Temperature

Refer to Technical Article MS-2251, *Data Sheet Intricacies—Absolute Maximum Ratings and Thermal Resistances*, for more information.

RAIL-TO-RAIL INPUT AND OUTPUT

The ADA4666-2 features rail-to-rail input and output with a supply voltage from 3 V to 18 V. Figure 72 shows the input and output waveforms of the ADA4666-2 configured as a unity-gain buffer with a supply voltage of ±9 V. With an input voltage of ±9 V, the ADA4666-2 allows the output to swing very close to both rails. Additionally, it does not exhibit phase reversal.

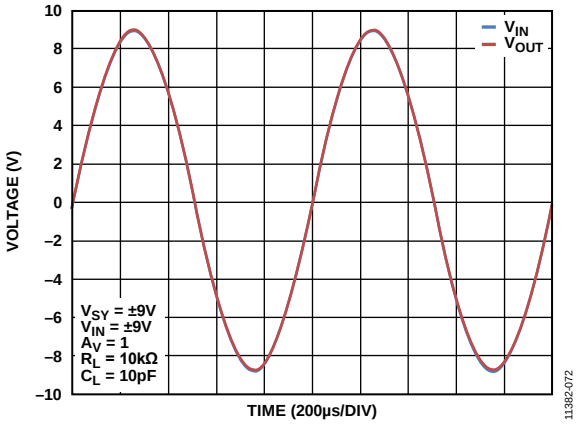


Figure 72. Rail-to-Rail Input and Output

COMPARATOR OPERATION

An op amp is designed to operate in a closed-loop configuration with feedback from its output to its inverting input. Figure 73 shows the ADA4666-2 configured as a voltage follower with an input voltage that is always kept at the midpoint of the power supplies. The same configuration is applied to the unused channel. A1 and A2 indicate the placement of ammeters to measure supply current. I_{SY}+ refers to the current flowing from the upper supply rail to the op amp, and I_{SY}− refers to the current flowing from the op amp to the lower supply rail. As shown in Figure 74, in normal operating conditions, the total current flowing into the op amp is equivalent to the total current flowing out of the op amp, where I_{SY}+ = I_{SY}− = 630 µA per amplifier at V_{SY} = 18 V.

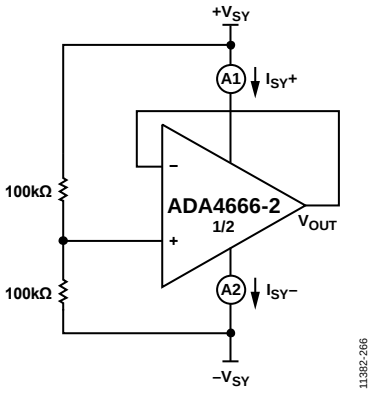


Figure 73. Voltage Follower

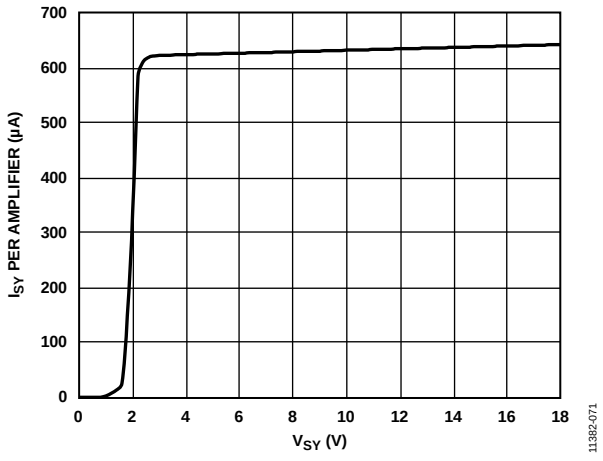


Figure 74. Supply Current vs. Supply Voltage (Voltage Follower)

In contrast to op amps, comparators are designed to work in an open-loop configuration and to drive logic circuits. Although op amps are different from comparators, occasionally an unused section of a dual op amp is used as a comparator to save board space and cost; however, this is not recommended for the ADA4666-2.

Figure 75 and Figure 76 show the ADA4666-2 configured as a comparator, with 100 kΩ resistors in series with the input pins. Any unused channels are configured as buffers with the input voltage kept at the midpoint of the power supplies.

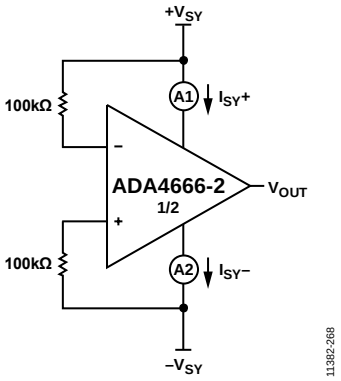


Figure 75. Comparator A

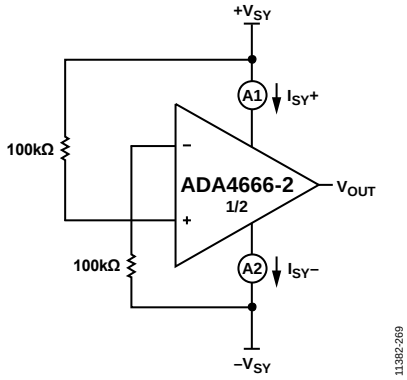


Figure 76. Comparator B

Figure 77 shows the supply currents for both comparator configurations. In comparator mode, the ADA4666-2 does not power up completely. For more information about configuring using op amps as comparators, see the AN-849 Application Note, *Using Op Amps as Comparators*.

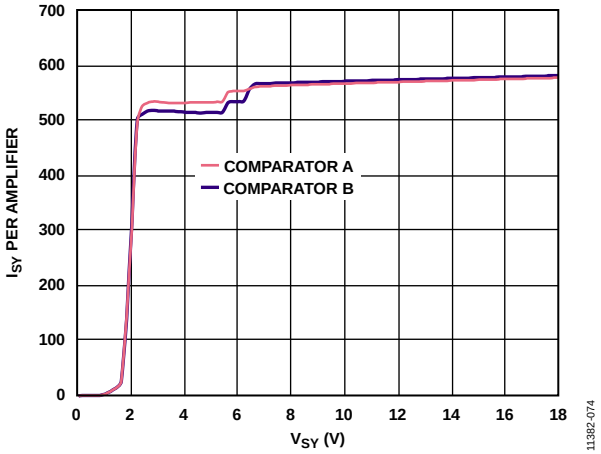


Figure 77. Supply Current vs. Supply Voltage (ADA4666-2 as a Comparator)

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency electromagnetic interference (EMI). When the signal strength is low and transmission lines are long, an op amp must accurately amplify the input signals. However, all op amp pins—the noninverting input, inverting input, positive supply, negative supply, and output pins—are susceptible to EMI signals. These high frequency signals are coupled into an op amp by various means, such as conduction, near field radiation, or far field radiation. For instance, wires and PCB traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op amps can rectify these out-of-band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

To describe the ability of the ADA4666-2 to perform as intended in the presence of electromagnetic energy, the electromagnetic interference rejection ratio (EMIRR) of the noninverting pin is specified in Table 2, Table 3, and Table 4 of the Specifications section. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN_PEAK}/\Delta V_{OS})$$

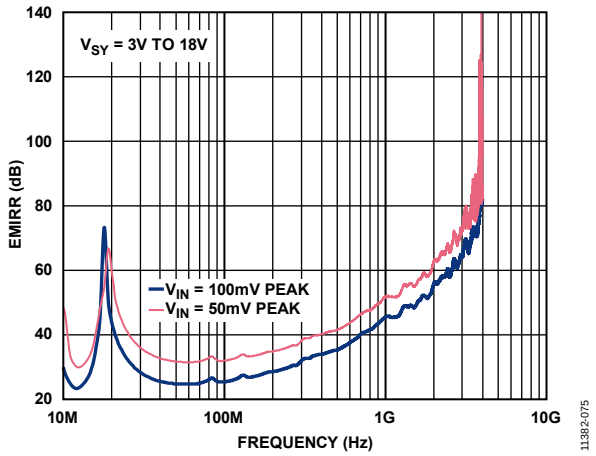


Figure 78. EMIRR vs. Frequency

CURRENT SHUNT MONITOR

Many applications require the sensing of signals near the positive or negative rail. Current shunt monitors are one such application and are mostly used for feedback control systems. They are also used in a variety of other applications, including power metering, battery fuel gauging, and feedback controls in electrical power steering. In such applications, it is desirable to use a shunt with very low resistance to minimize the series voltage drop. This not only minimizes wasted power but also allows the measurement of high currents while saving power. The low input bias current, low offset voltage, and rail-to-rail feature of the ADA4666-2 makes the amplifier an excellent choice for precision current monitoring.

Figure 79 shows a low-side current sensing circuit, and Figure 80 shows a high-side current sensing circuit. Current flowing through the shunt resistor creates a voltage drop. The ADA4666-2, configured as a difference amplifier, amplifies the voltage drop by a factor of R2/R1. Note that for true difference amplification, matching of the resistor ratio is very important, where R2/R1 = R4/R3. The rail-to-rail output feature of the ADA4666-2 allows the output of the op amp to almost reach its positive supply. This allows the current shunt monitor to sense up to approximately $V_{SY}/(R2/R1 \times R_S)$ amperes of current. For example, with V_{SY} = 18 V, R2/R1 = 100, and R_S = 100 mΩ, this current is approximately 1.8 A.

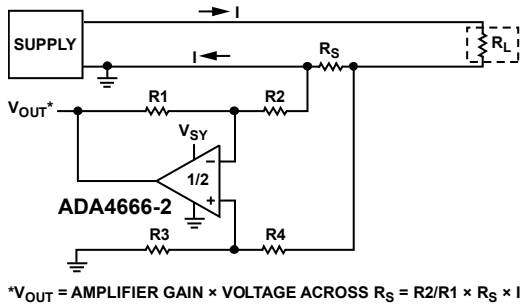


Figure 79. Low-Side Current Sensing Circuit

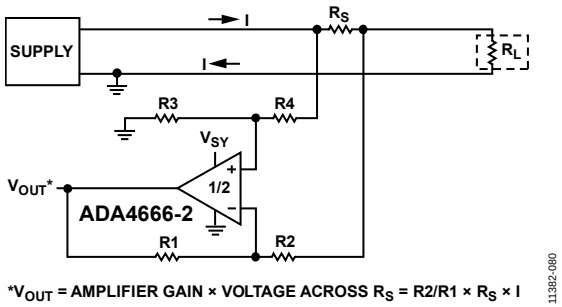


Figure 80. High-Side Current Sensing Circuit

ACTIVE FILTERS

Active filters are used to separate signals, passing those of interest and attenuating signals at unwanted frequencies. For example, low-pass filters are often used as antialiasing filters in data acquisition systems or as noise filters to limit high frequency noise.

The high input impedance, high bandwidth, low input bias current, and dc precision of the ADA4666-2 make it a good fit for active filters application. Figure 81 shows the ADA4666-2 in a four-pole Sallen-Key Butterworth low-pass filter configuration. The four-pole low-pass filter has two complex conjugate pole pairs and is implemented by cascading two two-pole low-pass filters. Section A and Section B are configured as two-pole low-pass filters in unity gain. Table 8 shows the Q requirement and pole position associated with each stage of the Butterworth filter. Refer to Chapter 8, "Analog Filters," in *Linear Circuit Design Handbook*, available at www.analog.com/AnalogDialogue, for pole locations on the S plane and Q requirements for filters of a different order.

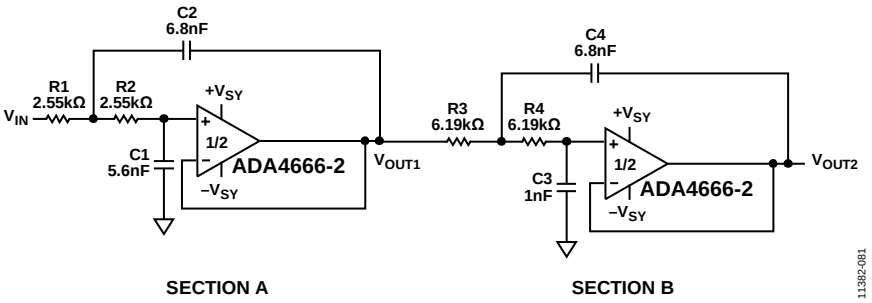


Figure 81. Four-Pole Low-Pass Filter

Table 8. Q Requirements and Pole Positions

Section	Poles	Q
A	−0.9239 ± j0.3827	0.5412
B	−0.3827 ± j0.9239	1.3065

The Sallen-Key topology is widely used due to its simple design with few circuit elements. This topology provides the user the flexibility of implementing either a low-pass or a high-pass filter by simply interchanging the resistors and capacitors. The ADA4666-2 is configured in unity gain with a corner frequency at 10 kHz. An active filter requires an op amp with a unity-gain bandwidth that is at least 100 times greater than the product of the corner frequency, f_C, and the quality factor, Q. The resistors and capacitors are also important in determining the performance over manufacturing tolerances, time, and temperature. At least 1% or better tolerance resistors and 5% or better tolerance capacitors are recommended.

Figure 82 shows the frequency response of the low-pass Sallen-Key filter, where:

$V_{OUT}1$ is the output of the first stage.

$V_{OUT}2$ is the output of the second stage.

$V_{OUT}1$ shows a 40 dB/decade roll-off and $V_{OUT}2$ shows an 80 dB/decade roll-off. The transition band becomes sharper as the order of the filter increases.

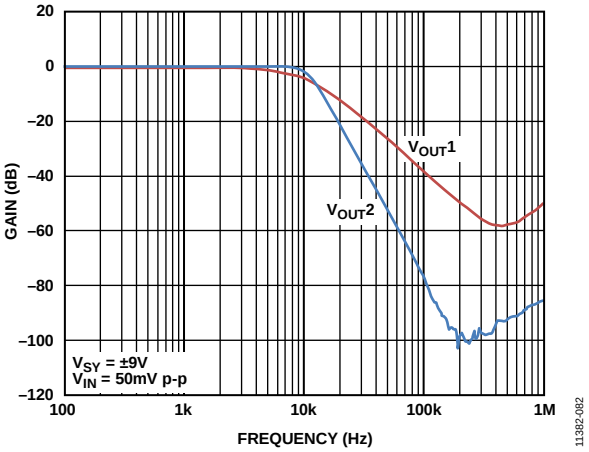


Figure 82. Low-Pass Filter: Gain vs. Frequency

CAPACITIVE LOAD DRIVE

The ADA4666-2 can safely drive capacitive loads of up to 50 pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. Heavy capacitive load reduces phase margin and causes the amplifier frequency response to peak. Peaking corresponds to overshooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the ADA4666-2 must drive a load exceeding 50 pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 83. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. However, with this compensation scheme, the output impedance as seen by the load increases, and this reduces gain accuracy.

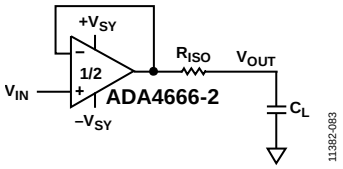


Figure 83. Stability Compensation with Isolating Resistor, R_{ISO}

Figure 84 shows the effect of the compensation scheme on the frequency response of the amplifier in unity-gain configuration driving 250 pF of load.

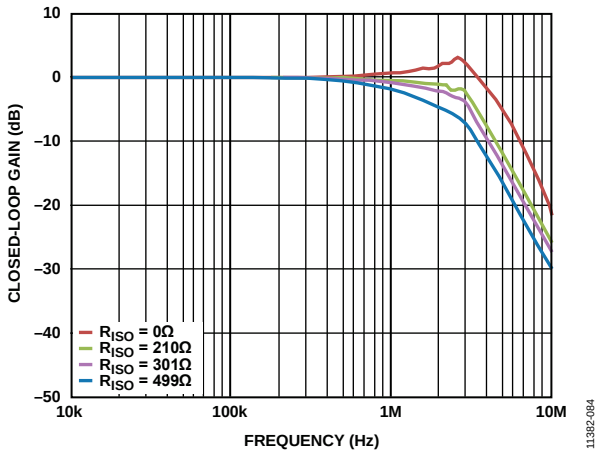


Figure 84. Frequency Response of Compensation Scheme

Figure 85 shows the output response of the unity-gain amplifier driving 250 pF of capacitive load. With no compensation, the amplifier is unstable. Figure 86 to Figure 88 show the amplifier output response with 210 Ω, 301 Ω, and 750 Ω of R_{ISO} compensation. Note that with lower R_{ISO} values, ringing is still noticeable, whereas with higher R_{ISO} values, higher frequency signals are filtered out.

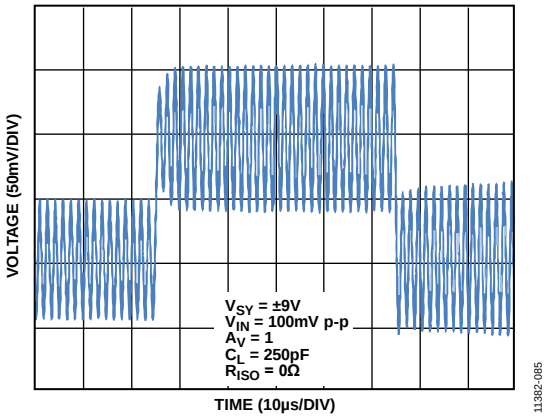


Figure 85. Output Response with No Compensation (R_{ISO} = 0 Ω)

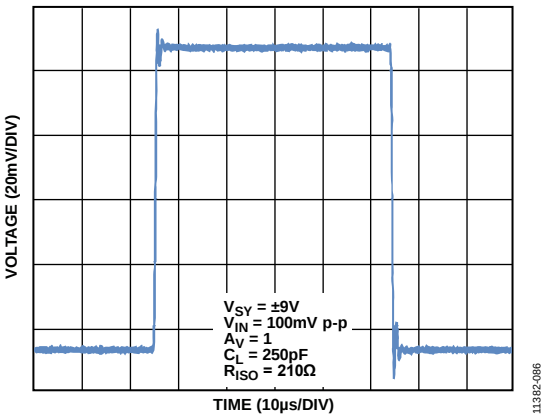


Figure 86. Output Response (R_{ISO} = 210 Ω)

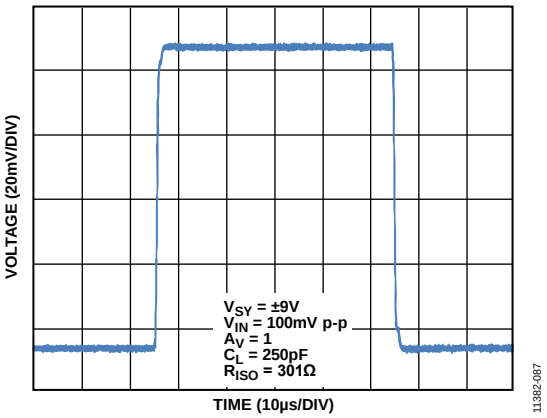


Figure 87. Output Response (R_{ISO} = 301 Ω)

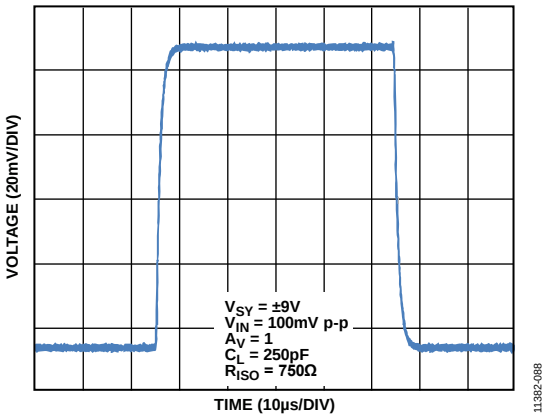


Figure 88. Output Response (R_{ISO} = 750 Ω)

NOISE CONSIDERATIONS WITH HIGH IMPEDANCE SOURCES

Current noise from input terminals can become a dominant contributor to the total circuit noise when an amplifier is driven with a high impedance source. Unlike bipolar amplifiers, CMOS amplifiers like the ADA4666-2 do not have an intrinsic shot noise source at the input terminals. The small amount of shot noise present is produced by the reverse saturation current in the ESD protection diodes. This current noise is typically on the order of 1 fA/√Hz to 10 fA/√Hz. Therefore, to measure current noise in this range, a large source impedance of greater than 10 GΩ is required.

For the ADA4666-2, the more relevant discussion centers around an effect referred to as blowback noise. The blowback effect comes from noise in the tail current source of the amplifier, which is capacitively coupled to the amplifier inputs through the gate-to-source capacitance (C_{GS}) of the input transistors. This blowback noise is multiplied by the source impedance and appears as voltage noise at the input terminal. A 10× increase in the source impedance results in a 10× increase in the voltage noise due to blowback.

The blowback noise spectrum has a high-pass response at low frequencies due to C_{GS} coupling. At high frequencies, the spectrum tends to roll off with two poles: an internal pole due to parasitic capacitances of the tail current source and an external pole due to parasitic capacitances on the PCB.

Figure 89 shows the voltage noise density of the ADA4666-2 with source impedances of 1 MΩ and 10 MΩ. At low frequencies (<1 Hz to 10 Hz), the amplifier 1/f voltage noise dominates the spectrum. At moderate frequencies, the spectrum flattens due to the thermal noise of the source resistors. As the frequency increases, blowback noise dominates and causes the voltage noise spectrum to increase. The noise spectrum continues to increase until it reaches either the internal or external pole frequency. After these poles, the spectrum starts to decrease.

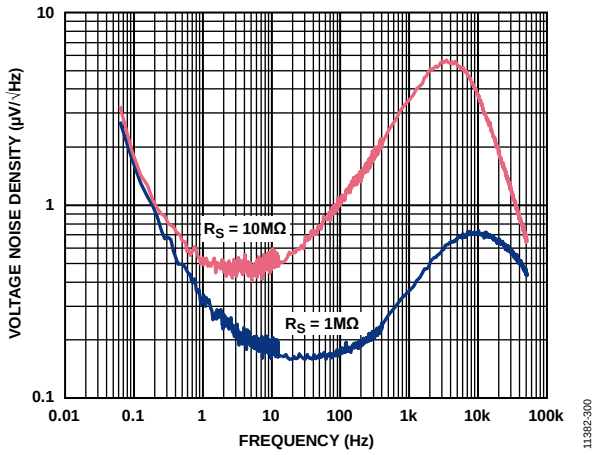


Figure 89. Voltage Noise Density vs. Frequency (with Input Series Resistor, R_S)

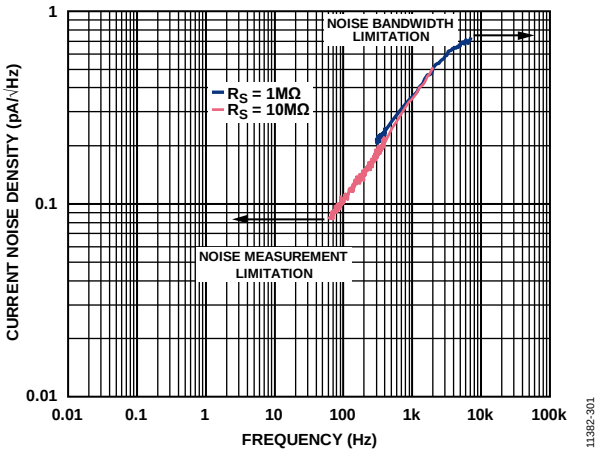


Figure 90. Current Noise Density vs. Frequency

Figure 90 shows the current noise density of the ADA4666-2 with source impedances of 1 MΩ and 10 MΩ. This current noise is extracted only from the voltage noise density curves in the frequency band where blowback noise is the dominant contributor. At low frequencies, the noise measurement is dominated by resistor thermal noise and amplifier 1/f noise. At high frequencies, parasitic capacitances dominate the source impedance. The uncertainty of this scale factor prevents an accurate current noise measurement for the entire frequency range.

Blowback noise is present in all amplifiers. The magnitude of the effect depends on the size of the input transistors and the construction of the biasing circuitry. CMOS amplifiers typically have more blowback noise than JFET amplifiers due to noisier MOS transistor biasing. On the other hand, bipolar amplifiers typically do not exhibit blowback noise because the large base current shot noise masks any blowback noise present.

OUTLINE DIMENSIONS

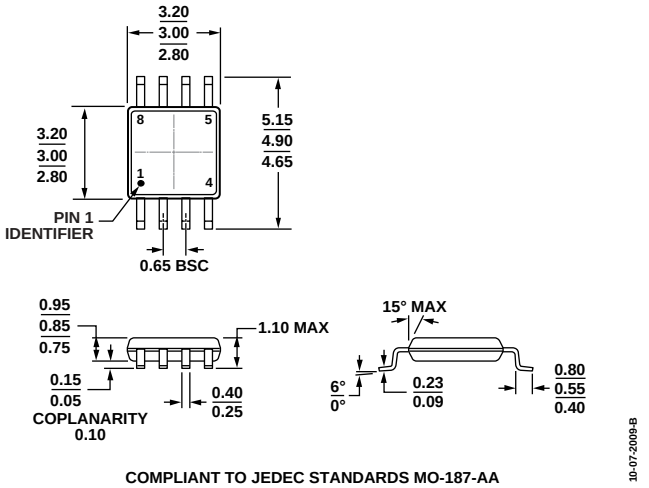


Figure 91. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

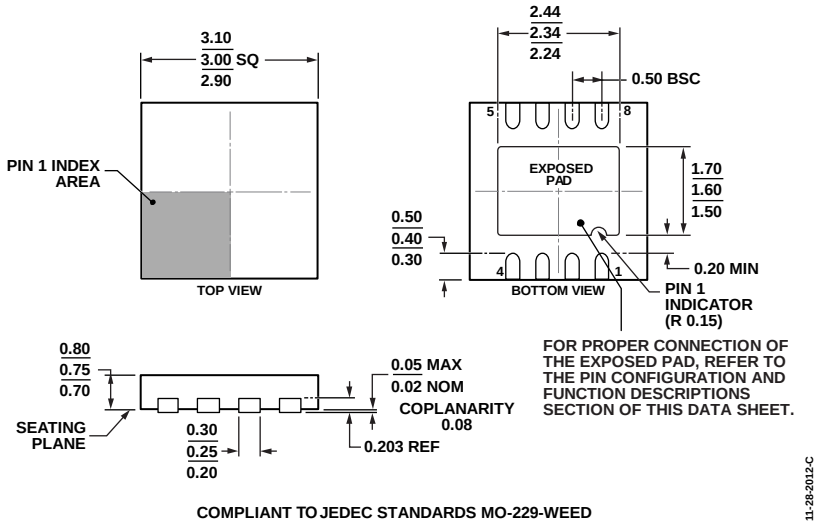


Figure 92. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4666-2ACPZ-R7	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-11	A34
ADA4666-2ACPZ-RL	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-11	A34
ADA4666-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	A34
ADA4666-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP	RM-8	A34
ADA4666-2ARMZ-R7	−40°C to +125°C	8-Lead MSOP	RM-8	A34

[1] Z = RoHS Compliant Part.

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