Integrated Triple Video Filter for High Definition Video

ADA4417-3

FEATURES

- **Optimized for high definition video**
  - **Sixth-order Butterworth filters**
  - **−1 dB bandwidth of 38 MHz**
  - **44 dB rejection at 75 MHz**
  - **5 ns group delay variation**
- **Fixed throughput gain of ×2**
- **0.06% differential gain**
- **0.21° differential phase**
- **Pin selectable output offset (DCO)**
- **Single-supply operation**
  - **3.3 V to 5 V range**
  - **Rail-to-rail output**
- **Output ESD protection exceeds 8 kV**
- **Small packaging: 10-lead MSOP**

APPLICATIONS

- **Set-top boxes**
- **HDTVs**
- **Projectors**
- **DVD players/recorders**
- **Personal video recorders**

FUNCTIONAL BLOCK DIAGRAM

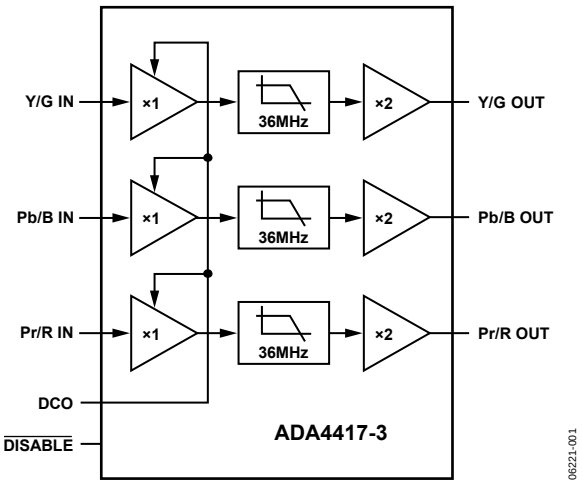


Figure 1.

GENERAL DESCRIPTION

The ADA4417-3 is a low cost, fully integrated, video reconstruction filter specifically designed for consumer high definition video. With 1 dB frequency flatness out to 38 MHz, and 44 dB of rejection at 75 MHz, the ADA4417-3 can handle the most demanding HD video applications.

The ADA4417-3 operates on a single 3.3 V to 5 V supply. It is well-suited for applications where power consumption is critical. A disable feature allows for further power conservation by reducing the supply current to 10 µA (typical) when the device is not in use. With rail-to-rail output, it can be efficiently used on a 3.3 V supply, while providing the user with a 2 V p-p output. The buffers can drive two 75 Ω terminated loads, either dc- or ac-coupled.

The ADA4417-3 also has an output dc offset function that can operate in two states. When the DCO pin is tied to V_{CC}, the video signal at the output is offset by 200 mV. When the DCO pin is tied to ground, the output dc level follows the input level.

The ADA4417-3 is available in a 10-lead MSOP package and is rated for operation over the extended industrial temperature range of −40°C to +85°C.

Rev. A
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REVISION HISTORY

11/09—Rev. 0 to Rev. A

Changes to Input and Output Coupling 13
Changes to Figure 28 14
Updated Outline Dimensions 15

7/06—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V (@ T_A = 25°C, V_{IN} = 1 V p-p, G = +2, R_T = 0 Ω[1], R_L = 150 Ω, DCO = 1, unless otherwise noted).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL PERFORMANCE					
DC Offset	DCO = 1, input referred	70	100	142	mV
	DCO = 0, input referred			40	mV
Input Voltage Range			See Note 2[2]		
Output Voltage Range		0.08		4.73	V
Linear Output Current	Per channel		30		mA
DC Voltage Gain		5.88		6.07	dB
Integrated Voltage Noise	f = 100 kHz to 30 MHz, input referred		0.4		mV rms
Filter Input Bias Current			3.2		µA
Slew Rate			150		V/µs
Settling Time to 0.5%			65		ns
Output Overdrive Recovery			125		ns
Total Harmonic Distortion	f = 1 MHz, V_{IN} = 0.7 V p-p		0.01		%
Gain Matching			0.01	0.09	dB
FILTER DYNAMIC PERFORMANCE					
−1 dB Bandwidth		27	38		MHz
−3 dB Bandwidth		31	42		MHz
Out-of-Band Rejection	f = 75 MHz	38	44		dB
Crosstalk	f = 5 MHz, input referred, R_T = 275 Ω[1]		−68		dB
Propagation Delay	f = 5 MHz		26		ns
Group Delay Variation	f = 1 MHz to 36 MHz		5		ns
Differential Gain	Modulated 10 step ramp, sync tip at 0 V		0.06		%
Differential Phase	Modulated 10 step ramp, sync tip at 0 V		0.21		Degrees
$\overline{\text{DISABLE}}$ PERFORMANCE					
$\overline{\text{DISABLE}}$ Assert Voltage				0.8	V
$\overline{\text{DISABLE}}$ Assert Time			100		ns
$\overline{\text{DISABLE}}$ Deassert Voltage		2.0			V
$\overline{\text{DISABLE}}$ Deassert Time			2.0		µs
$\overline{\text{DISABLE}}$ Input Bias Current			32		µA
Input-to-Output Isolation—Disabled	f = 5 MHz, $\overline{\text{DISABLE}}$ = 0		92		dB
POWER SUPPLY					
Operating Range			3.3 to 5.0		V
Quiescent Current	DCO = 0		19.5	22.5	mA
	DCO = 1		24.0	29.5	mA
Quiescent Current—Disabled	DCO = 0, $\overline{\text{DISABLE}}$ = 0		10		µA
PSRR	DCO = 0	55	71		dB

[1] See Figure 25.
[2] Limited by output range.

V_S = 3.3 V (@ T_A = 25°C, V_{IN} = 1.0 V p-p, G = +2, R_T = 0 Ω[1], R_L = 150 Ω, DCO = 1, unless otherwise noted).

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL PERFORMANCE					
DC Offset	DCO = 1, input referred	66	100	145	mV
	DCO = 0, input referred			42	mV
Input Voltage Range			See Note 2[2]		
Output Voltage Range		0.08		3.05	V
Linear Output Current	Per channel		20		mA
DC Voltage Gain		5.75		6.16	dB
Integrated Voltage Noise	f = 100 kHz to 30 MHz, input referred		0.4		mV rms
Filter Input Bias Current			3.2		µA
Slew Rate			130		V/µs
Settling Time to 0.5%			70		ns
Output Overdrive Recovery			125		ns
Total Harmonic Distortion	f = 1 MHz, V_{IN} = 0.7 V p-p		0.08		%
Gain Matching			0.02	0.18	dB
FILTER DYNAMIC PERFORMANCE					
−1 dB Bandwidth		27	38		MHz
−3 dB Bandwidth		31	42		MHz
Out-of-Band Rejection	f = 75 MHz	40	44		dB
Crosstalk	f = 5 MHz, input referred, R_T = 275 Ω[1]		−61		dB
Propagation Delay	f = 5 MHz		26.5		ns
Group Delay Variation	f = 1 MHz to 36 MHz		4		ns
Differential Gain	Modulated 10 step ramp, sync tip at 0 V		0.07		%
Differential Phase	Modulated 10 step ramp, sync tip at 0 V		0.14		Degrees
$\overline{\text{DISABLE}}$ PERFORMANCE					
$\overline{\text{DISABLE}}$ Assert Voltage				0.8	V
$\overline{\text{DISABLE}}$ Assert Time			110		ns
$\overline{\text{DISABLE}}$ Deassert Voltage		2.0			V
$\overline{\text{DISABLE}}$ Deassert Time			3.0		µs
$\overline{\text{DISABLE}}$ Input Bias Current			19		µA
Input-to-Output Isolation—Disabled	f = 5 MHz, $\overline{\text{DISABLE}}$ = 0		92		dB
POWER SUPPLY					
Operating Range			3.3 to 5.0		V
Quiescent Current	DCO = 0		19.0	21.5	mA
	DCO = 1		22.5	29.0	mA
Quiescent Current—Disabled	DCO = 0, $\overline{\text{DISABLE}}$ = 0		10		µA
PSRR	DCO = 0	52	71		dB

[1] See Figure 25.
[2] Limited by output range.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 2
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	Unit
10-Lead MSOP	130	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4417-3 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4417-3. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the supply voltage (V_S) times the quiescent current (I_S). Assuming the load (R_L) is midsupply, then the total drive power is

$$V_S/2 \times I_{OUT}$$

some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

RMS output voltages should be considered. If R_L is referenced to GND, the total power is $V_S \times I_{OUT}$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 10-lead MSOP (130°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximate.

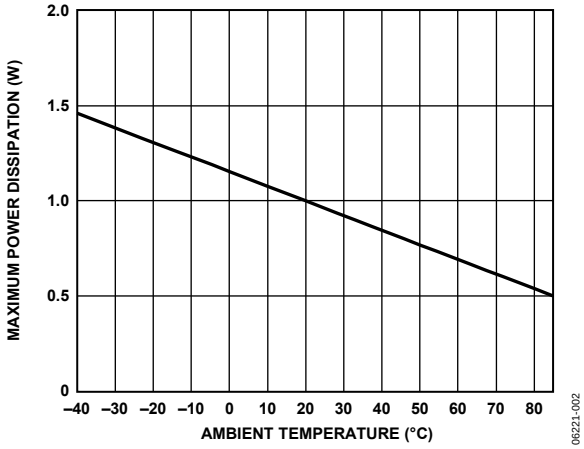


Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

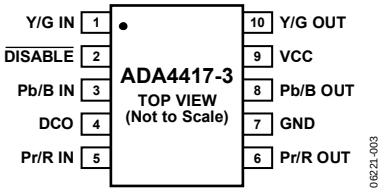


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y/G IN	Y/G HD Video Input
2	$\overline{\text{DISABLE}}$	Disable/Power Down (Active Low)
3	Pb/B IN	Pb/B HD Video Input
4	DCO	Output DC Offset Enable
5	Pr/R IN	Pr/R HD Video Input
6	Pr/R OUT	Pr/R HD Video Output
7	GND	Ground
8	Pb/B OUT	Pb/B HD Video Output
9	VCC	Power Supply
10	Y/G OUT	Y/G HD Video Output

TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: V_S = 5 V, T_A = 25°C, V_O = 2 V p-p, G = +2, R_T = 0 Ω (see Figure 25), R_L = 150 Ω, DCO = 1, unless otherwise noted.

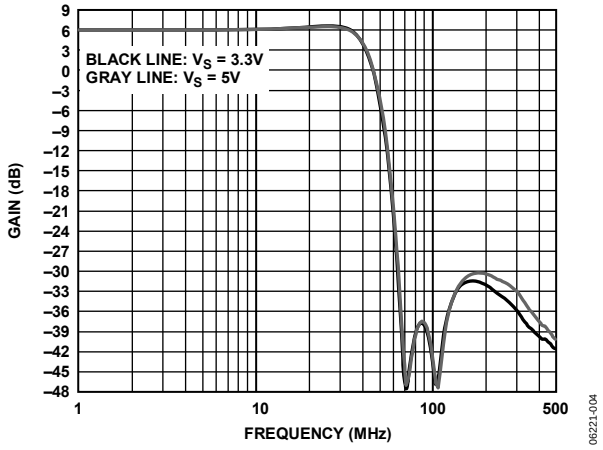


Figure 4. Frequency Response vs. Supply

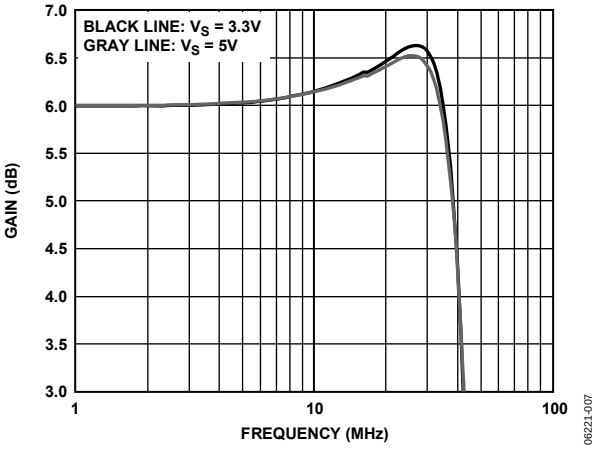


Figure 7. Flatness Response vs. Supply

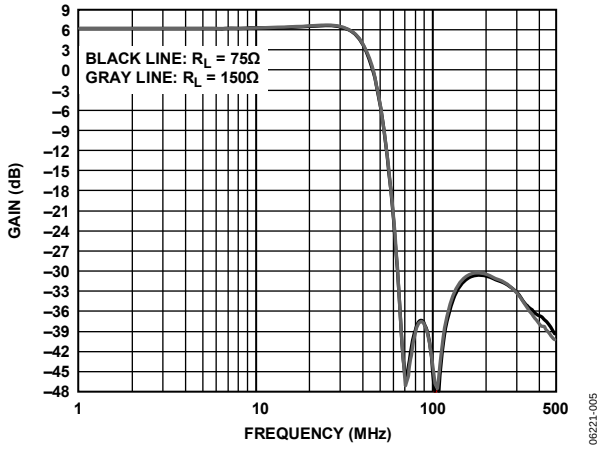


Figure 5. Frequency Response vs. Load

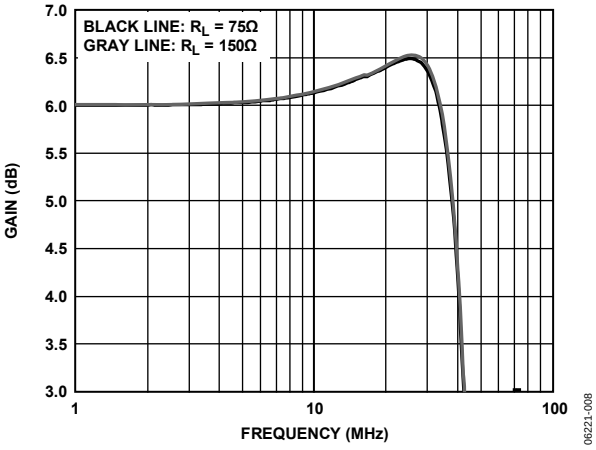


Figure 8. Flatness Response vs. Load

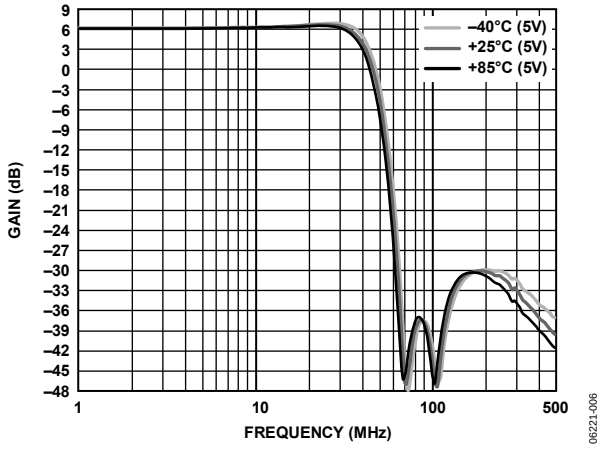


Figure 6. Frequency Response vs. Temperature

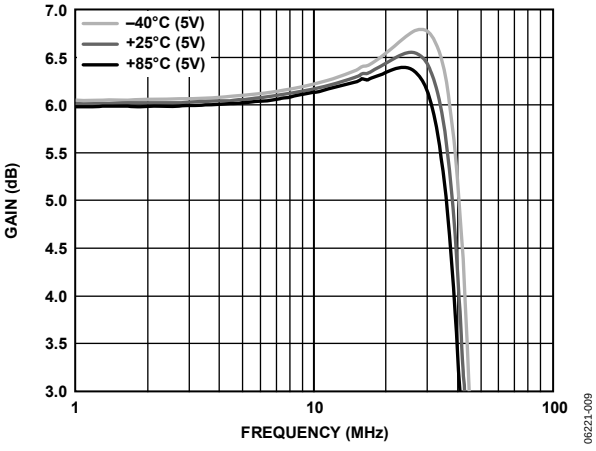


Figure 9. Flatness Response vs. Temperature

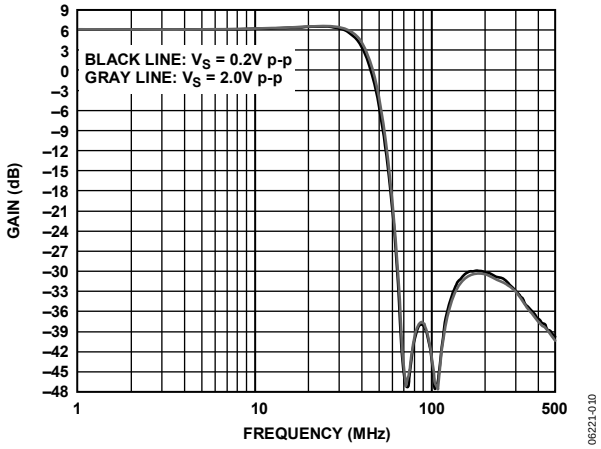


Figure 10. Frequency Response vs. Amplitude

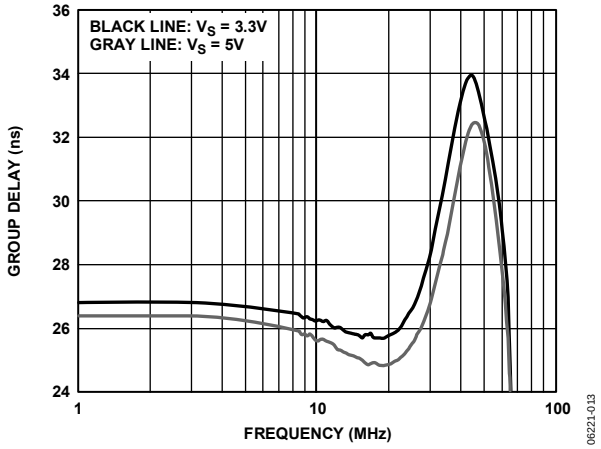


Figure 13. Group Delay vs. Frequency

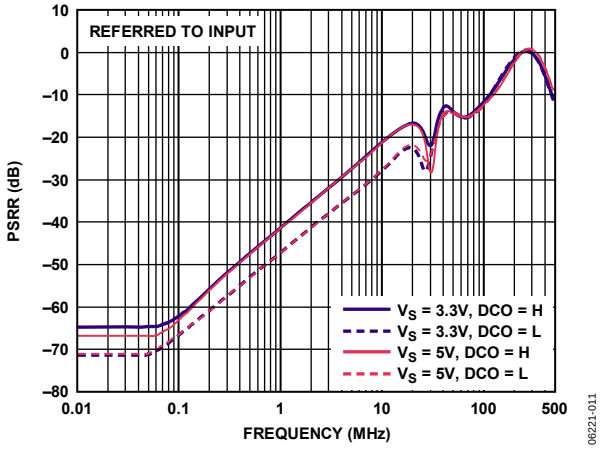


Figure 11. PSRR vs. Frequency

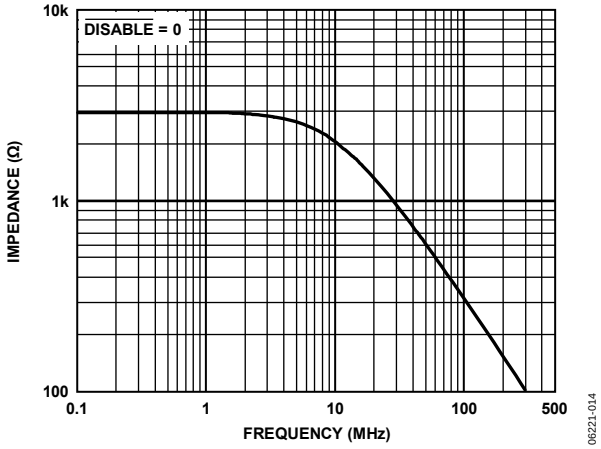


Figure 14. Output Impedance (Disabled) vs. Frequency

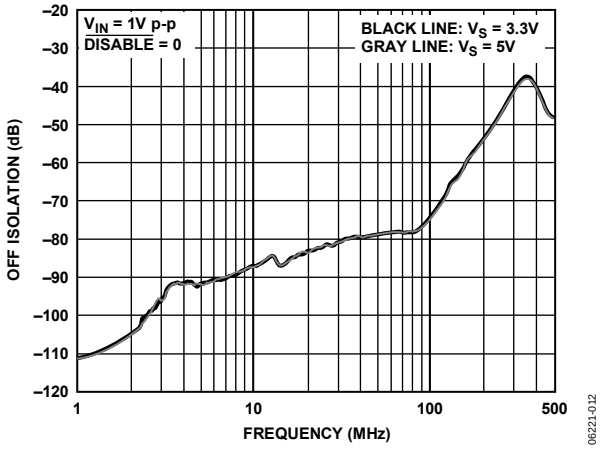


Figure 12. Off Isolation vs. Frequency

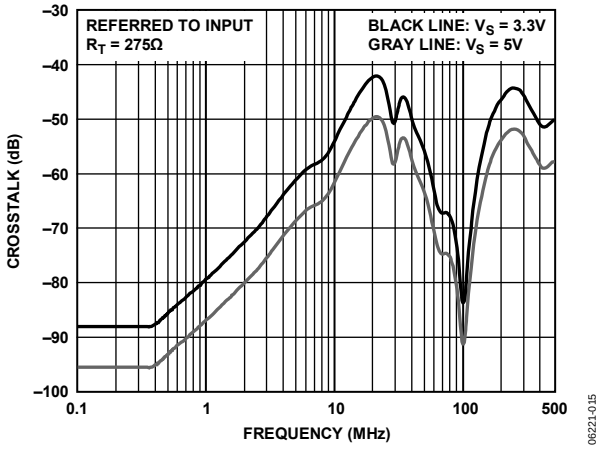


Figure 15. Crosstalk vs. Frequency

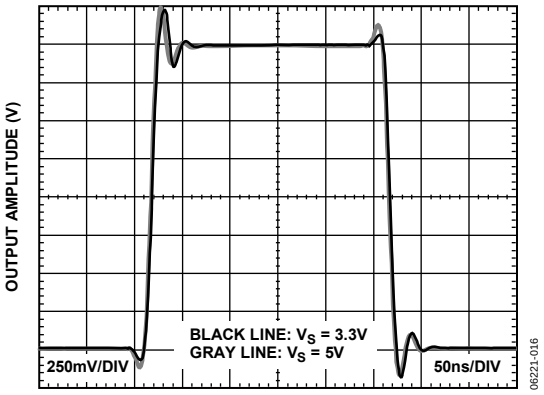


Figure 16. Transient Response

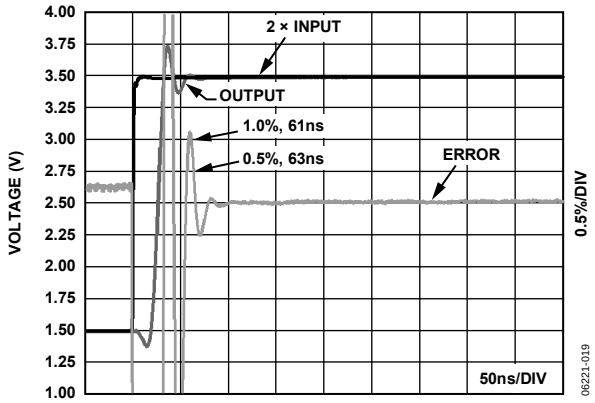


Figure 19. Settling Time

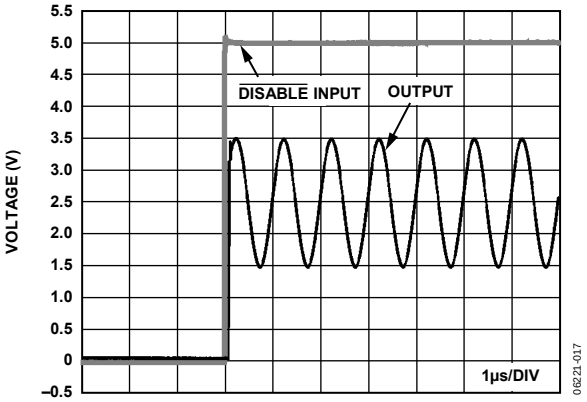


Figure 17. Enable Turn On Time

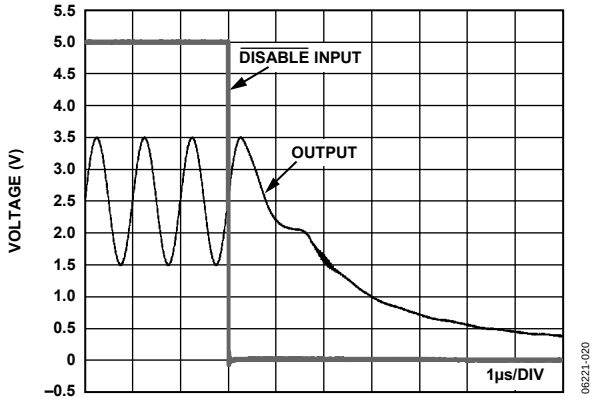


Figure 20. Enable Turn Off Time

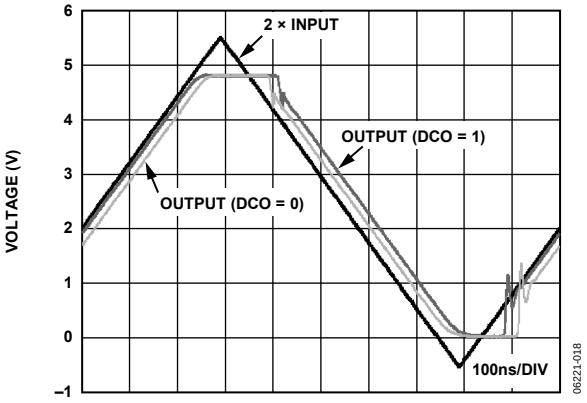


Figure 18. Output Overdrive Recovery

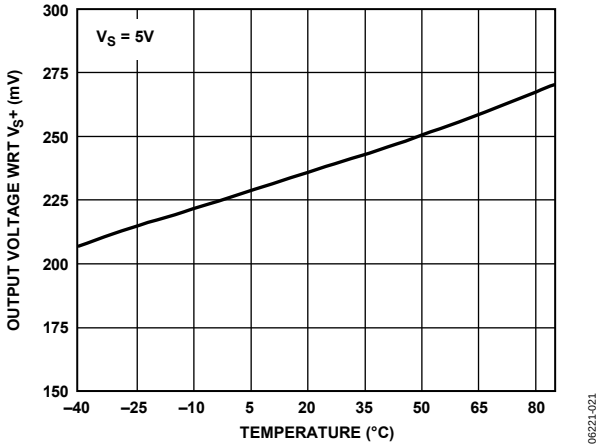


Figure 21. Output Saturation Voltage vs. Temperature

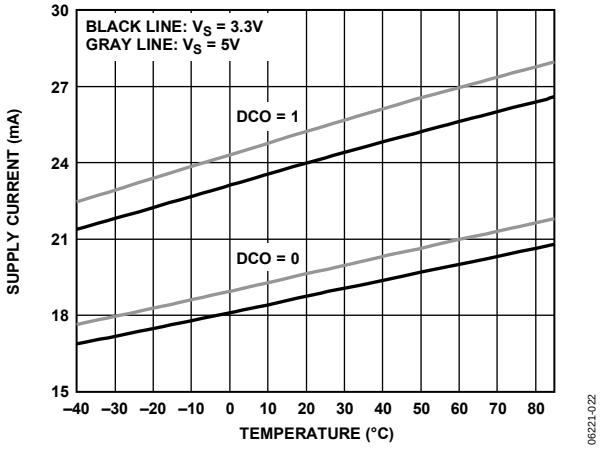


Figure 22. Supply Current vs. Temperature

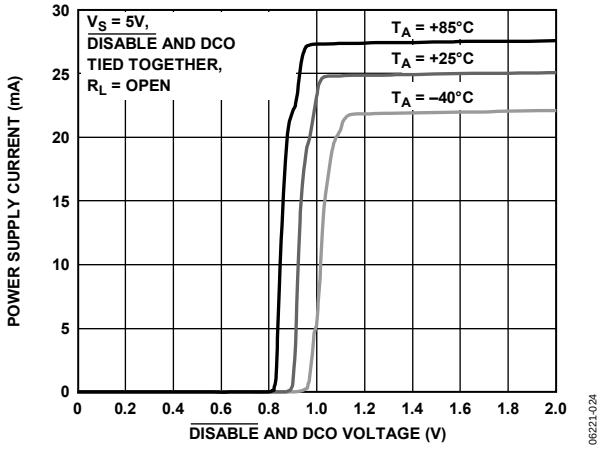


Figure 24. Supply Current vs. $\overline{DISABLE}$/DCO Voltage and Temperature

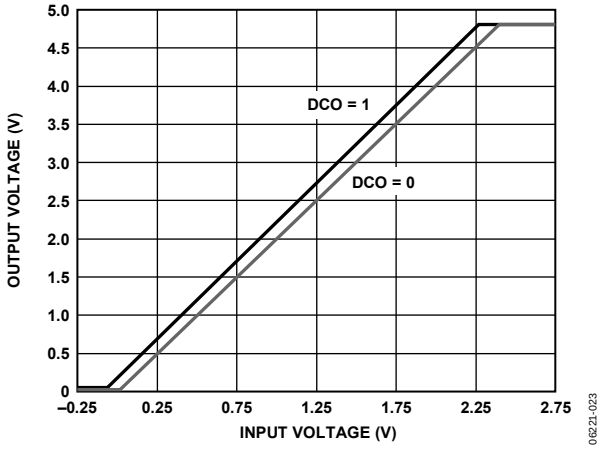


Figure 23. Output Voltage vs. Input Voltage

TEST CIRCUIT

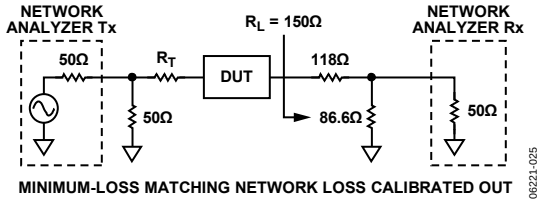


Figure 25. Basic Test Circuit for Swept Frequency Measurements

THEORY OF OPERATION

The ADA4417-3 is a low cost, integrated video filtering and driving solution that offers a 38 MHz, 1 dB bandwidth to meet the requirements of high definition video. Each of the three filters has a sixth-order Butterworth response that includes group delay equalization. Group delay variation from 1 MHz to 36 MHz is only 5 ns, resulting in greater stop-band attenuation and minimal phase distortion.

The ADA4417-3 is designed to operate in many video environments. With a supply range of 3.3 V to 5 V, it requires a relatively low nominal quiescent current of 10 mA per channel. This makes the ADA4417-3 well suited for portable high definition video applications. Additionally, for other low power applications, the part can be powered down to draw typically 10 μA by pulling the $\overline{\text{DISABLE}}$ pin to ground. The ADA4417-3 is also well suited for high encoding frequency applications because it maintains a stop-band attenuation of over 40 dB out to 500 MHz. Typical power supply rejection ratio (PSRR) is greater than 70 dB, providing excellent rejection in systems with supplies that are noisy or underregulated.

The ADA4417-3 is intended to accept dc-coupled inputs from an encoder or other ground-referenced video signals. The ADA4417-3 inputs are high impedance. No minimum or maximum input termination is required; however, terminations above 1 kΩ may degrade crosstalk performance at high frequencies.

Each filter input includes level-shifting circuitry. The level-shifting circuitry adds a dc component of 100 mV to ground-referenced input signals so that they reproduce accurately, without the output buffers hitting the ground rail. For lowest off state power consumption when using the dc offset function, it is recommended that the DCO and $\overline{\text{DISABLE}}$ pins be tied together.

The output drivers on the ADA4417-3 have rail-to-rail output capabilities with 6 dB gain. Each output is capable of driving two ac- or dc-coupled, 75 Ω source-terminated loads. If a large dc output level is required while driving two loads, ac coupling should be used to limit the power dissipation.

APPLICATIONS

OVERVIEW

With its high impedance inputs and high output drive, the ADA4417-3 is ideally suited to video reconstruction and antialias filtering applications. The high impedance inputs give designers flexibility with regard to how the input signals are terminated. Devices with DAC current source outputs that feed the ADA4417-3 can be loaded in whatever resistance provides the best performance, and devices with voltage outputs can be optimally terminated as well. The ADA4417-3 outputs can each drive up to two source-terminated, 75 Ω loads and can therefore directly drive the outputs from set-top boxes, DVDs, and a like without the need for a separate output buffer.

DISABLE

The ADA4417-3 includes a disable feature that can be used to save power when a particular device is not in use. The disable feature is asserted by pulling the $\overline{\text{DISABLE}}$ pin to ground.

Table 6 summarizes the disable feature operation.

Table 6. $\overline{\text{DISABLE}}$ Function

$\overline{\text{DISABLE}}$ Pin Connection	Status
V_S	Enabled
GND	Disabled

OUTPUT DC OFFSET CONTROL

The ADA4417-3 has a fixed, pin-selectable, input-referred dc offset. When the DCO pin is tied to V_S, the output is offset by 200 mV, preventing the video sync tips from hitting the ground rail. When DCO is tied to GND, the dc level of the output follows that of the input.

Table 7 summarizes the dc offset operation.

Table 7. DC Offset Function

DCO Pin Connection	Status
V_S	Output offset = 200 mV
GND	No output offset

INPUT AND OUTPUT COUPLING

Inputs to the ADA4417-3 may be ac- or dc-coupled. AC coupling requires suitable circuitry following the ac coupling element to provide proper dc level and bias currents at the input stages. The ADA4417-3 outputs can be either ac- or dc-coupled.

When driving single, ac-coupled loads in standard 75 Ω video distribution systems, 220 µF coupling capacitors are recommended for use on all outputs.

There are two ac coupling options when driving two loads from one output. One simply uses the same value capacitor on the second load, while the other is to use a common coupling capacitor that is at least twice the value used for the single load (see Figure 26 and Figure 27).

When driving two parallel 150 Ω loads (75 Ω effective load), the 3 dB bandwidth of the filters typically varies from that of the filters with a single 150 Ω load. Typical variation is within ±2.5%.

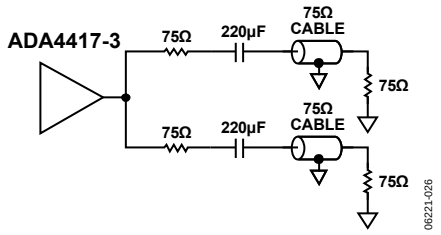


Figure 26. Driving Two AC-Coupled Loads with Two Coupling Capacitors

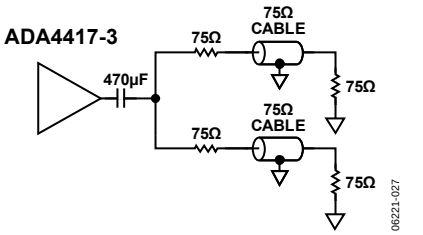


Figure 27. Driving Two AC-Coupled Loads with One Common Coupling Capacitor

PRINTED CIRCUIT BOARD LAYOUT

As with all high speed applications, attention to printed circuit board layout is of paramount importance. Standard high speed layout practices should be adhered to when designing with the ADA4417-3. A solid ground plane is recommended, and surface-mount, ceramic power supply decoupling capacitors should be placed as close as possible to the supply pins. All of the ADA4417-3 GND pins should be connected to the ground plane with traces that are as short as possible. Controlled impedance traces of the shortest length possible should be used to connect to the signal I/O pins and should not pass over any voids in the ground plane. A 75 Ω impedance level is typically used in video applications. All signal outputs of the ADA4417-3 should include series termination resistors when driving transmission lines.

When the ADA4417-3 receives its inputs from a device with current outputs, the required load resistor value for the output current is often different from the characteristic impedance of the signal traces. In this case, if the interconnections are sufficiently short (<< 0.1 wavelength), the trace does not have to be terminated in its characteristic impedance. Traces of 75 Ω can be used in this instance, provided their lengths are an inch or two at most. This is easily achieved because the ADA4417-3 and the device feeding it are usually adjacent to each other, and connections can be made that are less than one inch in length.

VIDEO ENCODER RECONSTRUCTION FILTER

The ADA4417-3 is easily applied as a reconstruction filter at the DAC outputs of a video encoder. Figure 28 illustrates how to use the ADA4417-3 in this type of application with an ADV7322 video encoder in a single-supply application with ac-coupled outputs.

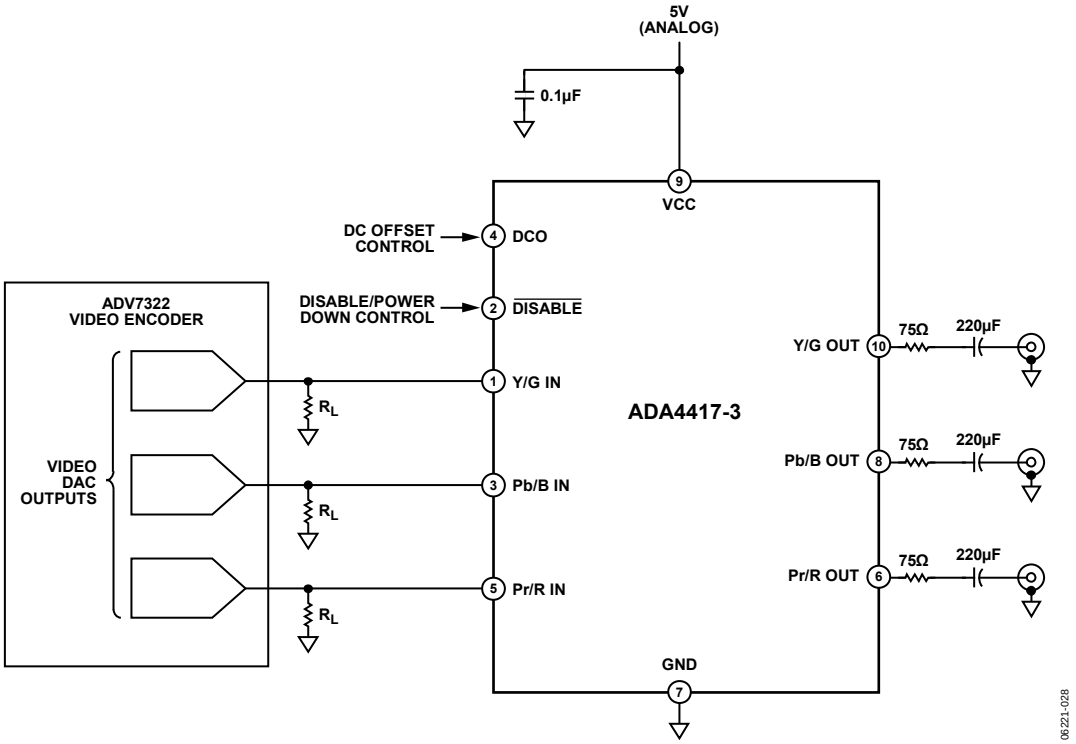


Figure 28. The ADA4417-3 Applied as a Video Reconstruction Filter Following the ADV7322

OUTLINE DIMENSIONS

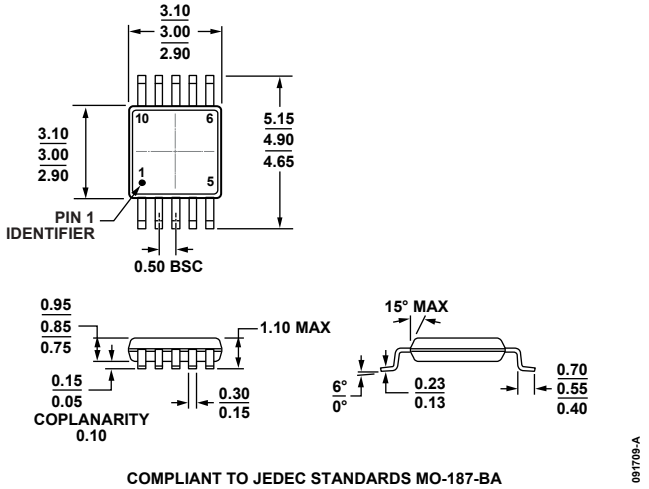


Figure 29. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Order Quantity	Branding
ADA4417-3ARMZ[1]	−40°C to +85°C	10-Lead MSOP	RM-10	1	H0Q
ADA4417-3ARMZ-R7[1]	−40°C to +85°C	10-Lead MSOP	RM-10	1,000	H0Q
ADA4417-3ARMZ-RL[1]	−40°C to +85°C	10-Lead MSOP	RM-10	2,500	H0Q

[1] Z = RoHS Compliant part.

NOTES

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