Wideband, Differential, High Output Current Line Driver with Shutdown

Data Sheet

ADA4312-1

FEATURES

High speed
- **−3 dB bandwidth: 195 MHz, G_{DIFF} = +16 V/V, $R_{L, DIFF}$ = 40 Ω**
- **Differential slew rate: 2100 V/µs**

Wide output swing: 18.0 V p-p differential, 12 V supply
High output current: 225 mA peak
G.hn MTPR at 16 dBm line power
- **−64 dBc typical at 5 MHz, referred to −58 dBm/Hz**
- **−64 dBc typical at 17 MHz, referred to −58 dBm/Hz**
- **−64 dBc typical at 28 MHz, referred to −58 dBm/Hz**
- **−63 dBc typical at 31 MHz, referred to −58 dBm/Hz**
- **−61 dBc typical at 59 MHz, referred to −58 dBm/Hz**
- **−62 dBc typical at 82 MHz, referred to −58 dBm/Hz**

Shutdown
- **CMOS-compatible SD pin**
- **Shutdown quiescent current: 3 mA**
- **Z_{OUT} in shutdown: 10 kΩ differential (open-loop)**

Resistor adjustable quiescent current

APPLICATIONS

ITU G.hn (ITU G.9960/G.9961)
HomePlug AV
HomePlug AV2
IEEE 1901

GENERAL DESCRIPTION

The ADA4312-1 is a high speed, differential, current feedback line driver designed for half-duplex G.hn power line communication (PLC) modems. The high output current, high bandwidth, and slew rate of 2100 V/µs make the ADA4312-1 an excellent choice for G.hn broadband applications that require high linearity while driving low impedance loads.

The CMOS-compatible shutdown control pin (SD) reduces the quiescent current to 3 mA while maintaining an output impedance of 10 kΩ differential. The ADA4312-1 also provides resistor adjustable quiescent current for improved efficiency in transmit mode.

The ADA4312-1 is available in a thermally enhanced, 16-lead LFCSP with an exposed pad to facilitate robust thermal management. The ADA4312-1 is rated to operate over the extended industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

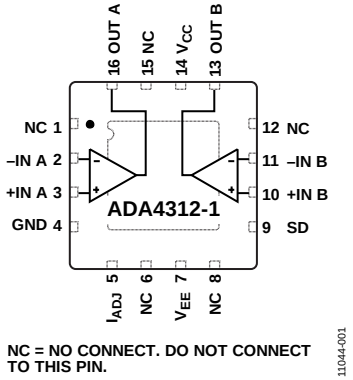


Figure 1. Thermally Enhanced, 4 mm × 4 mm, 16-Lead LFCSP

TYPICAL APPLICATION CIRCUIT

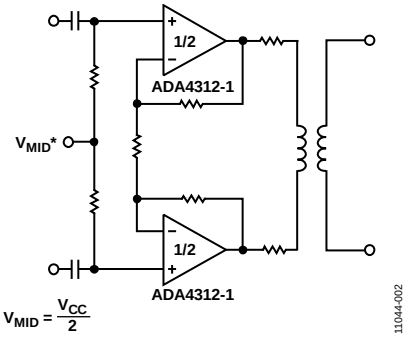


Figure 2. Typical PLC Driver Application

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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Technical Support www.analog.com

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REVISION HISTORY

4/2017—Rev. 0 to Rev. A

Changed LFCSP_WQ to LFCSP ... Throughout
Updated Outline Dimensions ... 12
Changes to Ordering Guide ... 12

10/2012—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 12 V, V_{EE} = GND, R_F = 732 Ω, R_{IADJ}[1] = 0 Ω (at T_A = 25°C, G_{DIFF} = +16 V/V, $R_{L, DIFF}$ = 40 Ω, SD = 0 V), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p differential		195		MHz
Full Power Bandwidth	V_{OUT} = 5 V p-p differential		168		MHz
Slew Rate	V_{OUT} = 4 V p-p differential, G_{DIFF} = +2 V/V		2100		V/µs
NOISE/DISTORTION PERFORMANCE					
G.hn Multitone Power Ratio (MTPR)	V_{OUT} = 16 dBm line power				
	f_C = 5 MHz, referred to −58 dBm/Hz		−64		dBc
	f_C = 17 MHz, referred to −58 dBm/Hz		−64		dBc
	f_C = 28 MHz, referred to −58 dBm/Hz		−64		dBc
	f_C = 31 MHz, referred to −58 dBm/Hz		−63		dBc
	f_C = 59 MHz, referred to −58 dBm/Hz		−61		dBc
	f_C = 82 MHz, referred to −58 dBm/Hz		−62		dBc
Differential Output Voltage Noise	f = 10 MHz		57		nV/√Hz
DC PERFORMANCE					
Differential Input Offset Voltage		−1.2		+1.2	mV
Input Bias Current					
Noninverting Input		−20		+20	µA
Inverting Input		−175		+175	µA
Open-Loop Transimpedance			47		kΩ
Common-Mode Rejection Ratio (CMRR)			−70		dB
OUTPUT CHARACTERISTICS					
Positive Swing		10.4	10.5		V peak
Negative Swing			1.5	1.6	V peak
Differential Swing		17.6	18		V p-p
Peak Output Current Drive			225		mA peak
Differential Output Impedance[2]	Disabled (SD ≥ 2.0 V)		10		kΩ
Disabled Output Voltage	SD ≥ 2.0 V, referred to V_{MID}		±15		mV
POWER SUPPLY					
Single-Supply Voltage			12		V
Supply Current	SD ≤ 0.8 V		46	49.5	mA
	SD ≥ 2.0 V		3	4	mA
SHUTDOWN PIN					
High Level Input Voltage, V_{IH}	Referenced to GND		2.0		V
Low Level Input Voltage, V_{IL}	Referenced to GND		0.8		V
SD = Low Bias Current	SD = 0.8 V	−30	−20		µA
SD = High Bias Current	SD = 2.0 V	−15	−9		µA
Enable Time			1		µs
Disable Time			1		µs
Power Supply Rejection Ratio (PSRR)			−70		dB

[1] R_{IADJ} is the resistor that must be installed between I_{ADJ} (Pin 5) and GND (Pin 4).
[2] Differential output impedance is measured open-loop.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{CC}	13.2 V
SD Voltage	V_{CC}
Power Dissipation	1.25 W
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The thermal resistance (θ_{JA}) was specified using the ADA4312-1 evaluation board (EVAL-ADA4312-1ACPZ).

Table 3.

Package Type	θ_{JA}	Unit
16-Lead LFCSP	31.8	°C/W

MAXIMUM POWER DISSIPATION

Exceeding a junction temperature of 150°C can result in changes to silicon devices, potentially causing degradation or loss of functionality.

The power dissipation of the ADA4312-1 is 750 mW for a typical G.hn application delivering 16 dBm into a 40 Ω differential load.

The maximum internal power dissipation should not exceed 1.25 W over the extended industrial temperature range of −40°C to +85°C on a PCB designed according to the guidelines in the Thermal Management section.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

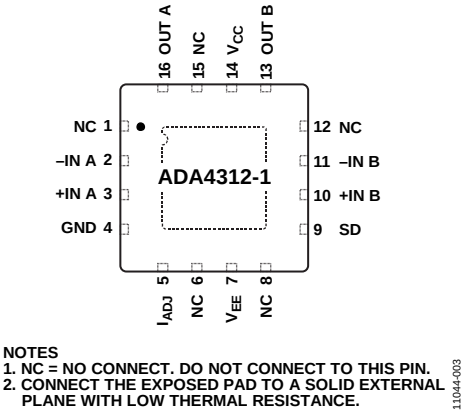


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. Do not connect to this pin.
2	−IN A	Amplifier A Inverting Input.
3	+IN A	Amplifier A Noninverting Input.
4	GND	Ground (Reference for SD and I_{ADJ}). Electrical connection required.
5	I_{ADJ}	Resistor Controlled Bias Current Adjust. A resistor connection to GND is required.
6	NC	No Connect. Do not connect to this pin.
7	V_{EE}	Negative Power Supply Input.
8	NC	No Connect. Do not connect to this pin.
9	SD	Shutdown Control.
10	+IN B	Amplifier B Noninverting Input.
11	−IN B	Amplifier B Inverting Input.
12	NC	No Connect. Do not connect to this pin.
13	OUT B	Amplifier B Output.
14	V_{CC}	Positive Power Supply Input.
15	NC	No Connect. Do not connect to this pin.
16	OUT A	Amplifier A Output.
	EPAD	No electrical connection. Connect the exposed pad to a solid external plane with low thermal resistance (see the Thermal Management section).

TYPICAL PERFORMANCE CHARACTERISTICS

The figures in this section refer to the test circuit shown in Figure 16, unless otherwise noted.

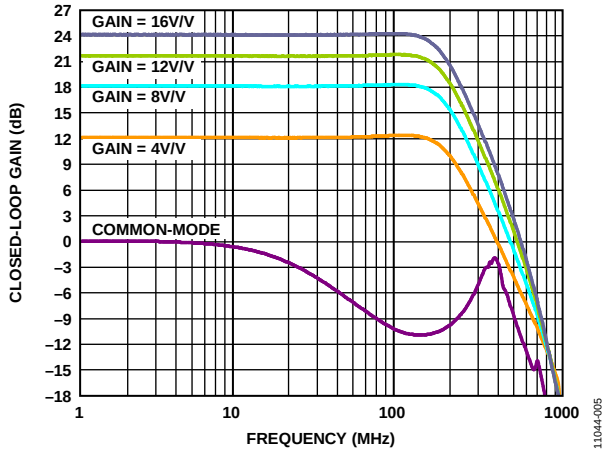


Figure 4. Small Signal Differential and Common-Mode Frequency Response

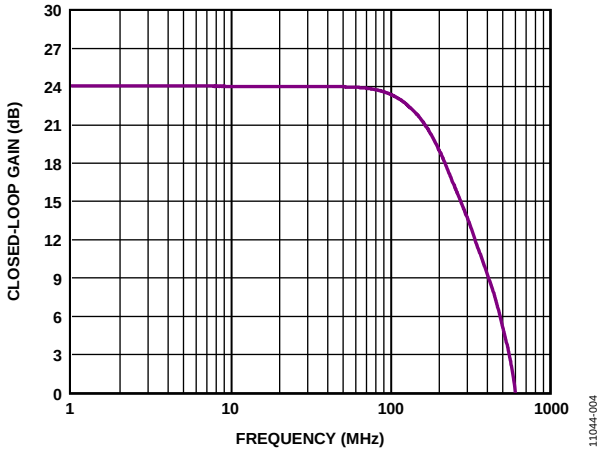


Figure 7. Large Signal Differential Frequency Response, Gain = +16 V/V, Differential V_{OUT} = 5 V p-p

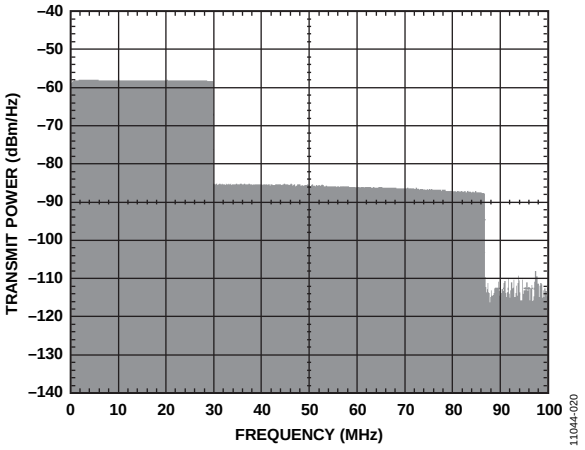


Figure 5. G.hn Transmit Spectrum, 16 dBm into 40 Ω Differential

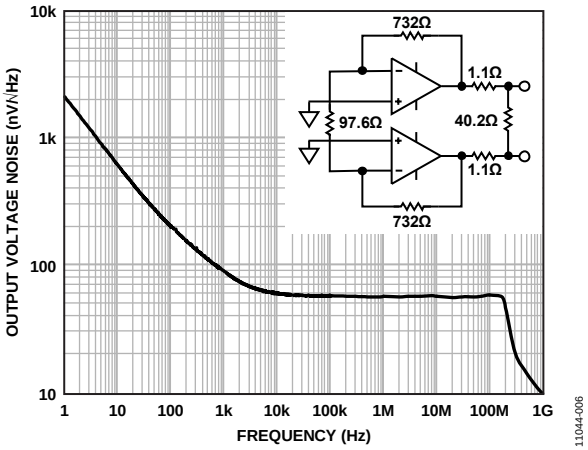


Figure 8. Differential Output Voltage Noise vs. Frequency, Gain = +16 V/V

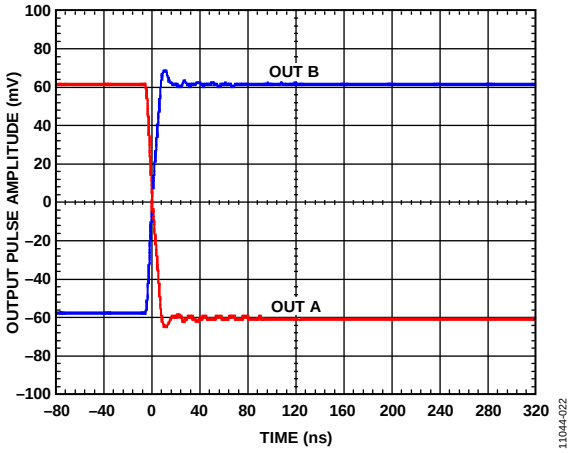


Figure 6. Small Signal Output Transient Response, Normalized to 0 V, 10 ns Rise Time, 10 ns Fall Time, 1 µs Pulse Width, 10% Duty Cycle

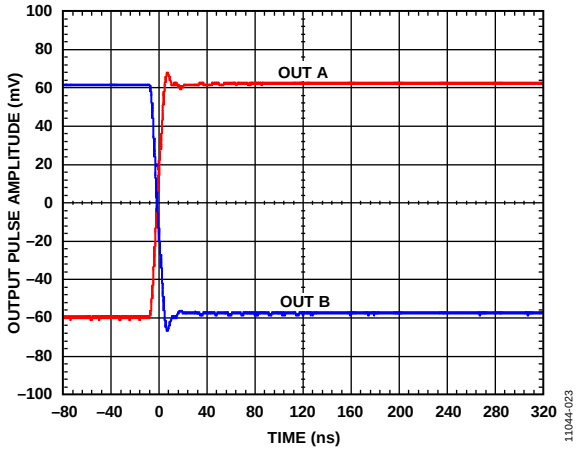


Figure 9. Small Signal Output Transient Response, Normalized to 0 V, 10 ns Rise Time, 10 ns Fall Time, 1 µs Pulse Width, 10% Duty Cycle

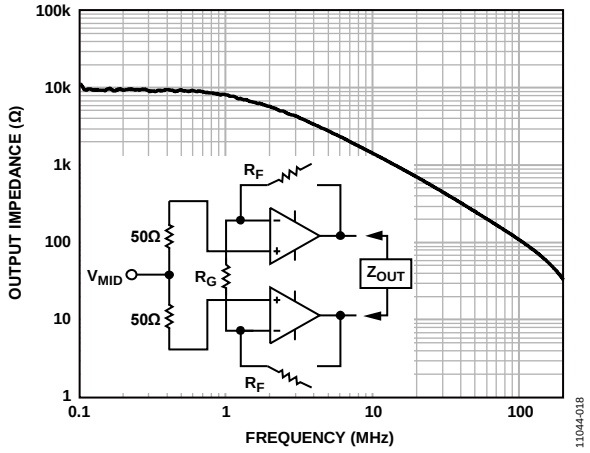


Figure 10. Open-Loop Disabled Differential Output Impedance vs. Frequency

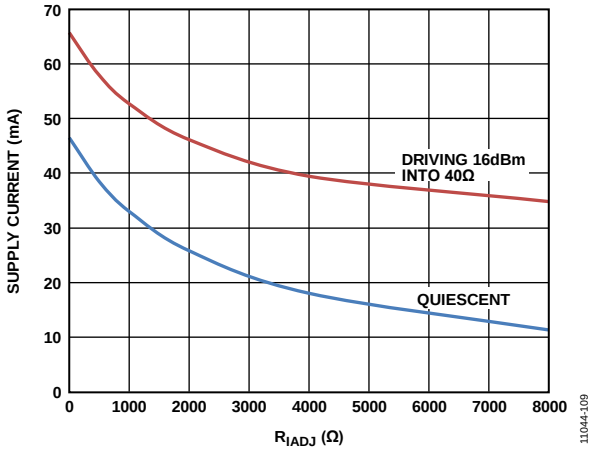


Figure 13. Supply Current vs. I_{ADJ} Resistance (R_{IADJ})

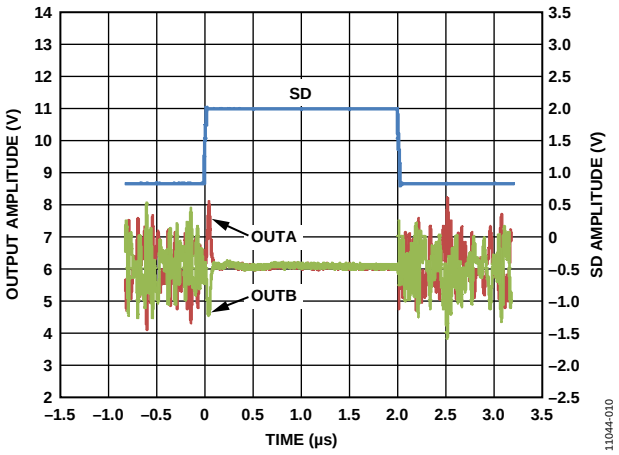


Figure 11. Shutdown Enable/Disable with Differential OFDM Input

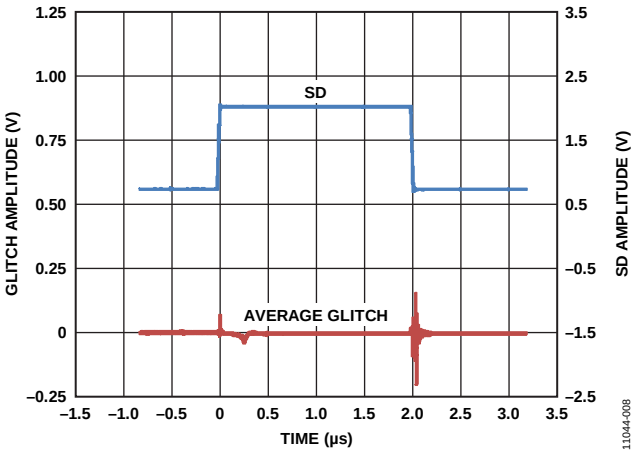


Figure 14. Shutdown Enable/Disable Glitch, Normalized to 0 V, Differential Input = 0 V

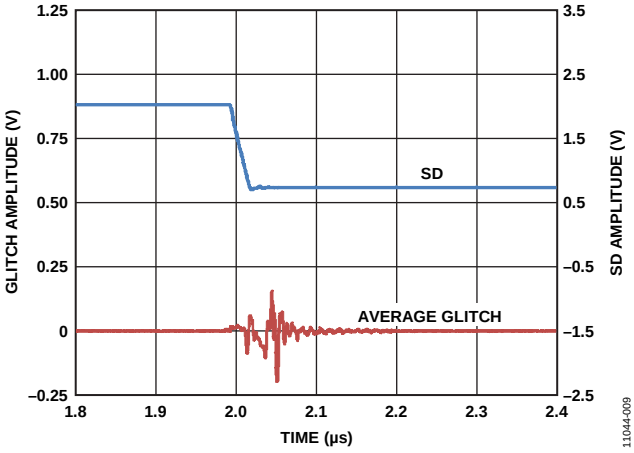


Figure 12. Differential Output Enable Glitch, Normalized to 0 V

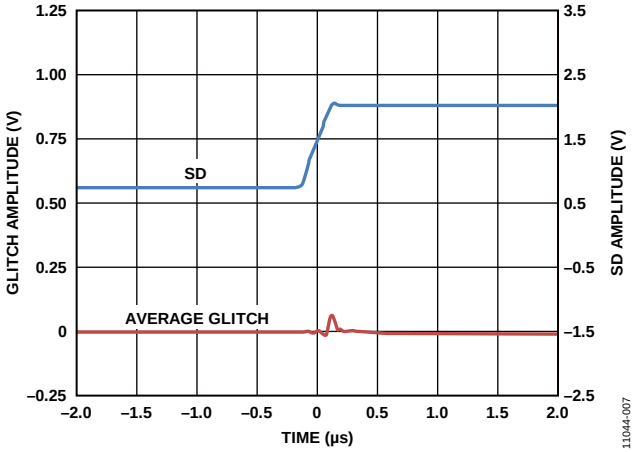


Figure 15. Differential Output Disable Glitch, Normalized to 0 V

TEST CIRCUIT

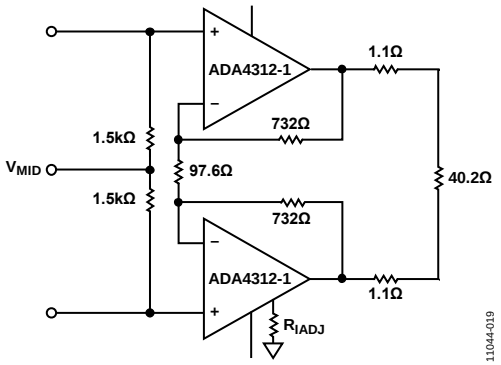


Figure 16. Test Circuit, R_{IADJ} = 0 Ω

APPLICATIONS INFORMATION

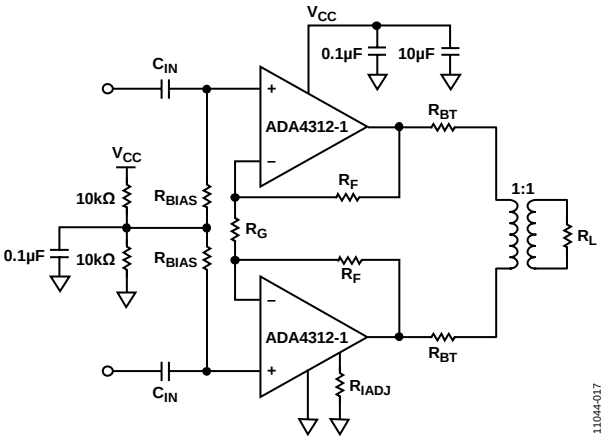


Figure 17. Typical G.hn Application Circuit

FEEDBACK RESISTOR SELECTION

The feedback resistor value has a direct impact on the closed-loop bandwidth of the current feedback amplifiers used in the architecture of the ADA4312-1 differential line driver. Table 5 provides a guideline for the selection of feedback resistor values used in typical differential line driver circuits (refer to Figure 17).

Table 5. Resistor Values and Frequency Performance

Gain	R_F (Ω)	R_G (Ω)	−3 dB SS BW (MHz)
16 V/V	732	97.6	195
12 V/V	750	137	200
8 V/V	768	221	209
4 V/V	806	536	222

Selecting a feedback resistor with a value that is lower than the values in Table 5 can create peaking in the frequency response; in extreme cases, this peaking can lead to instability. Conversely, a feedback resistor that exceeds the values in Table 5 can limit the closed-loop bandwidth.

GENERAL OPERATION

The ADA4312-1 is a differential line driver designed for single-supply operation in G.hn line driver applications. The core architecture comprises two high speed current feedback amplifiers. The inputs of these amplifiers are arranged in a unique way that facilitates extended differential bandwidth, linearity, and stability while limiting common-mode bandwidth and enhancing common-mode stability.

The patented input stage of the core amplifiers is not conducive to operating either core amplifier independently. The ADA4312-1 input stage is designed to operate only in differential applications similar to the circuit shown in Figure 17.

HALF-DUPLEX OPERATION

In systems such as G.hn PLC modems, half-duplex or time-division duplex (TDD) systems require the line driver to be switched between transmit mode and high output impedance receive mode. The ADA4312-1 is equipped with a shutdown pin (SD, Pin 9) that stops the line driver from transmitting while switching the outputs to a high output impedance equivalent to 10 kΩ in parallel with $2R_F + R_G$ (see Figure 17). The shutdown (SD) pin is compatible with standard 3.3 V CMOS logic. If the SD pin is left floating, an internal pull-up resistor places the output in a disabled, high output impedance state. SD logic is referred to GND (Pin 4), which should be connected to 0 V.

ESTABLISHING V_{MID}

In single-supply applications such as the one shown in Figure 17, it is necessary to establish a midsupply operating point (V_{MID}). To establish V_{MID}, use two 10 kΩ resistors to form a resistor divider from V_{CC} to ground and a 0.1 µF ceramic chip capacitor for decoupling. Place the V_{MID} decoupling capacitor and the R_{BIAS} resistors as close as possible to the ADA4312-1.

BIAS CONTROL AND LINEARITY

The ADA4312-1 is equipped with a biasing adjustment feature that lowers the quiescent operating current. A resistor (R_{IADJ}) must be placed between I_{ADJ} (Pin 5) and GND (Pin 4) for proper operation of the ADA4312-1. Using a resistor larger than 0 Ω reduces the quiescent current of the line driver and improves efficiency in transmit mode. Figure 13 shows the quiescent current vs. R_{IADJ}.

Note that there is a trade-off between the adjusted quiescent current and the linearity (or MTPR) of the transmitted signal. Multitone power ratio (MTPR) was monitored at 5 MHz, 17 MHz, 28 MHz, 31 MHz, 59 MHz, and 82 MHz. Figure 18 can be used to gauge the approximate degradation of MTPR vs. R_{IADJ} and quiescent current while transmitting the G.hn signal across a 40 Ω differential load in the circuit shown in Figure 17.

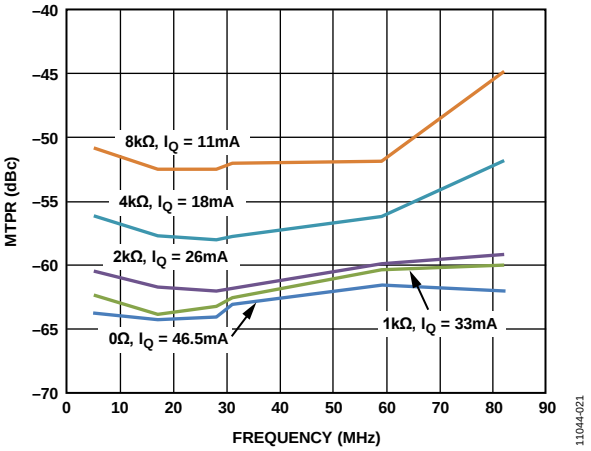


Figure 18. MTPR vs. R_{IADJ}

PCB LAYOUT

As is the case with many high speed line driver applications, careful attention to printed circuit board (PCB) layout can improve performance and help maintain stability while preventing excessive die temperatures during normal operation. Differential signal balance can be maintained by using symmetry in the PCB layout of input and output signal traces.

Keeping the input and output traces as short as possible helps prevent excessive parasitics from affecting overall performance and stability. Keep the feedback resistors and gain setting resistor as close to the line driver as physically possible. The back termination resistors and line coupling transformer should be placed as close to the ADA4312-1 outputs as possible.

For more information about high speed board layout, see *A Practical Guide to High-Speed Printed-Circuit-Board Layout* (Analog Dialogue, Volume 39, September 2005).

THERMAL MANAGEMENT

The thermal pad of the ADA4312-1 is an electrically isolated copper pad that should be soldered to an external thermal ground plane. The number of thermal vias that connect the exposed pad of the ADA4312-1 to the PCB can influence the thermal conductivity of the PCB assembly. Moving heat away from the ADA4312-1 die to the ambient environment is the objective of a PCB designed in accordance with the guidelines found in the AN-772 Application Note.

The outer layers of the PCB are the best choice to radiate heat into the environment by convection. Conducting heat away from the ADA4312-1 die into the outer layers of the PCB can be accomplished with nine thermal vias connecting the exposed pad to both outer layers. The vias can be spaced 0.75 mm apart in a 3 × 3 matrix.

The ADA4312-1 evaluation board (EVAL-ADA4312-1ACPZ) represents a robust example of an effective thermal management approach (see Figure 19 and Figure 20).

For more information about thermal management, solder assembly techniques for LFCSP packages, and important package mechanical and materials information, refer to the following link:

http://www.analog.com/en/technical-library/packages/csp-chip-scale-package/lfcsp/index.html

POWER SUPPLY BYPASSING

The ADA4312-1 should be operated on a well-regulated single +12 V power supply. Pay careful attention to power supply decoupling. Use high quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), to minimize supply voltage ripple and power dissipation.

Locate the 0.1 µF MLCC decoupling capacitor no more than one-eighth of an inch away from the V_{CC} supply pin. In addition, a 10 µF tantalum capacitor is recommended to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the ADA4312-1 outputs. Lay out bypassing capacitors to keep return currents away from the inputs of the amplifiers. A large ground plane provides a low impedance path for the return currents.

EVALUATION BOARD

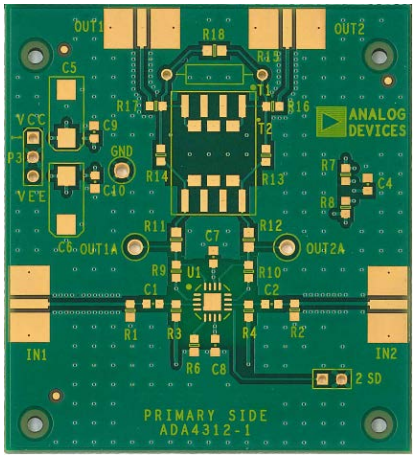


Figure 19. Evaluation Board Top Layer

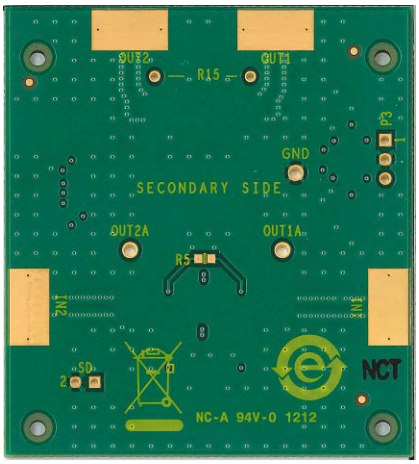
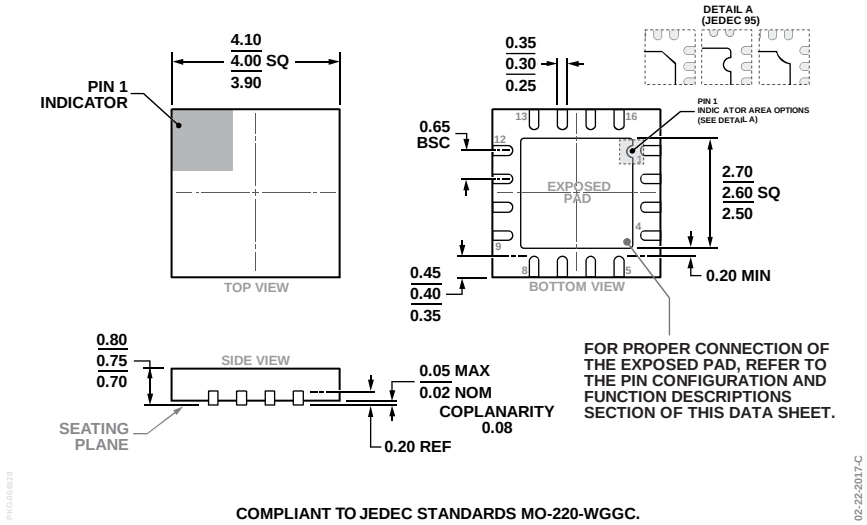


Figure 20. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 21. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4312-1ACPZ-R2	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17
ADA4312-1ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17
ADA4312-1ACPZ-RL	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17

[1] Z = RoHS Compliant Part.

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D11044-0-4/17(A)