1:2 Single-Ended, Low Cost Active RF Splitter

ADA4303-2

FEATURES

- Ideal for CATV applications
- Excellent frequency response
  - 1.7 GHz, −3 dB bandwidth
  - 1 dB flatness to 1.2 GHz
- Low noise figure: 4.4 dB
- Low distortion
  - Composite second order (CSO): −62 dBc
  - Composite triple beat (CTB): −72 dBc
  - 1 dB compression point of 8.5 dBm
- 3 dB of gain per output channel
- 24 dB isolation between output channels
- 75 Ω input and outputs
- Small package size
  - 12-lead, 3 mm × 3 mm lead frame chip scale package

APPLICATIONS

- Set-top boxes
- Home gateways
- CATV distribution systems
- Splitter modules
- Digital cable ready (DCR) TVs

GENERAL DESCRIPTION

The ADA4303-2 is a 75 Ω, two-output active splitter for use in applications where a lossless signal split is required. Typical applications include multituner digital set-top boxes, cable splitter modules, multituner/digital cable ready (DCR) televisions, and home gateways where traditional solutions require discrete passive splitter modules with separate fixed gain amplifiers.

The ADA4303-2 is a low cost alternative that simplifies designs and improves system performance by integrating a signal splitter element and a gain block into a single IC. The ADA4303-2 is available in a 12-lead chip scale package (LFCSP_VQ) and operates in the extended industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

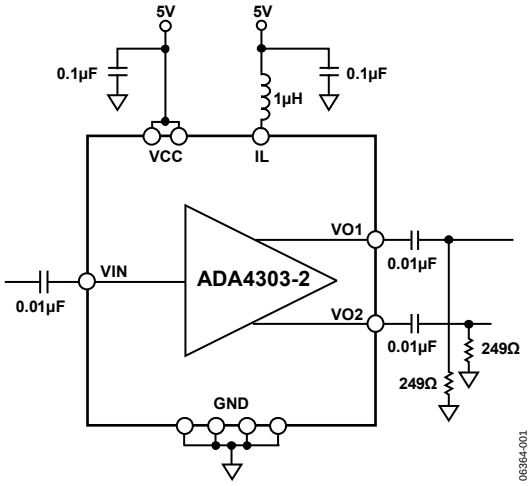


Figure 1.

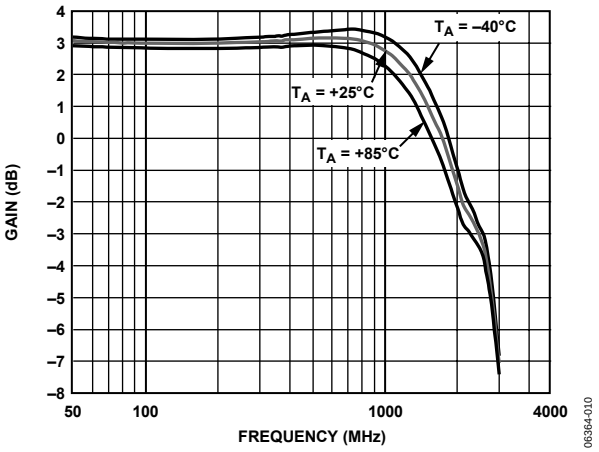


Figure 2. Gain (S21) vs. Frequency

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2006 Analog Devices, Inc. All rights reserved.**

TABLE OF CONTENTS

Features 1
Applications 1
Functional Block Diagram 1
General Description 1
Revision History 2
Specifications 3
Absolute Maximum Ratings 4
Thermal Resistance 4
ESD Caution 4
Pin Configuration and Function Descriptions 5
Typical Performance Characteristics 6
Applications 8
Circuit Description 8
Evaluation Board 8
RF Layout Considerations 8
Power Supply 8
Outline Dimensions 9
Ordering Guide 9

REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V, R_{IN} = R_L = 75 Ω, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth (−3 dB)			1700		MHz
Specified Frequency Range		54		865	MHz
Gain (S21)	f = 100 MHz	2.0	3.0	4.0	dB
1 dB Gain Flatness			1200		MHz
NOISE/DISTORTION PERFORMANCE					
Noise Figure	@ 54 MHz		4.0	4.3	dB
	@ 550 MHz		4.3	4.9	dB
	@ 865 MHz		4.4	5.1	dB
Output IP3	f_1 = 97.25 MHz, f_2 = 103.25 MHz		26.5		dBm
Output IP2	f_1 = 97.25 MHz, f_2 = 103.25 MHz		44.0		dBm
Composite Triple Beat (CTB)	135 Channels, 15 dBmV/Channel, f = 865 MHz		−72	−66	dBc
Composite Second-Order (CSO)	135 Channels, 15 dBmV/Channel, f = 865 MHz		−62	−60	dBc
Cross Modulation (CXM)	135 Channels, 15 dBmV/Channel, 100% modulation @ 15.75 kHz, f = 865 MHz		−68	−65	dBc
INPUT CHARACTERISTICS					
Input Return Loss (S11)	Referenced to 75 Ω				
	@ 54 MHz		−15.0	−11.5	dB
	@ 550 MHz		−19.5	−14.0	dB
	@ 865 MHz		−12.0	−7.5	dB
Output-to-Input Isolation (S12)	Any output, 54 MHz to 865 MHz				
	@ 54 MHz		−31.8	−29.0	dB
	@ 550 MHz		−32.0	−29.5	dB
	@ 865 MHz		−32.5	−30.0	dB
OUTPUT CHARACTERISTICS					
Output Return Loss (S22)	Referenced to 75 Ω				
	@ 54 MHz		−31.2	−23.0	dB
	@ 550 MHz		−19.4	−14.0	dB
	@ 865 MHz		−15.5	−11.0	dB
Output-to-Output Isolation	Between any two outputs, 54 MHz to 865 MHz				
	@ 54 MHz		−24.6		dB
	@ 550 MHz		−24.0		dB
	@ 865 MHz		−24.5		dB
1 dB Compression	Output referred, f = 100 MHz		8.5		dBm
POWER SUPPLY					
Nominal Supply Voltage		4.5	5.0	5.5	V
Quiescent Supply Current			78	90	mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for a device (including exposed pad) soldered to the circuit board.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
12-Lead LFCSP_VQ (exposed pad)	99.2	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4303-2 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4303-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through-holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 12-lead LFCSP_VQ (99.2°C/W) on a JEDEC standard 4-layer board.

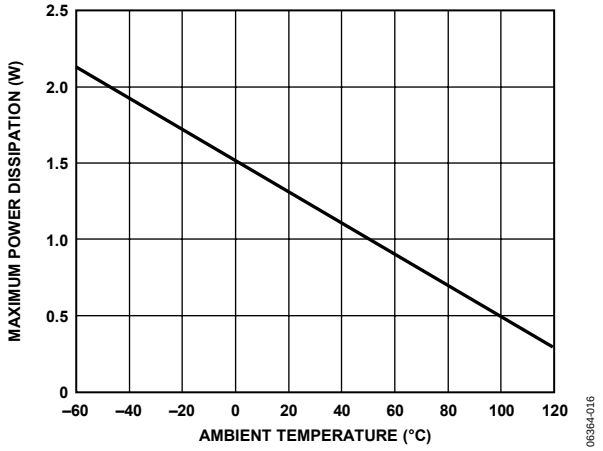


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

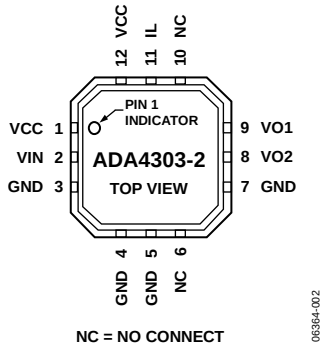


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC	Supply Pin
2	VIN	Input
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	NC	No Connection
7	GND	Ground
8	VO2	Output 2
9	VO1	Output 1
10	NC	No Connection
11	IL	Bias Pin
12	VCC	Supply Pin

TYPICAL PERFORMANCE CHARACTERISTICS

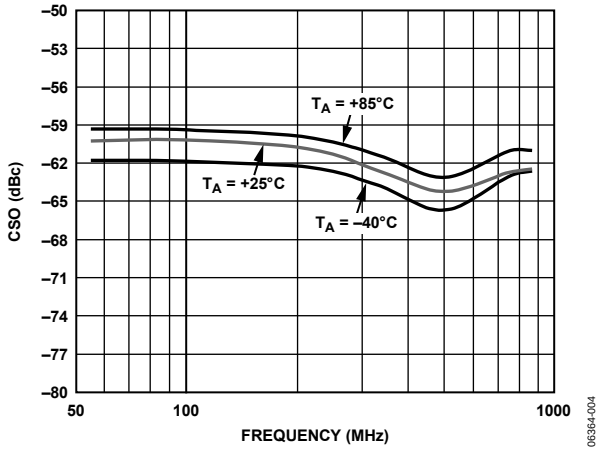


Figure 5. Composite Second-Order (CSO) vs. Frequency

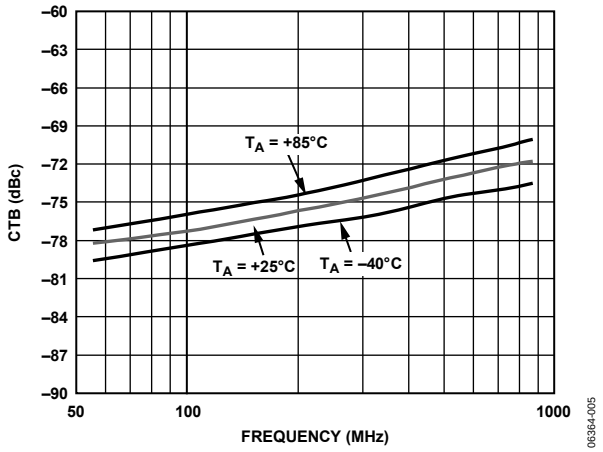


Figure 6. Composite Triple Beat (CTB) vs. Frequency

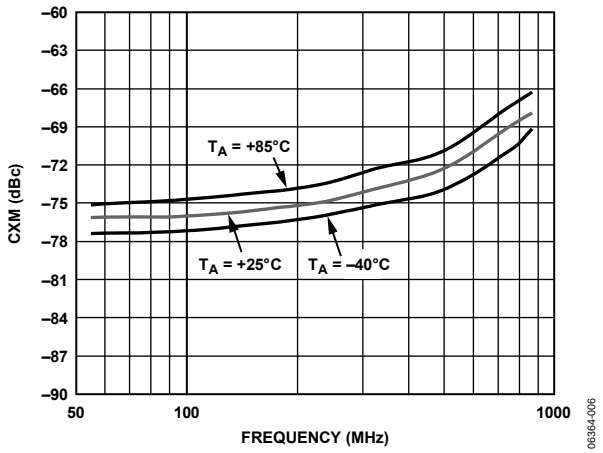


Figure 7. Cross Modulation (CXM) vs. Frequency

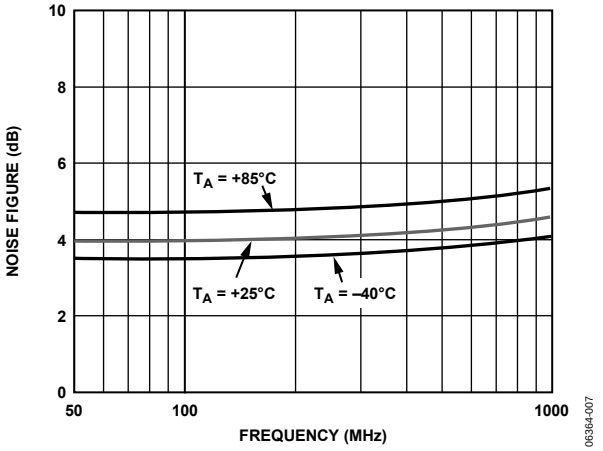


Figure 8. Noise Figure vs. Frequency

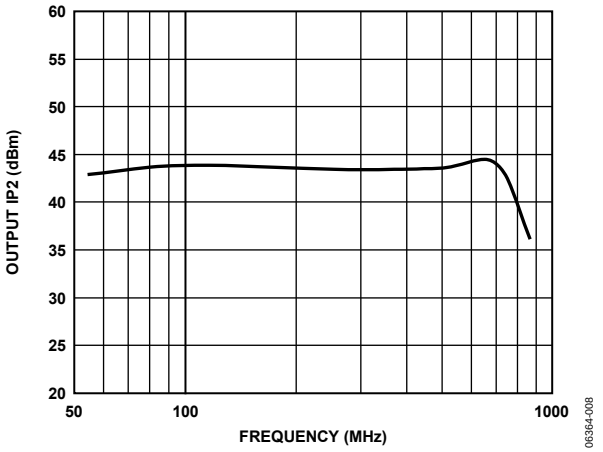


Figure 9. Output IP2 vs. Frequency

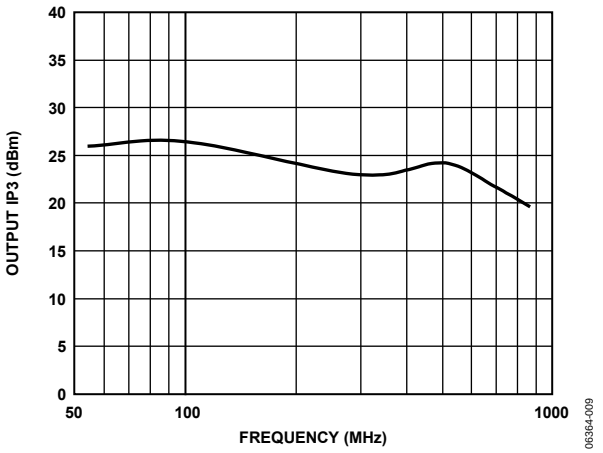


Figure 10. Output IP3 vs. Frequency

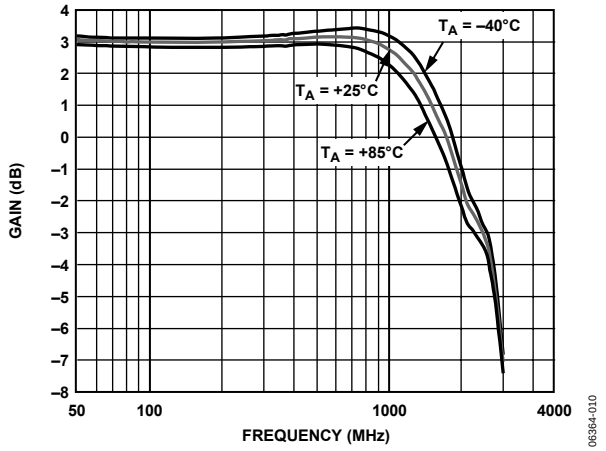


Figure 11. Gain (S21) vs. Frequency

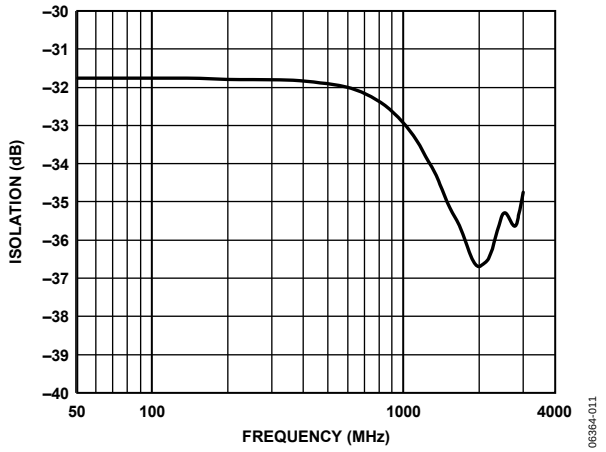


Figure 12. Output-to-Input Isolation (S12) vs. Frequency

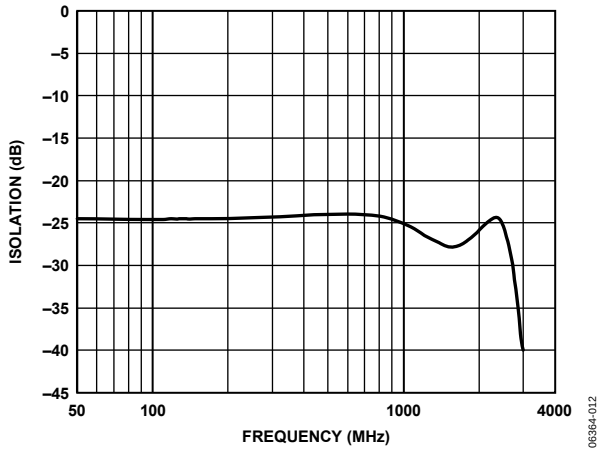


Figure 13. Output-to-Output Isolation vs. Frequency

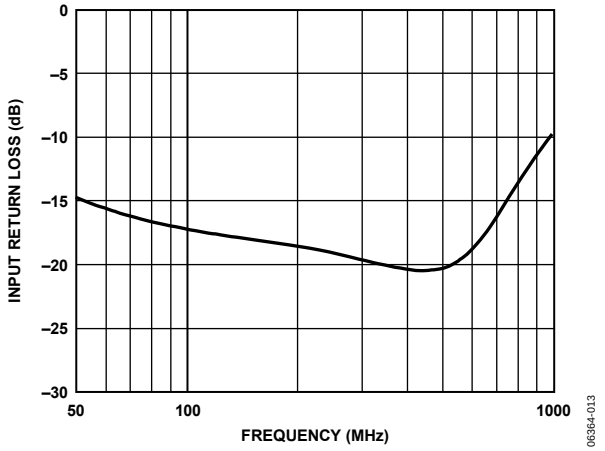


Figure 14. Input Return Loss (S11) vs. Frequency

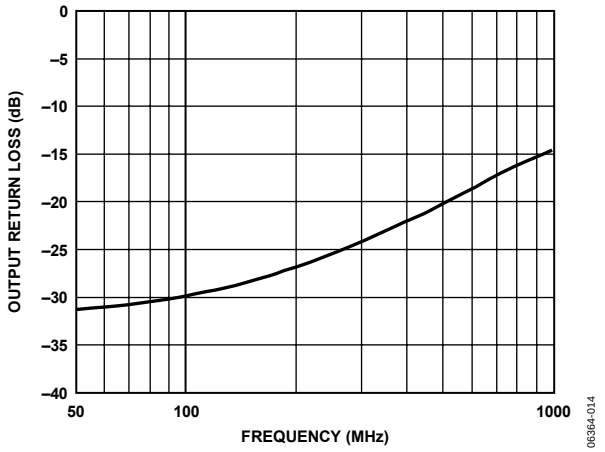


Figure 15. Output Return Loss (S22) vs. Frequency

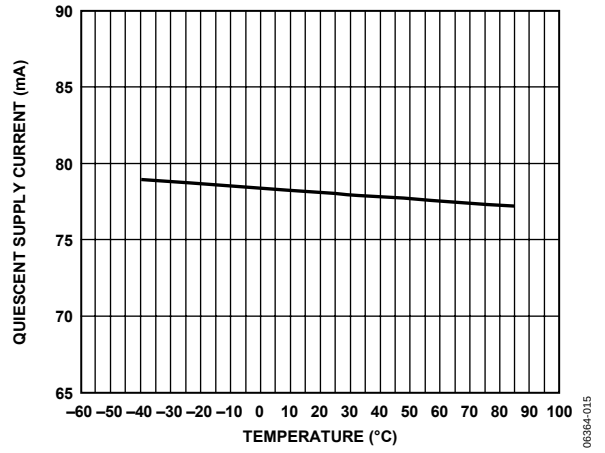


Figure 16. Quiescent Supply Current vs. Temperature

APPLICATIONS

The ADA4303-2 active splitter is primarily intended for use in the downstream path of television set-top boxes (STBs) that contain multiple tuners. It is typically located directly after the diplexer in a CATV customer premise unit. The ADA4303-2 provides a single-ended input and two single-ended outputs that allow the delivery of the RF signal to two different signal paths. These paths can include, but are not limited to, a main picture tuner, a picture-in-picture (PIP) tuner, an out-of-band (OOB) tuner, a digital video recorder (DVR), and a cable modem (CM).

The ADA4303-2 exhibits composite second-order (CSO) and composite triple beat (CTB) products that are −62 dBc and −72 dBc, respectively. The use of the SiGe process also allows the ADA4303-2 to achieve a noise figure (NF) of less than 4.5 dB.

CIRCUIT DESCRIPTION

The ADA4303-2 consists of a low noise buffer amplifier followed by a resistive power divider. This arrangement provides 3 dB of gain relative to the RF signal present at the input of the device. The input and each output must be properly matched to a 75 Ω environment for distortion and noise performance to match the data sheet specifications. In addition, to achieve the specified gain, a 1% 249 Ω resistor should be installed to ground on each output. AC coupling capacitors of 0.01 µF are recommended for the input and outputs.

A 1 µH RF choke (Coilcraft chip inductor 0805LS-102X) is required to correctly bias internal nodes of the ADA4303-2. It should be connected between the 5 V supply and IL (Pin 11).

EVALUATION BOARD

The ADA4303-2 evaluation board allows designers to assess the performance of the part in their particular applications. The board includes 75 Ω coaxial connectors and 75 Ω controlled-impedance signal traces that carry the input and output signals. Power (5 V) is applied to the red VCC loop connector, and ground is connected to the black GND loop connector.

The board has two 249 Ω resistors between each output and ground that set the gain of the overall circuit to 3 dB and improve output-to-output isolation. A schematic of the ADA4303-2 evaluation board is shown in Figure 17.

RF LAYOUT CONSIDERATIONS

Appropriate impedance matching techniques are mandatory when designing a circuit board for the ADA4303-2. Improper characteristic impedances on traces can cause reflections that can lead to poor linearity. The characteristic impedance of the signal trace from each output should be 75 Ω.

POWER SUPPLY

The 5 V supply should be applied to each of the VCC pins and RF choke via a low impedance power bus. The power bus should be decoupled to ground using a 10 µF tantalum capacitor and a 0.1 µF ceramic chip capacitor located close to the ADA4303-2. In addition, the VCC pins should be decoupled to ground with a 0.1 µF ceramic chip capacitor located as close to each of the pins as possible.

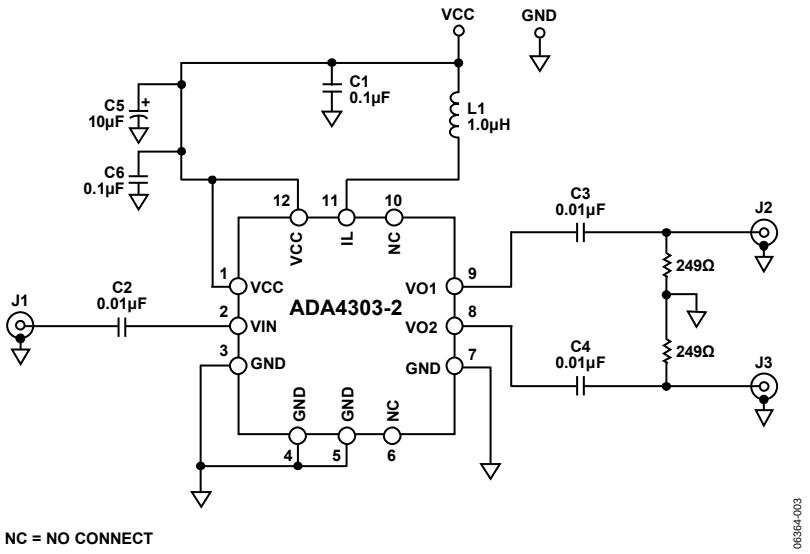
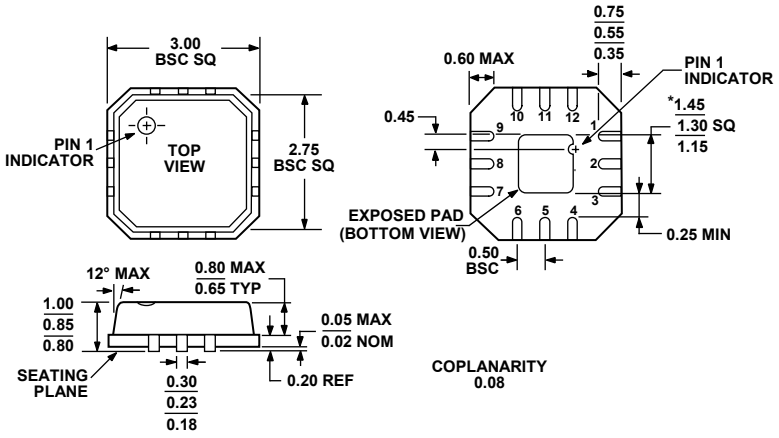


Figure 17. ADA4303-2 Evaluation Board Schematic

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-1
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 18. 12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-12-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4303-2ACPZ-RL[1]	−40°C to +85°C	12-Lead LFCSP_VQ	CP-12-1	5000	H0V
ADA4303-2ACPZ-R7[1]	−40°C to +85°C	12-Lead LFCSP_VQ	CP-12-1	1500	H0V
ADA4303-2ACPZ-R2[1]	−40°C to +85°C	12-Lead LFCSP_VQ	CP-12-1	250	H0V
ADA4303-2ACPZ-EB[1]		Evaluation Board			

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

©2006 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D06364-0-10/06(0)