High Performance 10-Bit Display Interface

AD9981

FEATURES

10-bit analog-to-digital converter
95 MSPS maximum conversion rate
9% or less p-p PLL clock jitter at 95 MSPS
Automated offset adjustment
2:1 input mux
Power-down via dedicated pin or serial register
4:4:4, 4:2:2, and DDR output format modes
Variable output drive strength
Odd/even field detection
External clock input
Regenerated Hsync output
Programmable output high impedance control
Hsyncs per Vsyncs counter
Pb-free package

APPLICATIONS

Advanced TVs
Plasma display panels
LCDTV
HDTV
RGB graphics processing
LCD monitors and projectors
Scan converters

FUNCTIONAL BLOCK DIAGRAM

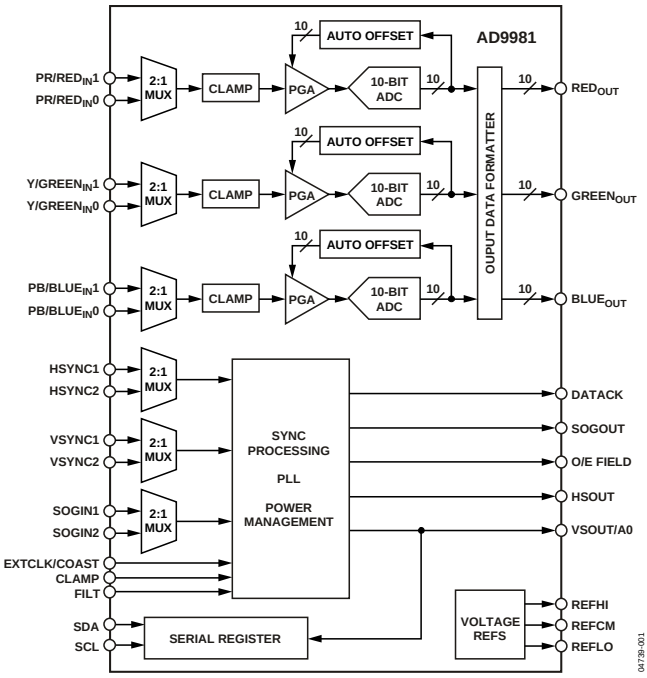

Figure 1.

GENERAL DESCRIPTION

The AD9981 is a complete, 10-bit, 95 MSPS, monolithic analog interface optimized for capturing YPbPr video and RGB graphics signals. Its 95 MSPS encode rate capability and full-power analog bandwidth of 200 MHz supports all HDTV video modes and graphics resolutions up to XGA (1024 × 768 at 85 Hz).

The AD9981 includes a 95 MHz triple ADC with an internal reference, a PLL, programmable gain, offset, and clamp controls. The user provides only 3.3 V and 1.8 V power supplies and an analog input. Three-state CMOS outputs may be powered from 1.8 V to 3.3 V.

The AD9981's on-chip PLL generates a sample clock from the three-level sync (for YPbPr video) or the horizontal sync (for RGB graphics). Sample clock output frequencies range from 10 MHz to 95 MHz. PLL clock jitter is 9% or less p-p typical at 95 MSPS.

With internal Coast generation, the PLL maintains its output frequency in the absence of sync input. A 32-step sampling clock phase adjustment is provided. Output data, sync, and clock phase relationships are maintained.

The auto-offset feature can be enabled to automatically restore the signal reference levels and to automatically calibrate out any offset differences between the three channels. The AD9981 also offers full sync processing for composite sync and sync-on-green applications. A clamp signal is generated internally or may be provided by the user through the CLAMP input pin.

Fabricated in an advanced CMOS process, the AD9981 is provided in a space-saving, 80-pin, Pb-free, LQFP surface mount plastic package. It is specified over the 0°C to +70°C temperature range.

Rev. 0
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REVISION HISTORY

1/05—Initial Version: Revision 0

ANALOG INTERFACE SPECIFICATIONS

V_D = 3.3 V, V_{DD} = 3.3 V, PV_D = 1.8 V, DAV_{DD} = 1.8 V, ADC clock = maximum conversion rate , full temperature range = 0°C to 70°C.

Table 1. Electrical Characteristics

			AD9981KSTZ-80[1]			AD9981KSTZ-95[2]			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION									
Number of Bits				10			10		Bits
LSB Size				0..098			0.098		% of full scale
DC ACCURACY									LSB
Differential Nonlinearity	25°C	I		0.3	1.0		0.3	1.0	LSB
80 MSPS Conversion Rate	Full	VI		0.4	1.8		0.4	1.8	
Differential Nonlinearity	25°C	I					1.3	2.75	LSB
95 MSPS Conversion Rate	Full	VI					1.75	5.4	
Integral Nonlinearity	25°C	I		±1.4	±3.75		±1.4	±3.75	LSB
80 MSPS Conversion Rate	Full	VI		±1.4	±5.0		±1.4	±5.0	
Integral Nonlinearity	25°C	I					±2.7	±4.75	LSB
95 MSPS Conversion Rate	Full	VI					±3.7	±8.6	
No Missing Codes	25°C	I		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		105			105		ppm/°C
Input Bias Current	25°C	V			1			1	µA
	Full	V			1			1	µA
Input Full-Scale Matching	Full	VI		1	9		1	10	% FS
Offset Adjustment Range	Full	VI		44			44		% FS
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	80			95			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Clock to Data Skew t_{SKEW}	Full	IV	−0.5		+2	−0.5		+2	ns
t_{BUFF}	Full	VI	4.7			4.7			µS
t_{STAH}	Full	VI	4.0			4.0			µS
t_{DHO}	Full	VI	0			0			µS
t_{DAL}	Full	VI	4.7			4.7			µS
t_{DAH}	Full	VI	4.0			4.0			µS
t_{DSU}	Full	VI	250			250			nS
t_{STASU}	Full	VI	4.7			4.7			µS
t_{STOSU}	Full	VI	4.0			4.0			µS
Maximum PLL Clock Rate	Full	VI	80			95			MHz
Minimum PLL Clock Rate	Full	IV			10			10	MHz
PLL Jitter	25°C	IV		750			980		ps p-p
	Full	IV							ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS[3]									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Current, High (I_{IH})	Full	V		−82			−82		µA
Input Current, Low (I_{IL})	Full	V		82			82		µA
Input Capacitance	25°C	V		2			2		pF

Parameter	Temp	Test Level	AD9981KSTZ-80[1] Min	Typ	Max	AD9981KSTZ-95[2] Min	Typ	Max	Unit
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_{DD} − 0.2			V_{DD} − 0.2			V
Output Voltage, Low (V_{OL})	Full	VI			0.2			0.1	V
Duty Cycle, DATACK	Full	IV		50			50		%
Output Coding				Binary			Binary		
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{DD} Supply Voltage	Full	IV	1.7	3.3	3.47	1.7	3.3	3.47	V
PV_D Supply Voltage	Full	IV	1.7	1.8	1.9	1.7	1.8	1.9	V
DAV_D Supply Voltage	Full	IV	1.7	1.8	1.9	1.7	1.8	1.9	V
I_D Supply Current (V_D)	25°C	V		233			205		mA
I_{DD} Supply Current (V_{DD})[4]	25°C	V		42			49		mA
IP_{VD} Supply Current (P_{VD})	25°C	V		11			8		mA
$IDAV_D$ Supply Current (DAV_D)	25°C	V		10			12		mA
Total Power Dissipation	Full	VI		953	1070		993	1114	mW
Power-Down Supply Current	Full	VI		18	27		18	28	mA
Power-Down Dissipation	Full	VI		55	81		55	88	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		200			200		MHz
Crosstalk	Full	V		60			60		dBc
THERMAL CHARACTERISTICS									
θ_{JC}, Junction-to-Case Thermal Resistance		V		16			16		°C/W
θ_{JA}, Junction-to-Ambient Thermal Resistance		V		35			35		°C/W

[1] Output drive strength = 0 was used for all 80 MHz parameters.
[2] Output drive strength = 1 was used for all 95 MHz parameters.
[3] Digital inputs are: HSYNC0, HSYNC1, VSYNC0, VSYNC1, SDA, SCL, EXTCLK, CLAMP, PWRDN, COAST
[4] DATACK load = 10 pF, data load = 5 pF

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_D	3.6 V
V_{DD}	3.6 V
PV_D	1.98 V
DAV_{DD}	1.98 V
Analog Inputs	V_D to 0.0 V
REFHI	V_D to 0.0 V
REFCM	V_D to 0.0 V
REFLO	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

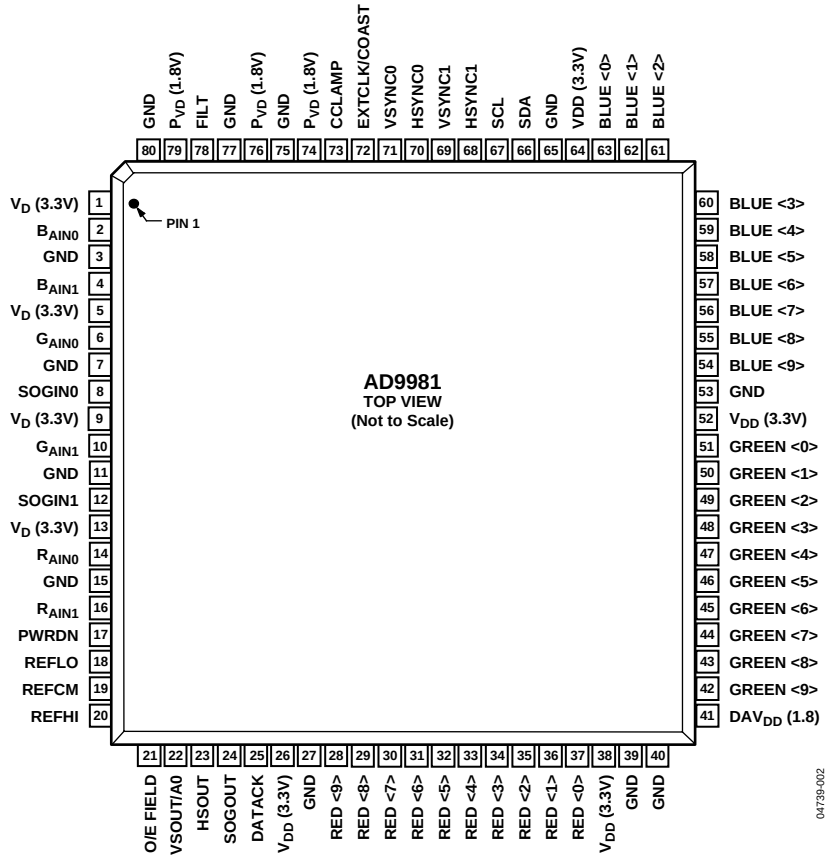


Figure 2. Top View (Pins Down)

Table 3. Complete Pinout List

Pin Type	Mnemonic	Function	Value	Pin No.
Inputs	R_{AIN0}	Channel 0 Analog Input for Converter R	0.0 V to 1.0 V	14
	R_{AIN1}	Channel 1 Analog Input for Converter R	0.0 V to 1.0 V	16
	G_{AIN0}	Channel 0 Analog Input for Converter G	0.0 V to 1.0 V	6
	G_{AIN1}	Channel 1 Analog Input for Converter G	0.0 V to 1.0 V	10
	B_{AIN0}	Channel 0 Analog Input for Converter B	0.0 V to 1.0 V	2
	B_{AIN1}	Channel 1 Analog Input for Converter B	0.0 V to 1.0 V	4
	HSYNC0	Horizontal Sync Input for Channel 0	3.3 V CMOS	70
	HSYNC1	Horizontal Sync Input for Channel 1	3.3 V CMOS	68
	VSYNC0	Vertical Sync Input for Channel 0	3.3 V CMOS	71
	VSYNC1	Vertical Sync Input for Channel 1	3.3 V CMOS	69
	SOGIN0	Input for Sync-on-Green Channel 0	0.0 V to 1.0 V	8
	SOGIN1	Input for Sync-on-Green Channel 1	0.0 V to 1.0 V	12
	EXTCK	External Clock Input	3.3 V CMOS	72[1]
	CLAMP	External Clamp Input Signal	3.3 V CMOS	73
	COAST	External PLL Coast Signal Input	3.3 V CMOS	72
	PWRDN	Power-Down Control	3.3 V CMOS	17
Outputs	RED [9:0]	Outputs of Converter R, Bit 9 is the MSB	3.3 V CMOS	28 to 37
	GREEN [9:0]	Outputs of Converter G, Bit 9 is the MSB	3.3 V CMOS	42 to 51
	BLUE [9:0]	Outputs of Converter B, Bit 9 is the MSB	3.3 V CMOS	54 to 63
	DATACK	Data Output Clock	3.3 V CMOS	25

Pin Type	Mnemonic	Function	Value	Pin No.
	HSOUT	Hsync Output Clock (Phase-Aligned with DATACK)	3.3 V CMOS	23
	VSOUT	Vsync Output Clock	3.3 V CMOS	22[2]
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	24
	O/E FIELD	Odd/Even Field Output	3.3V CMOS	21
References	FILT	Connection for External Filter Components for Internal PLL		78
	REFLO	Connection for External Capacitor for Input Amplifier		18
	REFCM	Connection for External Capacitor for Input Amplifier		19
	REFHI	Connection for External Capacitor for Input Amplifier		20
Power Supply	V_D	Analog Power Supply	3.3 V	1, 5, 9, 13
	V_{DD}	Output Power Supply	1.8 V or 3.3 V	26, 38, 52, 64
	PV_D	PLL Power Supply	1.8 V	74, 76, 79
	DAV_{DD}	Digital Logic Power Supply	1.8 V	41
	GND	Ground	0 V	3, 7, 11, 15, 27, 39, 40, 53, 65, 75, 77, 80
Control	SDA	Serial Port Data I/O	3.3 V CMOS	66
	SCL	Serial Port Data Clock (100 kHz maximum)	3.3 V CMOS	67
	A0	Serial Port Address Input	3.3 V CMOS	22

[1] EXTCLK and COAST share the same pin.
[2] VSOUT and A0 share the same pin.

Table 4. Pin Function Descriptions

Pin	Description
INPUTS	
RAIN0	Analog Input for the Red Channel 0.
GAIN0	Analog Input for the Green Channel 0.
BAIN0	Analog Input for the Blue Channel 0.
RAIN1	Analog Input for the Red Channel 1.
GAIN1	Analog Input for the Green Channel 1.
BAIN1	Analog Input for the Blue Channel 1. High impedance inputs that accept the red, green, and blue channel graphics signals, respectively. The three channels are identical and can be used for any colors, but colors are assigned for convenient reference. They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.
HSYNC0	Horizontal Sync Input Channel 0.
HSYNC1	Horizontal Sync Input Channel 1. These inputs receive a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin can be automatically determined by the chip or manually controlled by Serial Register 0x12, Bits [5:4] (Hsync polarity). Only the leading edge of Hsync is used by the PLL; the trailing edge is used in clamp timing. When Hsync polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity.
VSYNC0	Vertical Sync Input Channel 0.
VSYNC1	Vertical Sync Input Channel 1. These are the inputs for vertical sync and provide timing information for generation of the field (odd/even) and internal Coast generation. The logic sense of this pin can be automatically determined by the chip or manually controlled by Serial Register 0x14, Bits [5:4] (Vsync polarity).
SOGIN0	Sync-on-Green Input Channel 0.
SOGIN1	Sync-on-Green Input Channel 1. These inputs are provided to assist with processing signals with embedded sync, typically on the green channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 8 mV steps to any voltage between 8 mV and 256 mV above the negative peak of the input signal. The default voltage threshold is 128 mV. When connected to an ac-coupled graphics signal with embedded sync, it produces a noninverting digital output on SOGOUT. This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal for Hsync processing. When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.
CLAMP	External Clamp Input (Optional). This logic input may be used to define the time during which the input signal is clamped to ground or midscale. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting the control bit clamp function to 1, (Register 0x18, Bit 4; default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin can be automatically determined by the chip or controlled by clamp polarity Register 0x1B, Bits [7:6]. When not used, this pin may be left unconnected (there is an internal pull-down resistor) and the clamp function programmed to 0.
EXTCLK/COAST	Coast Input to Clock Generator (Optional). This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce Hsync pulses during the vertical interval. The Coast signal is generally *not* required for PC-generated signals. The logic sense of this pin can be determined automatically or controlled by Coast polarity (Register 0x18, Bits [7:6]). When not used and EXTCLK is not used, this pin may be grounded and Coast polarity programmed to 1. Input Coast polarity defaults to1 at power-up. This pin is shared with the EXTCLK function, which does not affect Coast functionality. For more details on EXTCLK, see the description in this section.
EXTCLK/COAST	External Clock. This allows the insertion of an external clock source rather than the internally generated, PLL locked clock. EXTCLK is enabled by programming Register 0x03, Bit 2 to 1. This pin is shared with the Coast function, which does not affect EXTCLK functionality. For more details on Coast, see the above description in this section.
PWRDN	Power-Down Control This pin can be used along with Register 0x1E, Bit 3 for manual power-down control. If manual power-down control is selected (Register 0x1E, Bit 4) and this pin is not used, it is recommended to set the pin polarity (Register 0x1E, Bit 2) to active high and hardwire this pin to ground with a 10 kΩ resistor.

Pin	Description
REFLO REFCM REFHI	Input Amplifier Reference. REFLO and REFHI are connected together through a 10 µF capacitor; REFCM is connected through a 10 µF capacitor to ground. These are used for stability in the input PGA (programmable gain amplifier) circuitry. See Figure 4.
FILT	External Filter Connection. For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 5to this pin. For optimal performance, minimize noise and parasitics on this node. For more information, see the PCB Layout Recommendations section.
OUTPUTS	
HSOUT	Horizontal Sync Output. A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATACK and Data Output, data timing with respect to Hsync can always be determined.
VSOUT/A0	Vertical Sync Output. Pin shared with A0, serial port address. This can be either a separated Vsync from a composite signal or a direct pass through of the Vsync signal. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes can be set by the graphics transmitter or the duration can be set by Register 0x14 and Register 0x15. This pin is shared with the A0 function, which does not affect Vsync Output functionality. For more details on A0, see the description in the Serial Control Port section.
SOGOUT	Sync-On-Green Slicer Output. This pin outputs one of four possible signals (controlled by Register 0x1D, Bits [1:0]): raw SOG, raw Hsync, regenerated Hsync from the filter, or the filtered Hsync. See the sync processing block diagram (see Figure 8) to view how this pin is connected. Other than slicing off SOG, the output from this pin gets no other additional processing on the AD9981. Vsync separation is performed via the sync separator.
O/E FIELD	Odd/Even Field Bit for Interlaced Video. This output will identify whether the current field (in an interlaced signal) is odd or even.
SERIAL PORT	
SDA	Serial Port Data I/O.
SCL	Serial Port Data Clock.
VSOUT/A0	Serial Port Address Input 0. Pin shared with VSOUT. This pin selects the LSB of the serial port device address, allowing two Analog Devices parts to be on the same serial bus. A high impedance external pull-up resistor enables this pin to be read at power-up as 1, or a high impedance, external pull-down resistor enables this pin to be read at power-up as a 0 and not interfere with the VSOUT functionality. For more details on VSOUT, see the Data Outputs section in this table.
DATA OUTPUTS	
RED [9:0]	Data Output, Red Channel.
GREEN [9:0]	Data Output, Green Channel.
BLUE [9:0]	Data Output, Blue Channel. The main data outputs. Bit 9 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the phase register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained.
DATA CLOCK OUTPUT	
DATACK	Data Clock Output. This is the main clock output signal used to strobe the output data and HSOUT into external logic. Four possible output clocks can be selected with Register 0x20, Bits [7:6]. Three of these are related to the pixel clock (pixel clock, 90° phase-shifted pixel clock and 2× frequency pixel clock). They are produced either by the internal PLL clock generator or EXTCLK and are synchronous with the pixel sampling clock. The fourth option for the data clock output is an internally generated 40 MHz clock. The sampling time of the internal pixel clock can be changed by adjusting the phase register (Register 0x04). When this is changed, the pixel related DATACK timing is also shifted. The Data, DATACK, and HSOUT outputs are all moved so that the timing relationship among the signals is maintained.

Pin	Description
POWER SUPPLY	
V_D (3.3 V)	Main Power Supply. These pins supply power to the main elements of the circuit. They should be as quiet and filtered as possible.
V_{DD} (1.8 V–3.3 V)	Digital Output Power Supply. A large number of output pins (up to 35) switching at high speed (up to 95 MHz) generate a lot of power supply transients (noise). These supply pins are identified separately from the V_D pins, so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9981 is interfacing with lower voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 1.8 V) for compatibility.
PV_D (1.8 V)	Clock Generator Power Supply. The most sensitive portion of the AD9981 is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins.
DAV_{DD} (1.8 V)	Digital Input Power Supply. This supplies power to the digital logic.
GND	Ground. The ground return for all circuitry on-chip. It is recommended that the AD9981 be assembled on a single solid ground plane, with careful attention to ground current paths.

DESIGN GUIDE

GENERAL DESCRIPTION

The AD9981 is a fully integrated solution for capturing analog RGB or YPbPr signals and digitizing them for display on advanced TVs, flat panel monitors, projectors, and other types of digital displays. Implemented in a high-performance CMOS process, the interface can capture signals with pixel rates of up to 95 MHz.

The AD9981 includes all necessary input buffering, signal DC restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a two-wire serial interface ($I^2C^®$). Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of less than 900 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

DIGITAL INPUTS

All digital inputs on the AD9981 operate to 3.3 V CMOS levels. The following digital inputs are 5 V tolerant (Applying 5 V to them will not cause any damage.): HSYNC0, HSYNC1, VSYNC0, VSYNC1, SOGIN0, SOGIN1, SDA, SCL and CLAMP.

INPUT SIGNAL HANDLING

The AD9981 has six high-impedance analog input pins for the red, green, and blue channels. They accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board with a DVI-I connector, a 15-pin D connector, or RCA connectors. The AD9981 should be located as close as possible to the input connector. Signals should be routed using matched-impedance traces (normally 75 Ω) to the IC input pins.

At the input pins the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9981 inputs through 47 nF capacitors. These capacitors form part of the DC restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The wide bandwidth inputs of the AD9981 (200 MHz) can continuously track the input signal as it moves from one pixel level to the next and can digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0-High Speed, Signal Chip Bead Inductor in the circuit shown in Figure 3 gives good results in most applications.

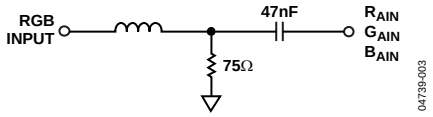


Figure 3. Analog Input Interface Circuit

HSYNC AND VSYNC INPUTS

The interface also accepts Hsync and Vsync signals, which are used to generate the pixel clock, clamp timing, Coast and field information. These can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic; however, it is tolerant of 5 V logic signals.

OUTPUT SIGNAL HANDLING

The digital outputs are designed to operate from 1.8 V to 3.3 V (V_{DD}).

CLAMPING

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board ADCs.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at 300 mV; then white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9981.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced that results in the ADC producing a black output (Code 0x00) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most PC graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. Because the input is not at black level at this time, it is important to avoid clamping during Hsync. Fortunately, there is virtually always a period following Hsync, called the 'back porch', where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time with clamp source (Register 0x18, Bit 4) = 1. The polarity of this signal is set by the clamp polarity bit (Register 0x1B, Bits [7:6]).

A simpler method of clamp timing employs the AD9981 internal clamp timing generator. The clamp placement register (Register 0x19) is programmed with the number of pixel periods that should pass after the trailing edge of Hsync before clamping starts. A second register, clamp duration, (Register 0x1A) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 0x04 (providing 4 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 0x28 (giving the clamp 40 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within 1 LSB in 30 lines with a clamp duration of 20 pixel periods on a 85 Hz XGA signal.

YPbPr Clamping

YPbPr graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) of color difference signals is at the midpoint of the video signal rather than at the bottom. The three inputs are composed of luminance (Y) and color difference (Pb and Pr) signals. For color difference signals it is necessary to clamp to the midscale range of the ADC range (512) rather than to the bottom of the ADC range (0), while the Y channel is clamped to ground.

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be independently clamped to either midscale or ground. These bits are located in Register 0x18, Bits [3:1]. The midscale reference voltage is internally generated for each converter.

GAIN AND OFFSET CONTROL

The AD9981 contains three programmable gain amplifiers (PGAs), one for each of the three analog inputs. The range of the PGA is sufficient to accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The gain is set in three 9-bit registers (red gain [0x05, 0x06], green gain [0x07, 0x08], blue gain [0x09, 0x0A]). For each of these registers, a gain setting of 0 corresponds to the highest gain, while a gain setting of 511 corresponds to the lowest gain. Note that increasing the gain setting results in an image with less contrast.

The offset control shifts the analog input, resulting in a change in brightness. Three 11-bit registers (red offset [0x0B, 0x0C], green offset [0x0D, 0x0E], blue offset [0x0F, 0x10]) provide independent settings for each channel. Note that the function of the offset register depends on whether auto-offset is enabled (Register 0x1B, Bit 5).

If manual offset is used, nine bits of the offset registers (for the red channel Register 0x0B, Bits [6:0] plus Register 0x0C, Bits [7:6]) control the absolute offset added to the channel. The offset control provides ±255 LSBs of adjustment range, with one LSB of offset corresponding to one LSB of output code.

Automatic Offset

In addition to the manual offset adjustment mode, the AD9981 also includes circuitry to automatically calibrate the offset for each channel. By monitoring the output of each ADC during the back porch of the input signals, the AD9981 can self-adjust to eliminate any offset errors in its own ADC channels and any offset errors present on the incoming graphics or video signals.

To activate the auto-offset mode, set Register 0x1B, Bit 5 to 1. Next, the target code registers (0x0B through 0x10) must be programmed. The values programmed into the target code registers should be the output code desired from the AD9981 during the back porch reference time. For example, for RGB signals, all three registers would normally be programmed to Code 1, while for YPbPr signals the green (Y) channel is normally set to Code 1 and the blue and red channels (Pb and Pr) are set to 512. The target code registers have 11 bits per channel and are in twos complement format. This allows any value between –1024 and +1023 to be programmed. Although any value in this range can be programmed, the AD9981's offset range may not be able to reach every value. Intended target code values range from (but are not limited to) –160 to –1 and +1 to +160 when ground clamping, and +350 to +670 when midscale clamping. Note that a target code of 0 is not valid.

Negative target codes are included in order to duplicate a feature that is present with manual offset adjustment. The benefit that is being mimicked is the ability to easily adjust brightness on a display. By setting the target code to a value that does not correspond to the ideal ADC range, the end result is an image that is either brighter or darker. A target code higher than ideal results in a brighter image, while a target code lower than ideal results in a darker image.

The ability to program a target code gives a large degree of freedom and flexibility. While in most cases all channels are set to either 1 or 512, the flexibility to select other values allows the possibility of inserting intentional skews between channels. It also allows the ADC range to be skewed so that voltages outside of the normal range can be digitized. For example, setting the target code to 40 allows the sync tip, which is normally below black level, to be digitized and evaluated.

The internal logic for the auto-offset circuit requires 16 data clock cycles to perform its function. This operation is executed immediately after the clamping pulse. Therefore, it is important to end the clamping pulse signal at least 16 data clock cycles before active video. This is true whether using the AD9981's internal clamp circuit or an external clamp signal. The auto-offset function can be programmed to run continuously or on a one-time basis (see auto-offset hold, Register 0x2C, Bit 4). In continuous mode, the update frequency can be programmed (Register 0x1B, Bits [4:3]). Continuous operation with updates every 64 Hsyncs is recommended.

A guideline for basic auto-offset operation is shown in Table 5 and Table 6.

Table 5. RGB Auto-Offset Register Settings

Register	Value	Comments
0x0B	0x00	Sets red target to 4
0x0C	0x80	Must be written
0x0D	0x00	Sets green target to 4
0x0E	0x80	Must be written
0x0F	0x00	Sets blue target to 4
0x10	0x80	Must be written
0x18, Bits [3:1]	000	Sets red, green, and blue channels to ground clamp
0x1B, Bit [5:3]	110	Selects update rate and enables auto-offset.

Table 6. PbPr Auto-Offset Register Settings

Register	Value	Comments
0x0B	0x40	Sets Pr (red) target to 512
0x0C	0x00	Must be written
0x0D	0x00	Sets Y (green) target to 4
0x0E	0x80	Must be written
0x0F	0x40	Sets Pb (blue) target to 512
0x10	0x00	Must be written
0x18 Bits [3:1]	101	Sets Pb, Pr to midscale clamp and Y to ground clamp
0x1B, Bit [5:3]	110	Selects update rate and enables auto-offset.

Sync-on-Green

The sync-on-green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level to a programmable (Register 0x1D, Bits [7:3]) level (typically 128 mV) above the negative peak. The sync-on-green input must be ac-coupled to the green analog input through its own capacitor. The value of the capacitor must be 1 nF ±20%. If sync-on-green is not used, this connection is not required. The sync-on-green signal always has negative polarity.

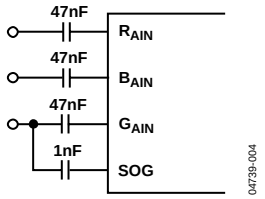


Figure 4. Typical Input Configuration

Reference Bypassing

REFLO and REFHI are connected to each other by a 10 µF capacitor. REFCM is connected to ground by a 10 µF capacitor. These references are used by the input PGA circuitry.

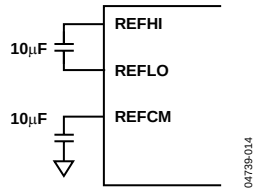


Figure 5. Input Amplifier Reference Capacitors

Clock Generation

A PLL is used to generate the pixel clock. The Hsync input provides a reference frequency to the PLL. A voltage-controlled oscillator (VCO) generates a much higher pixel clock frequency. The pixel clock is divided by the PLL divide value (Register 0x01 and Register 0x02) and phase-compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period when the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (see Figure 6). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter and the stable pixel time also becomes shorter.

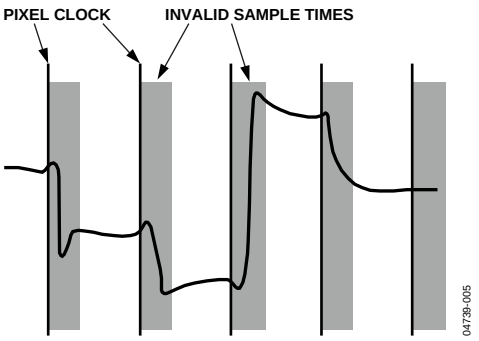


Figure 6. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined and must also be subtracted from the stable pixel time. Considerable care has been taken in the design of the AD9981's clock generation circuit to minimize jitter. The clock jitter of the AD9981 is 9% or less of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is illustrated in Figure 7. Recommended settings of the VCO range and charge pump current for VESA standard display modes are listed in Table 9.

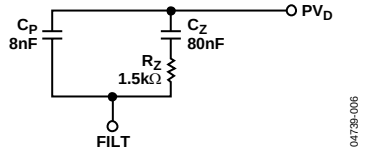


Figure 7. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are

1. The 12-Bit Divisor Register. The input Hsync frequencies can accommodate any Hsync as long as the product of the Hsync and the PLL divisor falls within the operating range of the VCO. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 10 MHz to 95 MHz. The divisor register controls the exact multiplication factor. This register may be set to any value between 2 and 4095 as long as the output frequency is within range.

2. The 2-Bit VCO Range Register. To improve the noise performance of the AD9981, the VCO operating frequency range is divided into four overlapping regions. The VCO range register sets this operating range. The frequency ranges for the four regions are shown in Table 7.

Table 7. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)	KVCO Gain (MHz/V)
0	0	10–21	150
0	1	21–42	150
1	0	42–84	150
1	1	84-95	150

3. The 3-Bit Charge Pump Current Register. This register varies the current that drives the low-pass loop filter. The possible current values are listed in Table 8.

Table 8. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

4. The 5-Bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The phase adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin. Phase adjust is still available if an external pixel clock is used. The COAST pin or the internal Coast is used to allow the PLL to continue to run at the same frequency in the absence of the incoming Hsync signal or during disturbances in Hsync (such as from equalization pulses). This may be used during the vertical sync period or at any other time that the Hsync signal is unavailable. The polarity of the Coast signal may be set through the Coast polarity register (Register 0x18, Bits [6:5]). Also, the polarity of the Hsync signal may be set through the Hsync polarity register (Register 0x12, Bits [5:4]). For both Hsync and Coast, a value of 1 is active high. The internal Coast function is driven off the Vsync signal, which is typically a time when Hsync signals may be disrupted with extra equalization pulses.

Table 9. Recommended VCO Range and Charge Pump and Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate (Hz)	Horizontal Frequency (kHz)	Pixel Rate (MHz)	PLL Divider	VCORNGE	Current
VGA	640 × 480	60	31.500	25.175	800	01	100
		72	37.700	31.500	832	01	100
		75	37.500	31.500	840	01	100
		85	43.300	36.000	832	01	101
SVGA	800 × 600	56	35.100	36.000	1024	01	101
		60	37.900	40.000	1056	01	100
		72	48.100	50.000	1040	10	100
		75	46.900	49.500	1056	10	100
		85	53.700	56.250	1048	10	100
XGA	1024 × 768	60	48.400	65.000	1344	10	101
		70	56.500	75.000	1328	10	110
		75	60.000	78.750	1312	10	110
		80	64.000	85.500	1336	11	100
		85	68.300	94.500	1376	11	100
TV	480i	30	15.750	13.510	858	00	100
	480p	60	31.470	27.000	858	01	100
	576i	30	15.625	13.500	864	00	100
	576p	60	31.250	27.000	864	01	100
	720p	60	45.000	74.250	1650	10	101
	1035i	30	33.750	74.250	2200	10	101
	1080i	60	33.750	74.250	2200	10	101

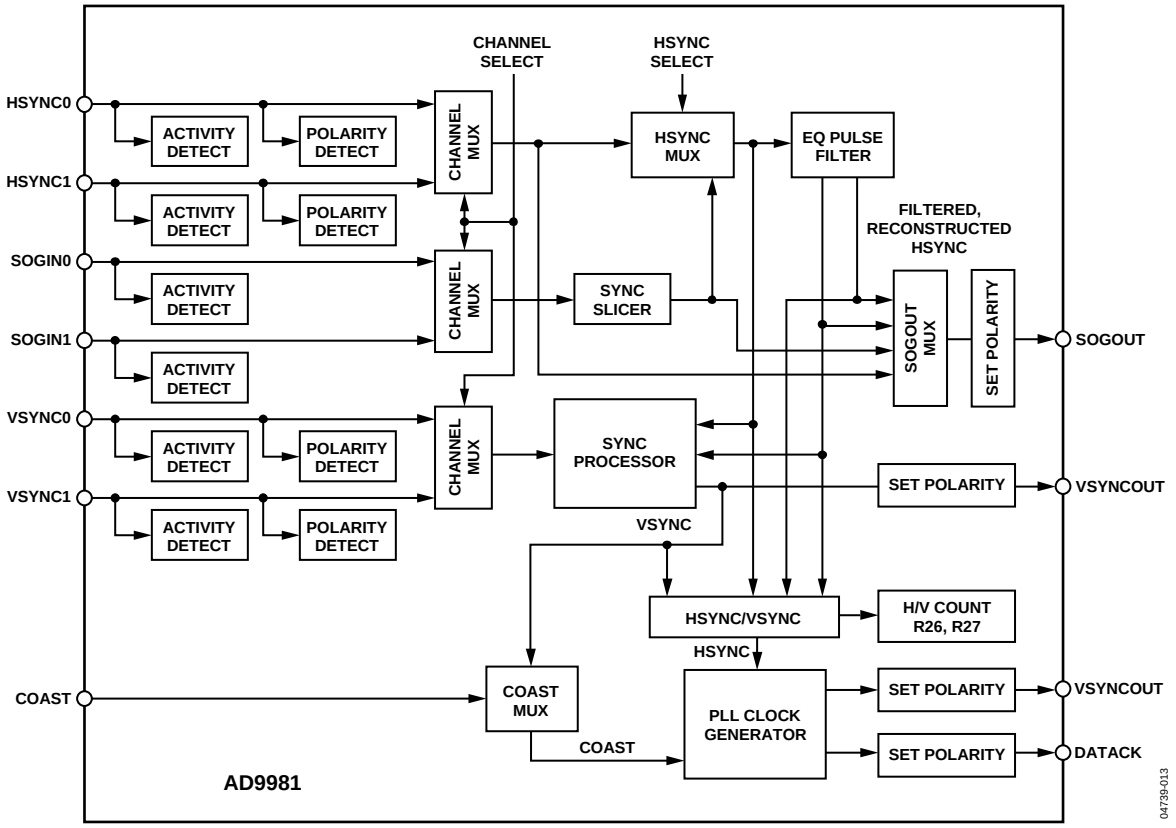


Figure 8. Sync Processing Block Diagram

Sync Processing

The inputs of the sync processing section of the AD9981 are combinations of digital Hsyncs and Vsyncs, analog sync-on-green, or sync-on-Y signals, and an optional external Coast signal. From these signals it generates a precise, jitter-free (9% or less at 95 MHz) clock from its PLL; an odd-/even-field signal; Hsync and Vsync out signals; a count of Hsyncs per Vsync; and a programmable SOG output. The main sync processing blocks are the sync slicer, sync separator, Hsync filter, Hsync regenerator, Vsync filter, and Coast generator.

The sync slicer extracts the sync signal from the green graphics or luminance video signal that is connected to the SOGIN input and outputs a digital composite sync. The sync separator's task is to extract Vsync from the composite sync signal, which can come from either the sync slicer or the Hsync input. The Hsync filter is used to eliminate any extraneous pulses from the Hsync or SOGIN inputs, outputting a clean, low-jitter signal that is appropriate for mode detection and clock generation. The Hsync regenerator is used to recreate a clean, although not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync. The Vsync filter is used to eliminate spurious Vsyncs, maintain a stable timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output. The Coast generator creates a robust Coast signal that allows the PLL to maintain its frequency in the absence of Hsync pulses.

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the green graphics or luminance video signal that is connected to the SOGIN input. The sync signal is extracted in a two step process. First, the SOG input is clamped to its negative peak, (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level (set by Register 0x1D, Bits [7:3]), but nominally 0.128 V above the clamped level. The sync slicer output is a digital composite sync signal containing both Hsync and Vsync information (see Figure 9).

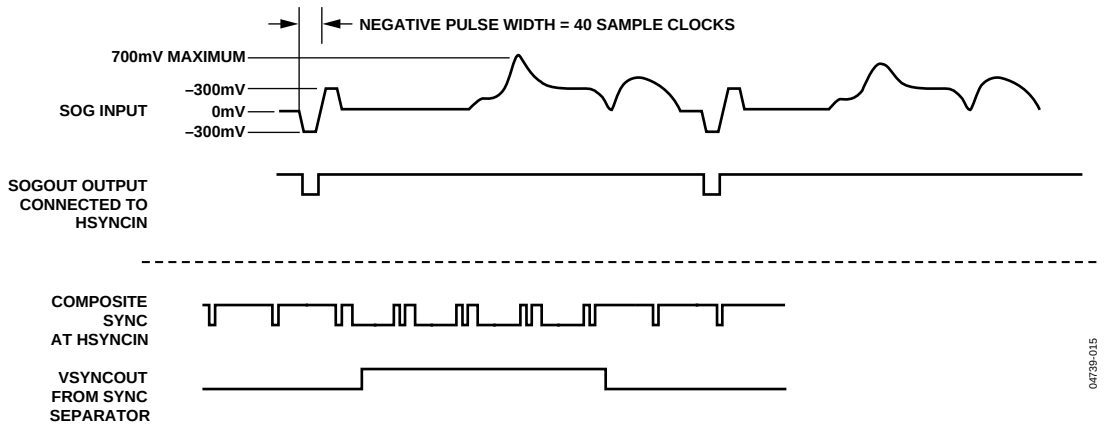


Figure 9. Sync Slicer and Sync Separator Output

Sync Separator

As part of sync processing, the sync separator's task is to extract Vsync from the composite sync signal. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. By using a digital low-pass filter and a digital comparator, it rejects pulses with small durations (such as Hsyncs and equalization pulses) and only passes pulses with large durations, such as Vsync (see Figure 9).

The threshold of the digital comparator is programmable for maximum flexibility. To program the threshold duration, write a value (N) to Register 0x11. The resulting pulse width is N × 200 ns. So, if N = 5 the digital comparator threshold is 1 µs. Any pulse less than 1 µs is rejected, while any pulse greater than 1 µs passes through.

There are two things to keep in mind when using the sync separator. First, the resulting clean Vsync output is delayed from the original Vsync by a duration equal to the digital comparator threshold (N × 200 ns). Second, there is some variability to the 200 ns multiplier value. The maximum variability over all operating conditions is ±20% (160 ns to 240 ns). Since normal Vsync and Hsync pulse widths differ by a factor of about 500 or more, the 20% variability is not an issue.

Hsync Filter and Regenerator

The Hsync filter is used to eliminate any extraneous pulses from the Hsync or SOGIN inputs, outputting a clean, low-jitter signal that is appropriate for mode detection and clock generation. The Hsync regenerator is used to recreate a clean, although not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync. The Hsync regenerator has a high degree of tolerance to extraneous and missing pulses on the Hsync input, but is not appropriate for use by the PLL in creating the pixel clock due to jitter.

The Hsync regenerator runs automatically and requires no setup to operate. The Hsync filter requires the setting up of a filter window. The filter window sets a periodic window of time around the regenerated Hsync leading edge where valid Hsyncs are allowed to occur. The general idea is that extraneous pulses on the sync input occur outside of this filter window and thus are filtered out. In order to set the filter window timing, program a value (x) into Register 0x23. The resulting filter window time is ±x times 25 ns around the regenerated Hsync leading edge. Just as for the sync separator threshold multiplier, allow a ±20% variance in the 25 ns multiplier to account for all operating conditions (20 ns to 30 ns range).

A second output from the Hsync filter is a status bit (0x25, Bit 1) that tells whether extraneous pulses were present on the incoming sync signal or not. Many times extraneous pulses are included for copy protection purposes, so this status bit can be used to detect that.

The filtered Hsync (rather than the raw Hsync/SOGIN signal) for pixel clock generation by the PLL is controlled by Register 0x20, Bit 2. The regenerated Hsync (rather than the raw Hsync/ SOGIN signal) for the sync processing is controlled by Register 0x20, Bit 1. Use of the filtered Hsync and regenerated Hsync is recommended. See Figure 10 for an illustration of a filtered Hsync.

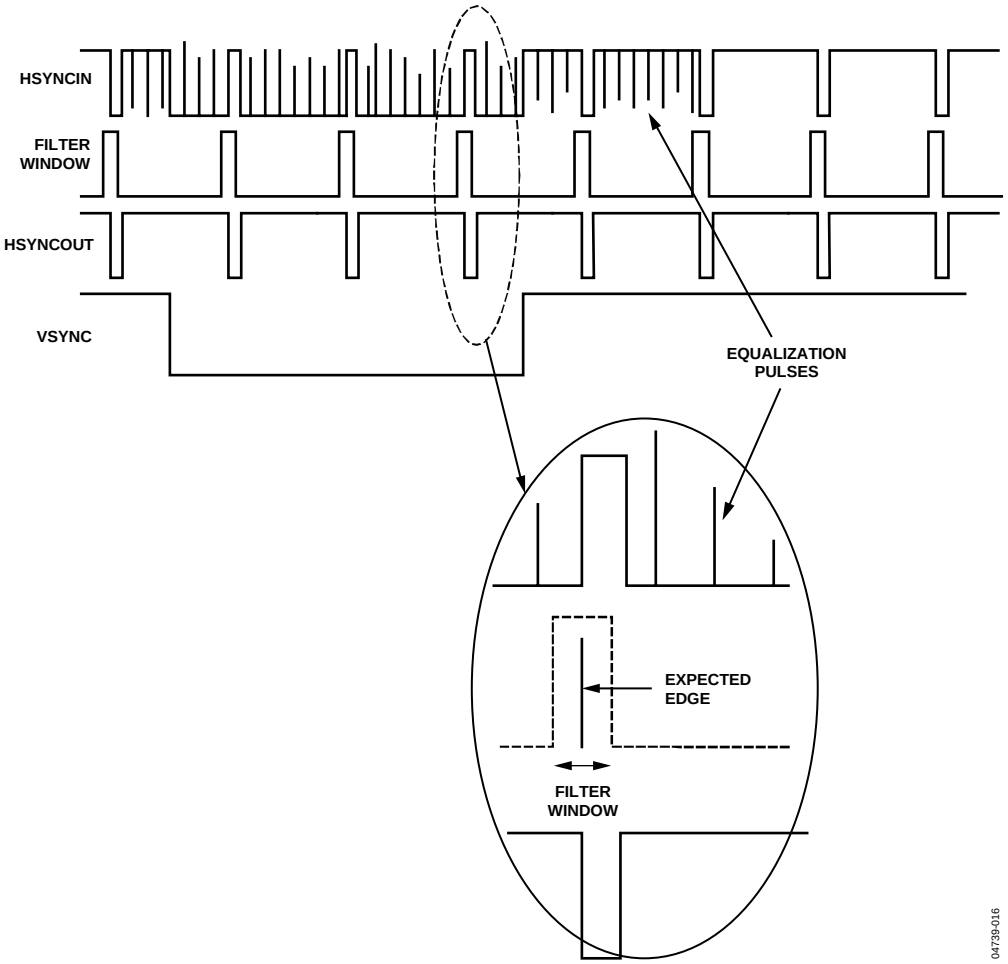


Figure 10. Sync Processing Filter

Vsync Filter and Odd/Even Fields

The Vsync filter is used to eliminate spurious Vsyncs, maintain a stable timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output.

The filter works by examining the placement of Vsync with respect to Hsync and if necessary shifting it in time slightly. The goal is to keep the Vsync and Hsync leading edges from switching at the same time, thus eliminating confusion as to when the first line of a frame occurs. Register 0x14, Bit 2 enables the Vsync filter. Use of the Vsync filter is recommended for all cases, including interlaced video, and is required when using the Hsyncs per Vsync counter. Figure 12 illustrates even/odd field determination in two situations.

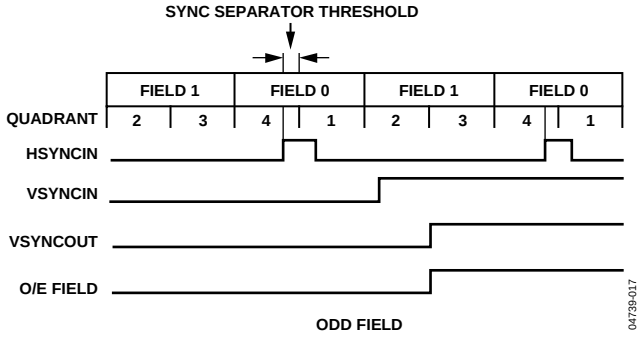


Figure 11.

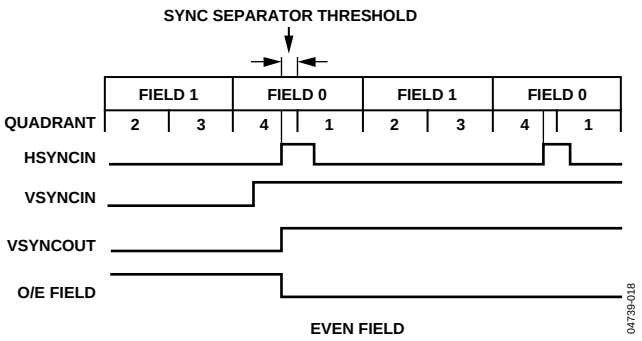


Figure 12. Vsync Filter—Odd/Even

Power Management

To meet display requirements for low standby power, the AD9981 includes a power-down mode. The power-down state can be controlled manually (via Pin 17 or Register 0x1E, Bit 3), or completely automatically by the chip. If automatic control is selected (0x1E, Bit 4), the AD9981's decision is based on the status of the sync detect bits (Register 0x24, Bits 2, 3, 6, and 7). If either an Hsync or a sync-on-green input is detected on any input, the chip powers up, or else it powers down. For manual control, the AD9981 allows flexibility of control through both a dedicated pin and a register bit. The dedicated pin allows a hardware watchdog circuit to control power-down, while the register bit allows power-down to be controlled by software.

With manual power-down control, the polarity of the power-down pin must be set (0x1E, Bit 2) regardless of whether the pin is used. If unused, it is recommended to set the polarity to active high and hardwire the pin to ground with a 10 kΩ resistor.

In power-down mode, there are several circuits that continue to operate as normal. The serial register and sync detect circuits maintain power so that the AD9981 can be woken up from its power-down state. The bandgap circuit maintains power because it is needed for sync detection. The sync-on-green and SOGOUT functions continue to operate because the SOGOUT output is needed when sync detection is performed by a secondary chip. All of these circuits require minimal power to operate. Typical standby power on the AD9981 is about 50 mW.

There are two options that can be selected when in power-down. These are controlled by Bits 0 and 1 in Register 0x1E. The first bit controls whether the SOGOUT pin is in high impedance or not. In most cases, the user will not place SOGOUT in high impedance during normal operation. The option to put SOGOUT in high impedance is included mainly to allow for factory testing modes. The second option keeps the AD9981 powered up while placing only the outputs in high impedance. This option is useful when the data outputs from two chips are connected on a PCB and the user wants to switch instantaneously between the two.

Table 10. Power-Down Control and Mode Descriptions

	Inputs			
Mode	**Auto Power-Down Control[1]**	**Power-Down[2]**	**Sync Detect[3]**	**Powered-On or Comments**
Power-Up	1	X	1	Everything
Power-Down	1	X	0	Only the serial bus, sync activity detect, SOG, bandgap reference
Power-Up	0	0	X	Everything
Power-Down	0	1	X	Only the serial bus, sync activity detect, SOG, bandgap reference

[1] Auto power-down control is set by Register 0x1E, Bit 4.
[2] Power-down is controlled by OR'ing Pin 17 with Register 0x1E, Bit 3. The polarity of Pin 17 is set by Register 0x1E, Bit 2.
[3] Sync detect is determined by OR'ing Register 0x24, Bits 2, 3, 6, and 7.

TIMING DIAGRAMS

The following timing diagrams show the operation of the AD9981.The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally. There is a pipeline in the AD9981, which must be flushed before valid data becomes available. This means six data sets are presented before valid data is available.

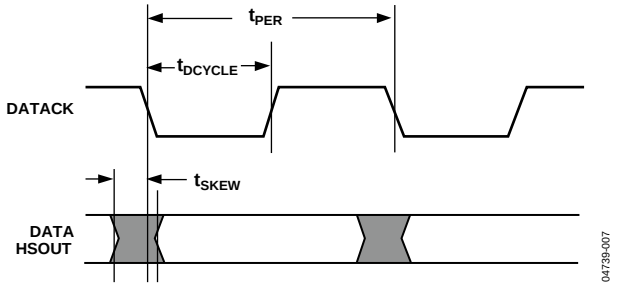


Figure 13. Output Timing

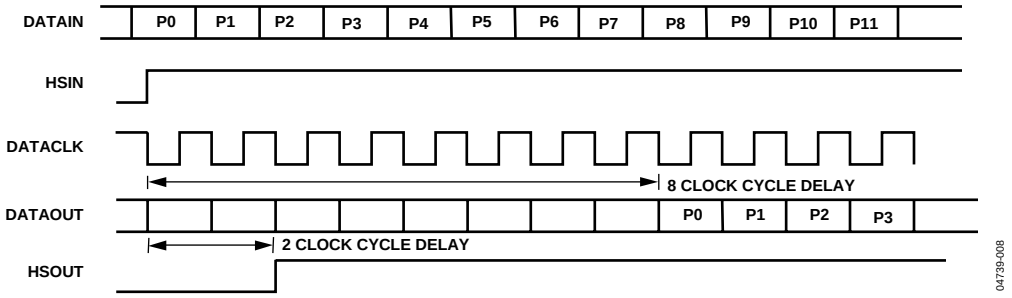


Figure 14. 4:4:4 Timing Mode

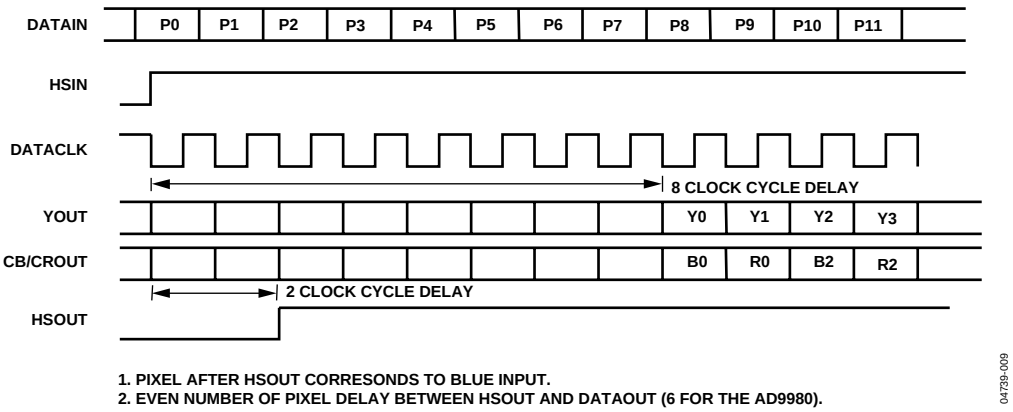


Figure 15. 4:2:2 Timing Mode

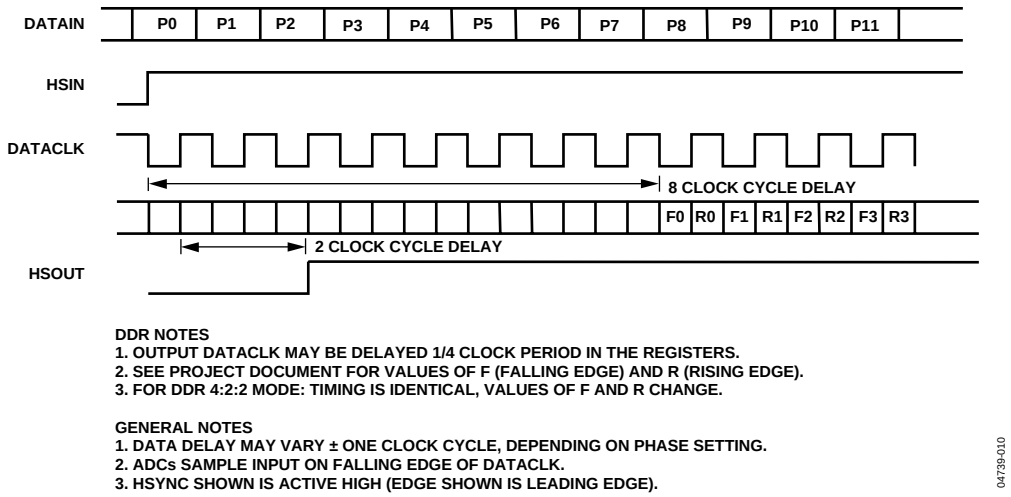


Figure 16. DDR Timing Mode

HSYNC TIMING

The Hsync is processed in the AD9981 to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted with respect to Hsync through a full 360° in 32 steps via the phase adjust register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and the data clock (DATACK).

Three things happen to Hsync in the AD9981. First, the polarity of Hsync input is determined and thus has a known output polarity. The known output polarity can be programmed either active high or active low (Register 0x12, Bit 3). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 0x13. HSOUT is the sync signal that should be used to drive the rest of the display system.

COAST TIMING

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the Coast input and function are unnecessary and should not be used.

In some systems, however, Hsync is disturbed during Vsync. In some cases, Hsync pulses disap-pear. In other systems, such as those that employ composite sync (Csync) signals or embedded sync-on-green, Hsync may include equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock to the new frequency and will have changed frequency by the end of the Vsync period. It then takes a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a tearing of the image at the top of the display.

The Coast input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and holds the clock at its current frequency. The PLL can free run for several lines without significant frequency drift. Coast can be generated internally by the AD9981 (see Register 0x18) or can be provided externally by the graphics controller.

When internal Coast is selected (Register 0x18, Bit 7 = 0, and Register 0x14, Bits [7:6] to select source), Vsync is used as a basis for determining the position of Coast. The internal Coast signal is enabled a programmed number of Hsync periods before the periodic Vsync signal (Precoast Register 0x16) and dropped a programmed number of Hsync periods after Vsync (Postcoast Register 0x17). It is recommended that the Vsync filter be enabled when using the internal Coast function to allow the AD9981 to determine precisely the number of Hsyncs/Vsync and their location. In many applications where disruptions occur and Coast is used, values of 2 for Precoast and 10 DDR for Postcoast are sufficient to avoid most extraneous pulses.

OUTPUT FORMATTER

The output formatter is capable of generating several output formats to be presented to the 30 data output pins. The output formats and the pin assignments for each format are listed in Table 11. Also, there are several clock options for the output clock. The user may select the pixel clock, a 90° phase-shifted pixel clock, a 2× pixel clock, or a fixed frequency 40 MHz clock for test purposes. The output clock may also be inverted.

Data output is available as 30 pin RGB or YCbCr or if either 4:2:2 or 4:4:4 DDR is selected, a secondary channel is available. This secondary channel is always 4:2:2 DDR and allows the flexibility of having a second channel with the same video data that can be utilized by another display or a storage device. Depending on the choice of output modes, the primary output can be 30 pins, 20 pins or as few as 15 pins.

Mode Descriptions

- 4:4:4—All channels come out with their 10 data bits at the same time. Data is aligned to the negative edge of the clock for easy capture. This is the normal 30-bit output mode for RGB or 4:4:4 YCbCr.
- 4:2:2—Red and green channels contain 4:2:2 formatted data (20 pins) with Y data on the green channel and Cb, Cr data on the red channel. Data is aligned to the negative edge of the clock. The blue channel contains the secondary channel with Cb, Y, Cr, Y formatted 4:2:2 DDR data. The data edges are aligned to both edges of the pixel clock, so use of the 90° clock may be necessary to capture the DDR data.
- 4:4:4 DDR—This mode puts out full 4:4:4 data on 15 bits of the red and green channels, thus saving 15 pins. The first half (RGB [14:0]) of the 30-bit data is sent on the rising edge and the second half (RGB [29:15]) is sent on the falling edge. DDR 4:2:2 data is sent on the blue channel, as in 4:2:2 mode.

  RGB [29:0] = R [9:0] + G [9:0] + B [9:0], so RGB [29:15] = R [9:0] + G [9:5] and RGB [14:0] = G [4:0] + B [9:0]

Table 11. Output Formats

Port	Red										Green										Blue									
Bit	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4:4:4	Red/Cr										Green/Y										Blue/Cb									
4:2:2[1]	Cb, Cr										Y										DDR 4:2:2 ↑ Cb, Cr ↓ Y,Y									
4:4:4 DDR	DDR ↑[2] G [4:0]						DDR ↑ B [9:0]									N/A					DDR 4:2:2 ↑ Cb,Cr									
	DDR ↓ R [9:0]										DDR ↓ G [9:5]					N/A					DDR 4:2:2 ↓ Y,Y									

[1] For 4:2:2 modes, the first item in the list is the first pixel after Hsync.
[2] Arrows in the table indicate clock edge. Rising edge of clock = ↑, falling edge = ↓.

TWO-WIRE SERIAL REGISTER MAP

The AD9981 is initialized and controlled by a set of registers, which determine the operating modes. An external controller is employed to write and read the control registers through the two-wire serial interface port.

Table 12. Control Register Map

Hexadecimal Address	Read and Write or Read Only	Bits	Default Value	Register Name	Description
0x00	RO	7:0		Chip Revision	An 8-bit register that represents the silicon revision level.
0x01	R/W	7:0	0110 1001	PLL Div MSB	This register is for bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. (This will give the PLL more time to lock.)[1]
0x02	R/W	7:4	1101 ****	PLL Div LSB	Bits [7:4] LSBs of the PLL Divider Word. Links to the PLL Div MSB to make a 12-bit register.
0x03	R/W	7:6	01** ****	VCO/CPMP	Bits [7:6] VCO Range. Selects VCO frequency range. (See PLL description).
		5:3	**00 1***		Bits [5:3] Charge Pump Current. Varies the current that drives the low-pass filter. (See PLL description).
		2	**** *0**		Bit 2. External Clock Enable.
0x04	R/W	7:3	1000 0***	Phase Adjust	ADC Clock Phase Adjustment. Larger values mean more delay. (1 LSB = T/32).
0x05	R/W	6:0	*100 0000	Red Gain MSBs	7-Bit Red Channel Gain Control. Controls ADC input range (contrast) of each respective channel. Bigger values give less contrast.
0x06	R/W	7:0	00** ****	Red Gain LSBs	Linked with Register 0x05 to form the 9-bit red gain that controls the ADC input range (contrast) of the red channel. A lower value corresponds to a higher gain.
0x07	R/W	6:0	*100 0000	Green Gain MSBs	7-Bit Green Channel Gain Control. Controls ADC input range (contrast) of each respective channel. Bigger values give less contrast.
0x08	R/W	7:0	00** ****	Green Gain LSBs	Linked to Register 0x07 to form the 9-bit green gain that controls the ADC input range (contrast) of the green channel. A lower value corresponds to a higher gain.
0x09	R/W	6:0	*100 0000	Blue Gain MSBs	7-Bit Blue Channel Gain Control. Controls ADC input range (contrast) of each respective channel. Bigger values give less contrast.
0x0A	R/W	7:0	00** ****	Blue Gain LSBs	Linked to Register 0x09 to form the 9-bit blue gain that controls the ADC input range (contrast) of the blue channel. A lower value corresponds to a higher gain.
0x0B	R/W	7:0	0100 0000	Red Offset MSBs	8-Bit MSBs of the Red Channel Offset Control. Controls dc offset (brightness) of each respective channel. Bigger values decrease brightness.
0x0C	R/W	7	000* ****	Red Offset LSBs	Linked to Register 0x0B to form the 11-bit red offset that controls the dc offset (brightness) of the red channel in auto-offset mode.
0x0D	R/W	7:0	0100 0000	Green Offset MSBs	8-Bit MSBs of the Green Channel Offset Control. Controls dc offset (brightness) of each respective channel. Bigger values decrease brightness.
0x0E	R/W	7	000* ****	Green Offset LSBs	Linked to Register 0x0D to form the 11-bit green offset that controls the dc offset (brightness) of the green channel in auto-offset mode.
0x0F	R/W	7:0	0100 0000	Blue Offset MSBs	8-Bit MSBs of the Red Channel Offset Control. Controls dc offset (brightness) of each respective channel. Bigger values decrease brightness.
0x10	R/W	7	000* ****	Blue Offset LSBs	Linked to Register 0x0F to form the 11-bit blue offset which controls the dc offset (brightness) of the blue channel in auto-offset mode.

Hexadecimal Address	Read and Write or Read Only	Bits	Default Value	Register Name	Description
0x11	R/W	7:0	0010 0000	Sync Separator Threshold	This register sets the threshold of the sync separator's digital comparator.
0x12	R/W	7	0*** ****	Hsync Control	Active Hsync Override. 0 = The chip determines the active Hsync source. 1 = The active Hsync Source is set by 0x12, Bit 6.
		6	*0** ****		Selects the source of the Hsync for PLL and sync processing. This bit is used only if 0x12, Bit 7 is set to 1 or if both syncs are active. 0 = Hsync is from Hsync input pin. 1 = Hsync is from SOG.
		5	**0* ****		Hsync Polarity Override. 0 = The chip selects the Hsync input polarity. 1 = The polarity of the input Hsync is controlled by 0x12, Bit 4. This applies to both Hsync0 and Hsync1.
		4	***1 ****		Hsync input polarity: this bit is used only if 0x12, Bit 5 is set to 1. 0 = Active low input Hsync. 1 = Active high input Hsync.
		3	**** 1***		Sets the polarity of the Hsync output signal. 0 = Active low Hsync output. 1 = Active high Hsync output.
0x13	R/W	7:0	0010 0000	Hsync Duration	Sets the number of pixel clocks that Hsync out is active.
0x14	R/W	7	0*** ****	Vsync Control	Active Vsync Override. 0 = The chip determines the active Vsync source. 1 = The active Vsync source is set by 0x14, Bit 6.
		6	*0** ****		Selects the source of Vsync for the sync processing. This bit is used only if 0x14, Bit 7 is set to 1. 0 = Vsync is from the VSYNC input pin. 1 = Vsync is from the sync separator.
		5	**0* ****		Vsync Polarity Override. 0 = The chip selects the input Vsync polarity. 1 = The polarity of the input Vsync is set by 0x14, Bit 4. This applies to both Vsync0 and Vsync1.
		4	***1 ****		Vsync input polarity: this bit is used only if 0x14, Bit 5 is set to 1. 0 = Active low input Vsync. 1 = Active high input Vsync.
		3	**** 1***		Sets the polarity of the output Vsync signal. 0 = Active low output Vsync. 1 = Active high output Vsync.
		2	**** *0**		0 = The Vsync filter is disabled. 1 = The Vsync filter is enabled. This needs to be enabled when using the Hsync to Vsync counter.
		1	**** **0*		Enables the Vsync duration block. This is designed to be used with the Vsync filter. 0 = Vsync output duration is unchanged. 1 = Vsync output duration is set by Register 0x15.
0x15	R/W	7:0	0000 1010	Vsync Duration	Sets the number of Hsyncs that Vsync out is active. This is only used if 0x14, Bit 1 is set to 1.
0x16	R/W	7:0	0000 0000	Precoast	The number of Hsync periods to Coast prior to Vsync.
0x17	R/W	7:0	0000 0000	Postcoast	The number of Hsync periods to Coast after Vsync.
0x18	R/W	7	0*** ****	Coast and Clamp Control	Coast Source. Selects the source of the Coast signal. 0 = Using internal Coast generated from Vsync. 1 = Using external Coast signal from external Coast pin.

Hexadecimal Address	Read and Write or Read Only	Bits	Default Value	Register Name	Description
		6	*0** ****		Coast Polarity Override. 0 = The chip selects the external Coast polarity. 1 = The polarity of the external Coast signal is set by 0x18, Bit 5.
		5	**1* ****		Coast Input Polarity. This bit is used only if 0x18, Bit 6 is set to 1. 0 = Active low external Coast. 1 = Active high external Coast.
		4	***0 ****		Clamp Source Select. 0 = Use the internal clamp generated from Hsync. 1 = Use the external clamp signal.
		3	**** 0***		Red Clamp. 0 = Clamp the red channel to ground. 1 = Clamp the red channel to midscale.
		2	**** *0**		Green Clamp. 0 = Clamp the green channel to ground. 1 = Clamp the green channel to midscale.
		1	**** **0*		Blue Clamp. 0 = Clamp the blue channel to ground. 1 = Clamp the blue channel to midscale.
		0	**** ***0		Must be set to 0 for proper operation.
0x19	R/W	7:0	0000 1000	Clamp Placement	Places the clamp signal an integer of clock periods after the trailing edge of the Hsync signal.
0x1A	R/W	7:0	0010 0000	Clamp Duration	Number of clock periods that the clamp signal is actively clamping.
0x1B	R/W	7	0*** ****	Clamp and Offset	External clamp polarity override. 0 = The chip selects the clamp polarity. 1 = The polarity of the clamp signal is set by 0x1B, Bit 6.
		6	*1** ****		External Clamp Input Polarity. This bit is used only if 0x1B, Bit 7 is set to 1. 0 = Active low external clamp. 1 = Active high external clamp.
		5	**0* ****		0 = Auto-offset is disabled. 1 = Auto-offset is enabled (offsets become the desired clamp code).
		4:3	***1 1***		This selects how often the auto-offset circuit operates. 00 = every clamp; 01 = 16 clamps; 10 = every 64 clamps; 11 = every Vsync.
		2:0	**** *011		Must be written to default (011) for proper operation.
0x1C	R/W	7:0	1111 1111	TestReg0	Must be set to 0xFF for proper operation.
0x1D	R/W	7:3	0111 1***	SOG Control	SOG slicer threshold. Sets the voltage level of the SOG slicer's comparator.
		2	**** *0**		SOGOUT Polarity. Sets the polarity of the signal on the SOGOUT pin. 0 = Active low SOGOUT. 1 = Active high SOGOUT.
		1:0	**** **00		SOGOUT Select. 00 = Raw SOG from sync slicer (SOG0 or SOG1). 01 = Raw Hsync (Hsync0 or Hsync1). 10 = Regenerated sync from sync filter. 11 = Filtered sync from sync filter.
0x1E	R/W	7	*** ****	Power	Channel Select Override. 0 = The chip determines which input channels to use. 1 = The input channel selection is determined by 0x1E, Bit 6.
		6	*0** ****		Channel Select. Input channel select: this is used only if 0x1E, Bit 7 is set to 1, or if syncs are present on both channels. 0 = Channel 0 syncs and data are selected. 1 = Channel 1 syncs and data are selected.

Hexadecimal Address	Read and Write or Read Only	Bits	Default Value	Register Name	Description
		5	**1* ****		Programmable Bandwidth. 0 = Low analog input bandwidth. 1 = High analog input bandwidth.
		4	***1 ****		Power-Down Control Select. 0 = Manual power-down control. 1 = Auto power-down control.
		3	**** 0***		Power-Down. 0 = Normal operation. 1 = Power-down.
		2	**** *0**		Power-Down Pin Polarity. 0 = Active low. 1 = Active high.
		1	**** **0*		Power-Down Fast Switching Control. 0 = Normal power-down operation. 1 = The chip stays powered up and the outputs are put in high impedance mode.
		0	**** ***0		SOGOUT High Impedance Control. 0 = SOGOUT operates as normal during power-down. 1 = SOGOUT is in high impedance during power-down.
0x1F	R/W	7:5	100* ****	Output Select 1	Output Mode. 100 = 4:4:4 output mode. 101 = 4:2:2 output mode. 110 = 4:4:4—DDR output mode.
		4	***1 ****		Primary Output Enable. 0 = Primary output is in high impedance state. 1 = Primary output is enabled.
		3	**** 0***		Secondary Output Enable. 0 = Secondary output is in high impedance state. 1 = Secondary output is enabled.
		2:1	**** *10*		Output Drive Strength. 00 = Low output drive strength. 01 = Medium low output drive strength. 10 = Medium high output drive strength. 11 = High output drive strength. Applies to all outputs except VSOUT.
		0	**** ***0		Output Clock Invert. 0 = Noninverted pixel clock. 1 = Inverted pixel clock. Applies to all clocks output on DATACK.
0x20	R/W	7:6	0*** ****	Output Select 2	Output Clock Select. 00 = Pixel clock. 01 = 90° phase shifted pixel clock. 10 = 2× pixel clock. 11 = 40 MHz internal clock.
		5	*0** ****		Output High Impedance. 0 = Normal outputs. 1 = All outputs except SOGOUT in high impedance mode.
		4	**0* ****		SOG High Impedance. 0 = Normal SOG output. 1 = SOGOUT pin is in high impedance mode.
		3	***0 ****		Field Output Polarity. Sets the polarity of the field output signal. 0 = Active low => even field, active high => odd field. 1 = Active low => odd field, active high => even field.
		2	**** 1***		PLL Sync Filter Enable. 0 = PLL uses raw Hsync/SOG. 1 = PLL uses filtered Hsync/SOG.

Hexadecimal Address	Read and Write or Read Only	Bits	Default Value	Register Name	Description
		1	**** *0**		Sync Processing Input Select. Selects the sync source for the sync processor. 0 = Sync processing uses raw Hsync/SOGIN. 1 = Sync processing uses regenerated Hsync from sync filter.
		0			Must be set to 1 for proper operation.
0x21	R/W	7:0	0010 0000		Must be set to default for proper operation.
0x22	R/W	7:0	0011 0010		Must be set to default for proper operation.
0x23	R/W	7:0	0000 1010	Sync Filter Window Width	Sets the window of time around the regenerated Hsync leading edge (in 25 ns steps) that sync pulses are allowed to pass through.
0x24	RO	7	_*** ****	Sync Detect	Hsync0 Detection Bit. 0 = Hsync0 is not active. 1 = Hsync0 is active.
		6	*_** ****		Hsync1 Detection Bit. 0 = Hsync 1 is not active. 1 = Hsync 1 is active.
		5	**_* ****		Vsync 0 Detection Bit. 0 = Vsync0 is not active. 1 = Vsync0 is active.
		4	***_ ****		Vsync1 Detection Bit. 0 = Vsync1 is not active. 1 = Vsync1 is active.
		3	**** _***		SOG0 Detection Bit 0 = SOG0 is not active. 1 = SOG0 is active.
		2	**** *_**		SOG1 Detection Bit 0 = SOG1 is not active. 1 = SOG1 is active.
		1	**** **_*		Coast Detection Bit. 0 = External Coast is not active. 1 = External Coast is active.
		0	**** ***_		Clamp Detection Bit. 0 = External clamp is not active. 1 = External clamp is active.
0x25	RO	7	_*** ****	Sync Polarity Detect	Hsync 0 Polarity. 0 = Hsync0 polarity is active low. 1 = Hsync0 polarity is active high.
		6	*_** ****		Hsync1 Polarity. 0 = Hsync1 polarity is active low. 1 = Hsync1 polarity is active high.
		5	**_* ****		Vsync0 Polarity. 0 = Vsync0 polarity is active low. 1 = Vsync0 polarity is active high.
		4	***_ ****		Vsync1 Polarity. 0 = Vsync1 polarity is active low. 1 = Vsync1 polarity is active high.
		3	**** _***		Coast Polarity. 0 = External Coast polarity is active low. 1 = External Coast polarity is active high.
		2	**** *_**		Clamp Polarity. 0 = External clamp polarity is active low. 1 = External clamp polarity is active high.
		1	**** **_*		Extraneous Pulses Detected. 0 = No equalization pulses detected on Hsync. 1 = Extraneous pulses detected on Hsync.

Hexadecimal Address	Read and Write or Read Only	Bits	Default Value	Register Name	Description
0x26	RO	7:0		Hsyncs Per Vsync MSBs	MSBs of Hsyncs per Vsync count.
0x27	RO	7:4		Hsyncs Per Vsync LSBs	LSBs of Hsyncs per Vsync count.
0x28	R/W	7:0	1011 1111	TestReg1	Must be written to 0xBF for proper operation.
0x29	R/W	7:0	0000 0010	TestReg2	Must be written to 0x02 for proper operation.
0x2A	RO	7:0		TestReg3	Read only bits for future use.
0x2B	RO	7:0		TestReg4	Read only bits for future use.
0x2C	R/W	7:5 4 3:0	000* **** ***0 **** **** 0000	Offset Hold	Must be written to default for proper operation. Auto-Offset Hold. Disables the auto-offset and holds the feedback result. 0 = One time update. 1 = Continuous update. Must be written to default for proper operation.
0x2D	R/W	7:0	1111 0000	TestReg5	Must be written to 0xE8 for proper operation.
0x2E	R/W	7:0	1111 0000	TestReg6	Must be written to 0xE0 for proper operation.

[1] Functions with more than eight control bits, such as PLL divide ratio, gain, and offset, are only updated when the LSBs are written to (for example, Register 0x02 for PLL divide ratio).

DETAILED 2-WIRE SERIAL CONTROL REGISTER DESCRIPTIONS

CHIP IDENTIFICATION

0x00 7:0 Chip Revision

An 8-bit register that represents the silicon revision.

PLL DIVIDER CONTROL

0x01 7:0 PLL Divide Ratio MSBs

The eight MSBs of the 12-bit PLL divide ratio PLLDIV.

The PLL derives a pixel clock from the incoming Hsync signal. The pixel clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095 as long as the output frequency is within range. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications, which will assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (see Table 9). However, many computer systems do not conform precisely to the recommendations and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV usually produces one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693. PLLDIVM = 0x69, PLLDIVL = 0xDX.

The AD9981 updates the full divide ratio only when the LSBs are written. Writing to this register by itself does not trigger an update.

0x02 7:4 PLL Divide Ratio LSBs

The four LSBs of the 12-bit PLL divide ratio PLLDIV.

The power-up default value of PLLDIV is 1693. PLLDIVM = 0x69, PLLDIVL = 0xDX.

CLOCK GENERATOR CONTROL

0x03 7:6 VCO Range Select

Two bits that establish the operating range of the clock generator. VCORNGE must be set to correspond to the desired operating frequency (incoming pixel rate). The PLL gives the best jitter performance at high frequencies. For this reason, in order to output low pixel rates and still get good jitter performance, the PLL actually operates at a higher frequency but then divides down the clock rate afterwards. See Table 13 for the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting. The power-up default value is 01.

Table 13. VCO Ranges

VCO Range	Pixel Rates
00	10 to 21
01	21 to 42
10	42 to 84
11	84 to 95

0x03 5:3 Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator. The current must be set to correspond with the desired operating frequency. The power-up default value is current = 001.

Table 14. Charge Pump Currents

Ip2	Ip1	Ip0	Current
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

0x03 2 External Clock Enable

This bit determines the source of the pixel clock.

Table 15. External Clock Select Settings

EXTCLK	Function
0	Internally generated clock
1	Externally provided clock signal

A Logic 0 enables the internal PLL that generates the pixel clock from an externally provided Hsync.

A Logic 1 enables the external EXTCLK input pin. In this mode, the PLL Divide Ratio (PLLDIV) is ignored. The clock phase adjust (PHASE) is still functional. The power-up default value is EXTCLK = 0.

PHASE ADJUST

0x04 7:3

Phase adjustment for the DLL to generate the ADC clock. A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase. The power up default is 16.

INPUT GAIN

0x05 6:0 Red Channel Gain Adjust MSBs

The 7-Bit Red Channel Gain Control. The AD9981 can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting the red gain to 511 corresponds to an input range of 1.0 V. A red gain of 0 establishes an input range of 0.5 V. Note that increasing red gain results in the picture having less contrast (the input signal uses fewer of the available converter codes). Values written to this register will not be updated until the LSB register (R0x06) has also been written. The power-up default is 1000000.

0x06 7:6 Red Channel Gain Adjust LSBs

The 2 Bit LSBs of the Red Channel Gain Control. Along with the 7 MSBs of gain control in the previous register, there are 9 bits of gain control. Default power up value is 00.

0x07 6:0Green Channel Gain Adjust MSBs

The 7-Bit Green Channel Gain Control. See red channel gain adjust above. Register update requires writing 0x00 to Register 0x08.

0x08 7:6 Green Channel Gain Adjust LSBs

The 2-Bit LSBs of the Green Channel Gain Control. Along with the 7 MSBs of gain control in the previous register, there are 9 bits of gain control. Default power-up value is 00.

0x09 6:0 Blue Channel Gain Adjust MSBs

The 7-Bit Blue Channel Gain Control. See red channel gain adjust above. Register update requires writing 0x00 to Register 0x0A.

0x0A 7:6 Blue Channel Gain Adjust LSBs

The 2-Bit LSBs of the Blue Channel Gain Control. Along with the 7 MSBs of gain control in the previous register, there are 9 bits of gain control. Default power-up value is 00.

INPUT OFFSET

0x0B 7:0 Red Channel Offset MSBs

The 8-Bit MSB of the Red Channel Offset Control. Along with the 1 LSBs in the following register, there are 11 bits of dc offset control in the red channel. The offset control shifts the analog input, resulting in a change in brightness. Note that the function of the offset register depends on whether auto-offset is enabled (Register 0x1B, Bit 5).

If auto-offset is disabled, the 9 bits of the offset registers (Bits [6:0] of the offset MSB register plus Bits [7:6] of the following register) control the absolute offset added to the channel (for the red channel, Register 0x0B, Bits[6:0] plus Register 0x0C, Bits [7:6]) control the absolute offset added to the channel. The offset control provides a ±255 LSBs of adjustment range, with 1 LSB of offset corresponding to 1 LSB of output code.

If auto-offset is enabled, the 11-bit offset (comprised of the 8 bits of the MSB register and Bits [7:5] of the following register) determines the clamp target code. The 11-bit offset consists of 1 sign bit plus 10 bits. If the register is programmed to 530 DDR, then the output code is equal to 530 DDR at the end of the clamp period. Note that incrementing the offset register setting by 1 LSB adds 1 LSB of offset, regardless of the auto-offset setting. Values written to this register are not updated until the LSB register (Register 0x0C) has also been written.

0x0C 7:5 Red Channel Offset LSBs

The LSBs of the red channel offset control combine with the 8 bits of MSB in the previous register to make 11 bits of offset control.

0x0D 7:0 Green Channel Offset MSBs

The 8-Bit Green Channel Offset Control. See red channel offset (0x0B). Update of this register occurs only when Register 0x0E is also written.

0x0E 7:5 Green Channel Offset LSBs

The LSBs of the green channel offset control combine with the 8 bits of MSB in the previous register to make 11 bits of offset control.

0x0F 7:0 Blue Channel Offset MSBs

The 8-Bit Blue Channel Offset Control. See red channel offset (0x0B). Update of this register occurs only when Register 0x10 is also written.

0x10 7:5 Blue Channel Offset LSBs

The LSBs of the blue channel offset control combine with the 8 bits of MSB in the previous register to make 11 bits of offset control.

HSYNC CONTROLS

0x11 7:0 Sync Separator Threshold

This register sets the threshold of the sync separator's digital comparator. The value written to this register is multiplied by 200 ns to get the threshold value. Therefore, if a value of 5 is written, the digital comparator threshold is 1 µs and any pulses less than 1 µS are rejected by the sync separator. There is some variability to the 200 ns multiplier value. The maximum variability over all operating conditions is ±20% (160 ns to 240 ns). Since normal Vsync and Hsync pulse widths differ by a factor of about 500 or more, the 20% variability is not an issue. The power-up default value is 32 DDR.

0x12 7 Hsync Source Override

This is the active Hsync override. Setting this to 0 allows the chip to determine the active Hsync source. Setting it to 1 uses Bit 6 of Register 0x12 to determine the active Hsync source. Power-up default value is 0.

Table 16.Active Hsync Source Override

Override	Result
0	Hsync Source determined by chip
1	Hsync Source determined by user Register 0x12, Bit 6

0x12 6 Hsync Source

This bit selects the source of the Hsync for PLL and sync processing—only if Bit 7 of Register 0x12 is set to 1 or if both syncs are active. Setting this bit to 0 specifies the Hsync from the input pin. Setting it to 1 selects Hsync from SOG. Power-up default is 0.

Table 17. Active Hsync Select Settings

Select	Result
0	Hsync Input
1	Hsync from SOG

0x12 5 Hsync Input Polarity Override

This bit determines whether the chip selects the Hsync input polarity or if it is specified. Setting this bit to 0 allows the chip to automatically select the polarity of the input Hsync; setting it to 1 indicates that Bit 4 of Register 0x12 specifies the polarity. Power-up default is 0.

Table 18. Hsync Input Polarity Override Settings

Override Bit	Result
0	Hsync Polarity Determined by Chip
1	Hsync Polarity Determined by User Register 0x12, Bit 4

0x12 4 Input Hsync Polarity

If Bit 5 of Register 0x12 is 1, the value of this bit specifies the polarity of the input Hsync. Setting this bit to 0 indicates an active low Hsync; setting this bit to 1 indicates an active high Hsync. Power-up default is 1.

Table 19. Hsync Input Polarity Settings

Hsync Polarity Bit	Result
0	Hsync Input Polarity is Negative
1	Hsync Input Polarity is Positive

0x12 3 Hsync Output Polarity

This bit sets the polarity of the Hsync output. Setting this bit to 0 sets the Hsync output to active low. Setting this bit to 1 sets the Hsync output to active high. Power-up default setting is 1.

Table 20. Hsync Output Polarity Settings

Hsync Output Polarity Bit	Result
0	Hsync Output Polarity is Negative
1	Hsync Output Polarity is Positive

0x13 7:0 Hsync Duration

An 8-bit register that sets the duration of the Hsync output pulse. The leading edge of the Hsync output is triggered by the internally-generated, phase-adjusted PLL feedback clock. The AD9981 then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the Hsync output, which is also phase-adjusted.

VSYNC CONTROLS

0x14 7 Vsync Source Override

This is the active Vsync override. Setting this to 0 allows the chip to determine the active Vsync source, setting it to 1 uses Bit 6 of Register 0x14 to determine the active Vsync source. Power-up default value is 0.

Table 21. Active Vsync Source Override

Override	Result
0	Vsync source determined by chip
1	Vsync source determined by user Register 0x14, Bit 6

0x14 6 Vsync Source

This bit selects the source of the Vsync for sync processing only if Bit 7 of Register 0x14 is set to 1. Setting Bit 6 to 0 specifies the Vsync from the input pin; setting it to 1 selects Vsync from the sync separator. Power-up default is 0.

Table 22. Active Vsync Select Settings

Select	Result
0	Vsync input
1	Vsync from sync separator

0x14 5 Vsync Input Polarity Override

This bit sets whether the chip selects the Vsync input polarity or if it is specified. Setting this bit to 0 allows the chip to automatically select the polarity of the input Vsync. Setting this bit to 1 indicates that Bit 4 of Register 0x14 specifies the polarity. Power-up default is 0.

Table 23. Vsync Input Polarity Override Settings

Override Bit	Result
0	Vsync polarity determined by chip
1	Vsync polarity determined by user Register 0x14, Bit 4

0x14 4 Input Vsync Polarity

If Bit 5 of Register 0x14 is 1, the value of this bit specifies the polarity of the input Vsync. Setting this bit to 0 indicates an active low Vsync; setting this bit to 1 indicates an active high Vsync. Power-up default is 1.

Table 24. Vsync Input Polarity Settings

Override Bit	Result
0	Vsync input polarity is negative
1	Vsync input polarity is positive

0x14 3 Vsync Output Polarity

This bit sets the polarity of the Hsync output. Setting this bit to 0 sets the Hsync output to active low. Setting this bit to 1 sets the Hsync output to active high. Power-up default is 1.

Table 25. Vsync Output Polarity Settings

Vsync Output Polarity Bit	Result
0	Vsync output polarity is negative
1	Vsync output polarity is positive

0x14 2 Vsync Filter Enable

This bit enables the Vsync filter allowing precise placement of the Vsync with respect to the Hsync and facilitating the correct operation of the Hsyncs/ Vsync count.

Table 26. Vsync Filter Enable

Vsync Filter Bit	Result
0	Vsync filter disabled
1	Vsync filter enabled

0x14 1 Vsync Duration Enable

This enables the Vsync duration block, which is designed to be used with the Vsync filter. Setting the bit to 0 leaves the Vsync output duration unchanged. Setting the bit to 1 sets the Vsync output duration based on Register 0x15. Power-up duration is 0.

Table 27. Vsync Duration Enable

Vsync Duration Bit	Result
0	Vsync output duration is unchanged
1	Vsync output duration is set by Register 0x15

0x15 7:0 Vsync Duration

This is used to set the output duration of the Vsync, and is designed to be used with the Vsync filter. This is valid only if Register 0x14, Bit 1 is set to 1. Power-up default is 10 DDR.

COAST AND CLAMP CONTROLS

0x16 7:0 Precoast

This register allows the internally generated Coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period. For Precoast to work correctly, it is necessary for the Vsync filter (0x14, Bit 2) and sync processing filter (Register 0x20, Bit 1) both to be either enabled or disabled. The power-up default is 00.

0x17 7:0 Postcoast

This register allows the internally generated Coast signal to be applied following the Vsync signal. This is necessary in cases where postequalization pulses are present. The step size for this control is one Hsync period. For Postcoast to work correctly, it is necessary for the Vsync filter (0x14, Bit 2) and sync processing filter (0x20, Bit 1) both to be either enabled or disabled. The power-up default is 00.

0x18 7 Coast Source

This bit is used to select the active Coast source. The choices are the COAST input pin or vsync. If Vsync is selected, the additional decision of using the VSYNC input pin or the output from the sync separator needs to be made (Register 0x14, Bits [7: 6]).

Table 28. Coast Source Selection Settings

Select	Result
0	Vsync (internal Coast)
1	COAST input pin

0x18 6 Coast Polarity Override

This register is used to override the internal circuitry that determines the polarity of the Coast signal going into the PLL. The power-up default setting is 0.

Table 29. Coast Polarity Override Settings

Override Bit	Result
0	Coast polarity determined by chip
1	Coast polarity determined by user

0x18 5 Input Coast Polarity

This register sets the input Coast polarity when Bit 6 of Register 0x18 = 1. The power-up default setting is 1.

Table 30. Coast Polarity Settings

Coast Polarity Bit	Result
0	Coast polarity is negative
1	Coast polarity is positive

0x18 4 Clamp Source

This bit determines the source of clamp timing. A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the leading edge of Hsync. A 1 enables the external clamp input pin. The three channels are clamped when the clamp signal is active. The polarity of clamp is determined by the clamp polarity bit. The power-up default setting is 0.

Table 31. Clamp Source Selection Settings

Clamp Source	Result
0	Internally generated clamp
1	Externally provided clamp signal

0x18 3 Red Clamp Select

This bit determines whether the red channel is clamped to ground or to midscale. The power-up default setting is 0.

Table 32. Red Clamp Select Settings

Clamp	Result
0	Clamp to ground
1	Clamp to midscale

0x18 2 Green Clamp Select

This bit determines whether the green channel is clamped to ground or to midscale. The power-up default setting is 0.

Table 33. Green Clamp Select Settings

Clamp	Result
0	Clamp to ground
1	Clamp to midscale

0x18 1 Blue Clamp Select

This bit determines whether the blue channel is clamped to ground or to midscale. The power-up default setting is 0.

Table 34. Blue Clamp Select Settings

Clamp	Result
0	Clamp to ground
1	Clamp to midscale

0x19 7:0 Clamp Placement

An 8-bit register that sets the position of the internally generated clamp. When EXTCLMP = 0 (Register 0x18, Bit 4), a clamp signal is generated internally, at a position established by the clamp placement register (Register 0x19) and for a duration set by the clamp duration register (Register 0x1A). Clamping is started a clamp placement count(Register 0x19) of pixel periods after the trailing edge of Hsync. The clamp placement may be programmed to any value between 1 and 255. A value of 0 is not supported.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image. When EXTCLMP = 1, this register is ignored. Power-up default setting is 8.

0x1A 7:0 Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp. When EXTCLMP = 0 (Register 0x18, Bit 4), a clamp signal is generated internally at a position established by the clamp placement register (and for a duration set by the clamp duration register). Clamping begins a clamp placement count (Register 0x19) of pixel periods after the trailing edge of Hsync. The clamp duration may be programmed to any value between 1 and 255. A value of 0 is not supported.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the average picture level (APL), or brightness. When EXTCLMP = 1, this register is ignored. Power-up default setting is 20 DDR.

0x1B 7 Clamp Polarity Override

This bit is used to override the internal circuitry that determines the polarity of the clamp signal. The power-up default setting is 0.

Table 35. Clamp Polarity Override Settings

Override Bit	Result
0	Clamp Polarity Determined by Chip
1	Clamp Polarity Determined by User Register 0x1B, Bit 6

0x1B 6 Input Clamp Polarity

This bit indicates the polarity of the clamp signal only if Bit 7 of Register 0x1B = 1. The power-up default setting is 1.

Table 36. Clamp Polarity Override Settings

CLMPOL	Result
0	Active low
1	Active high

0x1B 5 Auto-Offset Enable

This bit selects between auto-offset mode and manual offset mode (auto-offset disabled). See the section on auto-offset operation. The power-up default setting is 0.

Table 37. Auto-Offset Settings

Auto-Offset	Result
0	Auto-offset is disabled
1	Auto-offset is enabled (manual offset mode)

0x1B 4:3 Auto-Offset Update Frequency

These bits control how often the auto-offset circuit is updated (if enabled). Updating every 64 Hsyncs is recommended. The power-up default setting is 11.

Table 38. Auto-Offset Update Mode

Clamp Update	Result
00	Update offset every clamp period
01	Update offset every 16 clamp periods
10	Update offset every 64 clamp periods
11	Update offset every Vsync periods

0x1B 2-0 Must be written to 011 for proper operation.

SOG CONTROL

0x1D 7:3 SOG Comparator Threshold

This register allows the comparator threshold of the SOG slicer to be adjusted. This register adjusts it in steps of 8 mV, with the minimum setting equaling 8 mV and the maximum setting equaling 256 mV. The power-up default setting is 15 DDR and corresponds to a threshold value of 128 mV.

0x1D 2 SOG Output Polarity

This bit sets the polarity of the SOGout signal. The power-up default setting is 0.

Table 39. SOGOUT Polarity Settings

SOGOUT	Result
0	Active low
1	Active high

0x1D 1:0 SOG Output Select

These register bits control what is output on the SOGOUT pin. Options are the raw SOG from the slicer (this is the unprocessed SOG signal produced from the sync slicer), the raw Hsync, the regenerated sync from the sync filter which can generate missing syncs either due to coasting or drop-out, or finally the filtered sync which excludes extraneous syncs not occurring within the sync filter window. The power-up default setting is 0.

Table 40. SOGOUT Polarity Settings

SOGOUT Select	Function
00	Raw SOG from sync slicer (SOG0 or SOG1)
01	Raw Hsync (HSYNC0 or HSYNC1)
10	Regenerated Sync from sync filter
11	Filtered sync from sync filter

INPUT AND POWER CONTROL

0x1E 7 Channel Select Override

This bit provides an override to the automatic input channel selection. Power-up default setting is 0.

Table 41. Channel Source Override

Override	Result
0	Channel input source determined by chip
1	Channel input source determined by user Register 0x1E, Bit 6

0x1E 6 Channel Select

This bit selects the active input channel if Register 0x1E, bit 7 = 1. This selects between Channel 0 data and syncs or Channel 1 data and syncs. Power-up default setting is 0.

Table 42. Channel Select

Channel Select	Result
0	Channel 0 data and syncs are selected
1	Channel 1 data and syncs are selected

0x1E 5 Programmable Bandwidth

This bit selects between a low or high input bandwidth. It is useful in limiting noise for lower frequency inputs. The power-up default setting is 1. Low analog input bandwidth is ~100 MHz; high analog input bandwidth is ~200 MHz.

Table 43. Input Bandwidth Select

Input Bandwidth	Result
0	Low analog input bandwidth
1	High analog input bandwidth

0x1E 4 Power-Down Control Select

This bit determines whether power-down is controlled manually or automatically by the chip. If automatic control is selected (Register 0x1E, Bit 4), the AD9981's decision is based on the status of the sync detect bits (Register 0x24, Bits 2, 3, 6, and 7). If either an Hsync or a sync-on-green input is detected on any input, the chip powers up or powers down. For manual control, the AD9981 allows the flexibility of control through both a dedicated pin and a register bit. The dedicated pin allows a hardware watchdog circuit to control power-down, while the register bit allows power-down to be controlled by software. With manual power-down control, the polarity of the powerdown pin must be set (0x1E, Bit 2) whether it is used or not. If unused, it is recommended to set the polarity to active high and hardwire the pin to ground with a 10 kΩ resistor.

Table 44. Auto Power-Down Select

Power-Down Select	Result
0	Manual power-down control (User determines power-down)
1	Auto power-down control (Chip determines power-down)

0x1E 3 Power-Down

This bit is used to manually place the chip in power-down mode. It is only used if manual power-down control is selected (see Bit 4 above). Both the state of this register bit and the power-down pin (Pin 17) are used to control manual power-down. (See the Power Management section for more details on power-down.)

Table 45. Power-Down Settings

Power-Down Select	Pin 17	Result
0	0	Normal operation
1	X	Power-down

0x1E 2 Power-Down Polarity

This bit defines the polarity of the power-down pin (Pin 17). It is only used if manual power-down control is selected (see Bit 4 above).

Table 46. Power-Down Pin Polarity

Select	Result
0	Power-down pin is active low
1	Power-down pin is active high

0x1E 1 Power-Down Fast Switching Control

This bit controls a special fast switching mode. With this bit the AD9981 can stay active during power-down and only put the outputs in high impedance. This option is useful when the data outputs from two chips are connected on a PCB and the user wants to switch instantaneously between the two.

Table 47. Power-Down Fast Switching Control

Fast Switching Control	Result
0	Normal power-down operation
1	The chip stays powered up and the outputs are put in high impedance mode

0x1E 0 SOGOUT High Impedance Control

This bit controls whether the SOGOUT output pin is in high impedance or not, when in power-down mode. In most cases, SOGOUT is not put in high impedance during normal operation. It is usually needed for sync detection by the graphics controller. The option to put SOGOUT in high impedance is included mainly to allow for factory testing modes.

Table 42. SOGOUT High Impedance Control

SOGOUT Control	Result
0	The SOGOUT output operates as normal during power-down.
1	The SOGOUT output is in high impedance during power-down.

OUTPUT CONTROL

0x1F 7:5 Output Mode

These bits choose between three options for the output mode. In 4:4:4 mode, RGB is standard. In 4:2:2 mode, YCbCr is standard, which allows a reduction in the number of output pins from 30 to 20. In 4:4:4 DDR output mode, the data is in RGB mode, but changes on every clock edge. The power-up default setting is 100.

Table 43. Output Mode

Output Mode	Result
100	4:4:4 RGB mode
101	4:2:2 YCbCr mode
110	4:4:4 DDR mode

0x1F 4 Primary Output Enable

This bit places the primary output in active or high impedance mode. The power-up default setting is 1.

Table 44. Primary Output Enable

Select	Result
0	Primary output is in high impedance mode
1	Primary output is enabled

0x1F 3 Secondary Output Enable

This bit places the secondary output in active or high impedance mode.

The secondary output is designated when using either 4:2:2 or 4:4:4 (DDR). In these modes, the data on the blue output channel is the secondary output while the output data on the red and green channels are the primary output. Secondary output is always a DDR YCbCr data mode. See the Output Formatter section and Table 11. The power-up default setting is 0.

Table 45. Secondary Output Enable

Select	Result
0	Secondary output is in high impedance mode
1	Secondary output is enabled

0x1F 2:1 Output Drive Strength

These two bits select the drive strength for all the high-speed digital outputs (except VSOUT, A0, and the O/E field). Higher drive strength results in faster rise/fall times and in general makes it easier to capture data. Lower drive strength results in slower rise/fall times and helps to reduce EMI and digitally generated power supply noise. The power-up default setting is 10.

Table 46. Output Drive Strength

Output Drive	Result
00	Low output drive strength
01	Medium low output drive strength
10	Medium high output drive strength
11	High output drive strength

0x1F 0 Output Clock Invert

This bit allows inversion of the output clock. The power-up default setting is 0.

Table 47. Output Clock Invert

Select	Result
0	Noninverted pixel clock
1	Inverted pixel clock

0x20 7:6 Output Clock Select

These bits allow selection of optional output clocks such as a fixed 40 MHz clock, a 2× clock, a 90° phase-shifted clock, or the normal pixel clock. The power-up default setting is 00.

Table 48. Output Clock Select

Select	Result
00	Pixel clock
01	90° phase-shifted pixel clock
10	2× pixel clock
11	40 MHz internal clock

0x20 5 Output High Impedance

This bit puts all outputs (except SOGOUT) in a high impedance state. The power-up default setting is 0.

Table 49. Output High Impedance

Select	Result
0	Normal outputs
1	All outputs (except SOGOUT) in high impedance mode

0x20 4 SOG High Impedance

This bit allows the SOGOUT pin to be placed in high impedance mode. The power-up default setting is 0.

Table 50. SOGOUT High Impedance

Select	Result
0	Normal SOG output
1	SOGOUT pin is in high impedance mode

0x20 3 Field Output Polarity

This bit sets the polarity of the field output bit. The power-up default setting is 1.

Table 51. Field Output Polarity

Select	Result
0	Active low = even field; active high = odd field
1	Active low = odd field; active high = even field

SYNC PROCESSING

0x20 2 PLL Sync Filter

This bit selects which signal the PLL uses. It can select between either raw Hsync or SOG or filtered versions. The filtering of the Hsync and SOG can eliminate nearly all extraneous transitions which have traditionally caused PLL disruption. The power-up default setting is 0.

Table 52. PLL Sync Filter Enable

Select	Result
0	PLL uses raw Hsync or SOG inputs
1	PLL uses filtered Hsync or SOG inputs

0x20 1 Sync Processing Input Source

This bit selects whether the sync processor uses a raw sync or a regenerated sync for the following functions: Coast, H/V count, field detection and Vsync duration counts. Using the regenerated sync is recommended.

Table 53. SP Filter Enable

Select	Result
0	Sync processing uses raw Hsync or SOG
1	Sync processing uses the internally regenerated Hsync

0x21 7:0 Must be set to default

0x22 7:0 Must be set to default

0x23 7:0 Sync Filter Window Width

This 8-bit register sets the window of time for the regenerated Hsync leading edge (in 25 ns steps) and that sync pulses are allowed to pass through. Therefore with the default value of 10, the window width is ±250 ns. The goal is to set the window width so that extraneous pulses are rejected. (see the Sync Processing section). As in the sync separator threshold, the 25 ns multiplier value is somewhat variable. The maximum variability over all operating conditions is ±20% (20 ns to 30 ns).

DETECTION STATUS

0x24 7 Hsync0 Detection Bit

This bit is used to indicate when activity is detected on the HSYNC0 input pin. If Hsync is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = Hsync0 not active. 1 = Hsync0 is active.

Table 54. Hsync0 Detection Results

Detect	Result
0	No activity detected
1	Activity detected

0x24 6 Hsync1 Detection Bit

This bit is used to indicate when activity is detected on the HSYNC1 input pin. If HSYNC is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = HSYNC1 not active. 1 = HSYNC1 is active.

Table 55. Hsync1 Detection Results

Detect	Result
0	No activity detected
1	Activity detected

0x24 5 Vsync0 Detection Bit

This bit is used to indicate when activity is detected on the VSYNC0 input pin. If Vsync is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = Vsync0 not active. 1 = Vsync0 is active.

Table 56. Vsync0 Detection Results

Detect	Result
0	No activity detected
1	Activity detected

0x24 4 VSYNC1 Detection Bit

This bit is used to indicate when activity is detected on the VSYNC1 input pin. If Vsync is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = Vsync1 not active. 1 = Vsync1 is active.

Table 57. Vsync1 Detection Results

Detect	Result
0	No activity detected
1	Activity detected

0x24 3 SOG0 Detection Bit

This bit is used to indicate when activity is detected on the SOG0 input pin. If SOG is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = SOG0 not active. 1 = SOG0 is active.

Table 58. SOG0 Detection Results

Detect	Result
0	No activity detected
1	Activity detected

0x24 2 SOG1 Detection Bit

This bit is used to indicate when activity is detected on the SOG1 input pin. If SOG is held high or low, activity is not detected. The sync processing block diagram shows where this function is implemented. 0 = SOG1 not active. 1 = SOG1 is active.

Table 59. SOG1 Detection Results

Detect	Result
0	No activity detected
1	Activity detected

0x24 1 COAST Detection Bit

This bit detects activity on the EXTCLK/EXTCOAST pin. It indicates that one of the two signals is active, but it doesn't indicate which one. A dc signal is not detected.

Table 60. Coast Detection Result

Detect	Result
0	No activity detected
1	Activity detected

0x24 0 Clamp Detection Bit

This bit is used to indicate when activity is detected on the external CLAMP pin. If external clamp is held high or low, activity is not detected.

Table 61. Clamp Detection Results

Detect	Result
0	No activity detected
1	Activity detected

POLARITY STATUS

0x25 7 Hsync0 Polarity

Indicates the polarity of the HSYNC0 input.

Table 62. Detected Hsync0 Polarity Results

Detect	Result
0	Hsync polarity is negative
1	Hsync polarity is positive

0x25 6 Hsync1 Polarity

Indicates the polarity of HSYNC1 input.

Table 63. Detected Hsync1 Polarity Results

Detect	Result
0	Hsync polarity is negative
1	Hsync polarity is positive

0x25 5 Vsync0 Polarity

Indicates the polarity of Vsync0 input.

Table 64. Detected Vsync0 Polarity Results

Detect	Result
0	Vsync polarity is negative
1	Vsync polarity is positive

0x25 4 Vsync1 Polarity

Indicates the polarity of Vsync1 input.

Table 65. Detected Vsync1 Polarity Results

Detect	Result
0	Vsync polarity is negative
1	Vsync polarity is positive

0x25 3 Coast Polarity

Indicates the polarity of the external Coast signal.

Table 66. Detected Coast Polarity Results

Detect	Result
0	Coast polarity is negative
1	Coast polarity is positive

0x25 2 Clamp Polarity

Indicates the polarity of the clamp signal.

Table 67. Detected Clamp Polarity Results

Detect	Result
0	Clamp polarity is negative
1	Clamp polarity is positive

0x25 1 Extraneous Pulses Detection

A second output from the Hsync filter, this status bit tells whether extraneous pulses are present on the incoming sync signal. Often extraneous pulses are used for copy protection, so this status bit can be used for this purpose.

Table 68. Equalization Pulse Detect Bit

Detect	Result
0	No equalization pulses detected during active Hsync
1	Equalization pulses detected during active Hsync

HSYNC COUNT

0x26 7:0 Hsyncs/Vsync MSB

The eight MSBs of the 12-bit counter that reports the number of Hsyncs/Vsync on the active input. This is useful for determining the mode and is an aid in setting the PLL divide ratio.

0x27 7:4 Hsyncs/Vsync LSBs

The four LSBs of the 12-bit counter that reports the number of Hsyncs/Vsync on the active input.

Test Registers

0x28 7:0 Test Register 0

Must be written to 0xBF for proper operation.

0x29 7:0 Test Register 1

Must be written to 0x00 for proper operation.

0x2A 7:0 Test Register 2

Read-only bits for future use.

0x2B 7:0 Test Register 3

Read-only bits for future use.

0x2C 7:0 Test Register 4

Must be written to 0x00 for proper operation.

0x2C 4 Auto-Offset Hold

A bit for controlling whether the auto-offset function runs continuously or runs once and holds the result. Continuous updates are recommended because it allows the AD9981 to compensate for drift-over time, temperature, and so on. If one-time updates are preferred, these should be performed every time the part is powered up and when there is a mode change. To do a one-time update, first auto-offset must be enabled (0x1B, Bit 5). Next, this bit (auto-offset hold) must be set to 1 to let the auto-offset function operate and settle to a final value. Auto-offset hold should then be set to 0 to hold the offset values that the auto circuitry calculates. The AD9981's auto-offset circuit's maxi-mum settle time is 10 updates. For example, if the update frequency is set to once every 64 Hsyncs, then the maximum settling time would be 640 Hsyncs (10 × 64 Hsyncs).

Table 69. Auto-Offset Hold

Select	Result
0	Disables auto-offset updates and holds the current auto-offset values
1	Allows auto-offset to update continuously

0x2C **3:0** Must be written to 0x0 for proper operation.

0x2D **7:0** **Test Register 5**

Read/write bits for future use. Must be written to 0xE8 for proper operation.

0x2E **7:0** **Test Register 6**

Read/write bits for future use. Must be written to 0xE0 for proper operation.

TWO-WIRE SERIAL CONTROL PORT

A two-wire serial interface control interface is provided. Up to two AD9981 devices may be connected to the two-wire serial interface, with each device having a unique address.

The two-wire serial interface comprises a clock (SCL) and a bi-directional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

The following are the five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/W\ bit (the eighth bit). The R/W\ bit indicates the direction of data transfer, read from 1 or write to 0 on the slave device. If the transmitted slave address matches the address of the device (set by the state of the Serial A0 address [SA0] input pin in Table 70), the AD9981 acknowledges the match by bringing SDA low on the 9th SCL pulse. If the addresses do not match, the AD9981 does not acknowledge it.

Table 70. Serial Port Addresses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
A6 (MSB)	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

DATA TRANSFER VIA SERIAL INTERFACE

For each byte of data read or written, the MSB is the first bit in the sequence.

If the AD9981 does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9981 during a read sequence, the AD9981 interprets this as end-of-data. The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9981 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 0x2E. Any base address higher than 0x2E will not produce an acknowledge signal. Data are read from the control registers of the AD9981 in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte low to set up a sequential read operation. Reading (the R/W\ bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9981, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

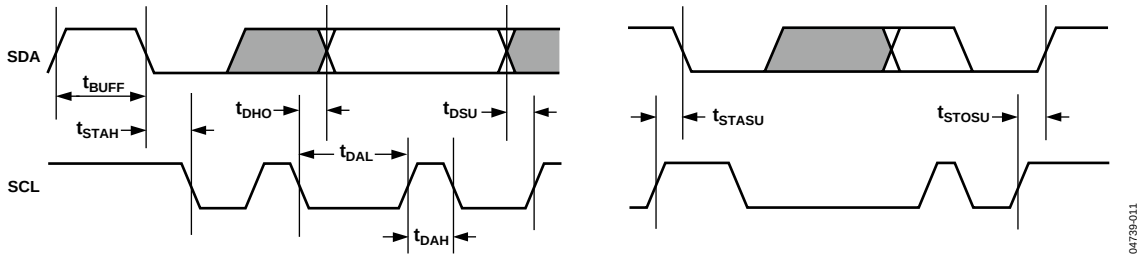


Figure 17. Serial Port Read/Write Timing

Serial Interface Read/Write Examples

Write the following to one control register:

- Start signal
- Slave address byte (R/W\bit = low)
- Base address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers:

- Start signal
- Slave address byte (R/W\bit = low)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one control register:

- Start signal
- Slave address byte (R/W\bit = low)
- Base address byte
- Start signal
- Slave address byte (R/W\ bit = high)
- Data byte from base address
- Stop signal

Read from four consecutive control registers:

- Start signal
- Slave address byte (R/W\bit = low)
- Base address byte
- Start signal
- Slave address byte (R/W\bit = high)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

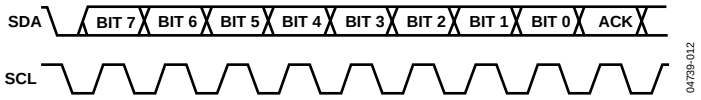


Figure 18. Serial Interface—Typical Byte Transfer

PCB LAYOUT RECOMMENDATIONS

The AD9981 is a high-precision, high-speed analog device. To achieve the maximum performance from the part, it is important to have a well laid-out board. The Analog Interface Inputs section provides a guide for designing a board using the AD9981.

Analog Interface Inputs

Using the following layout techniques on the graphics inputs is extremely important:

1. Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9981 as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they pick up noise from the board and other external sources.

2. Place the 75 Ω termination resistors (see Figure 3) as close as possible to the AD9981 chip. Any additional trace length between the termination resistors and the input of the AD9981 increases the magnitude of reflections, which corrupts the graphics signal.

3. Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω also increases the chance of reflections.

4. The AD9981 has a very high input bandwidth, (200 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it also means that it captures any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

5. Due to the high bandwidth of the AD9981, sometimes low-pass filtering the analog inputs can help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a ferrite bead in series prior to the 75 Ω termination resistor is helpful in filtering excess noise. Specifically, the Fair-Rite #2508051217Z0 was used, but an application could work best with a different bead value. Alternatively, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor is beneficial.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1 μF capacitor. The exception is where two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9981, since that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of the PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_D).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D, from a different, cleaner, power source (for example, from a 12 V supply).

It is also recommended to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to at least place a single ground plane under the AD9981. The location of the split should be at the receiver of the digital outputs. In this case it is even more important to place components wisely because the current loops will be much longer (current takes the path of least resistance). An example of a current loop is power plane to AD9981 to digital output trace to digital data receiver to digital ground plane to analog ground plane.

PLL

Place the PLL loop filter components as close to the FILT pin as possible. Do not place any digital or other high frequency traces near these components. Use the values suggested in the data sheet with 10% tolerances or less.

Outputs (Both Data and Clocks)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance and require more instantaneous current to drive, which creates more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 50 Ω to 200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9981. If series resistors are used, place them as close to the AD9981 pins as possible, (although try not to add vias or extra length to the output trace to get the resistors closer).

If possible, limit the capacitance that each digital output drives to less than 10 pF. This is easily accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside of the AD9981 and creates more digital noise on its power supplies.

Digital Inputs

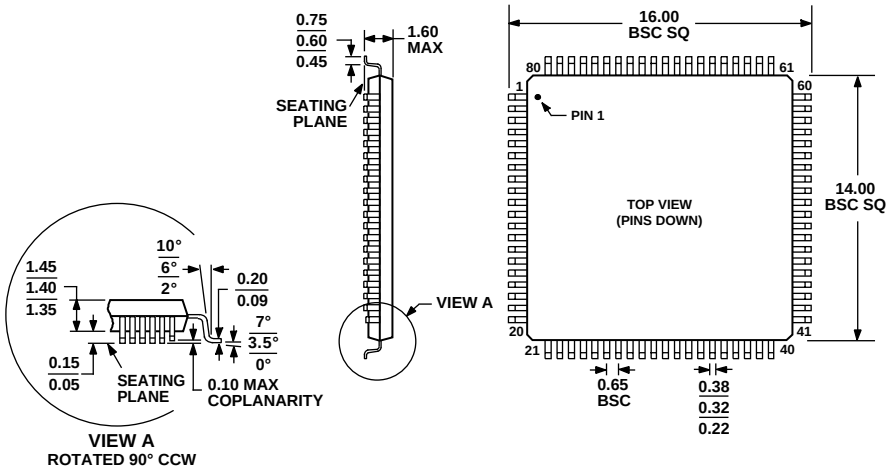
Digital inputs on the AD9981 (HSYNC0, HSYNC1, VSYNC0, VSYNC1, SOGIN0, SOGIN1, SDA, SCL and CLAMP) were designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. Therefore, no extra components need to be added if using 5.0 V logic.

Any noise that gets onto the Hsync input trace adds jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

REFERENCE Bypass

The AD9981 has three reference voltages that must be bypassed for proper operation of the input PGA. REFLO and REFHI are connected to each other through a 10 µF capacitor. REFCM is connected to ground through a 10 µF capacitor. These references are used by the input PGA circuitry to assure the greatest stability. Place them as close to the AD9981 pin as possible. Make the ground connection as short as possible.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 19. 80-Lead Low Profile Quad Flat Pack [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9981KSTZ-80[1]	0°C to +70°C	80-lead LQFP	ST-80-2
AD9981KSTZ-95[1]	0°C to +70°C	80-lead LQFP	ST-80-2
AD9981/PCB		Evaluation Kit	

[1] Z = Pb-free part.

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