10-/12-Bit, Low Power, Broadband MxFE

Data Sheet

AD9961/AD9963

FEATURES

Dual 10-bit/12-bit, 100 MSPS ADC
SNR = 67 dB, f_{IN} = 30.1 MHz
Dual 10-bit/12-bit, 170 MSPS DAC
ACLR = 74 dBc
5 channels of analog auxiliary input/output
Low power, <425 mW at maximum sample rates
Supports full and half-duplex data interfaces
Small 72-lead LFCSP lead-free package

APPLICATIONS

Wireless infrastructure
Picocell, femtocell basestations
Medical instrumentation
Ultrasound AFE
Portable instrumentation
Signal generators, signal analyzers

GENERAL DESCRIPTION

The AD9961/AD9963 are pin-compatible, 10-/12-bit, low power MxFE® converters that provide two ADC channels with sample rates of 100 MSPS and two DAC channels with sample rates to 170 MSPS. These converters are optimized for transmit and receive signal paths of communication systems requiring low power and low cost. The digital interfaces provide flexible clocking options. The transmit is configurable for 1×, 2×, 4×, and 8× interpolation. The receive path has a bypassable 2× decimating low-pass filter.

The AD9961 and AD9963 have five auxiliary analog channels. Three are inputs to a 12-bit ADC. Two of these inputs can be configured as outputs by enabling 10-bit DACs. The other two channels are dedicated outputs from two independent 12-bit DACs.

The high level of integrated functionality, small size, and low power dissipation of the AD9961/AD9963 make them well-suited for portable and low power applications.

FUNCTIONAL BLOCK DIAGRAM

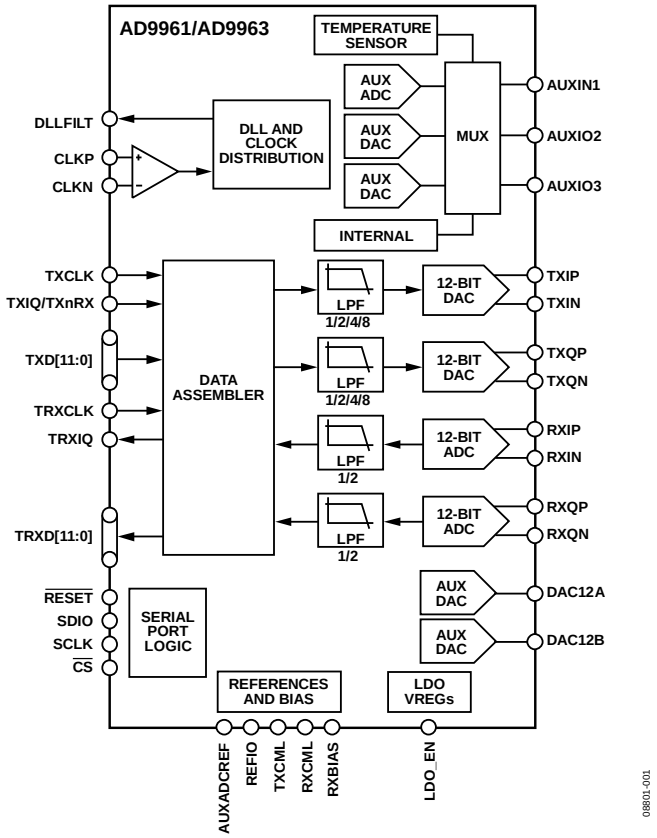

Figure 1.

PRODUCT HIGHLIGHTS

1. High Performance with Low Power Consumption.
   The DACs operate on a single 1.8 V to 3.3 V supply. Transmit path power consumption is <100 mW at 170 MSPS. Receive path power consumption is <350 mW at 100 MSPS from 1.8 V supply. Sleep and power-down modes are provided for low power idle periods.
2. High Integration.
   The dual transmit and dual receive data converters, five channels of auxiliary data conversion and clock generation offer complete solutions for many modem designs.
3. Flexible Digital Interface.
   The interface mates seamlessly to most digital baseband processors.

Rev. A
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REVISION HISTORY

8/12—Rev. 0 to Rev. A

Changes to Table 15 ... 24
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Added DLL Duty Cycle Caution Section ... 46
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Added Example Start-Up Sequences Section ... 58
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7/10—Revision 0: Initial Version

SPECIFICATIONS

T_{MIN} to T_{MAX}, RX33V = TXVDD = CLK33V = DRVDD = AUX33V = 3.3 V. All LDOs enabled, I_{OUTFS} = 2 mA, DAC sample rate = 125 MSPS. No interpolation, unless otherwise noted.

Table 1. Tx Path Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
TxDAC DC CHARACTERISTICS							
Resolution		10			12		Bits
Differential Nonlinearity		0.1			0.3		LSB
Gain Variation (Internal Reference)	−10	0.4	+10	−10	0.4	+10	%FSR
Gain Matching	−2.4	0.4	+2.4	−2.4	0.4	+2.4	%FSR
Offset Error	−0.03		+0.03	−0.03		+0.03	%FSR
Full-Scale Output Current (Default Setting)		2.0			2.0		mA
Output Compliance Range							
TXVDD = 3.3 V, V_{TXCML} = 0 V	−0.5		+1.0	−0.5		+1.0	V
TXVDD = 3.3 V, V_{TXCML} = 0.5 V	+0.7		+1.7	+0.7		+1.7	V
TXVDD = 1.8 V, V_{TXCML} = 0 V	−0.5		+0.8	−0.5		+0.8	V
Offset Temperature Drift		0			0		ppm/°C
Gain Temperature Drift (Internal Reference)		±40			±40		ppm/°C
Tx REFERENCE (DEFAULT REGISTER SETTINGS)							
Internal Reference Voltage (REFIO)		1.02			1.02		V
Output Resistance		10			10		kΩ
Temperature Drift		±25			±25		ppm/°C
Adjustment Range (TXVDD = 3 V)	0.8		1.2	0.8		1.2	V
Adjustment Range (TXVDD = 1.8 V)	0.8		REFIO	0.8		REFIO	V
TxDAC AC CHARACTERISTICS							
Maximum Update Rate	175			175			MSPS
Spurious-Free Dynamic Range							
f_{OUT} = 5 MHz		78			81		dBc
f_{OUT} = 20 MHz		68			70		dBc
Two-Tone Intermodulation Distortion							
f_{OUT1} = 5 MHz, f_{OUT2} = 6 MHz		85			89		dBc
f_{OUT1} = 20 MHz, f_{OUT2} = 21 MHz		78			80		dBc
Noise Spectral Density							
f_{OUT} = 5 MHz		−140			−145		dBm/Hz
f_{OUT} = 20 MHz		−136			−141		dBm/Hz
W-CDMA Adjacent Channel Leakage Ratio, 1 Carrier							
f_{DAC} = 122.88 MHz, f_{OUT} = 11 MHz		70			74		dBc
Tx PATH DIGITAL FILTER INPUT RATES							
SRRC (8× Interpolation Mode)	21.875			21.875			MHz
INT0 (4× Interpolation Mode)	43.75			43.75			MHz
INT1 (2× Interpolation Mode	87.5			87.5			MHz
Transmit DAC (1× Interpolation Mode)	175			175			MHz

T_{MIN} to T_{MAX}, RX33V = TXVDD = CLK33V = DRVDD = AUX33V = 3.3 V. All LDOs enabled, ADC sample rate = 100 MSPS. No decimation, unless otherwise noted.

Table 2. Rx Path Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Rx ADC DC CHARACTERISTICS							
Resolution		10			12		Bits
Differential Nonlinearity		0.1			0.3		LSB
Gain Error		±1			±1		%FSR
Offset Error		±0.5			±0.5		%FSR
Input Voltage Range		1.56			1.56		V p-p diff
Input Capacitance		8			8		pF
Rx ADC AC SPECIFICATIONS							
Maximum Sample Rate	100			100			MSPS
Spurious Free Dynamic Range							
f_{IN} = 10.1 MHz		77			77		dBc
f_{IN} = 70.1 MHz		75			73		dBc
Two-Tone Intermodulation Distortion							
f_{IN1} = 10 MHz, f_{IN2} = 11 MHz		78			82		dBc
f_{IN1} = 29 MHz, f_{IN2} = 32 MHz		76			80		dBc
Signal-to-Noise Ratio							
f_{IN} = 10.1 MHz		61			68		dBFS
f_{IN} = 30.1 MHz		60			67		dBFS
f_{IN} = 70.1 MHz		60			66		dBFS
RXCML OUTPUTS							
Output Voltage		1.4			1.4		V
Output Current			0.1			0.1	mA
Rx DIGITAL FILTER CHARACTERISTICS							
2× Decimation							
Latency (ADC Clock Cycles)	49			49			Cycles
Passband Ripple; f_{OUT}/f_{DAC} ($0.4 \times f_{DATA}$)	0.2			0.2			f_{OUT}/f_{DAC}
Stop-Band Rejection ($f_{DATA} \pm 0.4 \times f_{DATA}$)	70			70			dB

T_{MIN} to T_{MAX}, RX33V = TXVDD = CLK33V = DRVDD = AUX33V = 3.3 V. All LDOs enabled, unless otherwise noted.

Table 3. Auxiliary Converter Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
AUXILIARY DAC12A/AUXDAC12B							
Resolution	12			12			Bits
Differential Nonlinearity		±0.8			±0.8		LSB
Gain Error		±2.0			±2.0		%
Settling Time (±1%)		1			1		µs
AUXILIARY DAC10A/DAC10B (Range = 0.5 V to 1.5 V)							
Resolution	10			10			Bits
Differential Nonlinearity		±1.0			±1.0		LSB
Gain Error		±2.0			±2.0		%
Settling Time (±1%)		10			10		µs
AUXILIARY ADC							
Resolution	12			12			Bits
Differential Nonlinearity	−1.0		+1.0	−1.0		+1.0	LSB
Gain Error (Internal Reference)	−2.0		+2.0	−2.0		+2.0	%
Input Voltage Range	0		3.2	0		3.2	V
Maximum Sample Rate	50			50			kHz

f_{CLK} = 125 MHz, f_{DLL} = 250 MHz, DAC sample rate = 125 MSPS, ADC sample rate = 62.5 MSPS, unless otherwise noted.

Table 4. Power Consumption Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
1.8 V ONLY OPERATION (EXTERNAL 1.8 V)							
CLK33V		1.65			1.65		mA
TXVDD		10.7			10.7		mA
DRVDD		29.4			34.9		mA
DVDD18V		21.0			22.7		mA
CLK18V		3.84			3.84		mA
DLL18V		9.98			9.98		mA
RX18V		79.2			79.2		mA
RX18VF		34.3			34.3		mA
3.3 V ONLY OPERATION (ON-CHIP REGULATORS)							
TXVDD		12.1			12.1		mA
CLK33V		17.0			17.0		mA
RX33V		113			113		mA
DRVDD		93			108		mA
AUX33V		0.55			0.55		mA
SUPPLY VOLTAGE RANGE							
CLK33V, TXVDD (These Supplies Must Be Tied Together)	1.72		3.63	1.72		3.63	V
DRVDD	1.72		3.63	1.72		3.63	V
DVDD18V	1.72		1.89	1.72		1.89	V
CLK18V	1.72		1.89	1.72		1.89	V
DLL18V	1.72		1.89	1.72		1.89	V
RX18V	1.72		1.89	1.72		1.89	V
RX18VF	1.72		1.89	1.72		1.89	V
RX33V	2.50		3.63	2.50		3.63	V
AUX33V (AUXADC Enabled)	3.14		3.63	3.14		3.63	V
AUX33V (AUXADC Disabled)	1.72		3.63	1.72		3.63	V

Table 5. Digital Logic Level Specifications

Parameter	Conditions	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
V_{IN} Logic High	DRVDD = 1.8 V	1.2			V
V_{IN} Logic High	DRVDD = 2.5 V	1.7			V
V_{IN} Logic High	DRVDD = 3.3 V	2.0			V
V_{IN} Logic Low	DRVDD = 1.8 V			0.5	V
V_{IN} Logic Low	DRVDD = 2.5 V			0.7	V
V_{IN} Logic Low	DRVDD = 3.3 V			0.8	V
CMOS OUTPUT LOGIC LEVEL					
V_{OUT} Logic High	DRVDD = 1.8 V	1.35			V
V_{OUT} Logic High	DRVDD = 2.5 V	2.05			V
V_{OUT} Logic High	DRVDD = 3.3 V	2.4			V
V_{OUT} Logic Low	DRVDD = 1.8 V			0.4	V
V_{OUT} Logic Low	DRVDD = 2.5 V			0.4	V
V_{OUT} Logic Low	DRVDD = 3.3 V			0.4	V
DAC CLOCK INPUT					
Differential Peak-to-Peak Voltage		200	400	CLK33V	mV p-p diff
Duty Cycle		45		55	%
Slew Rate		0.1			V/ns
DIRECT CLOCKING					
Clock Rate	CLKP/CLKN inputs	0.1		200	MHz
DLL ENABLED					%
Clock Rate	DLL delay line output	100		310	MHz
SERIAL PERIPHERAL INTERFACE					
Maximum Clock Rate		50			MHz
Minimum Pulse Width High (t_{HIGH})		10			ns
Minimum Pulse Width Low (t_{LOW})		10			ns
Setup Time, SDIO (Data In) to SCLK (t_{DS})		5.0			ns
Hold Time, SDI to SCLK (t_{DH})		5.0			ns
Data Valid, SDIO (Data Out) to SCLK (t_{DV})				5.0	ns
Setup Time, $\overline{CS}$ to SCLK (t_S)		5.0			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect to	Rating
RX33V, AUX33V	RXGND	−0.3 V to +3.9 V
TXVDD	TXGND	−0.3 V to +3.9 V
DRVDD	DGND	−0.3 V to +3.9 V
CLK33V	EPAD	−0.3 V to +3.9 V
RX18V, RX18VF	RXGND	−0.3 to +2.1 V
DVDD18V	EPAD	−0.3 to +2.1 V
CLK18V, DLL18V	EPAD	−0.3 to +2.1 V
RXGND, TXGND, DGND,	EPAD	−0.3 V to +0.3 V
TXIP, TXIN, TXQP, TXQN	TXGND	−1.0 V to TXVDD + 0.3 V
RXIP, RXIN, RXQP, RXQN	RXGND	−0.3 V to RX18V + 0.3 V
$\overline{CS}$, SCLK, SDIO, $\overline{RESET}$, LDO_EN	DGND	−0.3V to DRVDD + 0.3 V
TRXD[11:0], TXD[11:0], TXIQ, TRXIQ, TXCLK, TRXCLK	DGND	−0.3 V to DRVDD + 0.3 V
CLKP, CLKN	EPAD	−0.3 V to CLK33V + 0.3 V
Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Airflow	θ_{JA}	θ_{JB}	θ_{JC}	Unit
1 m/sec	17.1	10.6	1.0	°C/W
0 m/sec	20.3			°C/W

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified for a JEDEC standard 51-7 High-κ thermal test board. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

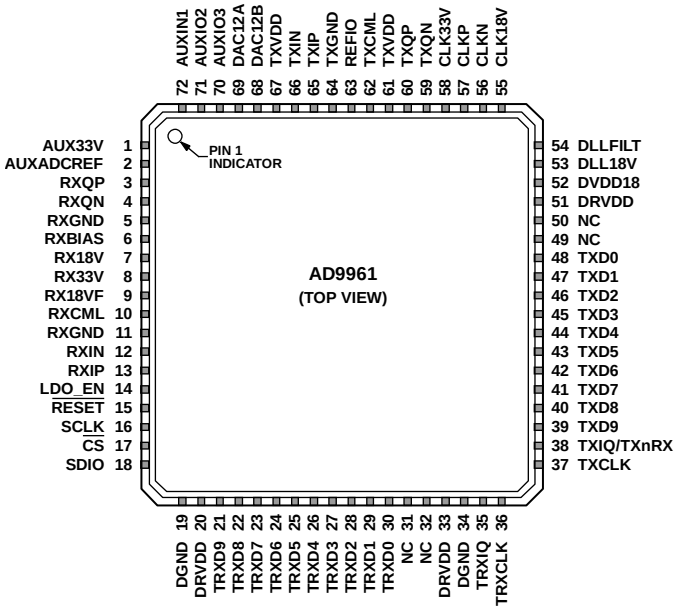
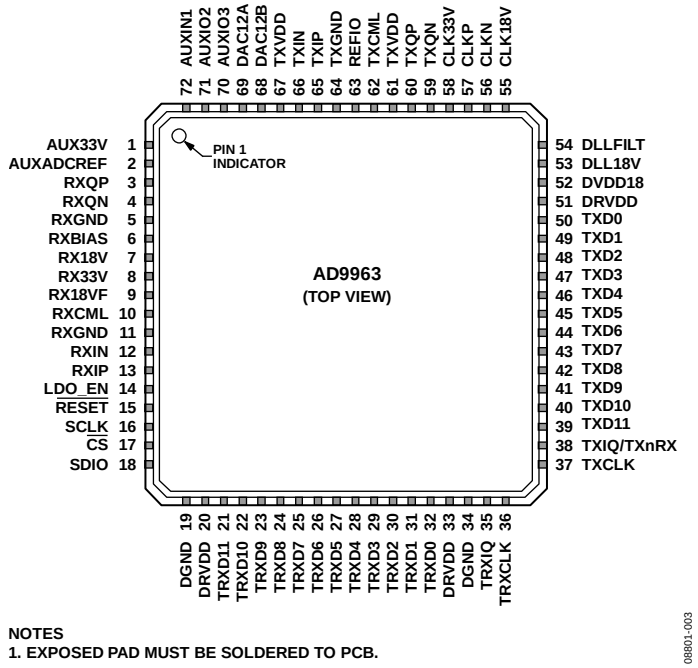


Figure 2. AD9961 Pin Configuration

Table 8. AD9961 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AUX33V	Analog Supply for the Auxiliary ADC and Auxiliary DACs (3.3 V ± 5%, 1.8 V ± 5% If Auxiliary ADC Is Powered Down).
2	AUXADCREF	Reference Output (Or Input) for Auxiliary ADC.
3, 4	RXQP, RXQN	Differential ADC Q Inputs. The default full-scale input voltage range is 1.56 V p-p differential.
5, 11	RXGND	Receive Path Ground.
6	RXBIAS	External Bias Resistor Connection. An optional 10 kΩ resistor can be connected between this pin and the analog ground to improve the accuracy of the full-scale range of the Rx ADCs.
7	RX18V	Output of RX18V Voltage Regulator.
8	RX33V	Input to RX18V and RX18VF Voltage Regulators (2.5 V to 3.3 V). If LDOs are not being used, short Pin 8 to Pin 7.
9	RX18VF	Output of RX18VF Voltage Regulator.
10	RXCML	ADC Common-Mode Voltage Output.
12, 13	RXIN, RXIP	Differential ADC I Inputs. The default full-scale input voltage range is 1.56 V p-p differential.
14	LDO_EN	Control Pin for LDOs (GND = Disable all LDOs, Float = Enable DVDD18 LDO Only, DRVDD = Enable All LDOs).
15	$\overline{\text{RESET}}$	Reset. Active low to reset the configuration registers to default values and reset device.
16	SCLK	Clock Input for Serial Port.
17	$\overline{\text{CS}}$	Active Low Chip Select.
18	SDIO	Bidirectional Data Line for Serial Port.
19, 34	DGND	Digital Core Ground.
20, 33, 51	DRVDD	Input/Output Pad Ring Supply Voltage (1.8 V to 3.3 V).
21 to 30	TRXD9 to TRXD0	ADC Output Data in Full Duplex Mode. ADC output data and DAC input data in half-duplex mode.
31, 32, 49, 50	NC	Not Connected.
35	TRXIQ	Output Signal Indicating from Which ADC the Output Data Is Sourced.

Pin No.	Mnemonic	Description
36	TRXCLK	Qualifying Clock for the TRXD Bus.
37	TXCLK	Qualifying Clock for the TXD Bus. It can be configured as either an input or output.
38	TXIQ/TXnRX	Dual Function Pin. In half-duplex mode (TXnRX), this pin controls the direction of the TRX port. In full-duplex mode (TXIQ), this input signal indicates to which DAC, I or Q, the TxDAC input data is intended.
39 to 48	TXD9 to TXD0	TxDAC Input Data.
52	DVDD18	Digital Core 1.8 V Supply.
53	DLL18V	Output of DLL18V Voltage Regulator.
54	DLLFILT	DLL Filter Output.
55	CLK18V	Output of CLK18V Voltage Regulator.
56, 57	CLKN, CLKP	Differential Input Clock.
58	CLK33V	Input to CLK18V and DLL18V Voltage Regulators (1.8 V to 3.3 V). If LDOs are not being used, short Pin 58 to Pin 55. CLK33V must track TXVDD.
59, 60	TXQN, TXQP	Complementary DAC Q Current Outputs.
61, 67	TXVDD	Analog Supply Voltage for Tx Path (1.8 V to 3.3 V). TXVDD must track CLK33V.
62	TXCML	Common-Mode Input Voltage for the I and Q Tx DACs.
63	REFIO	Decoupling Point for Internal DAC 1.0 V Bandgap Reference. Use a 0.1 µF capacitor to AGND.
64	TXGND	Transmit Path Ground.
65, 66	TXIP, TXIN	Complementary DAC I Current Outputs.
68	DAC12B	Auxiliary DAC B Output.
69	DAC12A	Auxiliary DAC A Output.
70	AUXIO3	Selectable Analog Pin. Programmable to either Input 3 of the auxiliary ADC or to the auxiliary DAC10B output.
71	AUXIO2	Selectable Analog Pin. Programmable to either Input 2 of the auxiliary ADC or to the auxiliary DAC10A output.
72	AUXIN1	Input 1 of Auxiliary ADC.
	EPAD	Thermal Pad Under Chip. This must be connected to AGND for proper chip operation. It provides both a thermal and electrical connection to the PCB.



NOTES
1. EXPOSED PAD MUST BE SOLDERED TO PCB.

Figure 3. AD9963 Pin Configuration

Table 9. AD9963 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AUX33V	Analog Supply for the Auxiliary ADC and Auxiliary DACs (3.3 V ± 10%, 1.8 V ± 10% If Auxiliary ADC Is Powered Down).
2	AUXADCREF	Reference Output (or input) for Auxiliary ADC.
3, 4	RXQP, RXQN	Differential ADC Q Inputs. Full-scale input voltage range is 1.56 V p-p differential.
5, 11	RXGND	Receive Path Ground.
6	RXBIAS	External Bias Resistor Connection. This voltage is nominally 0.5 V. A 10 kΩ resistor can be connected between this pin and analog ground to improve the Rx ADC full-scale accuracy.
7	RX18V	Output of RX18V Voltage Regulator.
8	RX33V	Input to RX18V and RX18VF Voltage Regulators (2.5 V to 3.3 V). If LDOs are not being used, short Pin 8 to Pin 7.
9	RX18VF	Output of RX18VF Voltage Regulator.
10	RXCML	ADC Common-Mode Voltage Output.
12, 13	RXIN, RXIP	Differential ADC I Inputs. Full-scale input voltage range is 1.56 V p-p differential.
14	LDO_EN	Control pin for LDOs (GND = Disable all LDOs, Float = Enable DVDD18 LDO Only, DRVDD = Enable All LDOs).
15	$\overline{\text{RESET}}$	Reset. Active low to reset the configuration registers to default values and reset device.
16	SCLK	Clock Input for Serial Port.
17	$\overline{\text{CS}}$	Active Low Chip Select.
18	SDIO	Bidirectional Data Line for Serial Port.
19, 34	DGND	Digital Core Ground.
20, 33, 51	DRVDD	Input/Output Pad Ring Supply Voltage (1.8 V to 3.3 V).
21 to 32	TRXD11 to TRXD0	ADC Output Data in Full Duplex Mode. ADC output data and DAC input data in half-duplex mode.
35	TRXIQ	Output Signal Indicating from Which ADC the Output Data Is Sourced.
36	TRXCLK	Qualifying Clock for the TRXD Bus.
37	TXCLK	Qualifying Clock for the TXD Bus. It can be configured as either an input or output.
38	TXIQ/TXnRX	Dual Function Pin. In half-duplex mode (TXnRX), this pin controls the direction of the TRX port. In full-duplex mode (TXIQ), this input signal indicates to which DAC, I or Q, the TxDAC Input Data is intended.
39 to 50	TXD11 to TXD0	TxDAC Input Data.
52	DVDD18	Digital Core 1.8 V Supply.
53	DLL18V	Output of DLL18V Voltage Regulator.

Pin No.	Mnemonic	Description
54	DLLFILT	DLL Filter Output.
55	CLK18V	Output of CLK18V Voltage Regulator.
56,57	CLKN, CLKP	Differential Input Clock.
58	CLK33V	Input to CLK18V and DLL18V Voltage Regulators (1.8 V to 3.3 V). If LDOs are not being used, short Pin 58 to Pin 55. CLK33V must track TXVDD.
59, 60	TXQN, TXQP	Complementary DAC Q Current Outputs.
61, 67	TXVDD	Analog Supply Voltage for Tx Path (1.8 V to 3.3V). TXVDD must track CLK33V.
62	TXCML	Common-Mode Input Voltage for the I and Q Tx DACs.
63	REFIO	Decoupling Point for Internal DAC 1.0 V Bandgap Reference. Use a 0.1 µF capacitor to AGND.
64	TXGND	Transmit Path Ground.
65, 66	TXIP, TXIN	Complementary DAC I Current Outputs.
68	DAC12B	Auxiliary DAC B Output.
69	DAC12A	Auxiliary DAC A Output.
70	AUXIO3	Selectable Analog Pin. Programmable to either Input 3 of the auxiliary ADC or to the auxiliary DAC10B output.
71	AUXIO2	Selectable Analog Pin. Programmable to either Input 2 of the auxiliary ADC or to the auxiliary DAC10A output.
72	AUXIN1	Input 1 of Auxiliary ADC.
	EPAD	Thermal Pad Under Chip. This must be connected to AGND for proper chip operation. It provides both a thermal and electrical connection to the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

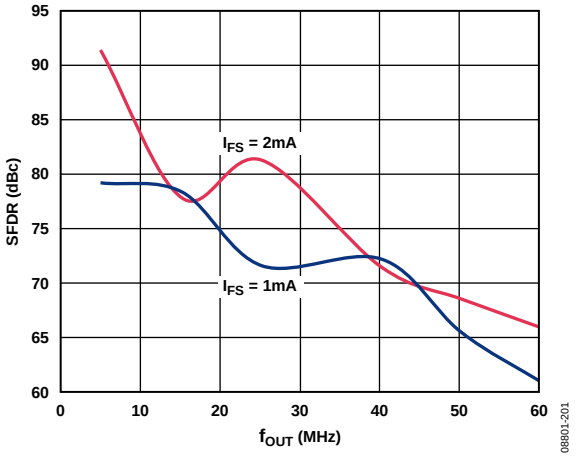


Figure 4. Second Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 1.8 V

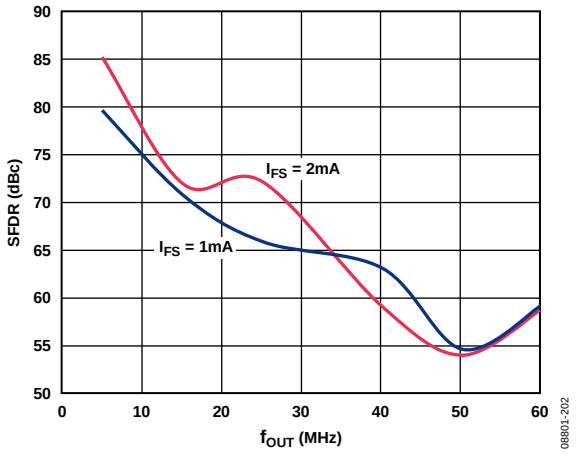


Figure 5. Third Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 1.8 V

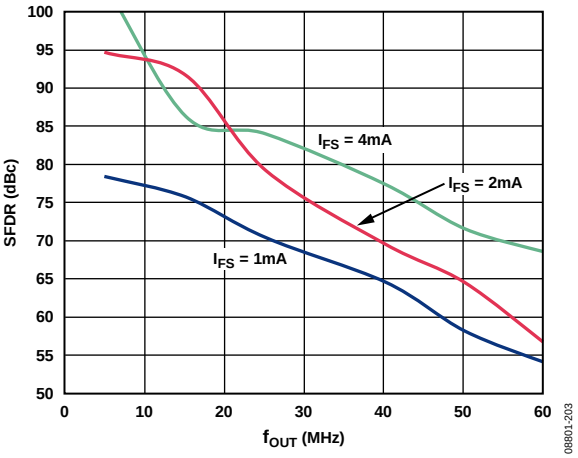


Figure 6. Second Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 3.3 V

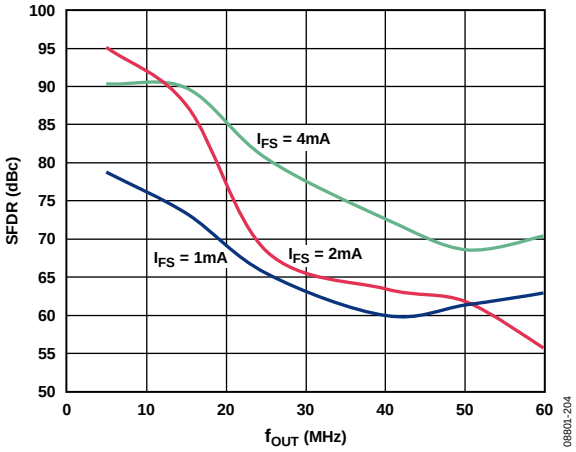


Figure 7. Third Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 3.3 V

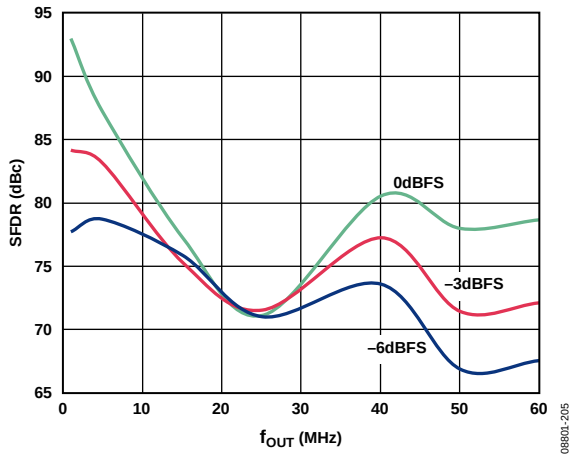


Figure 8. Second Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 1.8 V

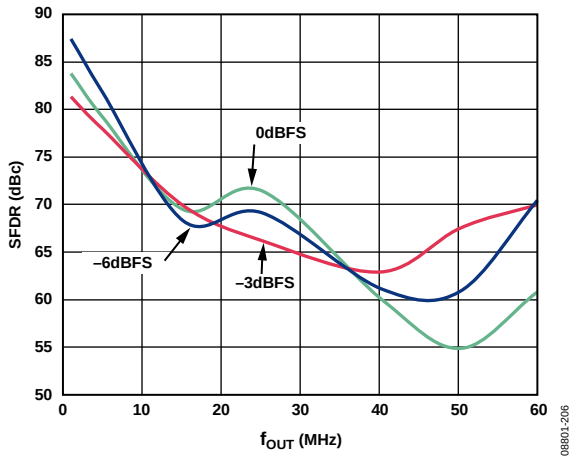


Figure 9. Third Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 1.8 V

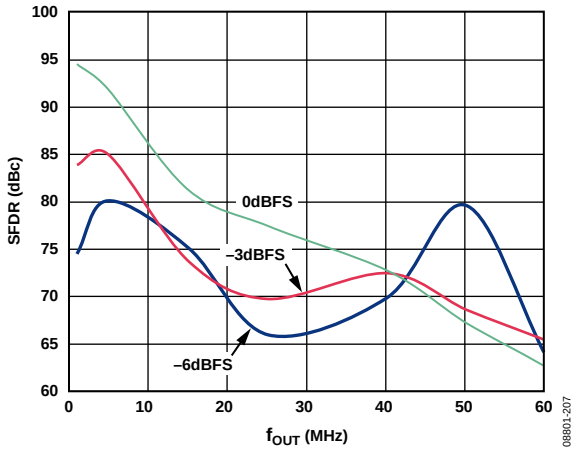


Figure 10. Second Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 3.3 V

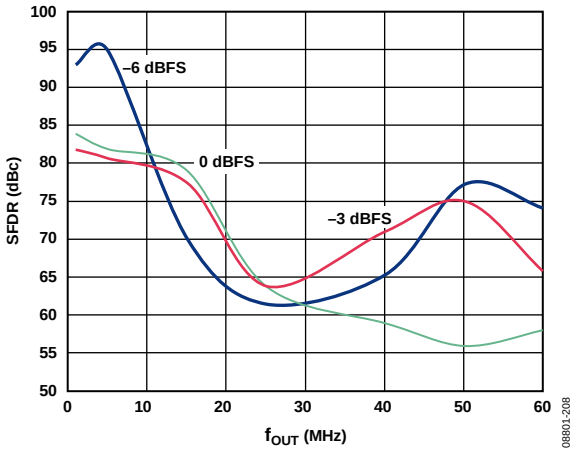


Figure 11. Third Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 3.3 V

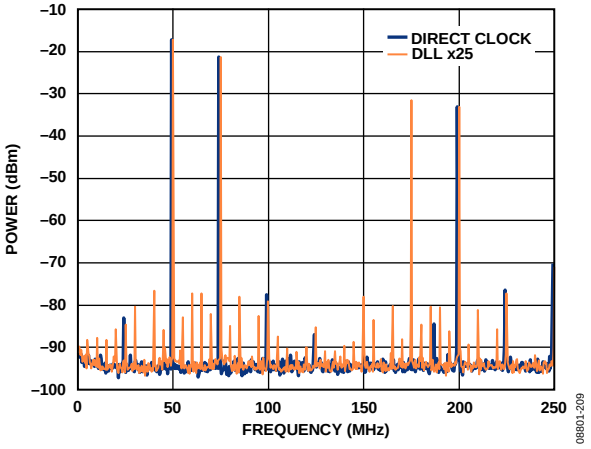


Figure 12. Transmit DAC Output Spectrum, Full-Scale Current = 2 mA, TXVDD = 3.3 V, f_{OUT} = 50 MHz, f_{DAC} = 125 MHz

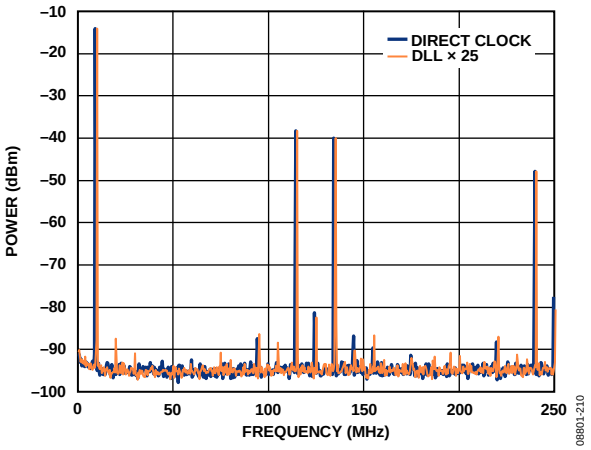


Figure 13. Transmit DAC Output Spectrum, Full-Scale Current = 2 mA, TXVDD = 3.3 V, f_{OUT} = 10 MHz, f_{DAC} = 125 MHz

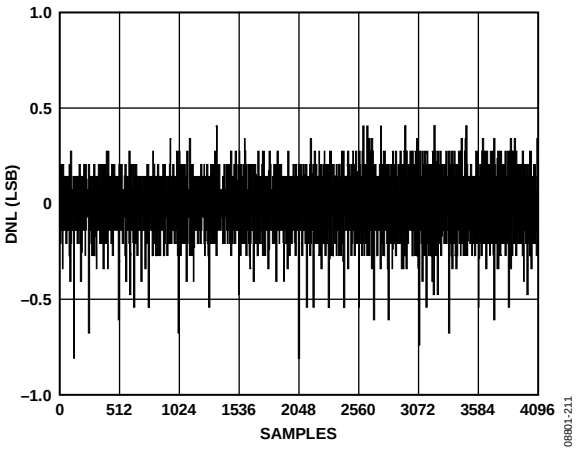


Figure 14. Auxiliary ADC DNL

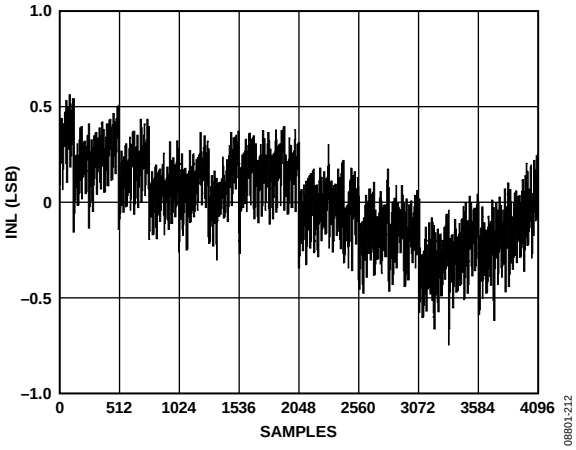


Figure 15. Auxiliary ADC INL

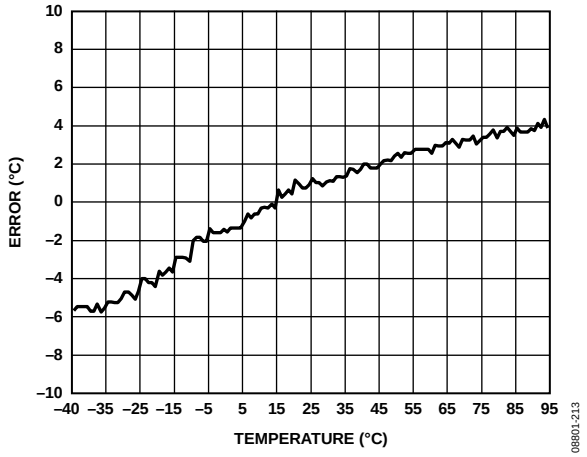


Figure 16. Typical Die Temperature Readback Error vs. Ambient Temperature

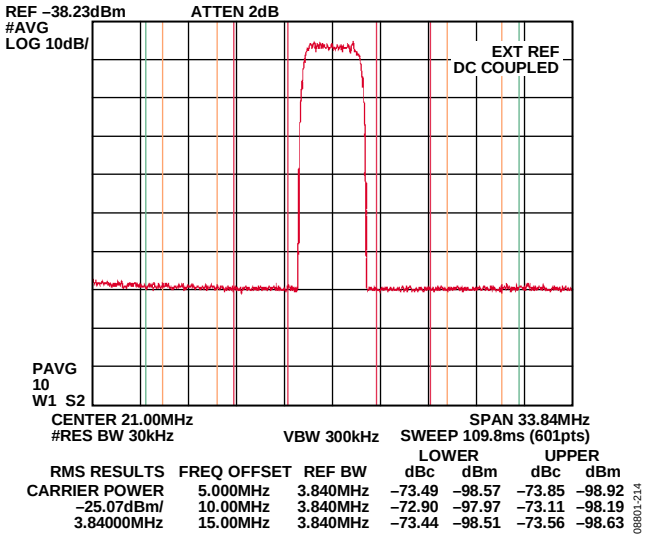


Figure 17. One-Carrier W-CDMA ACLR Performance, IF = ~21 MHz

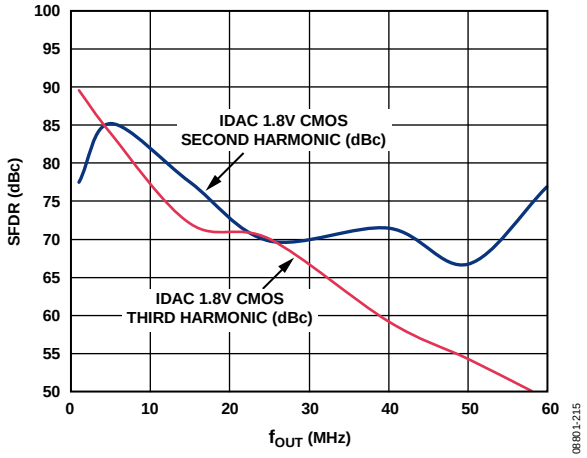


Figure 18. AD9961, Second and Third Harmonic Distortion vs. f_{OUT}, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 1.8 V

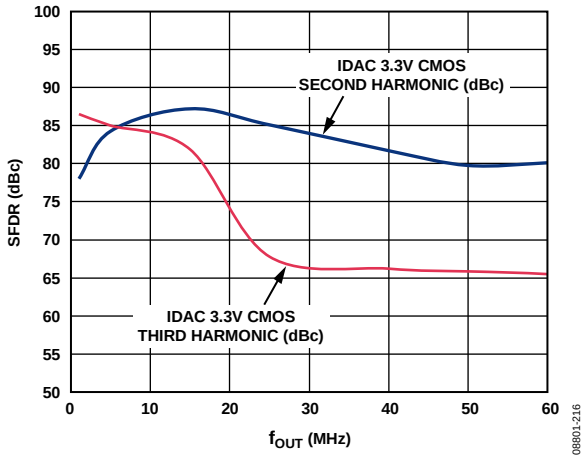


Figure 19. AD9961, Second and Third Harmonic Distortion vs. f_{OUT}, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 3.3 V

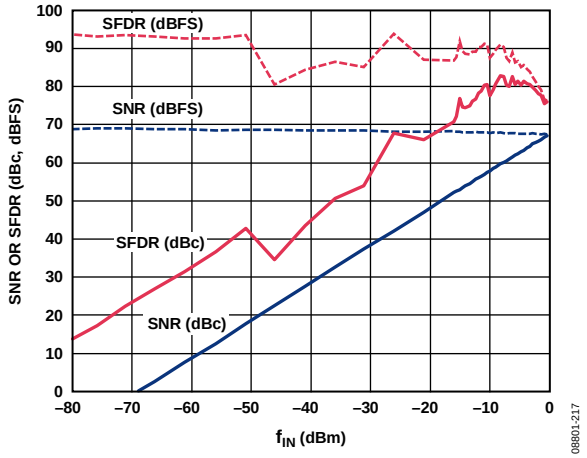


Figure 20. SNR/SFDR vs. Analog Input Level, f_{IN} = 10 MHz, f_{ADC} = 100 MSPS

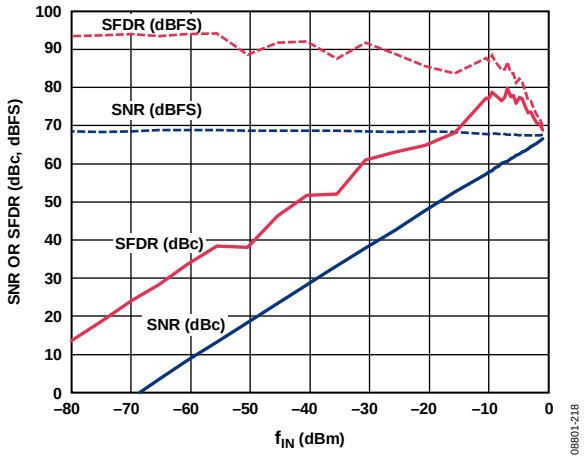


Figure 21. SNR/SFDR vs. Analog Input Level, f_{IN} = 70 MHz, f_{ADC} = 100 MSPS

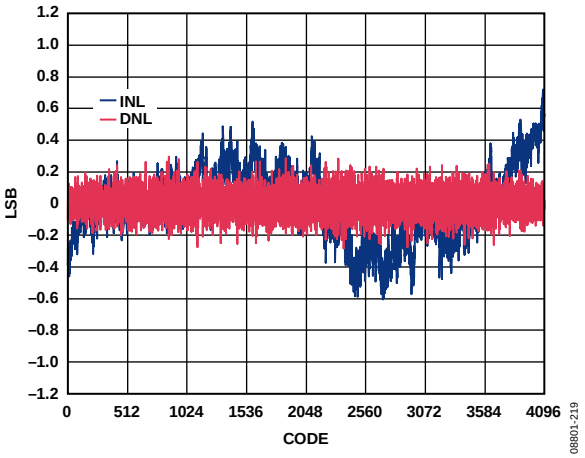


Figure 22. Rx Path ADC, INL and DNL

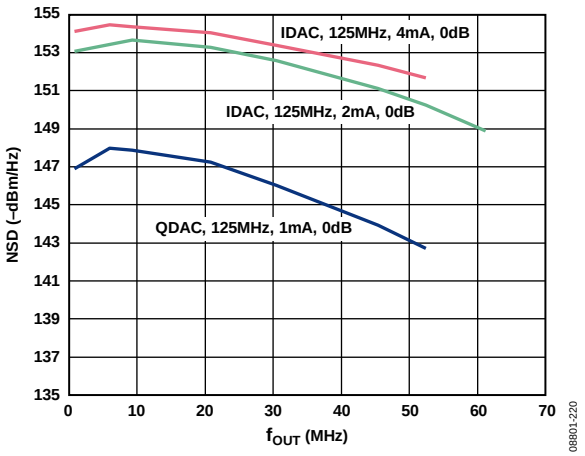


Figure 23. Transmit DAC Noise Spectral Density vs. f_{OUT} Over Full-Scale Current

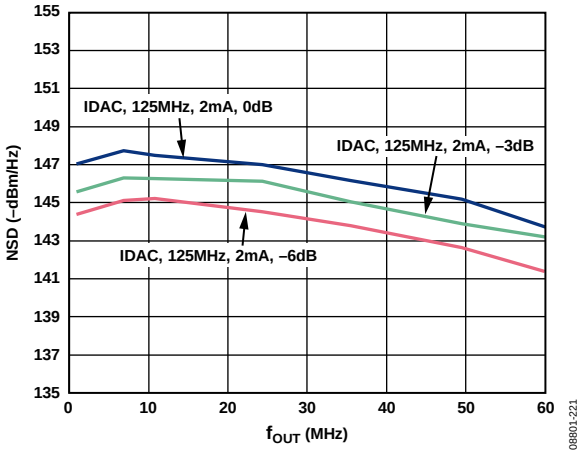


Figure 24. Transmit DAC Noise Spectral Density vs. f_{OUT} Over Digital Scale

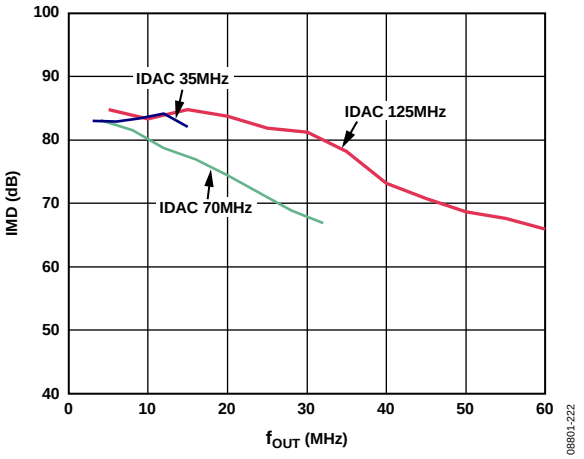


Figure 25. Intermodulation Distortion vs. f_{OUT} Over f_{DAC}, TXVDD = 3.3 V, Full-Scale Current = 2 mA

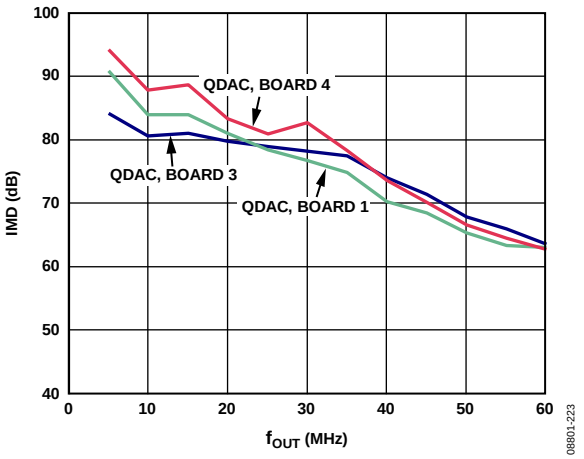


Figure 26. Intermodulation Distortion vs. f_{OUT}, TXVDD = 3.3 V, Full-Scale Current = 2 mA, Board-to-Board Variation

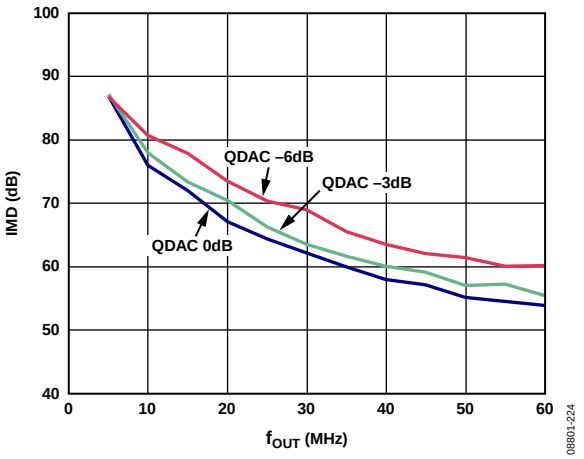


Figure 27. Intermodulation Distortion vs. f_{OUT} Over Digital Scale, TXVDD = 3.3 V, Full-Scale Current = 2 mA

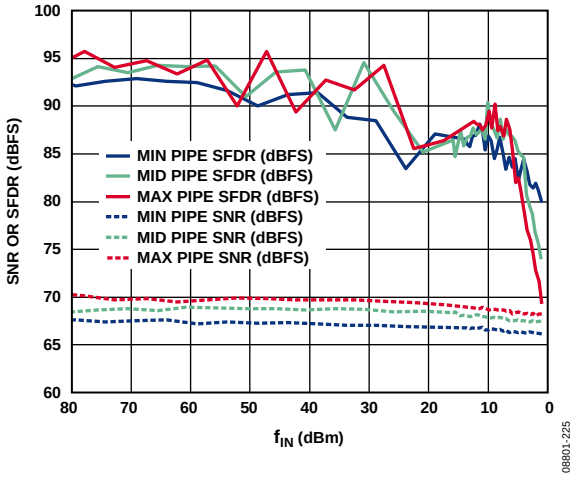


Figure 28. SNR/SFDR vs. Analog Input Level Over Full-Scale Input Range, f_{IN} = 70 MHz, f_{ADC} = 100 MSPS

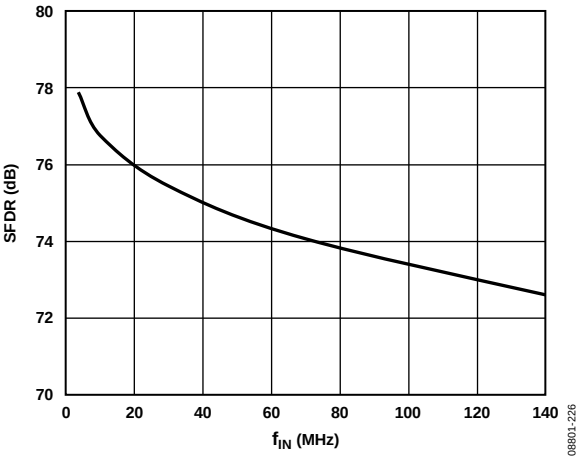


Figure 29. AD9963 100 MSPS Single Tone AC

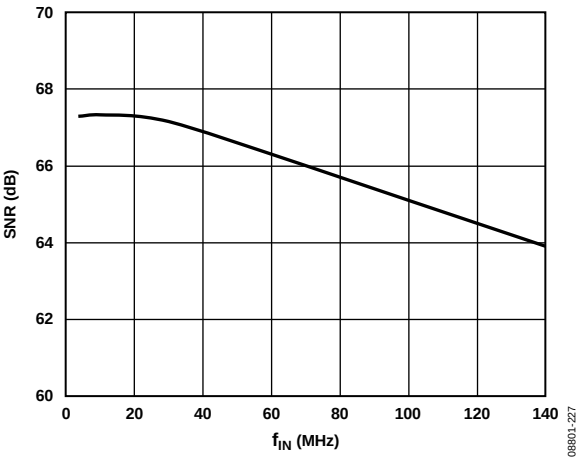


Figure 30. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

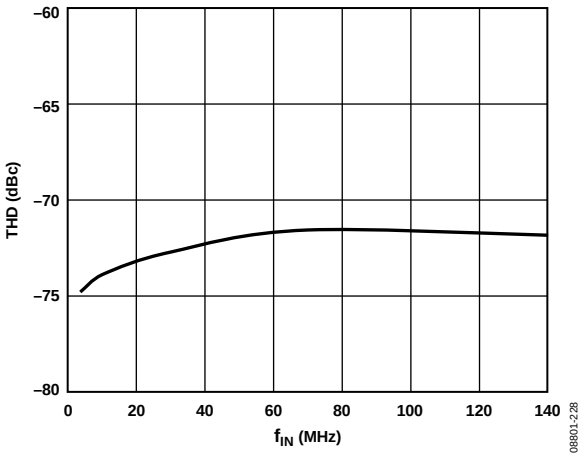


Figure 31. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

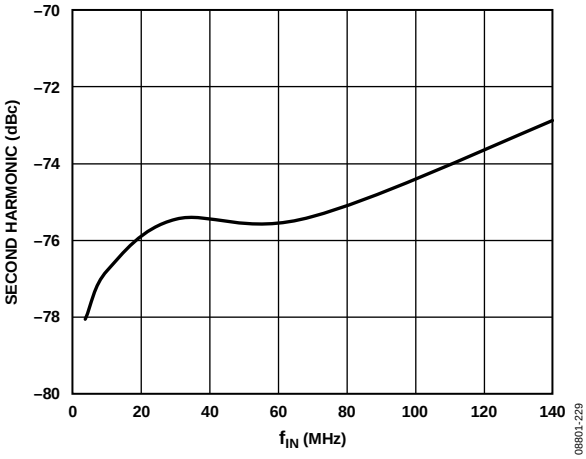


Figure 32. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

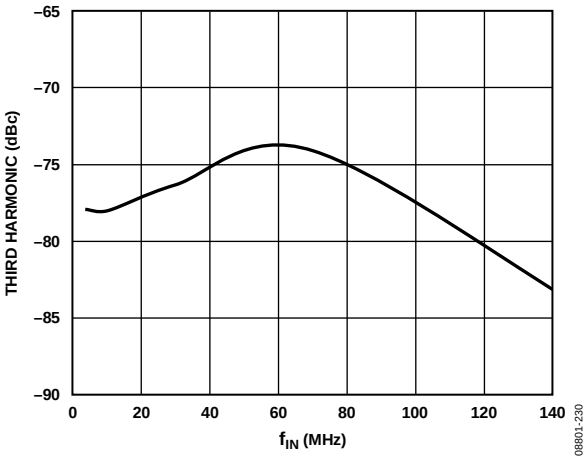


Figure 33. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For TXIN, 0 mA output is expected when the inputs are all 0s. For TXIP, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in parts per million of full-scale range (FSR) per degree Celsius (°C). For reference drift, the drift is reported in parts per ppm/°C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious Free Dynamic Range (SFDR)
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Adjacent Channel Leakage Ratio (ACLR)
The ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9961/AD9963 are targeted to cover the mixed-signal front-end needs of multiple wireless communications systems. They feature a receive path that consists of dual 10-/12-bit receive ADCs and a transmit path that consists of dual 10-/12-bit transmit DACs (TxDAC). The AD9961/AD9963 integrate additional functionality typically required in most systems, such as power scalability, Tx gain control, and clock multiplication circuitry.

The AD9961/AD9963 minimize both size and power consumption to address the needs of a range of applications from the low power portable market to the high performance femto base station market. The part is provided in a 72-lead lead frame chip scale package (LFCSP) that has a footprint of only 10 mm × 10 mm. Power consumption can be optimized to suit the particular application by incorporating power-down controls, low power ADC modes, and TxDAC power scaling.

In full duplex mode, the AD9961/AD9963 use two 12-bit buses, along with qualifying clock signals, to transfer Rx path data and Tx path data. These two buses support either single data rate or double data rate data transfers. The data bus, along with many other device options, is configurable through the serial port by writing internal registers. The device can also be used in a single-port, half-duplex configuration.

SERIAL CONTROL PORT

The AD9961/AD9963 serial control ports are a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. The AD9961/AD9963 serial control ports are compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR® protocols. The serial control port allows read/write access to all registers that configure the AD9961/AD9963. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats.

Serial Control Port Pin Descriptions

The serial control port has three pins, SCLK, SDIO, and $\overline{CS}$:

- SCLK (serial clock) is the input clock used to register serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.
- SDIO (serial data input/output) functions as both the input and output data pin.
- $\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDIO is in a high impedance state and SCLK is disabled. This pin is internally pulled up by a 30 kΩ resistor to DRVDD.

GENERAL OPERATION OF SERIAL CONTROL PORT

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of a communication cycle. There are two parts to a communication cycle with the AD9961/AD9963. The first part writes a 16-bit instruction word into the AD9961/AD9963, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9961/AD9963 serial control ports with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Instruction Header

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the serial port transfer is a read or a write. The next two bits, N1:N0, indicate the length of the transfer in bytes. The final 13 bits are the address (A12 to A0) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bit N1 to Bit N0 (see Table 10).

Table 10. Byte Transfer Count

N1	N0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

A12 to A0 select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. For multibyte transfers, the address is the starting byte address.

Only Address Bits[A7:A0] are needed to cover the range of the 0xFF registers used by the AD9961/AD9963. Address Bits[A12:A8] must always be 0.

Write Transfer

If the instruction header indicates a write operation, the bytes of data written onto the SDIO line are loaded into the serial control port buffer of the AD9961/AD9963. Data bits are registered on the rising edge of SCLK.

The length of the transfer (1 byte, 2 byte, 3 bytes, or streaming mode) is indicated by two bits (N1:N0) in the instruction byte. During a write, streaming mode does not skip over unused or reserved registers; therefore, the user must know what bit pattern to write to the reserved registers to preserve proper operation of the part. It does not matter what data is written to unused registers.

Read Transfer

If the instruction word is for a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by N1:N0. If N = 4, the read operation is in streaming mode, and continues until $\overline{CS}$ is raised. Streaming mode does not skip over reserved or unused registers. The readback data is valid on the falling edge of SCLK.

MSB/LSB First Transfers

The AD9961/AD9963 instruction word and byte data formats can be selected to be MSB first or LSB first. The default for the AD9961/AD9963 is MSB first. When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The internal byte address generator of the serial control port increments for each byte of the multibyte transfer cycle.

When LSB first is set by Register 0x00, Bit 2 and Register 0x00, Bit 6, it takes effect immediately. In multibyte transfers, subsequent bytes reflect any changes in the serial port configuration. To avoid problems reconfiguring the serial port operation, any data written to 0x00 must be mirrored (the eight bits should read the same, forward or backward). Mirroring the data makes it irrelevant whether LSB first or MSB first is in effect. As an example of this mirroring, the default setting for Register 0x00 is 00011000.

Ending Transfers

When the transfer is 1, 2, or 3 bytes, the data transfer ends after the required number of clock cycles have been received. $\overline{CS}$ can be raised after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Raising $\overline{CS}$ on a non byte boundary resets the serial control port.

The AD9961/AD9963 serial control port register addresses decrement from the register address just written toward 0x00 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the register address of the serial control port increments from the address just written toward 0xFF for multibyte I/O operations.

Streaming mode transfers always terminate when $\overline{CS}$ is raised. Streaming mode transfers also terminate whenever the address reaches 0xFF. Note that unused addresses are not skipped during multibyte I/O operations. To avoid unpredictable device behavior, do not write to reserved registers.

Table 11. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
LSB First	Increment	0xFD, 0xFE, 0xFF, stop
MSB First	Decrement	0x01, 0x00, 0xFF, stop

SUB SERIAL INTERFACE COMMUNICATIONS

The AD9963/AD9961 have two registers that require a different communication sequence. These registers are 0x0F and 0x10. The write sequence for these two registers requires a write to Register 0x05, a write to the Register (0x0F or 0x10), and then a write to Register 0xFF. The write takes effect when the write to Register 0xFF is completed.

For example, to enable the RXCML pin output buffer, the register write sequence is:

1. Write 0x03 into Register 0x05. This addresses both of the Rx ADCs.
2. Write 0x02 into Register 0x0F. This sets the RXCML enable bit.
3. Write 0x01 into Register 0xFF. This updates the internal register, which activates the RXCML buffer.
4. Write 0x00 into Register 0x05. This returns the SPI to the normal addressing mode.

An example of updating Register 0x10 is given in the ADC Digital Offset Adjustment section.

Table 12. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	N1	N0	0	0	0	0	0	A7	A6	A5	A4	A3	A2	A1	A0

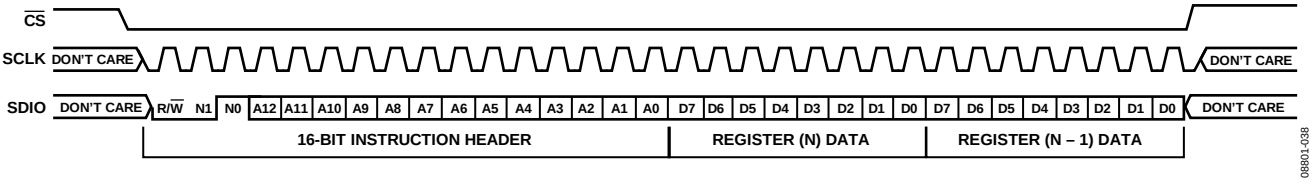


Figure 34. Serial Control Port Access—MSB First, 16-Bit Instruction, 2-Byte Data

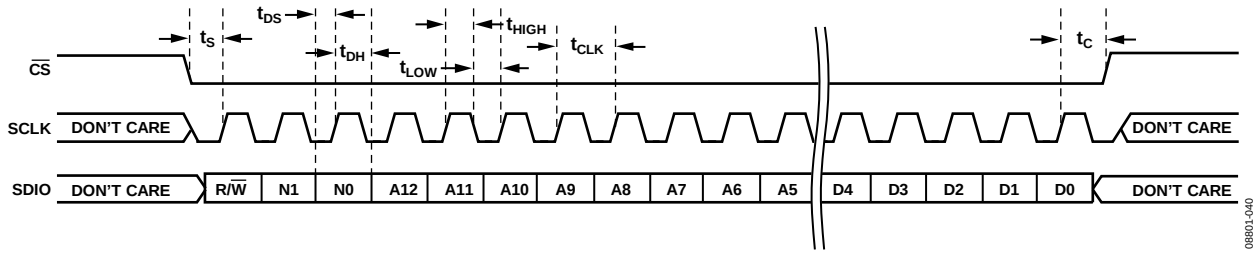


Figure 35. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

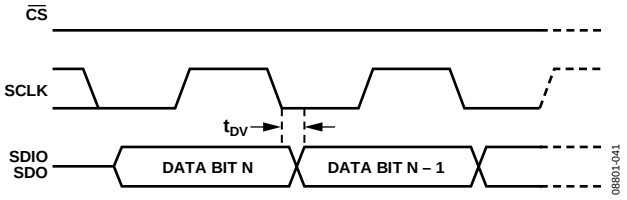


Figure 36. Timing Diagram for Serial Control Port Register Read

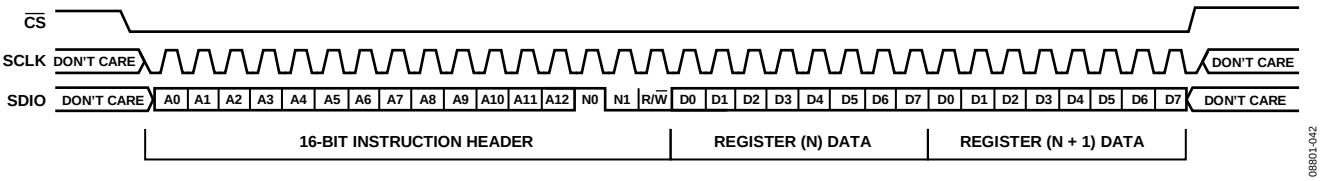


Figure 37. Serial Control Port Access—LSB First, 16-Bit Instruction, Two Bytes Data

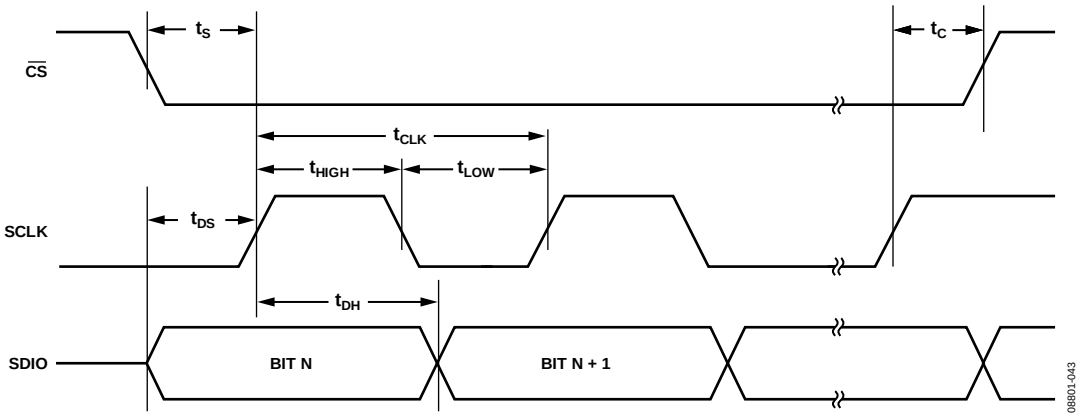


Figure 38. Serial Control Port Timing—Write

Table 13. Serial Control Port Timing

Parameter	Timing (Min, ns)	Description
t_{DS}	5.0	Setup time between data and rising edge of SCLK.
t_{DH}	5.0	Hold time between data and rising edge of SCLK.
t_{CLK}	20.0	Period of the clock.
t_S	5.0	Setup time between $\overline{CS}$ falling edge and SCLK rising edge (start of communication cycle).
t_C	2	Setup time between SCLK rising edge and $\overline{CS}$ rising edge (end of communication cycle).
t_{HIGH}	10	Minimum period that SCLK should be in a logic high state.
t_{LOW}	10	Minimum period that SCLK should be in a logic low state.
t_{DV}	5.0	SCLK to valid SDIO and SDO (see Figure 36).

CONFIGURATION REGISTERS

Table 14. Configuration Register Map

Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	0x18	SDIO	LSB First	Reset	1	1	Reset	LSB First	SDIO
0x05	0x00	Unused						ADDRQ	ADDRI
0x0F	0x00							RXCML	
0x10	0x00	Unused		ADC_OFFSET[5:0]					
0x30	0x3F	Unused		DEC_BP	INT1_BP	INT0_BP	SRRC_BP	TXCLK_EN	RXCLK_EN
0x31	0xA7	TX_SDR	TXCKO_INV	TXCLK_MD[1:0]		TXCKI_INV	TXIQ_HILO	TX_IFIRST	TX_BNRY
0x32	0xA7	RX_SDR	Unused	RXCLK_MD[1:0]		RXCLK_INV	RXIQ_HILO	RX_IFIRST	RX_BNRY
0x33	Varies	Unused	FIFO_INIT	Aligned	ALIGN_ACK	ALIGN_REQ	FIFO_OFFSET[2:0]		
0x34	Varies	FIFO_LVL[7:0]							
0x35	0x10	Unused			SRRC_SCALE[4:0]				
0x36	0x08	Unused			INT0_SCALE[4:0]				
0x37	0x10	Unused			INT1_SCALE[4:0]				
0x38	0x06	Unused			DEC_SCALE[4:0]				
0x39	0x00	RXDLLRST	TXDLLRST	Unused		RXDLL_LKD	TXDLL_LKD	RXDBL_SEL	TXDBL_SEL
0x3A	0x51	TX_UNLOCK[1:0]		TX_LOCK[1:0]		TX_DLYOFS[1:0]		TX_HYST[1:0]	
0x3B	0x51	RX_UNLOCK[1:0]		RX_LOCK[1:0]		RX_DLYOFS[1:0]		RX_HYST[1:0]	
0x3C	0xF0	DBL_TAPDLY[7:0]							
0x3D	0x00	Unused				RX_INVQ	RX_INVI	TX_INVQ	TX_INVI
0x3E	0x09	Unused		TX_DBLPW[2:0]			RX_DBLPW[2:0]		
0x3F	0x07	Unused	RX_CLK	RX_BUS	SINGLERX	TXCLK_MD	HD_BUSCTL	HD_CLKMD	FULL_DUPLEX
0x40	0x01	DAC12B_EN	DAC12A_EN	DAC12B_TOP	DAC12A_TOP	Unused		AUXDAC_REF	DAC_UPDATE
0x41	0x00	DAC12A[11:4]							
0x42	0x00	Unused				DAC12A[3:0]			
0x43	0x00	DAC12B[11:4]							
0x44	0x00	Unused				DAC12B[3:0]			
0x45	0x00	DAC10B_EN	Unused		DAC10B_TOP[2:0]			DAC10B_RNG[1:0]	
0x46	0x00	DAC10B[9:2]							
0x47	0x00	Unused						DAC10B[1:0]	
0x48	0x00	DAC10A_EN	Unused		DAC10A_TOP[2:0]			DAC10A_RNG[1:0]	
0x49	0x00	DAC10A[9:2]							
0x4A	0x00	Unused						DAC10A[1:0]	
0x50	0x00	Unused			TX_PTTRN	TX_INSEL	TX_CONT	TX_START	TX_BISTEN
0x51	0x00	Unused			RX_PTTRN	RX_INSEL	RX_CONT	RX_START	RX_BISTEN
0x52	0x93	TXI_CHK[15:8]							
0x53	0x34	TXI_CHK[7:0]							
0x54	0x5F	TXQ_CHK[15:8]							
0x55	0x36	TXQ_CHK[7:0]							
0x5C	0x08	Chip ID[7:0]							
0x60	0x00	DLL_EN	TXDAC_PD	TXI_SLEEP	TXQ_SLEEP	CLK_PD	RXADC_PD	RXQ_SLEEP	RXI_SLEEP
0x61	0x00	Unused	DLL_LDO_PD	DLLBIAS_PD	CLK_LDO_PD	RX_LDO_PD	RXF_LDO_PD	AUXADC_PD	AUX_REF_PD
0x62	0xF8	DLL_LDO_STAT	CLK_LDO_STAT	RX_LDO_STAT	RXF_LDO_STAT	DIG_LDO_STAT	Unused	Unused	RSET_SEL
0x63	0x00	TRXD_DRV		TRXIQ_DRV		TRXCLK_DRV		TXCLK_DRV	
0x66	0x28	TXI_DCLK	TXQ_DCLK	Unused	RXI_DCLK	RXQ_DCLK	DCS_BP	ADCDIV[1:0]	
0x68	0x00	Unused		IGAIN1[5:0]					
0x69	0x00	Unused		IGAIN2[5:0]					
0x6A	0x00	Unused		IRSET[5:0]					
0x6B	0x00	Unused		QGAIN1[5:0]					
0x6C	0x00	Unused		QGAIN2[5:0]					
0x6D	0x00	Unused		QRSET[5:0]					
0x6E	0x40	Unused		REFIO_ADJ[5:0]					

Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x71	0x00	ADCCLKSEL	DACCLKSEL	Unused	DLL_REF_EN	N[3:0]			
0x72	0x01	DLL_Locked	DLLDIV		M[4:0]				
0x75	0x00	0				DLL_RESB	0		
0x77	0x00	CONV_TIME[1:0]		Unused			AUXADC_CH[2:0]		
0x78	Varies	AUXADC[11:4]							
0x79	Varies	AUXADC[3:0]				CONV_COMPL	CHAN_SEL[2:0]		
0x7A	0x00	AUXADC_EN	AUXADC_RESB	Unused			AUXDIV[2:0]		
0x7B	0x00	TMPSNS_EN	Unused		AUXREF_ADJ[2:0]			Unused	
0x7D	0x00	Unused			RX_FSADJ[4:0]				
0x7E	0x00	Unused	RXTrim_EN	RXTrim_Fine	AUXCML_EN	0			RX_DC
0x7F	0x00	RXI_Trim[9:2]							
0x80	0x00	Unused					RXI_Trim[1:0]		GAINCAL_ENI
0x81	0x00	RXQ_Trim[9:2]							
0x82	0x00	Unused					RXQ_Trim[1:0]		GAINCAL_ENQ
0xFF	0x00	Unused							Update

CONFIGURATION REGISTER BIT DESCRIPTIONS

Table 15.

Register Name	Register Address	Bit(s)	Parameter	Function
Serial Port Config	0x00	7, 0	SDIO	0: use SDIO as both input and output data 1: use SDIO pin as input data only
		6, 1	LSB_First	0: first bit of serial data is MSB of data byte. 1: first bit of serial data is LSB of data byte.
		5, 2	RESET	A transition from 0 to 1 on this bit resets the device. All registers but Register 0x00 revert to their default values.
ADC Address	0x05	1:0	ADDRQ, ADDRI	Bits are set to determine which device on chip receives ADC specific write commands. ADC specific write commends include writes to Registers 0x0F and Register 0x10. These writes also require a rising end on the Update bit (Register 0xFF, Bit 0). 00: no ADCs are addressed. 01: I ADC is addressed. 10: Q ADC is addressed 11: both I and Q ADCs are addressed.
CM Buffer Enable	0x0F	1	RXCML	Enable control for the RXCML output buffer. Note that updating this bit also requires writing to Register 0x05 and Register 0xFF as described in the Sub Serial Interface Communications section. 0: RXCML pin is high impedance. 1: RXCML pin is a low impedance 1.4 V output.
ADC Offset	0x10	5:0	ADC_OFFSET[5:0]	Adds a dc offset to the ADC output of whichever ADC is addressed by Register 0x05. The offset applied is as follows: 011111: offset = +31 LSBs … 000001: offset = +1 LSB 000000: offset = 0 LSB 111111: offset = −1 LSB … 100000: offset = −32 LSBs
Digital Filters	0x30	7:6	Unused	
		5	DEC_BP	1: bypass 2× decimator in Rx path (D0).
		4	INT1_BP	1: bypass 2× Half-Band Interpolation Filter 1 (INT1).
		3	INT0_BP	1: bypass 2× Half-Band Interpolation Filter 0 (INT0).

Register Name	Register Address	Bit(s)	Parameter	Function
		2	SRRC_BP	1: bypass 2× SRRC interpolation filter (SRRC). The filter chain is SRRC→INT0→INT1. If SRRC filter is enabled, the other two filters are enabled too.
		1	TXCLK_EN	1: enables data clocks for transmit path.
		0	RxNTx	0: in HD SPI pin mode, TRx port operates in Tx mode. 1: in HD SPI pin mode, TRx port operates in Rx mode.
Tx Data Interface	0x31	7	TX_SDR	0: chooses DDR clocking mode. Tx data is driven out on both edges of the TXCLK signal. 1: chooses bus rate clocking mode. Tx data is driven out on one edge of the TXCLK signal.
		6	TXCKO_INV	This signal inverts the phase of the transmit path output clock signal. 0: does not invert TxCLK output. 1: inverts TxCLK output.
		5:4	TXCLK_MD[1:0]	Controls the mode of the TXCLK pin. The TXCLK pin can be configured as an input or an output. When configured as an output, it can have two possible sources, the internal TXCLK signal or the DLL output signal. 00: disabled. 01: the TXCLK pin is configured as an input. 10: the TXCLK pin is configured as an output. The source signal is the transmit path clock signal. 11: the TXCLK pin is configured as an output. The source signal is the DLL output signal. Note that the TXCLK signal may appear on either the TXCLK pin or the TRXCLK pin, depending on the mode of the device. In Half-Duplex 1-Clock mode, this signal is present on the TRXCLK pin when TX is active. In Half-Duplex 2-Clock mode and Full-Duplex mode, this signal is present on the TXCLK pin.
		3	TXCKI_INV	Selects which edge of the TXCLK signal samples the transmit path data. 0: TXPCLK negative edge latches transmit path data. 1: TXPCLK positive edge latches transmit path data.
		2	TXIQ_HILO	Data appears on the TXD bus sequentially but is loaded into the transmit path in pairs. TXIQ_HILO selects how the TXIQ signal marks each data pair. 0: each data pair is marked by TXIQ being low then high. 1: each data pair is marked by TXIQ being high then low.
		1	TX_IFIRST	This bit sets the data pairing order of the I and Q samples on transmit path. 0: selects that Q is first, followed by I. 1: selects that I is first, followed by Q.
		0	TX_BNRY	This bit selects the data format of the transmit path data. 0: Tx binary. 1: Tx twos complement.
Rx Data Interface	0x32	7	RX_SDR	0: chooses DDR clocking mode. Rx data is driven out on both edges of the TRXCLK signal. 1: chooses bus rate clocking mode. Rx data is driven out on one edge of the TRXCLK signal.
		6	Unused	
		5:4	RXCLK_MD[1:0]	This sets the way the internal RXCLK signal in the chip is driven. 00: disabled. 01: disabled. 10: RXCLK is driven by internal Rx path clock.

Register Name	Register Address	Bit(s)	Parameter	Function
				11: RXCLK is driven by the DLL output. Note that the RXCLK signal is present on the TRXCLK pin with one exception. In Half-Duplex 1-Clock mode, the RXCLK signal is present on the TRXCLK pin when Rx is active, but the TXCLK signal appears on the TRXCLK pin when TX is active.
		3	RXCLK_INV	0: uses TRxCLK negative edge to drive out Rxdata. 1: uses TRxCLK positive edge to drive out Rxdata.
		2	RXIQ_HILO	Data appears on the RXD bus sequentially but is sampled in the Rx path in pairs. RXIQ_HILO selects how the RXIQ signal marks each data pair. 0: each data pair is marked by RXIQ being low then high. 1: each data pair is marked by RXIQ being high then low.
		1	RX_IFIRST	The Rx path I and Q ADCs sample simultaneously producing a pair of samples. Because the RXD bus is shared, the sampled I and Q data appears on the TRXD bus sequentially. This bit determines the order of the paired samples. 0: Q appears first on Rx path. 1: I appears first on Rx path.
		0	RX_BNRY	0: straight binaryon Rx path. 1: twos compliment on Rx path.
FIFO Alignment	0x33	7	Unused	
		6	Unused	
		5	Unused	
		4	Unused	
		3	ALIGN_REQ	1: request FIFO read and write pointers alignment
		2:0	FIFO_OFFSET[2:0]	Sets the FIFO read and write pointer phase offset following FIFO reset. Normally this should be set to 000 to set the FIFO to half full.
FIFO Status	0x34	7:0	FIFO_LVL[7:0]	For valid transmit data path operation, the FIFO should be running half full, that is, it should always contain 4 valid DAC input samples for each DAC. FIFO_LVL values of 00011110, 00011111, 000001110, and 00001111 all indicate that the FIFO is half full. This phenomenon is due to ambiguities in reading back the FIFO_LVL level from this register using the SPI port versus the actual FIFO pointer values.
Tx Scale P	0x35	7:5	Unused	
		4:0	SRRC_SCALE[4:0]	Value of 1.4 multiplier applied to both I and Q channels just after the SRRC filter. 00000: multiply by 0.0. 00001: multiply by 0.0625. … 11111: multiply by 1.9375.
Tx Scale 0	0x36	7:5	Unused	
		4:0	INT0_SCALE[4:0]	Value of 1.4 multiplier applied to both I and Q channels just after Interpolation Filter 0.
				00000: multiply by 0.0. 00001: multiply by 0.0625. …
Tx Scale 1	0x37	7:5	Unused	11111: multiply by 1.9375.
		4:0	INT1_SCALE[4:0]	Value of 1.4 multiplier applied to both I and Q channels just after Interpolation Filter 1. 00000: multiply by 0.0. 00001: multiply by 0.0625. 11111: multiply by 1.9375.

Register Name	Register Address	Bit(s)	Parameter	Function
Rx Scale	0x38	7:5	Unused	
		4:0	DEC_SCALE[4:0]	Value of 3.2 multiplier applied to both I and Q channels just after the decimation filter. The value of the gain applied is equal to DEC_SCALE/4. 00000: multiply by 0.0. 00001: multiply by 0.25. 11111: multiply by 7.75.
Clock Doubler Config	0x39	7	RXDDLLRST	1: resets the Rx signal path clock doubler.
		6	TXDDLLRST	1: resets the Tx signal path clock doubler.
		5:4	Unused	
		3	Unused	.
		2	Unused	
		1	RXDBL_SEL	0: selects fixed pulse width clock doubler. 1: selects fixed duty cycle clock doubler. See Table 22 for configuration recommendations.
		0	TXDBL_SEL	0: selects fixed pulse width clock doubler. 1: selects fixed duty cycle clock doubler. See Table 22 for configuration recommendations.
TX Clock Doubler Config	0x3A	7:4	TX_UNLOCK[1:0]	Sets the number of clock cycles for the unlock indicator. Set to 01.
		3	TX_LOCK[1:0]	Sets the number of clock cycles for the lock indicator. Set to 01.
		2	TX_DLYOFS[1:0]	Sets delay line offset of clock doubler. Set to 01.
		1	TX_HYST[1:0]	Sets delay line hysteresis of clock doubler. Set to 01.
RX Clock Doubler Config	0x3B	7:4	RX_UNLOCK[1:0]	Sets the number of clock cycles for the unlock indicator. Set to 01.
		3	RX_LOCK[1:0]	Sets the number of clock cycles for the lock indicator. Set to 01.
		2	RX_DLYOFS[1:0]	Sets delay line offset of clock doubler. Set to 01.
		1	RX_HYST[1:0]	Sets delay line hysteresis of clock doubler. Set to 01.
Clock Doubler Config	0x3C	7:0	DBL_TAPDLY[7:0]	Sets the initial tap delay of the Rx and Tx clock doublers. Set to 0x00.
Data Spectral Inversion	0x3D	7:4	Unused	
		3	RX_INVQ	1: multiply Rxdata from QADC by −1.
		2	RX_INVI	1: multiply Rxdata from IADC by −1.
		1	TX_INVQ	1: multiply Txdata for QDAC by −1.
		0	TX_INVI	1: multiply Txdata for IDAC by −1.
Clock Doubler Pulse Width	0x3E	7:6	Unused	
		5:3	TX_DBLPW[2:0]	Sets the pulse width of the Tx clock doubler. See Table 22 for details.
		2:0	RX_DBLPW[2:0]	Sets the pulse width of the Rx clock doubler. See Table 22 for details.
Rx Data Interface	0x3F	7	Unused	
		6	RX_CLK	0: when SINGLERX is active, use Q side clock. 1: when SINGLERX is active, use I side clock.
		5	RX_BUS	0: when SINGLERX is active, use the Q ADC. 1: when SINGLERX is active, use the I ADC.
		4	SINGLERX	0: use both Rx paths. 1: use only one Rx path.
		3	TXCLK_MD	This bit controls the operation of the TXCLK pin when the chip is configured in half-duplex 1-clock mode. This bit is otherwise ignored. 0: the TXCLK pin is set to a high impedance output. 1: the DLL clock output is driven onto the TXCLK pin.

Register Name	Register Address	Bit(s)	Parameter	Function
		2	HD_BUSCTL	0: selects SPI mode to control bus direction in half-duplex mode. 1: selects Pin mode to control bus direction in half-duplex mode. SPI bit to set Tx or Rx is Register 0x30, Bit 0. Register 0x30, Bit 1 is ignored in this case.
		1	HD_CLKMD	0: selects 1-clock submode if in half-duplex mode. 1: selects 2-clock submode if in half-duplex mode.
		0	FULL_DUPLEX	0: configures the digital interface for half-duplex mode (covers both 1-clock and 2-clock submodes). 1: configures the digital interface for full-duplex mode.
DAC12 Config	0x40	7	DAC12B_EN	0: powers down DAC12B. 1: enables DAC12B.
		6	DAC12A_EN	0: powers down DAC12A. 1: enables DAC12A.
		5	DAC12B_TOP	0: sets DAC12B range to $3.3 \times V_{AUXDACREF}$. 1: sets DAC12B range to $1.8 \times V_{AUXDACREF}$.
		4	DAC12A_TOP	0: sets DAC12A range to $3.3 \times V_{AUXACREF}$. 1: sets DAC12A range to $1.8 \times V_{AUXDACREF}$.
		3:2	Unused	
		1	AUXDAC_REF	Selects where the voltage reference for all of the auxiliary DACs is derived. 0: resistive divider from AUX33V. $V_{AUXDACREF} = V_{AUX33V}/3.3$. 1: selects the 1.0 V bandgap voltage. $V_{AUXDACREF} = 1.0$ V.
		0	DAC_UPDATE	This bit determines which of the two data words updates all four of the auxiliary DACs. 0: update DACs after LSB write. 1: update DACs after MSB write.
DAC12A MSBs	0x41	7:0	DAC12A[11:4]	DAC12A voltage control word (upper eight bits).
DAC12A LSBs	0x42	7:4	Unused	
		3:0	DAC12A[3:0]	DAC12A voltage control word (lower four bits).
DAC12B MSBs	0x43	7:0	DAC12B[11:4]	DAC12B voltage control word (upper eight bits).
DAC12B LSBs	0x44	7:4	Unused	
		3:0	DAC12B[3:0]	DAC12B voltage control word (lower four bits).
DAC10B Config	0x45	7	DAC10B_EN	0: powers down DAC10B. 1: enables DAC10B.
		6:5	Unused	
		4:2	DAC10B_TOP[2:0]	Sets the DAC output voltage at the top range as follows: 000: 1.0 V. 001: 1.5 V.
				010: 2.0 V. 011: 2.5 V. 100: 3.0 V.
		1:0	DAC10B_RNG[1:0]	The total range of the DAC extends from top-of-range, to top-of-range minus the span. The span is set as: 00: 2.0 V. 01: 1.5 V. 10: 1.0 V. 11: 0.5 V.
DAC10BMSBs	0x46	7:0	DAC10B[9:2]	DAC10B voltage control word (eight most significant bits).
DAC10BLSBs	0x47	7:2	Unused	
		1:0	DAC10B[1:0]	DAC10Bvoltage control word (two least significant bits).

Register Name	Register Address	Bit(s)	Parameter	Function
DAC10A Config	0x48	7	DAC10A_EN	0: powers down DAC10A. 1: enables DAC10A.
		6:5	Unused	
		4:2	DAC10A_TOP[2:0]	Sets the DAC output voltage at the top range as follows: 000: 1.0 V. 001: 1.5 V. 010: 2.0 V. 011: 2.5 V. 100: 3.0 V.
		1:0	DAC10A_RNG[1:0]	The total range of the DAC extends from top-of-range to top-of-range minus the span. The span is set as: 00: 2.0 V. 01: 1.5 V. 10: 1.0 V. 11: 0.5 V.
DAC10A MSBs	0x49	7:0	DAC10A[9:2]	DAC10A voltage control word (eight most significant bits).
DAC10A LSBs	0x4A	7:2	Unused	
		1:0	DAC10A[1:0]	DAC10A voltage control word (two least significant bits).
TX BIST Control	0x50	7:5	Unused	Unused
		4	TX_PTTRN	Chooses the pattern type for the BIST sequence. 0: selects PRN output. 1: selects checker board pattern (0xA5A, 0x5A5, 0xA5A, …).
		3	TX_INSEL	0: selects pattern input from internal pattern generator. 1: selects pattern from the external pins of the Tx port.
		2	TX_CONT	0: runs the BIST for 512 cycles. 1: runs the BIST continuously.
		1	TX_START	0: keep the BIST engine in an idle state. 1: start the BIST sequence.
		0	TX_BISTEN	0: disable the BIST engine. 1: enable the BIST engine.
RX BIST Control	0x51	7:5	Unused	
		4	RX_PTTRN	Chooses the pattern type for the BIST sequence. 0: selects PRN output. 1: selects checker board pattern (0xA5A, 0x5A5, 0xA5A, …).
		3	RX_INSEL	0: selects pattern input from internal pattern generator. 1: selects pattern from the external pins of the Rx path.
		2	RX_CONT	0: runs the BIST for 512 cycles. 1: runs the BIST continuously.
		1	RX_START	0: keep the BIST engine in an idle state. 1: start the BIST sequence.
		0	RX_BISTEN	0: disable the BIST engine. 1: enable the BIST engine.
TXI Check MSB	0x52	7:0	TXI_CHK[15:8]	MSB of the BIST signature value for the I side transmit path.
TXI Check LSB	0x53	7:0	TXI_CHK[7:0]	LSB of the BIST signature value for the I side transmit path.
TXQ Check MSB	0x54	7:0	TXQ_CHK[15:8]	MSB of the BIST signature value for the Q side transmit path.
TXQ Check LSB	0x55	7:0	TXQ_CHK[7:0]	LSB of the BIST signature value for the Q side transmit path.
Version	0x5C	7:0	Chip ID[7:0]	Indicates device hardware revision number. Should read back as 0x08.
Power Down 0	0x60	7	DLL_EN	0: powers down DLL block. 1: enables DLL block.
		6	TXDAC_PD	1: powers down the bandgap reference voltage common to both transmit DACs and all of the auxiliary DACs.

Register Name	Register Address	Bit(s)	Parameter	Function
		5	TXI_SLEEP	1: turns off IDAC output current.
		4	TXQ_SLEEP	1: turns off QDAC output current.
		3	CLK_PD	1: turns off clock receiver. This disables all clocks on the chip except for the serial port clock.
		2	RXADC_PD	1: powers down main ADC clock and the bandgap reference voltage common to both receive ADCs.
		1	RXQ_SLEEP	1: powers down the Q ADC core.
		0	RXI_SLEEP	1: powers down the I ADC core.
Power Down 1	0x61	7	Unused	
		6	DLL_LDO_PD	1: powers down LDO that supplies the DLL18V voltage rail.
		5	DLLBIAS_PD	1: powers down bias sub-block inside DLL block.
		4	CLK_LDO_PD	1: powers down LDO that supplies the CLK18V voltage rail.
		3	RX_LDO_PD	1: powers down LDO that supplies the RX18V voltage rail.
		2	RXF_LDO_PD	1: powers down LDO that supplies the RX18VF voltage rail.
		1	AUXADC_PD	1: powers down AUXADC block.
		0	AUX_REF_PD	1: powers down the auxiliary ADC voltage reference, allowing an external reference to be used.
LDO Status	0x62	7	DLL_LDO_STAT	1: LDO to DLL block is on (read only).
		6	CLK_LDO_STAT	1: LDO to CLOCK block is on (read only).
		5	RX_LDO_STAT	1: LDO to ADC blocks is on (read only).
		4	RXF_LDO_STAT	1: LDO to FLASH section of ADC is on (read only).
		3	DIG_LDO_STAT	1: LDO to digital core is on (read only).
		2	Unused	
		1	Unused	
		0	RSET_SEL	0: selects internal 10 kΩ to generate 1 V reference. 1: selects external RSET to generate voltage reference.
Output Drive	0x63	7:6	TRXD_DRV	Controls the drive strength of the TRXD[11:0] pins. 00: 4 mA output drive. 01: 8 mA output drive. 10: 12 mA output drive. 11: not valid.
		5:4	TRXIQ_DRV	Controls the drive strength of the TRXIQ pin. 00: 4 mA output drive. 01: 8 mA output drive. 10: 12 mA output drive. 11: not valid.
		3:2	TRXCLK_DRV	Controls the drive strength of the TRXCLK pin. 00: 4 mA output drive. 01: 8 mA output drive. 10: 12 mA output drive. 11: not valid.
		1:0	TXCLK_DRV	Controls the drive strength of the TXCLK pin. 00: 4 mA output drive. 01: 8 mA output drive. 10: 12 mA output drive. 11: not valid.

Register Name	Register Address	Bit(s)	Parameter	Function
Clock Mode	0x66	7	TXI_DCLK	1: disables internal clock to I DAC.
		6	TXQ_DCLK	1: disables internal clock to Q DAC.
		5	Unused	
		4	RXI_DCLK	1: disables internal clock to I ADC.
		3	RXQ_DCLK	1: disables internal clock to Q ADC.
		2	DCS_BP	1: disables duty cycle stabilizer block.
		1:0	ADCDIV[1:0]	00: selects divide by 1. Bypasses internal divider block for RXCLK. 01: selects divide by 1. Bypasses internal divider block for RXCLK. 10: selects divide by 2. 11: selects divide by 4.
I DAC Gain Ctrl 0	0x68	7:6	Unused	
		5:0	IGAIN1[5:0]	Linear in dB adjustment of the full-scale current of I DAC. Provides an adjustment range of approximately ±6 dB in 0.25 dB steps. See Figure 57 for details.
I DAC Gain Ctrl 1	0x69	7:6	Unused	
		5:0	IGAIN2[5:0]	Linear adjustment of the full-scale current of I DAC. Provides an adjustment range of approximately ±2.5% in 0.08% steps. See Figure 55 for details.
I DAC Gain Ctrl 2	0x6A	7:6	Unused	
		5:0	IRSET[5:0]	Linear adjustment of the full-scale current of I DAC. Provides an adjustment range of approximately ±20% in 0.625% steps. See Figure 55 for details.
Q DAC Gain Ctrl 0	0x6B	7:6	Unused	
		5:0	QGAIN1[5:0]	Linear in dB adjustment of the full-scale current of Q DAC. Provides an adjustment range of approximately ±6 dB in 0.25 dB steps. See Figure 56 for details.
Q DAC Gain Ctrl 1	0x6C	7:6	Unused	
		5:0	QGAIN2[5:0]	Linear adjustment of the full-scale current of Q DAC. Provides an adjustment range of approximately ±2.5% in 0.08% steps. See Figure 57 for details.
Q DAC Gain Ctrl 2	0x6D	7:6	Unused	
		5:0	QRSET[5:0]	Linear adjustment of the full-scale current of Q DAC. Provides an adjustment range of approximately ±20% in 0.625% steps. See Figure 55 for details.
REFIO Adjust	0x6E	7:6	Unused	
		5:0	REFIO_ADJ[5:0]	Adjusts the on-chip reference voltage and output at REFIO. The transmit DAC full-scale currents and the auxiliary DAC full-scale voltages are proportional to the REFIO voltage. The approximate REFIO output voltage by code is: 000000: V_{REF} = 1.0 V. 000001: V_{REF} = 1.00625 V. … 011111: V_{REF} = 1.19375 V.
				100000: V_{REF} = 0.8 V. 100001: V_{REF} = 0.80625 V. … 111111 : V_{REF} = 0.99375 V.
DLL Control 0	0x71	7	ADCCLKSEL	1: selects DLL output as the ADC sampling clock. 0: selects external clock as the ADC sampling clock.
		6	DACCLKSEL	1: selects DLL output as the DAC sampling clock. 0: selects external clock as the DAC sampling clock.
		5	Unused	
		4	DLL_REF_EN	1: enables the input reference clock to the DLL.

Register Name	Register Address	Bit(s)	Parameter	Function
		3:0	N[3:0]	Sets DLL divide ratio (1 to 8) at the output of the DLL. 0000: not valid. 0001: 1. 0010: 2. … 0110: 6. 0111: not valid. 1000: 8. 1001: not valid. … 1111: not valid.
DLL Control 1	0x72	7	DLL_Locked	1: DLL has locked to reference clock (read only).
		6:5	DLLDIV[1:0]	00: DLL output is directly driven out. Divider is bypassed. 01: DLL output is directly driven out. Divider is bypassed. 10: DLL output is divided by 2. 11: DLL output is divided by 4.
		4:0	M[4:0]	Sets DLL multiplication factor (1 to 32). 00000: 1. 00001: 2. … 11111: 32.
DLL Control 2	0x75	7:4	0	Set these bits to 0.
		3	DLL_RESB	Reset DLL. The DLL must be reset by a low to high transition on this bit each time the DLL configuration is changed or the reference frequency is changed.
		2:0	0	Set these bits to 0.
Aux ADC Config and Conversion Start	0x77	7:6	CONV_TIME[1:0]	Sets the number of AUXADCCLK cycles required to perform a conversion. 00: 20 AUXADCCLK cycles. 01: 22 AUXADCCLK cycles. 10: 26 AUXADCCLK cycles. 11: 34 AUXADCCLK cycles.
		5:3	Unused	
		2:0	AUXADC_CH[2:0]	Selects analog input channel to the auxiliary ADC. 000: AUXIN1, Pin 72. 001: AUXIO2, Pin 71. 010: AUXIO3, Pin 70. 011: internal VPTAT voltage. 100: internal VCMLI voltage. 101: internal VCMLQ voltage. 110: RXCML voltage. 111: not connected. Any write to this register initiates an ADC conversion cycle.
Aux ADC MSBs	0x78	7:0	AUXADC[11:4]	This is the 8 MSBs of the most recent AUXADC conversion result.
Aux ADC LSBs	0x79	7:4	AUXADC[3:0]	This is the 4 LSBs of the most recent AUXADC conversion result.
		3	CONV_COMPL	0: indicates that the request auxiliary ADC conversion is in progress. 1: indicates that the auxiliary ADC conversion result is valid.
		2:0	CHAN_SEL[2:0]	Indicates the actual auxiliary ADC input channel selected for the conversion. This should match the channel that was selected in the write to Register 0x77 that initiated the conversion.

Register Name	Register Address	Bit(s)	Parameter	Function
Aux ADC CTRL 0	0x7A	7	AUXADC_EN	0: powers down the auxiliary ADC clock. 1: enables the auxiliary ADC clock.
		6	RES	1: resets the AUXADC. A transition from 0 to 1 triggers the reset. The bit should be returned to 0 after issuing the reset.
		5:3	Unused	
		2:0	AUXDIV[2:0]	Sets the frequency division ratio of the input clock driving the CLKP, CLKN pins over the AUXADCCLK. 000: 256. 001: 128. … 110: 4. 111: 2. The frequency of the AUXADCCLK should be less than 10 MHz. The sample conversion rate of the AUXADC is determined by the AUXCLK rate and CONV_TIME.
Aux ADC CTRL 1	0x7B	7	TEMPSNS_EN	1: enables the on-chip temperature sensor.
		6:5	Unused	
		4:2	AUXREF_ADJ[2:0]	Adjustment for tuning the internal auxiliary ADC reference voltage.
				011: +18 mV. 010: +12 mV. 001: +6 mV. 000: default. 111: −6 mV. 110: −12 mV. 101: −18 mV. 100: −24 mV.
		1:0	Unused	
ADC Full-Scale Adj	0x7D	7:5	Unused	
		4:0	RX_FSADJ[4:0]	This parameter adjusts the full-scale input voltage range of the Rx path ADCs. The peak-to-peak input voltage range can be set as follows: 10000: 1.25 V. 10001:1.27 V. 10010: 1.29 V. 10011: 1.31 V. … 11111: 1.54 V. 00000: 1.56 V. 00001: 1.58 V. … 01110: 1.873 V. 01111: 1.875 V.
Rx ADC Trim Ctrl	0x7E	7	Unused	
		6	RXTrim_EN	1: enables ADC gain calibration.
		5	RXTrim_Fine	1: decreases the step size (increases resolution) of the gain calibration adjustment.
		4	AUXCML_EN	Controls the buffers of internal bias points within each of the Rx ADCs to allow for checking of this voltage. These voltages should read back about 0.9 V. 0: disables the buffers. 1: enables the buffers.
		3:1	0	Set to 000.

Register Name	Register Address	Bit(s)	Parameter	Function
		0	RX_DC	0: the ADC common-mode buffer is active. This sets the ADC inputs to the desired common-mode voltage through 10 kΩ resistors to each single sided input. 1: disables the common-mode buffer. The buffer should be disabled whenever the user DC couples to the ADC inputs.
IGAIN CAL MSBs	0x7F	7:0	RXI_Trim[9:2]	The RXI_Trim[9:0] word is used to adjust the gain of the receive path I ADC. These bits have no effect unless the RXTrim_EN bit is set. The RXTrim_Fine bit reduces the LSB size of the calibration word by ½.
IGAIN CAL LSBS	0x80	7:3	Unused	
		2:1	RXI_Trim[1:0]	
		0	GAINCAL_ENI	1: enables the gain calibration DAC for the I Rx ADC.
IGAIN CAL MSBs	0x81	7:0	RXQ_Trim[9:2]	The RXQ_Trim[9:0] word is used to adjust the gain of the receive path Q ADC. These bits have no effect unless the RXTrim_EN bit is set. The RXTrim_Fine bit reduces the LSB size of the calibration word by ½.
IGAIN CAL LSBs	0x82	7:3	Unused	
		2:1	RXQ_Trim[1:0]	Bottom two LSBs of RXQ_Trim described in Register 0x81 above.
		0	GAINCAL_ENQ	1: enables the gain calibration DAC for the Q Rx ADC.
DDLL Lock Bits	0x84	1	TXDDLL lock bit	0: TXDDLL is unlocked. 1: TXDDLL is locked.
		0	RXDDLL lock bit	0: RXDDLL is unlocked. 1: RXDDLL is locked.
IGAIN CAL LSBS	0xFF	7:1	Unused	
		0	Update	Synchronously transfers ADC configuration data from the global register set to the local ADC register set and activates the changes. A 0-to-1 transition is required to initiate the transfer. 1: transfer ADC parameters to ADC to make changes active.

RECEIVE PATH

Rx Path General Description

The AD9961/AD9963 Rx paths consist of dual, differential input, 100 MSPS ADCs followed by an optional 2× decimation filter. The Rx path also has digital offset and gain adjustments.

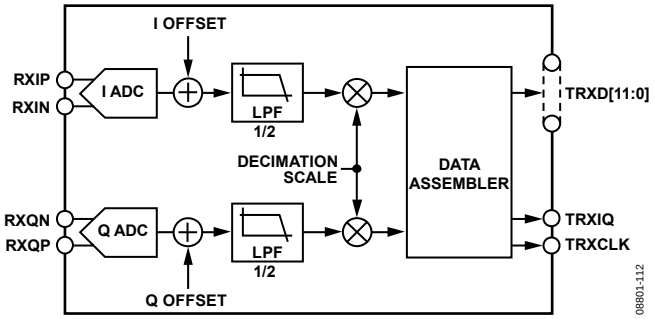


Figure 39. Receive Path Block Diagram

The dual ADC paths share the same clocking and reference circuitry to provide optimal matching characteristics. The ADCs have a multistage differential pipelined switched capacitor architecture with output error correction logic. The ADCs support IF sampling frequencies up to 140 MHz, making them suitable for undersampling receivers. Also, one of the ADCs can be powered down and the digital interface can be placed into single ADC mode. This flexibility makes the part well-suited for sampling real signals as well.

RECEIVE ADC OPERATION

The Rx path analog inputs look into a nominal differential impedance of 4 kΩ. The Rx inputs are self-biasing, so they can be either ac-coupled or direct coupled. The nominal dc bias level of the inputs is 1.4 volts. A buffered version of the bias voltage is available at the RXCML pin. This voltage can be used for biasing external buffer circuits when dc coupling is required.

For optimal dynamic performance, the analog inputs should be driven differentially. The source impedances driving the Rx inputs should be matched so that common-mode settling errors are symmetrical. The Rx inputs can be driven with a single-ended source, but SNR and SINAD performance is degraded.

ADC Reference Voltage

An internal differential voltage reference creates positive and negative reference voltages that define the full-scale input voltage of the ADCs. This full-scale input voltage range can be adjusted by means of the RX_FSADJ[4:0] parameter in configuration Register 0x7D. See the Configuration Registers section for more details on setting the voltage.

The nominal input voltage range is 1.56 V. In general, a tradeoff can be made between linearity and SNR. Increasing the input voltage range leads to higher SNR. Decreasing the input voltage range leads to better linearity.

RXBIAS

The AD9961/AD9963 provide the user with the option to place a 10 kΩ resistor between the RXBIAS pin and ground. This resistor is used to set the master current reference of the ADC core. The RXBIAS resistor should have a tolerance of 1% or better to preserve the accuracy of the ADC full-scale range. Care should be taken in the layout to avoid any noise from coupling into the RXBIAS pin.

RXCML

The RXCML pin of the AD9961/AD9963 provides the user with a buffered version of the expected ADC common-mode bias voltage. The RXCML output nominally is at 1.4 V. Bypassing the RXCML output to analog ground maintains the stability of the output buffer and lowers the noise. To maintain the accuracy of the RXCML bias voltage, the current draw from the pin should be kept below 1 mA.

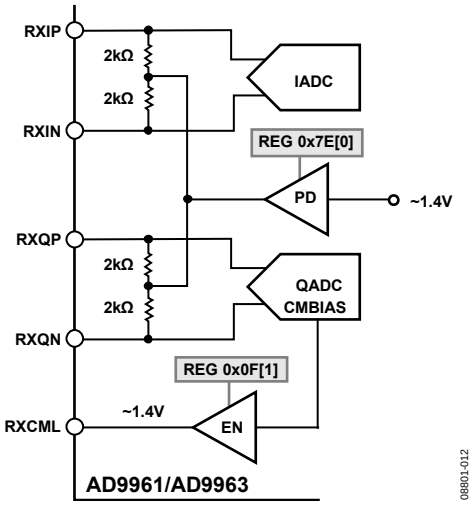


Figure 40. Simplified Schematic of Rx Path Inputs

Differential Input Configurations

Optimum performance is achieved by driving the analog inputs in a differential input configuration. For baseband applications, the ADA4937 differential driver provides excellent performance and a flexible interface to the ADC.

Figure 41 shows an ac-coupled input configuration. The VOCM pin should be connected to a voltage that provides sufficient headroom for the output driver of the differential amp. Usually, setting VOCM to ½ of the amplifier supply voltage is the optimal setting. Placing source resistance in series with the amplifiers outputs isolates the amplifier from on-board parasitic capacitances and leads to more stable operation.

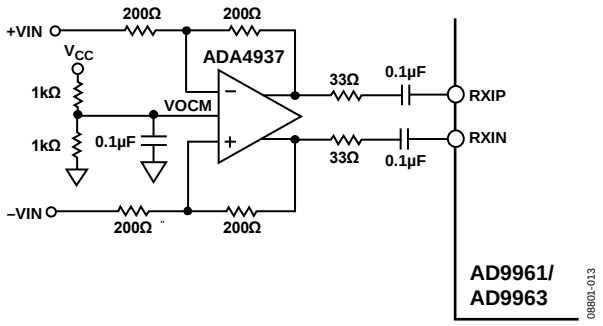


Figure 41. Differential Input Configuration, AC-Coupled

The output common-mode voltage of the ADA4937 is set to match the common-mode voltage required by the ADC by connecting the RXCML output to the VOCM input of the amplifier. The RXCML output nominally is at 1.4 V. Bypassing the RXCML output to analog ground maintains the stability of the output buffer and lowers the noise.

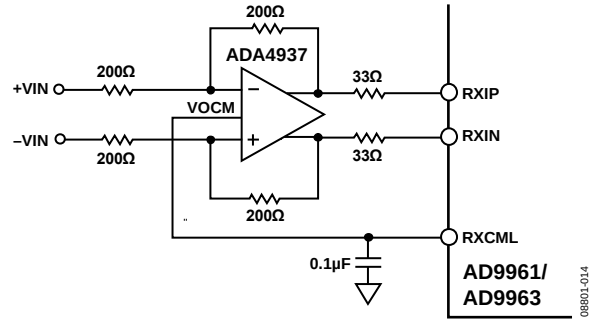


Figure 42. Differential Input Configuration, DC-Coupled

At higher input frequencies, the amplifiers required to maintain the full dynamic power of the AD9963 requires considerable supply current. For higher frequency power sensitive applications, differential transformer coupling is the recommended input configuration. The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz, and excessive signal power can also cause core saturation, which leads to distortion.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

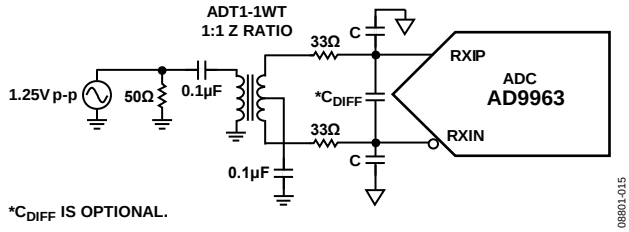


Figure 43. Differential Transformer—Coupled Configuration

Single-Ended Input Configuration

Driving the Rx inputs with a single-ended signal typically limits the achievable ADC performance. When using this configuration, best performance is achieved by maintaining a balanced impedance off each of the Rx inputs as shown in Figure 44.

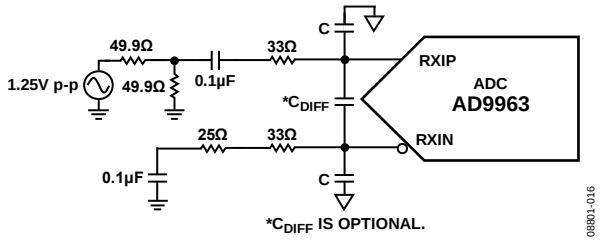


Figure 44. Single-Ended Input Configuration

Interfacing to the ADF4602 Rx Baseband Outputs

The ADF4602 is an RF transceiver suitable for femtocell and other wireless communications applications. The ADF4602 Rx baseband outputs have a nominal output common-mode voltage that can be set to 1.4 V. The ADF4602 can be dc-coupled to the AD9963. It is recommended that a first-order low-pass filter be placed between the two devices to reject unwanted high frequency signals that may alias into the desired baseband signal.

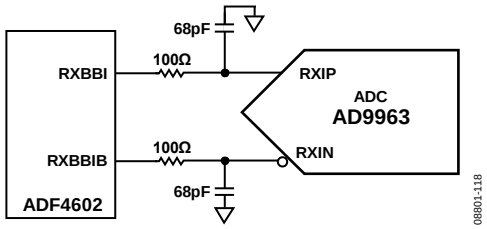


Figure 45. ADF4602 to AD9963 Receive Interface Circuit

In this application, the ADF4602 is setting the common-mode input voltage of the AD9963 ADCs. The input common-mode buffer of the AD9963 should be disabled (set Register 0x7E, Bit 1 = 1) to avoid contention with the ADF4602 output driver.

DECIMATION FILTER AND DIGITAL OFFSET

Decimation Filter

The I and Q receive paths each have a bypassable 2× decimating low-pass filter. The half-band digital filter reduces the output sample rate by a factor of 2 while rejecting aliases that fall into the band of interest. These low-pass filters provide >7 dB of stop-band rejection for 40% of the output data rate. When used with quadrature signals, the complex output band is 80% of the quadrature output data rate. A graph of the pass-band response of the decimation filter is shown in Figure 46.

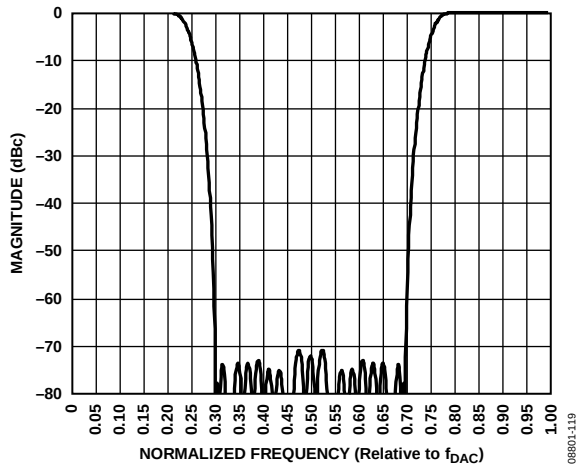


Figure 46. Pass-Band Response of the Rx Path Decimation Filter

The filter coefficients of the 2× decimation low-pass are shown in Table 16.

Table 16.

Lower Coefficient	Upper Coefficient	Value
H(1)	H(43)	12
H(3)	H(41)	−32
H(5)	H(39)	72
H(7)	H(37)	−140
H(9)	H(35)	252
H(11)	H(33)	−422
H(13)	H(31)	682
H(15)	H(29)	−1086
H(17)	H(27)	1778
H(19)	H(25)	−3284
H(21)	H(23)	10364
H(22)		16384

ADC Digital Offset Adjustment

The Rx paths also have individual digital offsets that can be applied to the data captured by the ADCs. The offset is a 6-bit digital value that is added directly to the LSBs of the ADC output data. The offset values are configured by first addressing the ADC by setting the appropriate address in Register 0x05, then writing the desired offset (in LSBs) into Register 0x10. For example, to set offsets of +6 and −2 to the I and Q channels respectively, the register write sequence is:

1. Write 0x01 into Register 0x05. This addresses the I channel ADC.
2. Write 0x06 into Register 0x10. This sets the IADC_Offset value to +6 LSBs.
3. Write 0x02 into Register 0x05. This addresses the Q channel ADC.
4. Write 0xFE into Register 0x10. This sets the QADC_Offset value to −2 LSBs.
5. Write 0x01 into Register 0xFF. This updates the data path registers and applies the offset to the data.
6. Write 0x00 into Register 0x05. This returns the SPI to the normal addressing mode.

TRANSMIT PATH

Tx Path General Description

The transmit section consists of two complete paths of interpolation filters stages, each followed by a high speed current output DAC. A data assembler receives interleaved data from one of two digital interface ports, and de-interleaves and buffers the data before supplying the data samples into the two datapaths. The interpolation filter bank consists of three stages that can be completely bypassed or cascaded to provide 2×, 4×, or 8× interpolation. The supported clock rates for each of the interpolation filters and the transmit DACs are listed in Table 1.

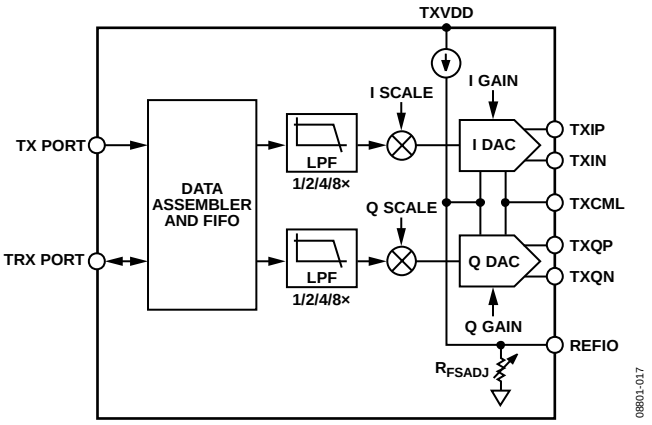


Figure 47. Transmit Path Block Diagram

INTERPOLATION FILTERS

The I and Q transmit paths contain three interpolation filters designated as INT0, INT1, and SRRC. Each of the interpolation filters provides a 2× increase in output data rate. The filters can be completely bypassed or cascaded to provide 2×, 4×, or 8× upsampling ratios. The interpolation filters effectively increase the DAC update rate while suppressing the images at the input date rate. This reduces the requirements on the analog output reconstruction filter.

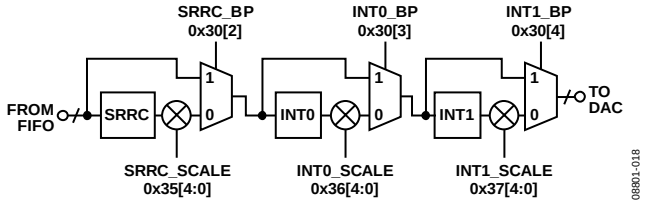


Figure 48. Block Diagram of Transmit Datapath

The digital filters should be cascaded such that INT0 is enabled for an interpolation factor of 2×, INT0 and INT1 should be enabled for an interpolation factor of 4×, and INT0, INT1, and the SRRC should be enabled for an interpolation factor of 8×.

The INT0 and INT1 filters have bandwidths of 40% of the input data rate. Over their usable bandwidth, the filters have a passband ripple of less than 0.1 dB. The SRRC has a roll-off factor of 0.22 with a 60 dB stop-band attenuation. In 2× and 4× interpolation modes, the interpolation filters have an image rejection of greater than 70 dB. In 8× interpolation mode, the image rejection is greater than 65 dB. The usable bandwidth of the filters is typically limited by the stop-band attenuation they provide, rather than the passband flatness. The transfer functions of the interpolation filters configured for 2×, 4×, and 8× interpolation ratios are shown in Figure 49 through Figure 51.

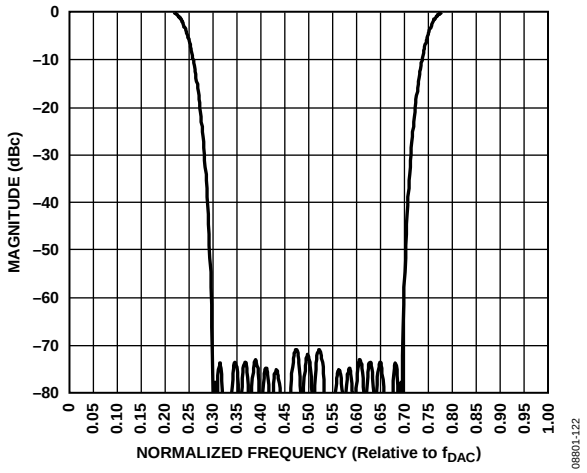


Figure 49. Digital Filter Transfer Function for 2× Interpolation

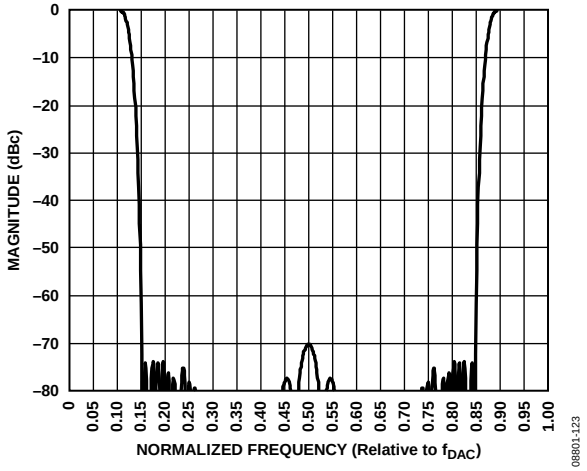


Figure 50. Digital Filter Transfer Function for 4× Interpolation

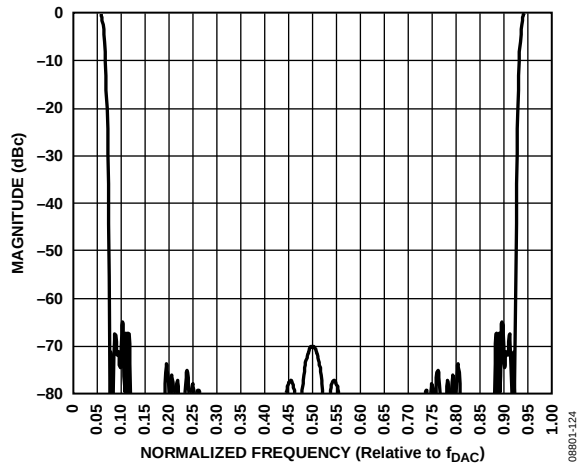


Figure 51. Digital Filter Transfer Function for 8× Interpolation

Interpolation Filter Coefficients

The interpolation filters, INT0 and INT1, are half-band filters implemented with a symmetric set of coefficients. Every other coefficient (even coefficients) except the center coefficient is zero. The coefficient values for the three interpolation filters are listed in Table 17 to Table 19.

Table 17. Coefficient Values for INT0

Lower Coefficient	Upper Coefficient	Value
H(1)	H(43)	12
H(3)	H(41)	−32
H(5)	H(39)	72
H(7)	H(37)	−140
H(9)	H(35)	252
H(11)	H(33)	−422
H(13)	H(31)	682
H(15)	H(29)	−1086
H(17)	H(27)	1778
H(19)	H(25)	−3284
H(21)	H(23)	10364
H(22)		16384

Table 18. Coefficient Values for INT1

Lower Coefficient	Upper Coefficient	Value
H(1)	H(19)	26
H(3)	H(17)	−138
H(5)	H(15)	466
H(7)	H(13)	−1314
H(9)	H(11)	5058
H(10)		8191

Table 19. Coefficient Values for SRRC Filter

Lower Coefficient	Upper Coefficient	Value
H(1)	H(53)	−2
H(2)	H(52)	−2
H(3)	H(51)	8
H(4)	H(50)	−4
H(5)	H(49)	−21
H(6)	H(48)	10
H(7)	H(47)	44
H(8)	H(46)	−29
H(9)	H(45)	−79
H(10)	H(44)	66
H(11)	H(43)	123
H(12)	H(42)	−127
H(13)	H(41)	−183
H(14)	H(40)	232
H(15)	H(39)	251
H(16)	H(38)	−394
H(17)	H(37)	−326
H(18)	H(36)	642
H(19)	H(35)	401
H(20)	H(34)	−1034
H(21)	H(33)	−469
H(22)	H(32)	1704
H(23)	H(31)	523
H(24)	H(30)	−3160
H(25)	H(29)	−560
H(26)	H(28)	9996
H(27)		16383

Data Flow and Clock Generation

The transmit port TXD[11:0] and TXIQ signals are captured from by the device with an input latch. The data is then formatted and buffered in an 8-word deep FIFO. The data exits the FIFO and is processed by whichever interpolation filters are enabled. The data is then sampled by the transmit DACs.

The FIFO absorbs any phase drift between the two clock domains that drive the transmit data. The data is read from the FIFO by the RDCLK signal. The RDCLK signal is always the DACCLK divided by the interpolation ratio, I. Data is written to the FIFO by the WRCLK signal at the quadrature data input rate, f_{DATA}. f_{DATA} is equal to one-half the bus speed because the I and Q samples are interleaved.

Figure 52 shows the block diagram of the transmit path data flow in full-duplex mode. Also shown in the diagram are the input data clocking options and the clock doubler selections.

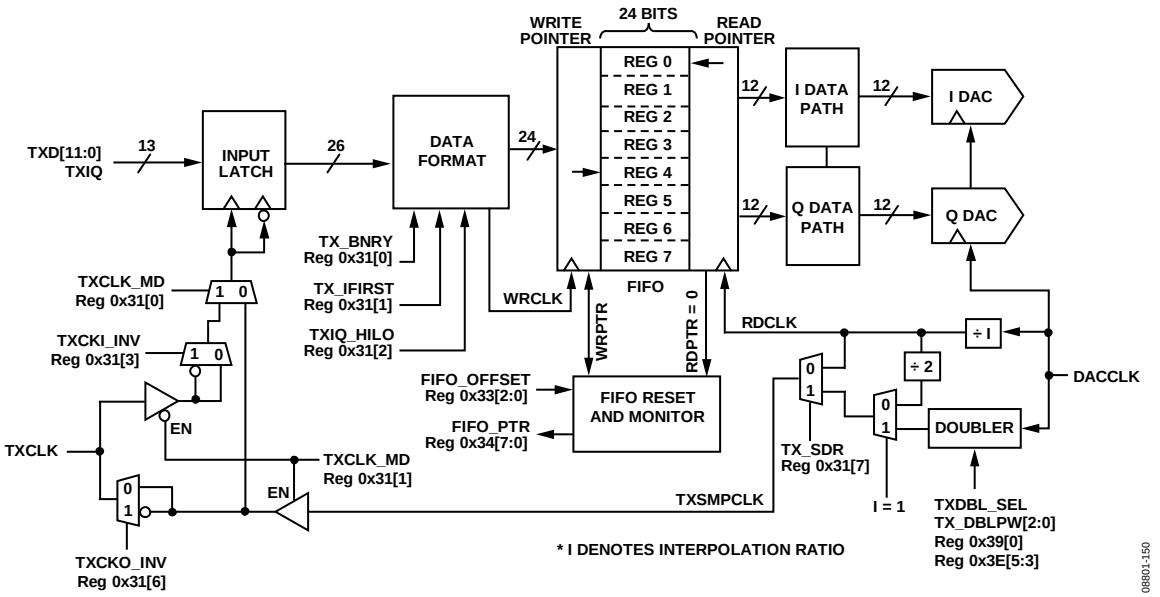


Figure 52. Transmit Path Data Flow and Clock Generation In Full Duplex Mode

The signal on the TXCLK pin can be configured as either an input or an output. This is configured by the TXCLK_MD variable (Register 0x31, Bits[5:4]). Whether configured as an input or an output, the TXCLK signal has the option of being inverted by configuring the TXCKI_INV or TXCKO_INV variables.

The transmit path clock doubler is only used when all of the interpolation filters are bypassed (I = 1) and the transmit path is configured in bus rate mode (TX_SDR = 1). For more information about configuring the clock doubler, see Table 22.

TRANSMIT DAC OPERATION

Figure 53 shows a simplified block diagram of one of the transmit path DACs. Each DAC consists of a current source array, switch core, digital control logic, and full-scale output current control. The DAC contains a current source array capable of providing a nominal full-scale current (I_{OUTFS}) of 2 mA. The output currents from the TXIP and TXIN pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load.

The DACs are powered through the TXVDD pin and can operate over a 1.8 V to 3.3 V supply range. To facilitate interfacing the output of the AD9961/AD9963 directly to a range of common-mode levels, an internal bias voltage is made available through the TXCML pin.

The DAC full-scale output current is regulated by the reference control amplifier and is determined by the product of a reference current, a programmable reference resistor, R_{REF}, an internal programmable resistor, R_{SET}, and a pair of programmable gain scaling parameters.

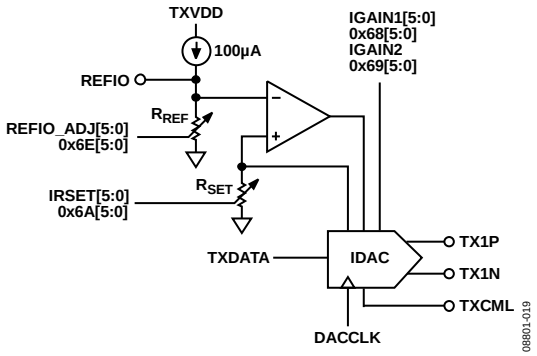


Figure 53. Simplified Block Diagram of I DAC Core

Transmit DAC Transfer Function

The output currents from the TXIP and TXIN pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load. TXIP provides maximum output current when all bits are high. The output currents vs. DACCODE for the DAC outputs are expressed as:

$$I_{TXIP} = \left[\frac{DACCODE}{2^N}\right] \times I_{OUTFS} \quad (1)$$

$$I_{TXIN} = I_{OUTFS} - I_{TXIP} \quad (2)$$

where $DACCODE = 0$ to $2^N - 1$.

There are a number of adjustments that can be made to scale I_{OUTFS} to provide programmability in the output signal level.

Transmit Path Gain Adjustment

Adjusting the output signal level is implemented by scaling the full-scale output current of the transmit DAC. There are four separate programmable parameters that can be used to adjust the full-scale output of the DACs; the REFIO voltage, the R_{SET} resistance, and the fine and coarse gain control parameters.

Adjusting the REFIO Voltage

There is a single reference voltage that is used by both the I and Q channel DACs. The REFIO reference voltage is generated by an internal 100 µA current source terminated into a programmable resistor, R_{REF}. The nominal R_{REF} resistance is 10 kΩ resulting in a 1.0 V reference voltage. The resistance can be varied by adjusting the REFIO_ADJ[5:0] bits in Register 0x6E. This adds or subtracts up to 20% from the R_{REF} resistance and hence the REFIO voltage and the DAC full-scale current. A secondary effect to changing the REFIO voltage is that the full-scale voltage in the auxiliary DACs also changes by the same magnitude.

The register uses twos complement format in which 011111 maximizes the voltage on the REFIO node and 100000 minimizes the voltage. A curve illustrating the variation of REFIO voltage vs. REFIO_ADJ value is shown in Figure 54.

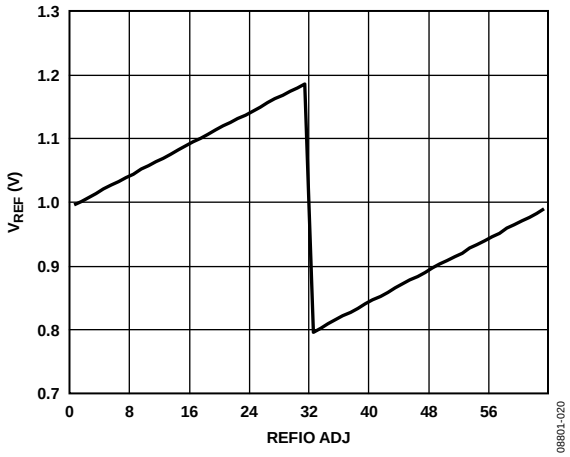


Figure 54. Typical V_{REFIO} Voltage vs. REFIO_ADJ Value

The REFIO pin should be decoupled to AGND with a 0.1 µF capacitor. If the voltage at REFIO is to be used for external purposes, an external buffer amplifier with an input bias current of less than 100 nA should be used.

An external reference can be used in applications requiring tighter gain tolerances or lower temperature drift. Also, a variable external voltage reference can be used to implement a method for gain control of the DAC output. The external reference is applied to the REFIO pin. Note that the 0.1 µF compensation capacitor is not required. The internal reference can be directly overdriven by the external reference, or the internal reference can be powered down. The input impedance of REFIO is 10 kΩ when powered up and 1 MΩ when powered down.

Table 20. Reference Operation

Reference Mode	REFIO Pin	Register Setting
Internal	Connect 0.1 µF capacitor	Register 0x60, Bit 6 = 0 (default)
External	Apply external reference	Register 0x60, Bit 6 = 1 (disables internal reference)

Adjusting the Current Scaling Resistor

Each transmit DAC has a resistor that is used to adjust the full-scale current. The nominal resistance is 16 kΩ, which results in a full-scale current of 2 mA (when V_{REFIO} equals 1.0 V). The 6-bit programmable values, IRSET[5:0] and QRSET[5:0] (Register 0x6A and Register 0x6D), provide an output current adjustment range of ±20% as shown in Figure 55.

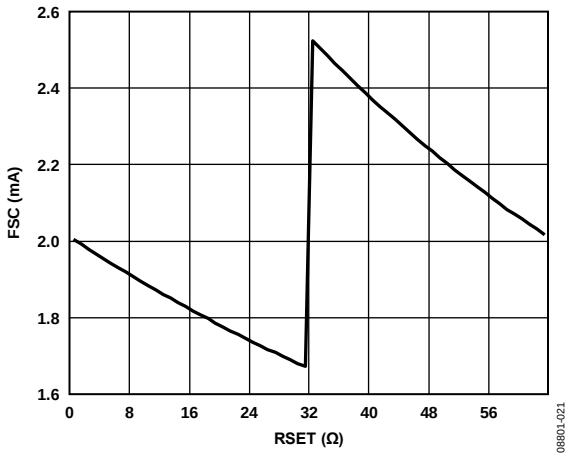


Figure 55. Output Current Scaling vs. IRSET and QRSET Values

Adjusting the GAIN Parameters

Each transmit DAC has coarse and fine gain control parameters for scaling the full-scale output currents. These adjustments change only the full-scale current of the DAC and have no impact on the REFIO voltage. The coarse scale adjust (GAIN1) allows the nominal output current to be changed by ±6 dB in approximately 0.25 dB steps. The adjustment range of the fine scale adjust (GAIN2) is about ±2.5%. Figure 56 and Figure 57 show the resulting gain scaling vs. the GAIN1 and GAIN2 parameters.

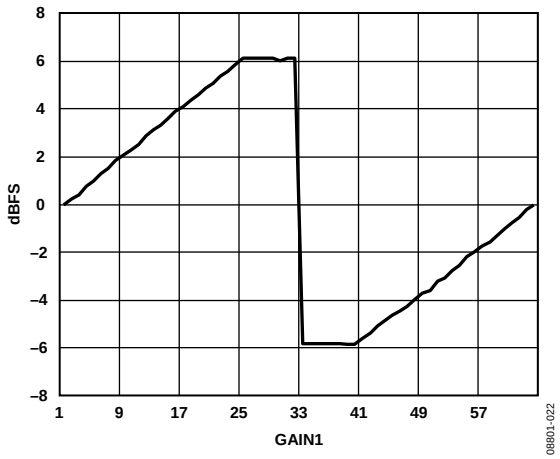


Figure 56. Typical DAC Full-Scale Current vs. GAIN1 Code

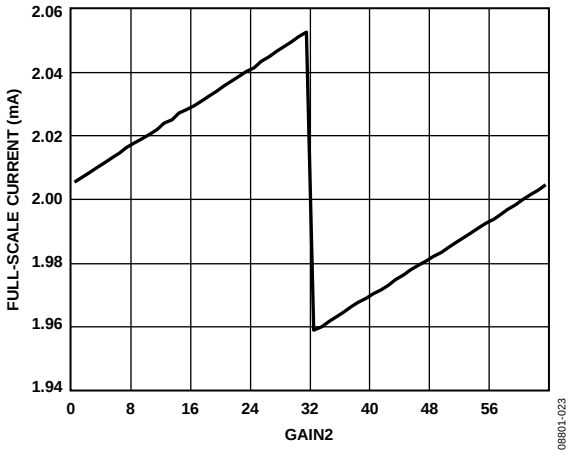


Figure 57. Typical DAC Full-Scale Current vs. GAIN2 Code

TRANSMIT DAC OUTPUTS

The optimum noise and distortion performances of the AD9961/AD9963 are realized when they are configured for differential operation. The common-mode error sources of the DAC outputs are significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude increases. This is due to the first-order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

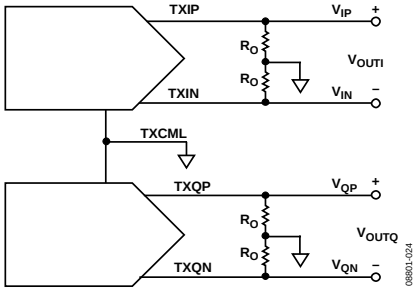


Figure 58. Basic Transmit DAC Output Circuit

Figure 58 shows the most basic DAC output circuitry. A pair of resistors, R_O, are used to convert each of the complementary output currents to a differential voltage output, V_{OUTX}. Because the current outputs of the DAC are very high impedance, the differential driving point impedance of the DAC outputs, R_{OUT}, is equal to $2 \times R_O$.

Figure 59 illustrates the output voltage waveforms.

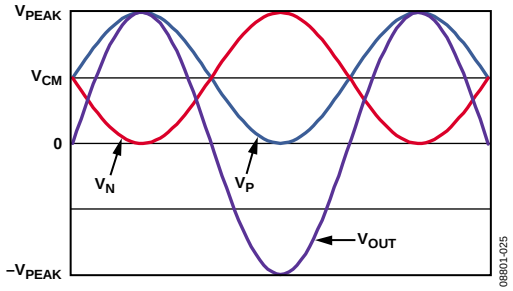


Figure 59. Voltage Output Waveforms

The common-mode signal voltage, V_{CM}, is calculated as:

$$V_{CM} = \frac{I_{FS}}{2} \times R_O$$

The peak output voltage, V_{PEAK}, is calculated as:

$$V_{PEAK} = I_{FS} \times R_O$$

With this circuit configuration, the single-ended peak voltage is the same as the peak differential output voltage.

Setting the TXCML Pin Voltage

The TXCML pin serves to change the DAC bias voltages in the part, allowing it to operate with higher output signal common-mode voltages. When the output signal common mode is below 0.8 V, the TXCML pin should be tied directly to AGND. When the output signal common mode is greater then 0.8 V, then the TXCML pin should be set to 0.5 V. The TXCML pin should be a low ac impedance source (capacitive decoupling is recommended).

When the TXVDD supply is 1.8 V, the output signal common-mode voltage should be kept close to 0 V and the TXCML pin should be connected directly to ground. When the TXVDD supply is 3.3 V, the output signal common mode can be operated as high as 1.25 V.

The circuit shown in Figure 60 shows a typical output circuit configuration that provides a non zero bias voltage at the TXCML pin. Resistance values of 499 Ω for R_L and 249 Ω for R_{CML} produces a 2 V p-p differential output voltage swing with a 1.0 V output common-mode voltage and a voltage of 0.5 V supplied to the TXCML pin. The 2 mA full-scale current flows through the 249 Ω R_{CML} creating the 0.5 V TXCML voltage. The decoupling capacitor, assures a low ac driving impedance for the TXCML pin.

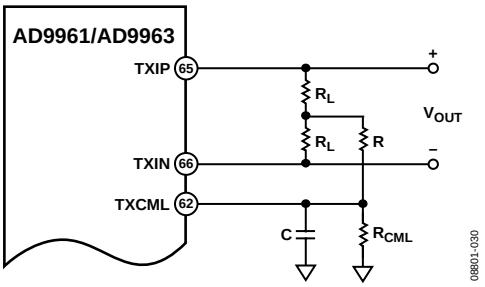


Figure 60. Circuit for Setting TXCML Level Using R_{CML}

Transmit DAC Output Circuit Configurations

The following section illustrates some typical output configurations for the AD9961/AD9963 transmit DACs. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 2.0 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application that allows ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, signal gain, and/or a low output impedance.

A single-ended output is suitable for applications where low cost and low power consumption are primary concerns.

Differential Coupling Using a Transformer

An RF transformer can be used to perform a differential-to-single-ended signal conversion, as shown in Figure 61. The distortion performance of a transformer typically exceeds that available from standard op amps, particularly at higher frequencies. Transformer coupling provides excellent rejection of common-mode distortion (that is, even-order harmonics) over a wide frequency range. It also provides electrical isolation and can deliver voltage gain without adding noise. Transformers with different impedance ratios can also be used for impedance matching purposes. The main disadvantages of transformer coupling are low frequency roll-off, lack-of-power gain, and high output impedance.

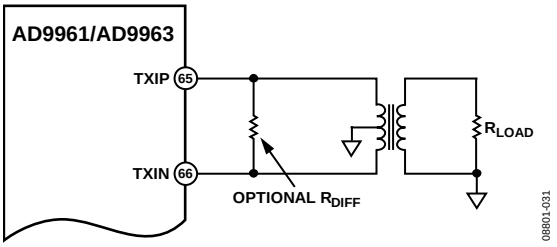


Figure 61. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to a voltage that keeps the voltages on TXIP and TXIN within the output common-mode voltage range of the device. Note that the dc component of the DAC output current is equal to I_{OUTFS} and flows out of both TXIP and TXIN. The center tap of the transformer should provide a path for this dc current. In most applications, AGND provides the most convenient voltage for the transformer center tap. The complementary voltages appearing at TXIP and TXIN (that is, V_{IOUTP} and V_{IOUTN}) swing symmetrically around AGND and should be maintained with the specified output compliance range of the AD9961/AD9963.

A differential resistor, R_{DIFF}, can be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF}, as reflected by the transformer, is chosen to provide a source termination that results in a low voltage standing wave ratio (VSWR). Note that approximately half the signal power is dissipated across R_{DIFF}.

Differential Buffered Output Using an Op Amp

A dual op amp (see the circuit shown in Figure 62) can be used in a differential version of the single-ended buffer shown in Figure 63. The same R-C network is used to form a one-pole, differential, low-pass filter to isolate the op amp inputs from the high frequency images produced by the DAC outputs. The feedback resistor, R_{FB}, determines the differential peak-to-peak signal swing by the formula

$$V_{OUT} = 2 \times R_{FB} \times I_{FS}$$

The minimum single-ended voltages out of the amplifier are, respectively,

$$V_{MIN} = V_{MAX} - R_{FB} \times I_{FS}$$

The common-mode voltage of the differential output is determined by the formula

$$V_{CM} = V_{MAX} - R_{FB} \times I_{FS}$$

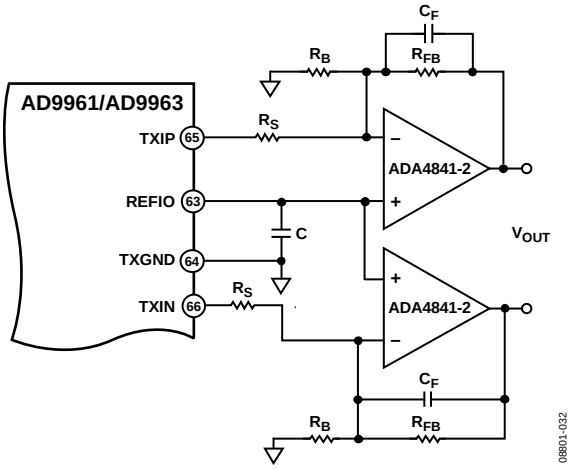


Figure 62. Single-Supply Differential Buffer

Single-Ended Buffered Output Using an Op Amp

An op amp such as the ADA4899-1 can be used to perform a single-ended current-to-voltage conversion, as shown in Figure 63. The AD9961/AD9963 are configured with a pair of series resistors, R_S, off each output. For best distortion performance, R_S should be set to 0 Ω. The feedback resistor, R_{FB}, determines the peak-to-peak signal swing by the formula

$$V_{OUT} = R_{FB} \times I_{FS}$$

The maximum and minimum voltages out of the amplifier are, respectively,

$$V_{MAX} = V_{REFIO}$$

$$V_{MIN} = V_{MAX} - I_{FS} \times R_{FB}$$

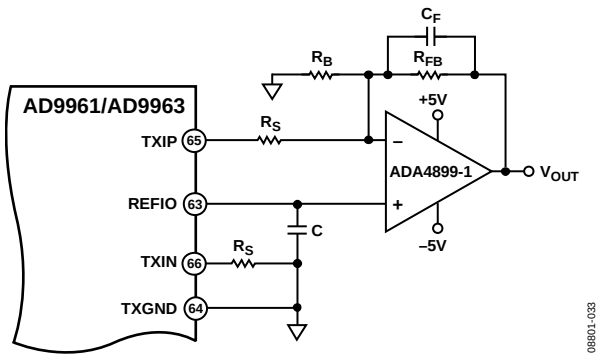


Figure 63. Single-Supply Single-Ended Buffer

Interfacing to the ADF4602

The ADF4602 is an RF transceiver suitable for Femtocell and other wireless communications applications. The ADF4602 Tx baseband inputs have a nominal input common-mode voltage requirement of 1.2 V. The AD9963 can be dc coupled to the ADF4602 as shown in Figure 64. When configured for a 2 mA full-scale current, the output swing of the circuit is 1 V ppd centered at 1.2 V. The TXMCL pin is biased at 0.5 V to increase the headroom of the DAC outputs. The TXVDD and CLK33V supplies must be supplied with 3.3 V to support this output compliance range from the DACs.

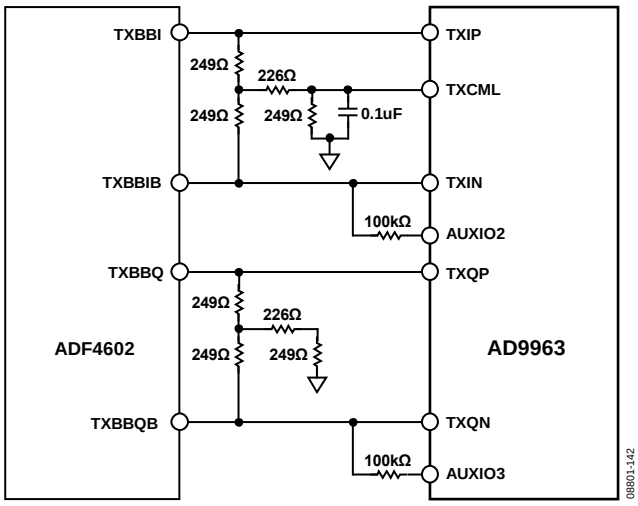


Figure 64. AD9963 to ADF4602 Tx Interface Circuitry

The optional 100 kΩ resistors connected between the AUXIO pins and the TXIN (and TXQN) pins allow a dc offset to be provided to null out LO feedthrough at the ADF4602 outputs.

DEVICE CLOCKING

CLOCK DISTRIBUTION

The clock distribution diagram shown in Figure 65 gives an overview of the clocking options for each of the data converters. The receive path ADCs and the transmit path DACs can be clocked directly from the CLKP/CLKN inputs or from the output of the on-chip DLL. The auxiliary ADC sampling clock is always a divided down version of the input clock. The auxiliary DACs are updated synchronously with the serial port clock and have no relationship with the CLKP/CLKN inputs.

The best data converter performance is realized when a low jitter clock source drives the CLKP/CLKN inputs, and this signal is used directly (or through the on-chip divider) as the data converter sampling clocks. The ADC and DAC sampling clocks are independently selected to be derived from either the CLKP/CLKN input or from the DLL output, DLLCLK. Using DLLCLK as the data converter sampling clock signal may degrade the noise and SFDR performance of the converters. More information is given in the Clock Multiplication Using the DLL section.

The receive path ADC has a duty cycle stabilizer (DCS) to help make the ADC performance insensitive to changes in the input clock duty cycle. The DCS can be bypassed. Recommendations for using the DCS can be found in the Clock Duty Cycle Considerations section.

The ADC clock divider and the DLL clock multiplication supports a variety of ratios between the receive path ADC sampling clock and the transmit path DAC sampling clock. Table 21 details the specific values the device supports and which register bits are require configuration.

Table 21. Clock Tree Configuration Variables

		Address	
Variable	**Values**	**Register**	**Bit(s)**
DCS_BP	0 or1	0x66	2
ADCDIV	1, 2, 4	0x66	[1:0]
ADCCLKSEL	0 or 1	0x71	7
DACCLKSEL	0 or 1	0x71	6
N	1 to 6, 8	0x71	[3:0]
M	1, 2, 3,…, 32	0x72	[4:0]
DLLDIV	1, 2, 4	0x72	[6:5]
AUXDIV	2J, J = 1 to 8	0x7A	[2:0]

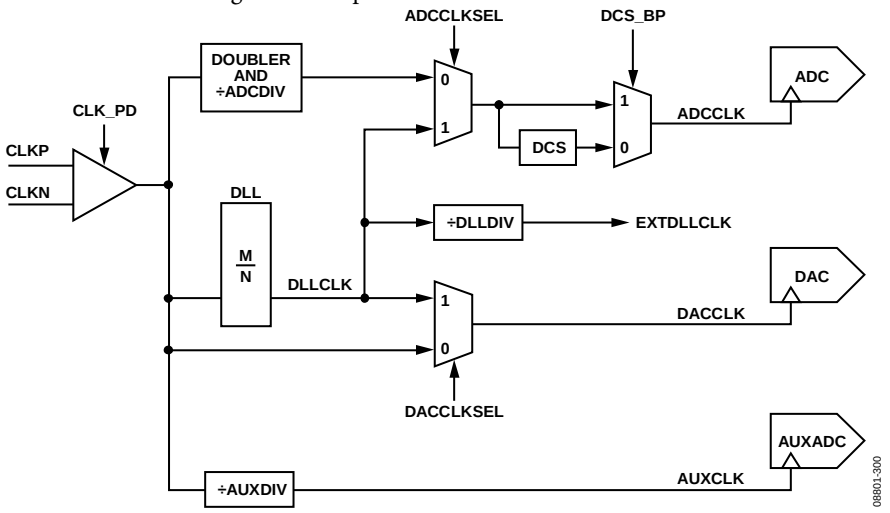


Figure 65. Clock Distribution Diagram

DRIVING THE CLOCK INPUT

For optimum performance, the AD9961/AD9963 clock inputs (CLKP and CLKN) should be clocked with a low jitter, fast rise time differential signal. This signal should be ac-coupled to the CLKP and CLKN pins via a transformer or capacitors. The CLKP/CLKN inputs are internally biased and require no external bias circuitry. Figure 66 through Figure 69 show preferred methods for clocking the AD9961/AD9963.

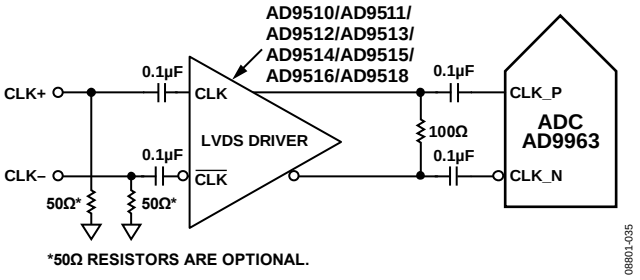


Figure 66. Differential LVDS Sample Clock

In applications where the receive analog input signals and the transmit analog output signals are at low frequencies, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLKP should be driven directly from a CMOS gate, and the CLKN pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 67). A series termination resistor off the clock driver output may improve the dynamic response of the driver.

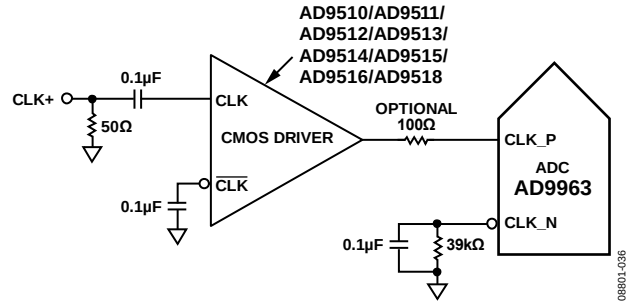


Figure 67. Single-Ended 1.8 V CMOS Sample Clock

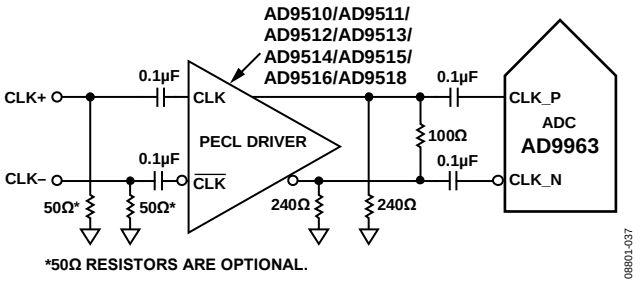


Figure 68. Differential PECL Sample Clock

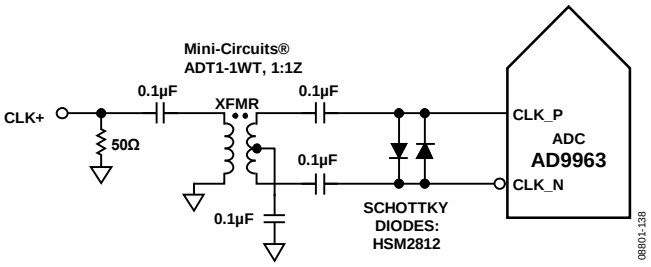


Figure 69. Transformer Coupled Clock

Note that the 39 kΩ resistor shown in the CMOS clock driver example shifts the CLK_N input to about 0.9 V. This is optimal when the CMOS driver is supplied from a 1.8 V supply.

A 2.5 V CMOS driver may also be used. In this case, the minimum CLK33V supply voltage should be 2.5 V. The 39 kΩ resistor should be removed in this case. Connecting CLKN to ground with just a 0.1 µF capacitor results in the CLKN voltage being biased to about 1.2 V.

Clock Duty Cycle Considerations

The duty cycle of the input clock should be maintained between 45% and 55%. Duty cycles outside of this range affects the dynamic performance of the ADC. This is especially true at sample rates greater than 75 MHz. It is recommended that the duty cycle stabilizer (DCS) be used at clock rates above 75 MHz to ensure the sampling clock maintains the proper duty cycle inside the device. Below 75 MHz, the DCS should be bypassed. The DCS is bypassed by setting Register 0x66, Bit 2 high.

DLL Duty Cycle Caution

Stability of the DLL output requires the main clock input to have a duty cycle of 50% or less. In systems where the duty cycle is greater than 50%, care should be taken to swap the CLKP and CLKN pins to reverse this effect.

CLOCK MULTIPLICATION USING THE DLL

The AD9961/AD9963 contain a recirculating DLL, as shown in Figure 70. This circuit allows the incoming CLK signal (REFCLK) to be multiplied by a programmable M/N factor. This provides a means of generating a wide range of DLL output clock (DLLCLK) frequencies. The DLLCLK signal can be used for either the receive ADC sampling clock, the transmit DAC sampling clock, or both. The EXTDLLCLK signal can be programmed to appear on the TXCLK pin or TRXCLK if desired.

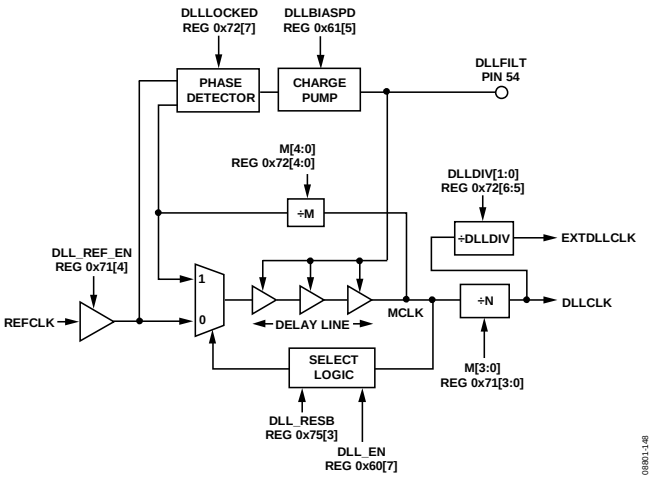


Figure 70. Functional Block Diagram of Clock Multiplier DLL

The DLL is composed of a ring oscillator made from a programmable delay line. The ring oscillator output signal is labeled as MCLK. The MCLK signal is set to oscillate at a frequency M times greater than the REFCLK signal. The DLL output clock, DLLCLK, is the MCLK signal divided by a programmable factor, N. M can be set to values from 1 to 32 and N can be set to values from 1 to 6 and 8.

DLL Frequency Locking Range

The DLL frequency lock range is determined by the output frequency of the ring oscillator, MCLK. The DLL locks over an MCLK frequency range of 100 MHz to 310 MHz. Verifying that the DLL is locked can be done by polling the DLL_Locked bit (Register 0x72, Bit 7).

DLL Filter Considerations

The DLL requires an external loop filter between the DLLFILT pin (Pin 54) and ground for stable operation. The circuit diagram in Figure 71 shows the recommended DLL filter configuration. The external components should be placed as close as possible to the device pins. It is important that no noise be coupled into the filter circuit or DLL output clock jitter performance is degraded.

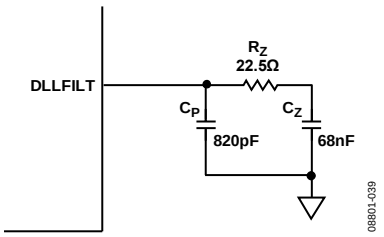


Figure 71. Recommended DLL Loop Filter

DLL Start-Up Routine

To enable the DLL, three bits should be set. The DLL_EN bit (Register 0x60, Bit 7) and the DLL_REF_EN bit (Register 0x71, Bit 4) should be set to 1 and the DLLBIAS_PD bit (Register 0x61, Bit 5) should be set to 0.

The CLK input signal should be stable. The DLL_RESB bit should be asserted low for a minimum of 25 µs, and then brought inactive (high) to start the frequency acquisition. The DLL takes several REFCLK cycles to acquire lock. The DLL_Locked bit can be queried to verify the DLL is locked.

CONFIGURING THE CLOCK DOUBLERS

The receive and transmit data paths each have a clock doubler used for clocking data through the device. These clock doublers are only used in single data rate clocking mode, when there is no interpolation or decimation being used.

These doublers should be configured according to the following guidelines.

Register 0x3A, Register 0x3B, and Register 0x3C configure the operating points of the doublers and should be initialized with the following values:

0x3A = 0x55, 0x3B = 0x55, 0x3C = 0x00

The clock doubler mode and pulse widths should be configured based on the DAC and ADC sample rates. These should be configured according to Table 22.

Table 22. Clock Doubler Configuration Guidelines

DACCLK/ADCCLK Freq (MHz)	TXDBLSEL Register 0x39, Bit 0	TX_DBLPW[2:0] Register 0x3E, Bits[5:3]	RXDBLSEL Register 0x39, Bit 1	RX_DBLPW[2:0] Register 0x3E, Bits[2:0]	DCS_BP[1] Register 0x66, Bit 2
0 to 15	0	111	0	111	1
15 to 30	1	X[2]	0	111	1
30 to 45	1	X[2]	0	110	1
45 to 55	1	X[2]	0	101	1
55 to 65	1	X[2]	0	100	1
65 to 70	1	X[2]	0	011	1
70 to ≥70	1	X[2]	1	X[2]	0

[1] The DCS_BP bit should be set based on the AUXADCCLK frequency.
[2] X = don't care.

DIGITAL INTERFACES

The AD9961/AD9963 have two parallel interface ports, the Tx port and the TRx port. The operation of the ports depends on whether the device is configured for full-duplex or half-duplex mode.

In full-duplex mode, the TRx and Tx port operate independently. The TRx port outputs samples from the receive path and the Tx port accepts incoming samples for the transmit port.

In half-duplex mode, the TRx port outputs samples from the receive path and accepts incoming samples for the transmit path. The Tx port is disabled. The operation of the digital interface is detailed in the sections that follow.

TRX PORT OPERATION (FULL-DUPLEX MODE)

In full-duplex mode, the TRX port sources the data from the AD9961/AD9963 I and Q receive channels. The interface consists of an output data bus (TRXD[11:0]) that carries the interleaved I and Q data. The data is accompanied by a qualifying output clock (TRXCLK) and an output signal (TRXIQ) that identifies the data as from either the I or Q channel. The maximum guaranteed data rate is 200 MSPS.

The basic timing diagram for the Rx path is shown in Figure 72. By default, the time-aligned TRXD[11:0] and TRXIQ output signals are driven on the rising edge of the TRXCLK signal. The t_{OD} parameters are specified in Table 23.

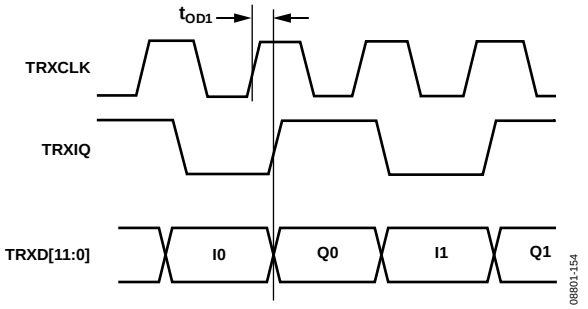


Figure 72. Receive Path Timing Diagram (Bus Rate Clock Mode)

An additional configuration bit, RXCLKPH, is available to invert the TRXCLK. In this case, the TRX data and the TRXIQ signals are driven out on the falling edge of TRXCLK and t_{OD} is measured with respect to the falling edge of TRXCLK.

The analog signals are sampled simultaneously, creating a quadrature pair of data. This creates two possible data pairing orders on the output bus, I data followed by Q data, or Q data followed by I data. There are also two possible ways to align the bus data with the TRXIQ signal, I data aligned with TRXIQ being high or I data aligned with TRXIQ being low. The IQ pairing and data to TRXIQ alignment relationships create four possible timing modes. The AD9961/AD9963 enable any of these four modes to be sourced from the device. The data pairing order is controlled by the RX_IFIRST bit. The phase relationship between the Rx data and the RXIQ signal is controlled by the RXIQ_HILO bit. The two programming options produce the four timing diagrams shown in Figure 73.

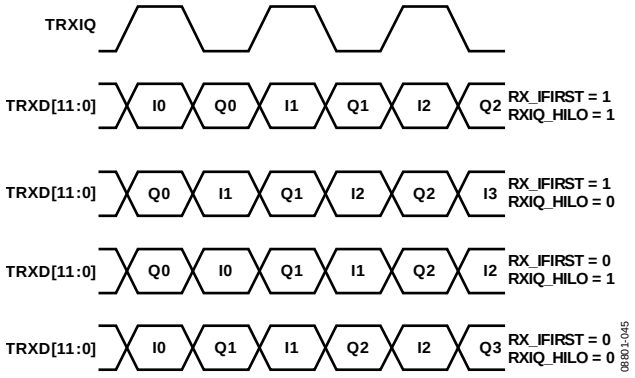


Figure 73. Receive Path Data Pairing Options

The output clock on TRXCLK can also be configured as a double data rate (DDR) clock. In this mode the output clock is divided by 2 and samples are placed on the TRXD[11:0] bus on both the rising and falling edges of the TRXCLK. Figure 74 shows the timing.

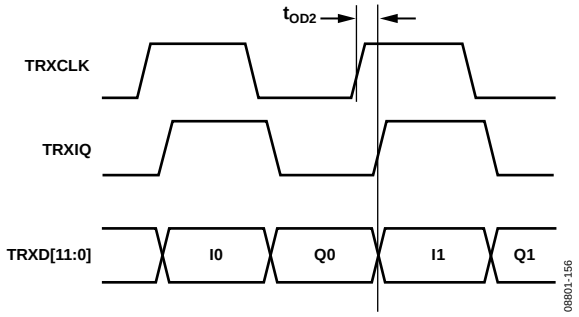


Figure 74. Receive Path Timing Diagram (DDR Clock Mode)

Table 23. Maximum Output Delay Between TRXCLK/ TRXD[11:0] and TRXIQ Signals from −40°C to +85°C

Parameter	Min	Max	Min	Max	Units
Drive Strength	Register 0x63 = 0x00		Register 0x63 = 0xAA		
t_{OD1}	0.55	0.93	0.36	0.57	ns
t_{OD2}	0.42	0.67	0.20	0.35	ns

SINGLE ADC MODE

The receive port can be operated with only one of the ADCs operational. In this mode the TRXCLK signal can operate in either bus rate clock mode or double data rate clock mode. The TRXIQ pin indicates which ADC is active. Figure 75 to Figure 78 show the timing options available.

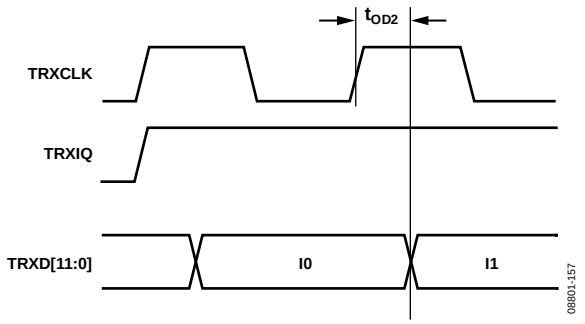


Figure 75. Rx Timing, I ADC Only, Bus Rate Clock Mode

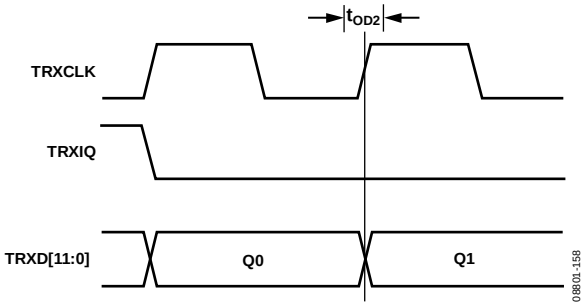


Figure 76. Rx Timing, Q ADC Only, Bus Rate Clock Mode

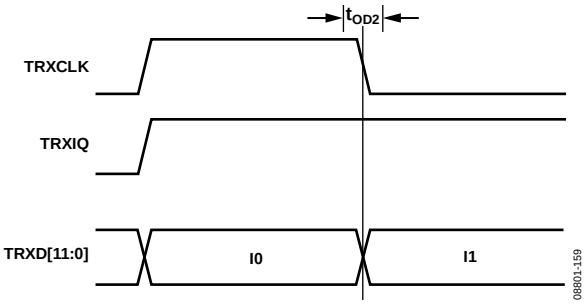


Figure 77. Rx Timing, I ADC Only, DDR Clock Mode

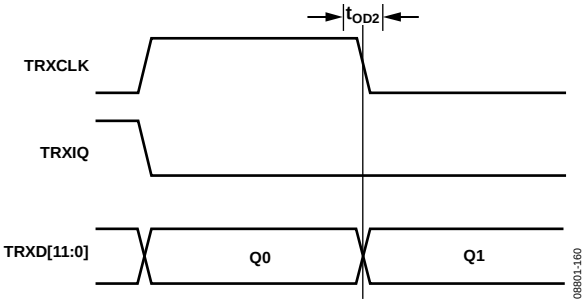


Figure 78. Rx Timing, Q ADC Only, DDR Clock Mode

In addition to the different timing modes listed in Figure 75 to Figure 78, the input data can also be delivered from the device in either unsigned binary or twos complement format. The format type is chosen via the RX_BNRY configuration bit.

TX PORT OPERATION (FULL-DUPLEX MODE)

The Tx port operates with a qualifying clock that can be configured as either an input or an output. The input data (TXD[11:0]) must be accompanied by the TXIQ signal which identifies to which transmit channel (I or Q) the data is intended. By default, the data and TXIQ signals are latched by the device on the rising edge of TXCLK. The timing diagram is shown in Figure 79,

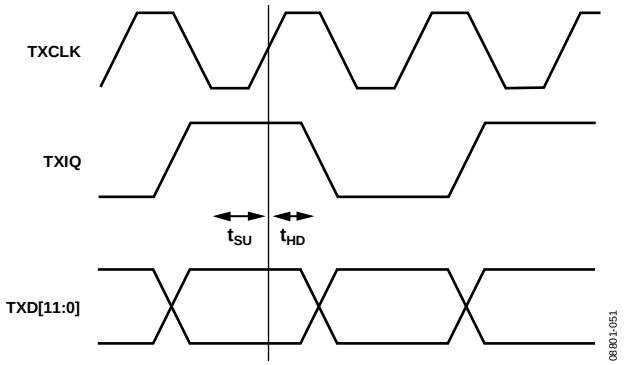


Figure 79. Tx Port Timing Diagram (Data Rate Clock Mode)

The setup and hold time requirements for the Tx port in data rate clock mode are given in Table 24.

The input samples to the device are assembled to create a quadrature pair of data. The data can be arranged in two possible data pairing orders and with two possible data to TXIQ signal phase relationships. This creates four possible timing modes. The AD9961/AD9963 can be configured to accept data in any of these four modes. The data pairing order is controlled by the TX_IFIRST bit. The data to TXIQ phase relationship is controlled by the TXIQ_HILO bit. The two programming options produce the four timing diagrams shown in Figure 80.

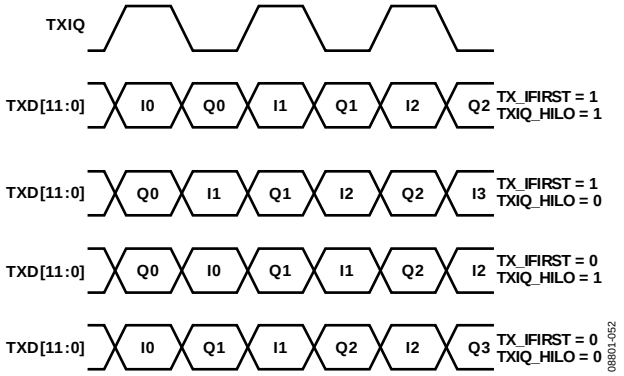


Figure 80. Transmit Path Data Pairing Options

In addition to the different timing modes listed above, the input data can also be accepted by the device in either unsigned binary or twos complement format. The format type is chosen via the TX_BNRY configuration bit.

The Tx port has an optional double data rate (DDR) clock mode. In DDR mode, the transmit data is latched on both the rising and falling edges of TXCLK. The polarity of the edge identifies to which channel the input data is intended. In this mode, the TXIQ signal is not required.

The interleaved digital data for the I and Q DACs is accepted by the Tx bus (TXD([11:0]). The data must be presented to the device such that it is stable throughout the setup and hold times, t_S and t_H, around both the rising and falling edges of the TXCLK signal. A detailed timing diagram is shown in Figure 81.

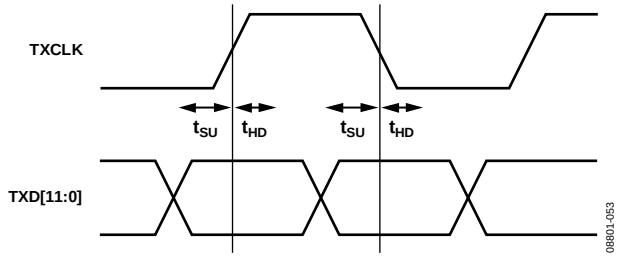


Figure 81. Tx Port Timing Diagram (DDR Clock Mode)

In DDR mode, the TXCLK signal is always an input and must be supplied along with the data. The setup and hold time requirements for the Tx port in DDR mode are given Table 24

Table 24. Tx Port Setup and Hold Times From −40°C to +85°C[1]

	DRVDD = 1.8 V		DRVDD = 3.3 V		
Tx Port Operating Mode	**t_{SU} (Min)**	**t_{HD} (Min)**	**t_{SU} (Min)**	**t_{HD} (Min)**	**Unit**
TXCLK_MD = 01	−0.02	+2.60	+0.29	+1.99	ns
TXCLK_MD = 10, TXDBLSEL = 1	−1.04	+4.24	−0.28	+3.92	ns
TXCLK_MD = 10, TXDBLSEL = 0	−0.61	+4.76	−0.14	+4.82	ns

[1] Specifications are preliminary and subject to change.

The input samples to the device are assembled to create a quadrature pair of data. The two possible data pairing orders and two possible data to TXIQ signal phase relationships create four possible timing modes. The AD9961/AD9963 can be configured to accept data in any of these four modes. The data pairing order is controlled by the TX_IFIRST bit. The data to TXIQ phase relationship is controlled by the TXIQ_HILO bit. The two programming options produce the four timing diagrams shown in Figure 82.

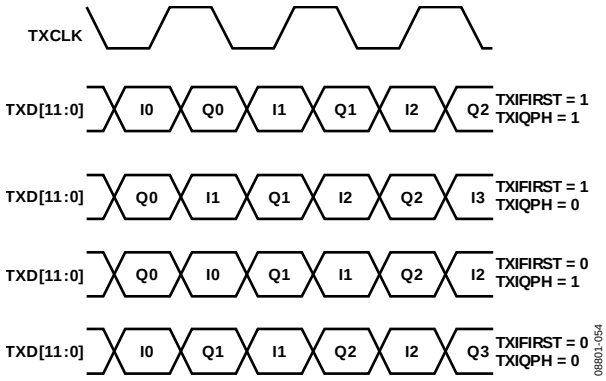


Figure 82. Transmit Path Timing Modes (DDR Mode)

HALF-DUPLEX MODE

The AD9961/AD9963 offer a half-duplex mode enabling a reduced width digital interface. In half-duplex mode, the transmit and receive ports are multiplexed onto the TRXD, TRXIQ, and TRXCLK lines. The direction of the bus can be controlled by either the TXIQ/TXnRX pin (for the rest of this section referred to as simply the TXnRX pin) or the serial port configuration registers.

The operation of the transmit and receive ports in half-duplex mode is very similar to the way they operate in full-duplex mode. In half-duplex mode, the interface can be configured to operate with a single clock pin, or with two clock pins. When in Rx mode (sourcing data) the TRX port operates the same in half-duplex mode as it does in full duplex. When in Tx mode, the TXIQ and TXD[11:0] signals are mapped onto the TRXIQ and TRXD[11:0] pins respectively. The TXCLK pin is mapped to the TRXCLK pin in one-clock mode and remains on the TXCLK pin in two-clock mode. Therefore, in one-clock mode, the TRXCLK pin carries the RXCLK signal when set in the Rx direction and the TXCLK signal when set in the Tx direction. In two-clock mode, the TRX pin carries the RXCLK signal and the TXCLK pin carries the TXCLK signal regardless of the bus direction. By default, the clocks sourced by the device are only present when the corresponding direction of the bus is active. Setup and hold times for the TRx port are shown in Table 25.

Table 25. TRx Port Setup and Hold Times From −40°C to +85°C

	DRVDD = 1.8 V		DRVDD = 3.3 V		
TRx Port Operating Mode	**t_{SU} (Min)**	**t_{HD} (Min)**	**t_{SU} (Min)**	**t_{HD} (Min)**	**Units**
TXCLK_MD = 01	+0.73	+1.61	+0.44	+1.90	ns
TXCLK_MD = 10, TXDBLSEL = 1	−1.66	+5.84	−0.96	+4.55	ns
TXCLK_MD = 10, TXDBLSEL = 0	−1.40	+6.62	−1.15	+5.11	ns

Table 26 shows the operating modes vs. serial port configuration bits.

Table 26. TRx Bus Operation via Serial Port

TXEN	RXEN	TRXD Bus Direction	Tx Bus Function
0	0	High-Z	High-Z
0	1	Rx	High-Z
1	0	Tx	High-Z
1	1	Rx	High-Z

Table 27 shows the operating modes of the TRXD bus as a function of the TXnRX signal. The Tx bus is high impedance in half-duplex mode.

Table 27. Rx Bus Operation via TXnRX Pin

TXnRX State	TRXD Bus Direction	Tx Bus Function
0	Rx	High-Z
1	Tx	High-Z

The timing of the bus turnaround is shown in the Figure 83 and Figure 84.

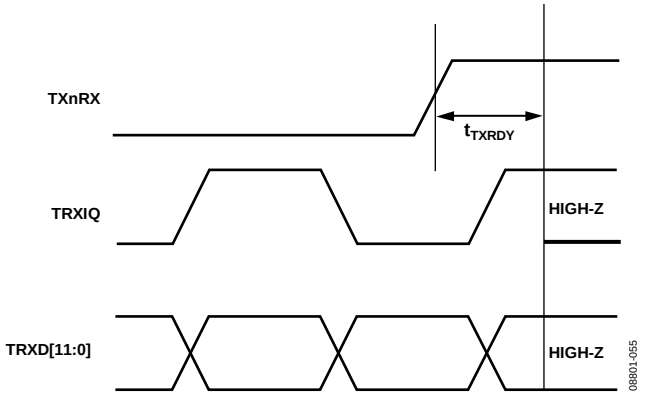


Figure 83. Half-Duplex Bus Turnaround, Rx to Tx

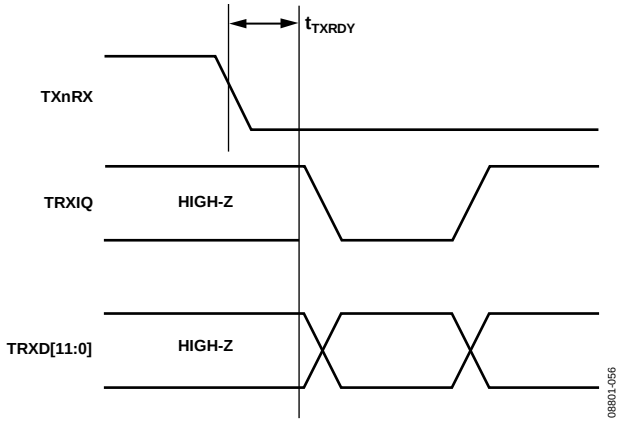


Figure 84. Half-Duplex Bus Turnaround, Tx to Rx

AUXILIARY CONVERTERS

The AD9961/AD9963 have two fast settling servo DACs, along with an analog input and two analog I/O pins. All of the auxiliary converters run off a dedicated supply pin. The input and output compliance ranges depend on the voltage supplied.

AUXILIARY ADC

The auxiliary ADC is a 12-bit SAR converter that is accessed and controlled through the serial port registers (Register 0x77 through Register 0x7B). The ADC voltage reference and clock signals are generated on chip. The auxiliary ADC is preceded by a seven-input multiplexer. The ADC inputs can be connected to either the AUXIN1, AUXIO2, AUXIO3 input pins, or one of four internal signals as shown in Figure 85.

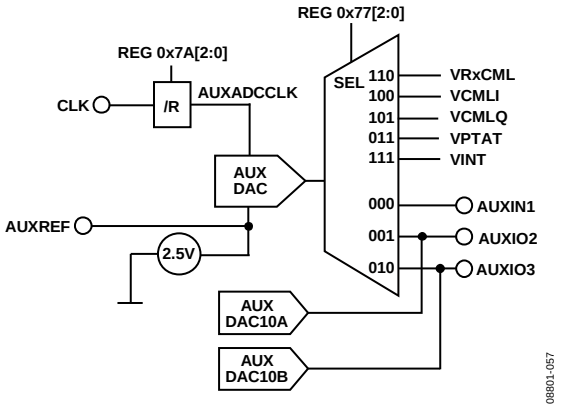


Figure 85. Block Diagram of Auxiliary ADC Circuitry

CONVERSION CLOCK

The auxiliary ADC conversion clock is generated through a programmable binary division of the CLK input signal. The frequency of the ADC conversion clock is programmable and can be calculated from the following equation:

$$f_{AUXCLK} = \frac{f_{CLK}}{R}$$

where *R* is programmed through Register 0x7A, Bits[2:0].

For best performance and lowest power consumption, the conversion clock speed should be set to the lowest speed that meets the system conversion time requirements. The maximum allowable auxiliary ADC clock speed is 10 MHz.

Voltage Reference

The auxiliary ADC has an internal, temperature stable, 2.5 V reference. This results in an input voltage range of 0 V to 3.2 V. When using the internal voltage reference, the AUXADCREF pin should be decoupled to AGND through a 0.22 µF capacitor. The AUXADCREF pin can be used as a reference output to external devices, but the current load on the pin should be limited to sourcing less than 5 mA and sinking less than 100 µA.

For systems with tight accuracy requirements, a higher accuracy external reference can be used to source a voltage into the AUXADCREF pin. The input voltage range for external voltage references is from 1.0 V to 2.5 V. The input impedance of the AUXADCREF pin is 100 kΩ. The full-scale input voltage of the ADC is a function of the voltage reference as:

$$V_{AUXFS} = \frac{3.2}{2.5} \times V_{AUXREF}$$

Analog Inputs

The ADC can be configured to sample one of eight analog inputs. The input is selected through the channels select bits (Register 0x77, Bits[2:0]). These eight signals are described in Table 28.

Table 28. Auxiliary ADC Channel Selections

Channel Select	Signal	Description
000	AUXIN1	Pin 72.
001	AUXIO2	Pin 71. The auxiliary DAC10A should be disabled when using this pin as an input.
010	AUXIO3	Pin 70. The auxiliary DAC10B should be disabled when using this pin as an input.
011	VPTAT	Voltage proportional to absolute temperature scaled to 0.2 °K per LSB. Therefore, the temperature in degrees C is: $T(\mathrm{C}^{\circ}) = \frac{ADC_CODE}{5} - 273.2$
100	VCMLI	Common mode level of the I and Q Rx ADC buffers. Should measure approximately 0.9 V. The buffer must be enabled (see Configuration Register 0x7E).
101	VCMLQ	
110	RXCML	The RXCML output voltage on Pin 10. This should measure approximately 1.4 V.
111	GND	Should measure 0 V.

When selected, Input Pin 70, Pin 71, and Pin 72 are connected to the sampling cap of the auxiliary ADC. Therefore, the circuits driving these inputs need to recover to the desired accuracy from having a discharged 10 pF capacitor connected to it at the initiation of the conversion, within the sampling window. A programmable delay (Register 0x7B, Bits[1:0]) can be added to the conversion cycle time to allow additional settling time of the input. If the ADC input is driven from a low source impedance, like the output of an op amp, a 20-cycle conversion time should yield good results. Higher impedance sources may require the 34-cycle conversion time to fully settle. Where the conversion cycle time is not an issue, it is recommended that the full 34-cycle conversion time be used.

Conversions where the input multiplexer is switched between inputs require a longer conversion cycle time than consecutive conversions from the same multiplexer input.

Digital Output Coding

The digital output coding is straight binary. The ideal transfer characteristic for the auxiliary ADC is shown in Figure 86.

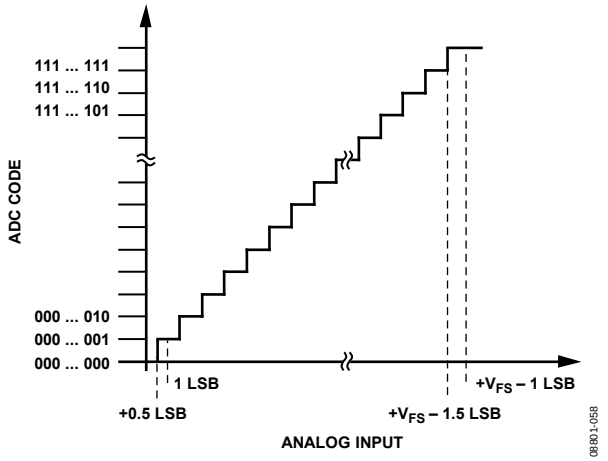


Figure 86. Auxiliary ADC Transfer Function

Auxiliary ADC Conversion Cycle

A conversion is initiated by writing to SPI Register 0x77. The conversion starts on the first rising edge of the AUXADCCLK following a write to Register 0x77 (serial port register writes are completed on the eighth rising edge of SCLK during the data word write cycle). The conversion takes from 20 to 34 AUXADCCLK cycles to complete depending on the conversion time setting programmed in Register 0x77. In most cases, the ADC throughput is a function of both the serial port clock rate and the ADC conversion time.

Figure 87 shows a typical timing scenario for an auxiliary ADC conversion period. The scenario shows the write that initiates the conversion, followed by the read that retrieves the conversion result. In some cases, it may be required to add a wait time between the write and read to ensure that the conversion is complete. The wait time depends on the ADC conversion cycle time and the speed of the serial port clock. The minimum wait time is calculated as:

$$t_{wait} \geq (N+1) \times t_{AUXADCCLK} - 7 \times t_{SCLK}$$

where N is the number of auxiliary ADC clock cycles that result from the conversion time setting in Register 0x7B. t_{SCLK} is the serial port clock period. A negative wait time indicates no wait time is required.

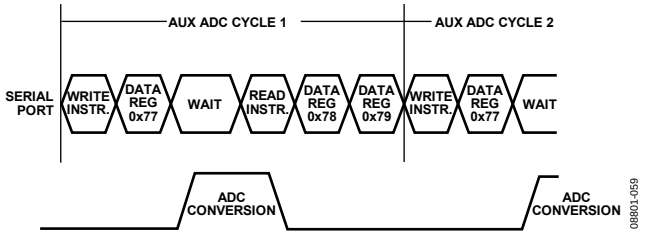


Figure 87. Timing Scenario for Auxiliary ADC Conversion Cycle

It should be noted that after initial power-up or recovery from power-down, the ADC needs about 100 µS to stabilize. In many cases, the results of the first conversion should be discarded in order for the auxiliary ADC to reach an optimum operating condition.

AUXILIARY DACs

The AD9963 has two 10-bit auxiliary DACs and two 12-bit auxiliary DACs suitable for calibration and control functions. The DACs have voltage outputs with selectable full-scale voltages and output ranges. The auxiliary DACs are configured and updated through the serial port interface.

10-Bit Auxiliary DACs

The two 10-bit DACs have identical transfer functions and are output on the AUXIO2 and AUXIO3 pins. The two DACs can be independently enabled and configured. The DACs have five selectable top-of-scale voltages and four selectable output ranges, which result in 20 possible transfer functions.

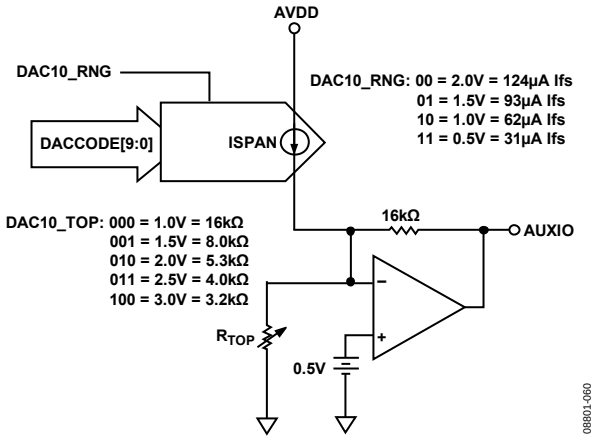


Figure 88. Simplified Circuit Diagram of the 10-Bit Auxiliary DAC

The circuit is most easily analyzed using superposition of two inputs to the op amp, the 0.5 V reference voltage, and the programmable current source. The following equation describes the no-load output voltage:

$$V_{OUT} = 0.5 + 16\text{k}\Omega \times \left(\frac{0.5V}{R_{TOP}} - \left(\frac{DACCODE}{1024} \right) \times I_{SPAN} \right)$$

The DACCODE (see Register 0x49 and Register 0x4A for DAC10A and Register 0x46 and Register 0x47 for DAC10B) is interpreted such that I_{SPAN} is full scale at 0x000 and zero at 0x3FF. This leads to an increasing output voltage with increasing code as shown in Figure 89 and Figure 90. The five selectable gain setting resistors of 3.2 kΩ, 4.0 kΩ, 5.3 kΩ, 8.0 kΩ, and 16 kΩ result in full-scale output voltage levels of 3.0 V, 2.5 V, 2.0 V, 1.5 V and 1.0 V respectively. The four selectable full-scale currents of 31 µA, 62 µA, 93 µA and 124 µA result in voltage output spans of 0.5 V, 1.0 V, 1.5 V, and 2.0 V, respectively.

The curves in Figure 89 represent four of the possible DAC transfer functions with the full-scale voltage of 3.0 V and spans of 0.5 V, 1.0 V, 1.5 V, and 2.0 V. The curves in Figure 90 represent four of the possible DAC transfer functions with the full-scale voltage of 1.5 V and spans of 0.5 V, 1.0 V, 1.5 V, and 2.0 V. Note that the 2.0 V span results in clamping at the lower end of the scale at 0 V where the equation resultsin negative output voltages.

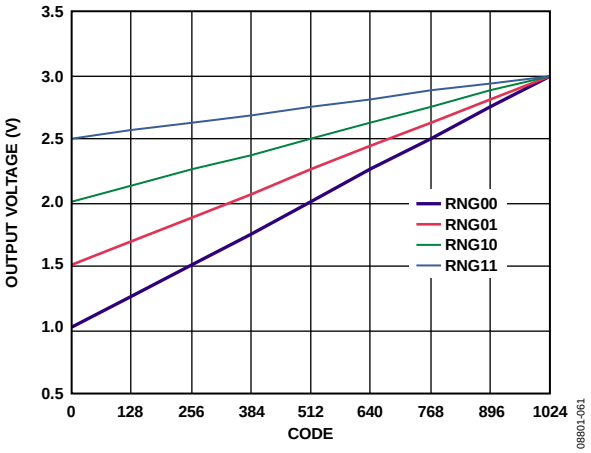


Figure 89. AUXDAC10 Voltage Output vs. Digital Code, V_{TOP} = 3.0 V (R_{TOP} = 3.2 kΩ)

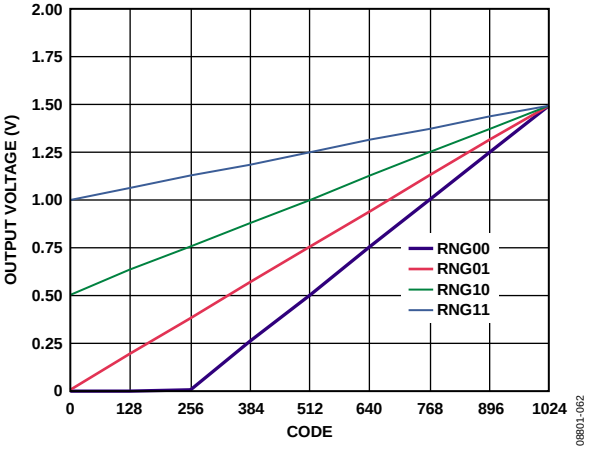


Figure 90. AUXDAC10 Voltage Output vs. Digital Code, V_{TOP} = 1.5 V (R_{TOP} = 8.0 kΩ)

12-Bit Auxiliary DACs

The two 12-bit DACs have similar transfer functions and are output on the DAC12A and DAC12B pins. The two DACs can be independently enabled and configured. Figure 91 shows a simplified schematic of the 12-bit auxiliary DAC.

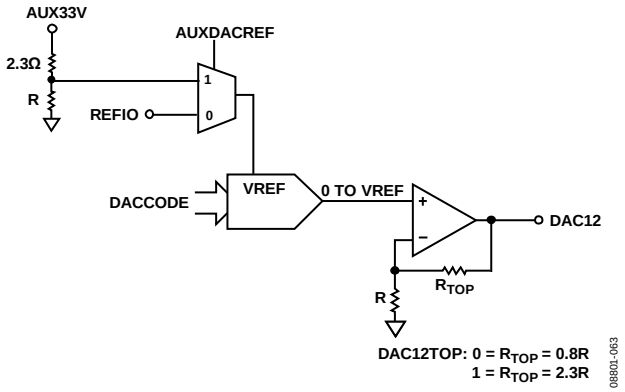


Figure 91. Simplified Schematic of the 12-Bit Auxiliary DAC

Note that VREF can be derived from a 1.0 V bandgap reference or be ratiometric with the AUX33V supply. An additional gain stage follows the DAC that sets the final full-scale output voltage . The following equation describes the no load output voltage:

$$V_{OUT} = \left(V_{FS} \times \left(\frac{DACCODE}{1024} \right) \right)$$

where V_{FS} is set with the combination of bits shown in Table 29.

Table 29. 12-Bit Auxiliary DAC Full-Scale Voltage Selection

AUXDAC_REF	DAC10x_RNG[1]	V_{FS}
0	0	AUX33V
0	1	0.54 × AUX33V
1	0	3.3 V
1	1	1.8 V

[1] x = A or B.

The curves in Figure 92 show the two transfer functions when using the internal 1.0 V bandgap reference.

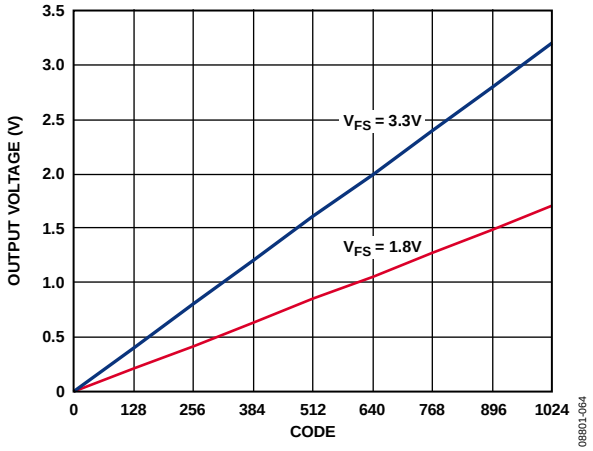


Figure 92. AUXDAC12 Voltage Output vs. Digital Code

POWER SUPPLIES

The AD9961/AD9963 power distributions are shown in Figure 93. The functional blocks labeled Rx ANLG, Rx ADCs, SPI and digital core, clocking, and DLL operate from 1.8 V supplies. The functional blocks labeled Tx DACs, AUX DACs and digital I/O operate over a supply voltage range from 1.8 V to 3.3 V. The auxiliary ADC operates from a 3.3 V supply.

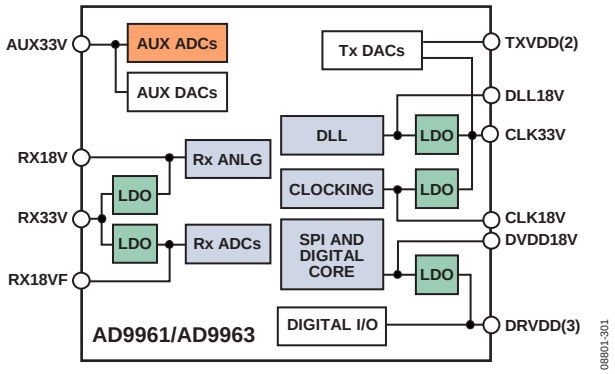


Figure 93. AD9961/AD9963 Power Distribution Block Diagram

The 1.8 V only blocks can be supplied directly with 1.8 V by using the RX18V, RX18VF, DLL18V, CLK18V, and DVDD18V supply pins. In this mode, the on-chip voltage regulators must be disabled. To provide optimal ESD protection for the device, the inputs of the LDO regulators should not be left floating. When unused, the LDO regulator inputs should be tied to one of the LDO outputs (for example, if RX33V is unused, tie RX33V to either RX18V or RX18VF).

When the LDO regulators are used, the RX18V, RX18VF, DLL18V, CLK18V, and DVDD18V pins should be decoupled to ground with a 0.1 µF or larger capacitor. The LDO inputs can operate over a range from 2.5 V to 3.3 V.

The LDO_EN pin (Pin 14) is a three-state input pin that controls the operation of the LDOs. When LDO_EN is high, all of the LDOs are enabled. When LDO_EN is low, all of the LDOs are disabled. When LDO_EN is floating or approximately DRVDD/2, only the DVDD18V LDO is enabled. All of the LDOs except the DVDD18V LDO can be independently disabled through serial port control as well by writing to Register 0x61.

The three DRVDD pins are internally connected together, therefore, these pins must be connected to the same voltage. The voltage applied to these pins affects the timing of the device as noted in the Digital Interfaces section.

The TXVDD and AUX33V supplies can operate over a range from 1.8 V to 3.3 V. It should be noted that the auxiliary ADC requires AUX33V to be 3.3 V for operation. The performance of the Tx DACs vary with the TXVDD supply as indicated in the Table 1 and Figure 4 to Figure 11.

POWER SUPPLY CONFIGURATION EXAMPLES

There are numerous ways of configuring the power supplies powering the AD9961/AD9963. Two power supply configuration examples are shown in Figure 94 and Figure 95.

Figure 94 shows a 3.3 V only power supply configuration. In this case, all of the internal circuits that require 1.8 V supplies are powered from the on-chip regulators. The LDO_EN pin is set high, and all of the internal LDOs are enabled. The transmit DAC, auxiliary converters, and I/O pads run from a 3.3 V supply.

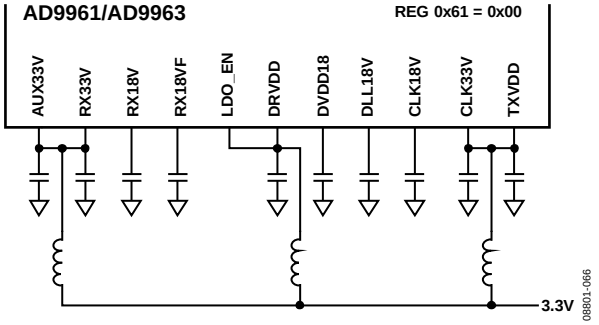


Figure 94. 3.3 V Only Supply Configuration

Figure 95 shows a power supply configuration where all 1.8 V voltage rails are powered by external supplies. The LDO_EN pin is grounded, and all of the internal LDOs are disabled. The transmit DAC, auxiliary converters and I/O pads run from a 3.3 V supply.

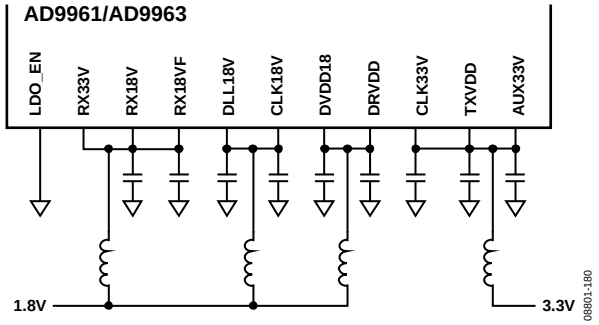


Figure 95. 3.3 V and 1.8 V Supply Configuration

POWER DISSIPATION

The AD9961/AD9963 power dissipation is highly dependent on operating conditions. Table 30 and Figure 96 to Figure 103 show the typical current consumption by power supply domain under different operating conditions.

The current draw from the 1.8 V supplies are independent of whether they are supplied by the on-chip regulators or by an external 1.8 V supply. The quiescent current of the LDO regulators are about 100 µA.

The current drawn from the AUX33V supply by the auxiliary ADC is typically 350 µA. The 10-bit auxiliary DACs each typically draw 275 µA from the AUX33V supply. The 12-bit auxiliary DACs typically draw 550 µA each from the AUX33V supply.

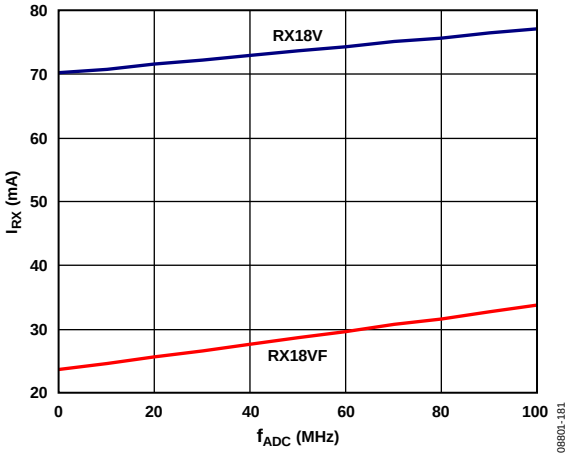


Figure 96. I_{RX18V} and I_{RX18VF} vs. f_{ADC}, Both ADCs Enabled

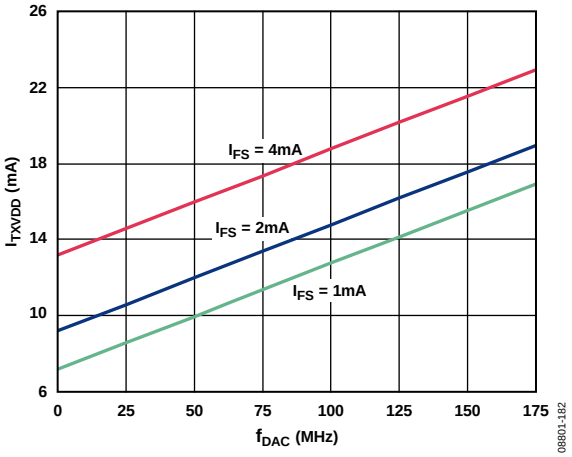


Figure 97. I_{TXVDD} vs. f_{DAC}, FSC = 1 mA, 2 mA, 4 mA, TXVDD = 3.3 V

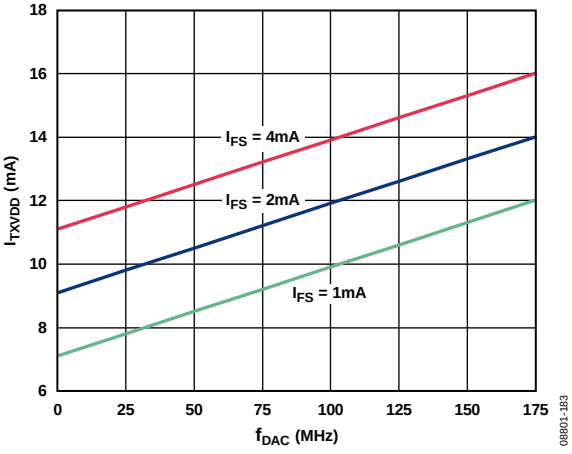


Figure 98. I_{TXVDD} vs. f_{DAC}, FSC = 1 mA, 2 mA, 4 mA, TXVDD = 1.8 V

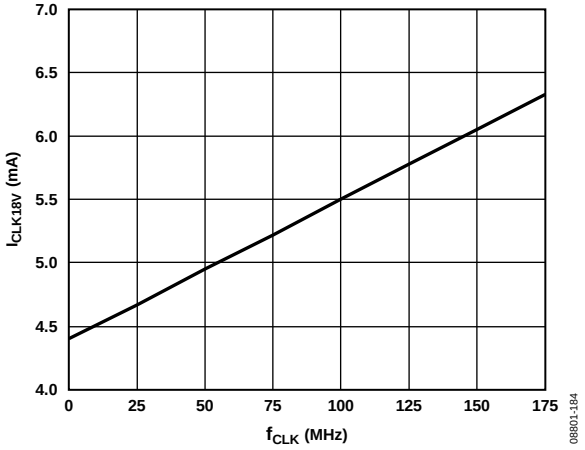


Figure 99. $I_{CLKVDD18}$ vs. f_{CLK}

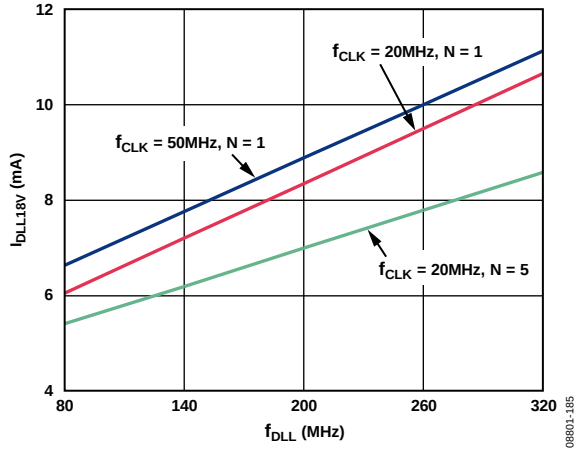


Figure 100. I_{DLL18V} vs. f_{DLL}, f_{CLKIN}= 19.2 MHz, 30.72 MHz

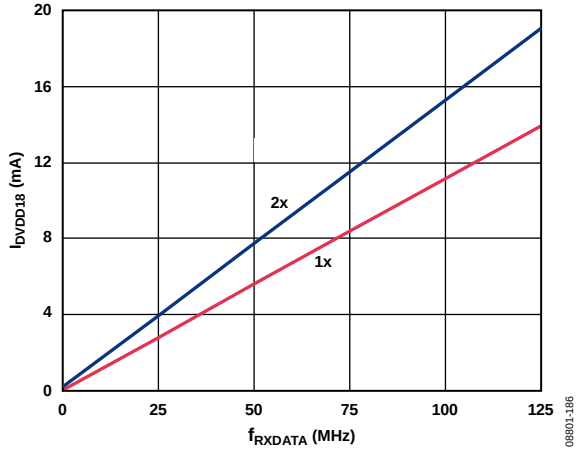


Figure 101. I_{DVDD18} vs. f_{RXDATA}, 1×, 2× (Rx Only)

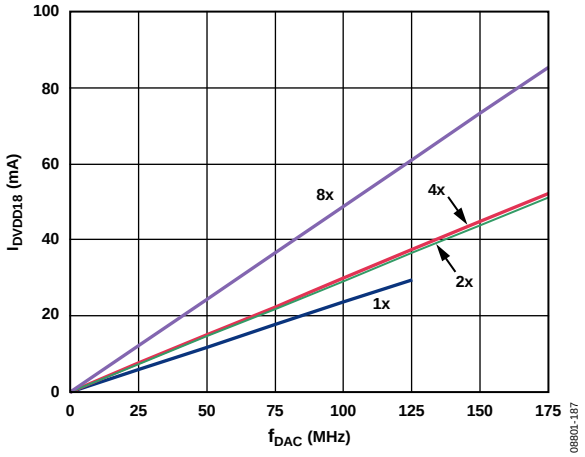


Figure 102. I_{DVDD18} vs. f_{DAC}, 1×, 2×, 4×, 8× (Tx only)

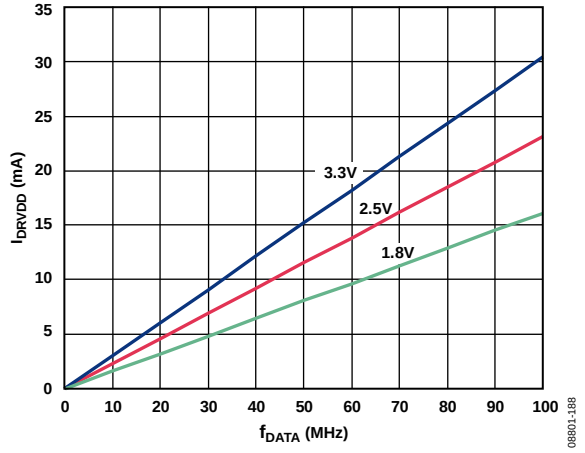


Figure 103. I_{DRVDD} vs. f_{DATA}, (Tx Enable and Disabled)

Power Calculation Example

The following example shows how to estimate the device power consumption under a typical operating condition.

Operating conditions:

f_{CLK} = 60 MHz

f_{DLL} = 120 MHz

f_{DAC} = 120 MHz

f_{ADC} = 60 MHz

4× interpolation

2× decimation

DAC full-scale current = 2 mA

TXVDD = CLK33V = AUX33V = 3.3 V

Auxiliary ADC enabled

All other supplies powered from external 1.8 V supplies.

Table 30. Example Power Supply Currents

Supply	Typical Current (mA)	Typical Power (mW)
RX18V	74	133
RX18VF	30	54
TXVDD	16	53
CLKVDD18V	5.2	9.5
DLL18V	7.5	13.5
DVDD18V (Rx)	9	16.2
DVDD18V (Tx)	35	63
DRVDD	5	9
AUX33V	0.5	1.7
Total (1.8 V)	169	298
Total (3.3 V)	16	55

EXAMPLE START-UP SEQUENCES

CONFIGURING THE DLL

The AD9963 DLL is shown in Figure 65, the clock distribution diagram. The register writes in Table 31 configures the DLL to drive the DACs with a multiplication in frequency of 10 and a division of 3 from the main CLKP/CLKN input. From the default register settings at reset, this would take a 20 MHz CLKP/CLKN clock, multiply it up to 200 MHz, then divide the clock down by 3 to produce 66.67 MHz. The write to Register 0x71 configures the DAC clock to be sourced from the DLL. By default, the Rx and Tx data buses operate in SDR mode. Each DAC is clocked at 66.67 MHz and the TxCLK pin outputs 133.33 MHz.

Table 31.

Register (hex)	Data (hex)	Comments
0x60	0x80	% enable DLL
0x71	0x53	% set DAC clock to DLL/enable DLL reference/N = 3
0x72	0x09	% M = 9, effective multiplication is M + 1 = 10
Delay 100 pS		
0x75	0x08	% hold DLL reset high
0xDelay 100 pS		
0x75	0x00	% hold DLL reset low
0x72	Read	% check Bit 7 to verify the DLL has locked

CONFIGURING THE CLOCK DOUBLERS (DDLL)

The AD9963 includes two clock doublers. The Rx clock doubler, if enabled, doubles the frequency of the CLKP/CLKN signal on its way into the circuit that generates ADCCLK (Figure 65). The Tx clock doubler doubles the DACCLK signal and can be selected to be included in the TxCLK generator circuit (Figure 52). Use of both clock doublers is recommended when the ADCs and DACs are operated above 15 MHz.

When operating below 75 MHz, bypass the duty cycle stabilizer in the ADCCLK generator circuit and take care to ensure a duty cycle 45% to 55% of the CLKP/CLKN clock input. The series of writes in Table 32 configures the Rx clock doubler to clock the ADCs from reset. These writes are for an ADC clock of < 75 MHz.

This same sequence could be used for setting up a clock >75 MHz by removing the write to Register 0x66.

Table 32.

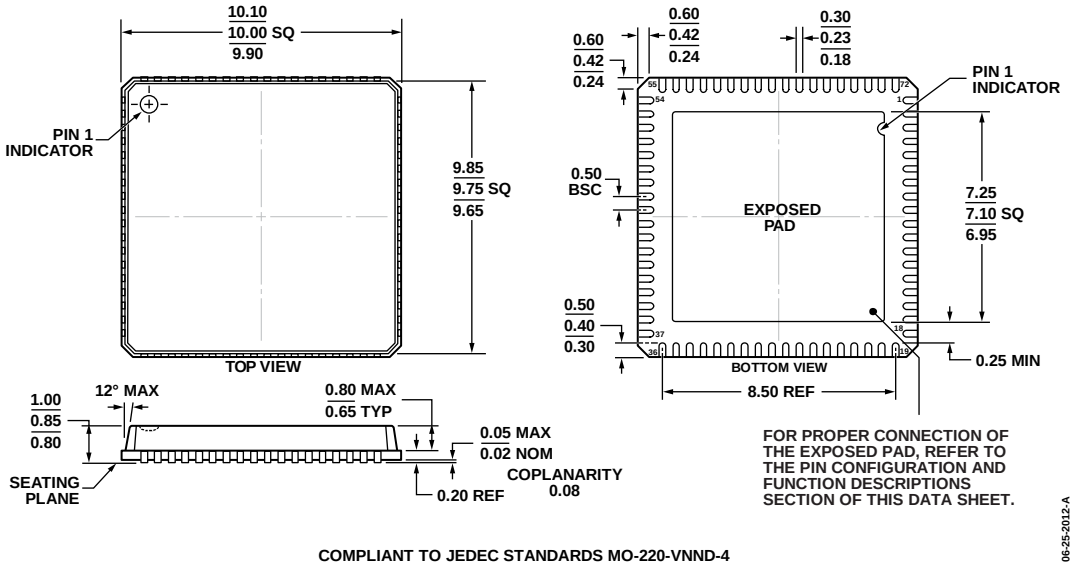
Register (hex)	Data (hex)	Comments
0x3C	0x00	% the recommended tap delay is 0
0x39	0x02	% configure RxCLK as DDLL
0x66	0x04	% bypass duty cycle correction (for CLKP/CLKN < 75 MHz)
0x3B	0x55	% the recommended offset is 1 (changing Bit 3 from default)
Delay 100 pS		
0x39	0x82	% reset Rx DDLL
Delay 100 pS		
0x39	0x02	% pull Rx DDLL out of reset
0x63	0x08	% set drive strength to 3 for the RxClk

SENSING TEMPERATURE WITH THE AUXADC

This sequence of register writes and reads configures the AUXADC to sense temperature.

Register (hex)	Data (hex)	Comments
0x77	0x03	Channel temperature sensor
0x7A	0x80	Aux ADC enable
0x7B	0x80	Temperature sensor enable
0x77	0x83	Choose channel to sample with AUX ADC
Read	0x78	MSB 7:0 = AUXADC[11:4]
Read	0x79	LSB bit 7:4 = AUXADC[3:0]

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 104. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9961BCPZ	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-4
AD9961BCPZRL	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-4
AD9963BCPZ	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-4
AD9963BCPZRL	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-4
AD9961-EBZ	−40°C to +85°C	Evaluation Board	
AD9963-EBZ	−40°C to +85°C	Evaluation Board	
AD-DPGIOZ	−40°C to +85°C	Pattern Generation and Capture Card	

[1] Z = RoHS Compliant Part.

NOTES

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