100 MSPS/140 MSPS Analog Flat Panel Interface

AD9884A

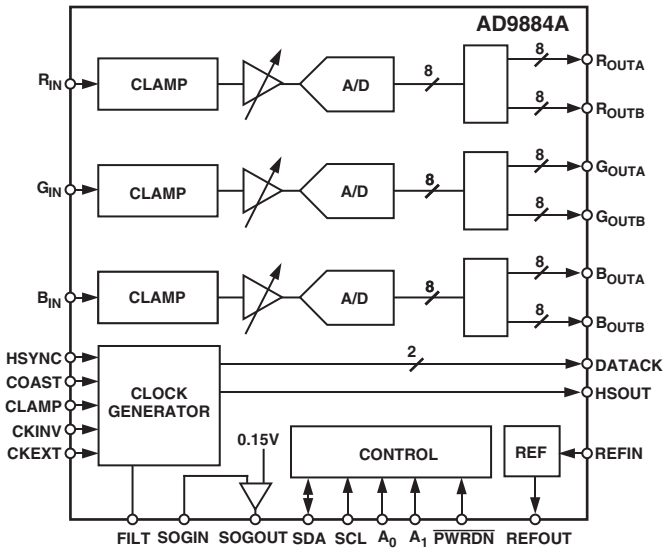
FEATURES

140 MSPS Maximum Conversion Rate
500 MHz Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
400 ps p-p PLL Clock Jitter
Power-Down Mode
3.3 V Power Supply
2.5 V to 3.3 V Three-State CMOS Outputs
Demultiplexed Output Ports
Data Clock Output Provided
Low Power: 570 mW Typical
Internal PLL Generates CLOCK from HSYNC
Serial Port Interface
Fully Programmable
Supports Alternate Pixel Sampling for Higher-Resolution Applications

APPLICATIONS

RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9884A is a complete 8-bit 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full-power analog bandwidth of 500 MHz supports display resolutions of up to 1280 × 1024 (SXGA) at 75 Hz with sufficient input bandwidth to accurately acquire and digitize each pixel.

To minimize system cost and power dissipation, the AD9884A includes an internal 1.25 V reference, PLL to generate a pixel clock from HSYNC, and programmable gain, offset and clamp circuits. The user provides only a 3.3 V power supply, analog input, and HSYNC signals. Three-state CMOS outputs may be powered by a supply between 2.5 V and 3.3 V.

The AD9884A's on-chip PLL generates a pixel clock from the HSYNC input. Pixel clock output frequencies range from 20 MHz to 140 MHz. PLL clock jitter is typically 400 ps p-p relative to the input reference. When the COAST signal is presented, the PLL maintains its output frequency in the absence of HSYNC. A 32-step sampling phase adjustment is provided. Data, HSYNC and Data Clock output phase relationships are always maintained. The PLL can be disabled and an external clock input provided as the pixel clock.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This device is fully programmable via a two-wire serial port.

Fabricated in an advanced CMOS process, the AD9884A is provided in a space-saving 128-lead MQFP surface mount plastic package and is specified over a 0°C to +70°C temperature range.

REV. C

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AD9884A–SPECIFICATIONS

(V_D = 3.3 V, V_{DD} = 3.3 V, PV_D = 3.3 V, ADC Clock Frequency = Maximum, PLL Clock Frequency = Maximum, Control Registers Programmed to Default State)

Parameter	Temp	Test Level	AD9884AKS-100 Min	AD9884AKS-100 Typ	AD9884AKS-100 Max	AD9884AKS-140 Min	AD9884AKS-140 Typ	AD9884AKS-140 Max	Unit
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.5	±1.0		±0.5	+1.15/–1.0	LSB
	Full	VI			±1.0			+1.25/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.25		±0.8	±1.4	LSB
	Full	VI			±1.75			±2.5	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		100			280		ppm/°C
Input Bias Current	25°C	I			1			1	µA
	Full	VI			1			1	µA
Input Offset Voltage	Full	VI		7	50		7	50	mV
Input Full-Scale Matching	Full	VI		1.5	5.0		1.5	5.0	%FS
Offset Adjustment Range	Full	VI	22	23.5	25	22	23.5	25	%FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	1.20	1.25	1.30	1.20	1.25	1.30	V
Temperature Coefficient	Full	V		±50			±50		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	100			140			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Data to Clock Skew, t_{SKEW}	Full	IV	–0.5		+2.0	–0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	0			0			µs
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			ns
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	100			140			MHz
Minimum PLL Clock Rate	Full	IV			20			20	MHz
PLL Jitter	25°C	IV		400	700[1]		475	750[2]	ps p-p
	Full	IV			1000[1]			1000[2]	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Current, High (I_{IH})	Full	VI			–1.0			–1.0	µA
Input Current, Low (I_{IL})	Full	VI			+1.0			+1.0	µA
Input Capacitance	25°C	V		3			3		pF
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_{DD} – 0.1			V_{DD} – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle									
DATACK, $\overline{\text{DATACK}}$	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		

Parameter	Temp	Test Level	AD9884AKS-100 Min	AD9884AKS-100 Typ	AD9884AKS-100 Max	AD9884AKS-140 Min	AD9884AKS-140 Typ	AD9884AKS-140 Max	Unit
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	V
PV_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25°C	V		125			135		mA
I_{DD} Supply Current (V_{DD})[3]	25°C	V		33			47		mA
IPV_D Supply Current (PV_D)	25°C	V		15			15		mA
Total Power Dissipation	Full	VI		570	675		650	775	mW
Power-Down Supply Current	Full	VI		2.0	25		2.0	25	mA
Power-Down Dissipation	Full	VI		6.6	82.5		6.6	82.5	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		500			500		MHz
Transient Response	25°C	V		2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR)[4]	25°C	I	44.0	46.5		43.5	46.2		dB
(Without Harmonics)	Full	V		46.0			45.0		dB
f_{IN} = 40.7 MHz									
Crosstalk	Full	V		60			60		dBc
THERMAL CHARACTERISTICS									
θ_{JC}–Junction-to-Case									
Thermal Resistance		V		8.4			8.4		°C/W
θ_{JA}–Junction-to-Ambient									
Thermal Resistance		V		35			35		°C/W

NOTES
[1]VCORNGE = 01, CURRENT = 001, PLLDIV = 1693_{10}.
[2]VCORNGE = 10, CURRENT = 110, PLLDIV = 1600_{10}.
[3]DEMUX = 1; DATACK and $\overline{\text{DATACK}}$ load = 15 pF; Data load = 5 pF.
[4]Using external pixel clock.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9884AKS-140	0°C to 70°C	MQFP	S-128
AD9884AKS-100	0°C to 70°C	MQFP	S-128
AD9884A/PCB	25°C	Evaluation Board	

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.
II. 100% production tested at 25°C and sample tested at specified temperatures.
III. Sample tested only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.
VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ABSOLUTE MAXIMUM RATINGS*

V_D, PV_D . . . . . –0.5 V to +4 V
PV_D to V_D . . . . . ±0.5 V
V_{DD} . . . . . –0.5 V to +4 V
Analog Inputs . . . . . V_D to –0.5 V
REFIN . . . . . V_D to 0.0 V
Digital Inputs . . . . . V_D to 0.0 V
Digital Output Current . . . . . 20 mA
Operating Temperature . . . . . –20°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Case Temperature . . . . . 150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

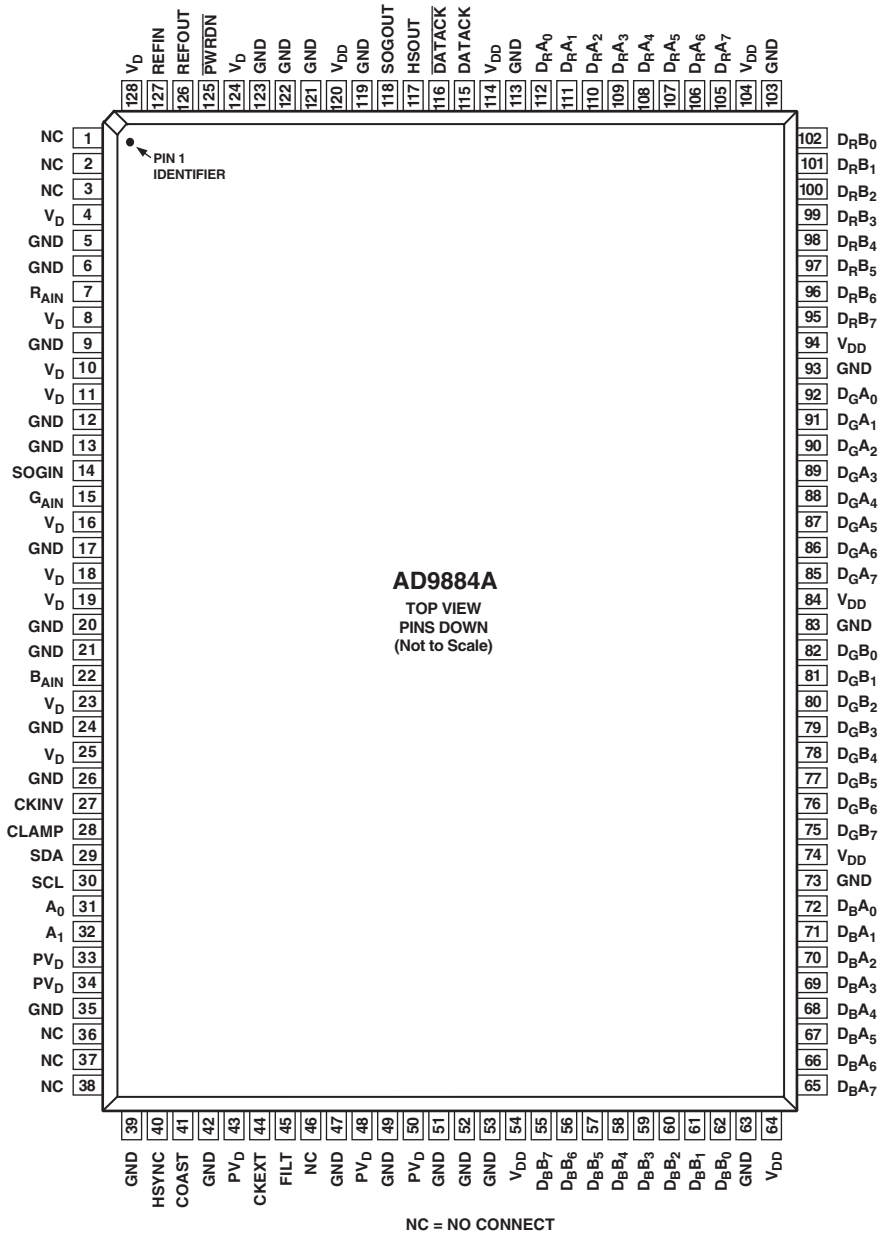
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9884A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. Package Interconnections

Signal Type	Name	Function	Value	Package Pin
Inputs	R_{AIN}	Analog Input for RED Channel	0.5 V to 1.0 V FS	7
	G_{AIN}	Analog Input for GREEN Channel	0.5 V to 1.0 V FS	15
	B_{AIN}	Analog Input for BLUE Channel	0.5 V to 1.0 V FS	22
	HSYNC	Horizontal Sync Input	3.3 V CMOS	40
	COAST	Clock Generator Coast Input (Optional)	3.3 V CMOS	41
	CLAMP	External Clamp Input (Optional)	3.3 V CMOS	28
	SOGIN	Sync On Green Slicer Input (Optional)	0.5 V to 1.0 V FS	14
	CKEXT	External Clock Input (Optional)	3.3 V CMOS	44
	CKINV	Sampling Clock Inversion (Optional)	3.3 V CMOS	27
Outputs	D_RA_{7-0}	Data Output, Red Channel, Port A	3.3 V CMOS	105–112
	D_RB_{7-0}	Data Output, Red Channel, Port B	3.3 V CMOS	95–102
	D_GA_{7-0}	Data Output, Green Channel, Port A	3.3 V CMOS	85–92
	D_GB_{7-0}	Data Output, Green Channel, Port B	3.3 V CMOS	75–82
	D_BA_{7-0}	Data Output, Blue Channel, Port A	3.3 V CMOS	65–72
	D_BB_{7-0}	Data Output, Blue Channel, Port B	3.3 V CMOS	55–62
	DATACK	Data Output Clock	3.3 V CMOS	115
	$\overline{\text{DATACK}}$	Data Output Clock Complement	3.3 V CMOS	116
	HSOUT	Horizontal Sync Output	3.3 V CMOS	117
	SOGOUT	Sync On Green Slicer Output	3.3 V CMOS	118
Control	SDA	Serial Data I/O	3.3 V CMOS	29
	SCL	Serial Interface Clock	3.3 V CMOS	30
	A_0, A_1	Serial Port Address LSBs	3.3 V CMOS	31, 32
	$\overline{\text{PWRDN}}$	Power-Down Control Input	3.3 V CMOS	125
Analog Interface	REFOUT	Internal Reference Output	1.25 V	126
	REFIN	Reference Input	1.25 V ± 10%	127
	FILT	External Filter Connection		45
Power Supply	V_D	Main Power Supply	3.3 V ± 10%	4, 8, 10, 11, 16, 18, 19, 23, 25, 124, 128
	V_{DD}	Digital Output Power Supply	2.5 V to 3.3 V ± 10%	54, 64, 74, 84, 94, 104, 114, 120
	PV_D	Clock Generator Power Supply	3.3 V ± 10%	33, 34, 43, 48, 50
	GND	Ground	0 V	5, 6, 9, 12, 13, 17, 20, 21, 24, 26, 35, 39, 42, 47, 49, 51, 52, 53, 63, 73, 83, 93, 103, 113, 119, 121, 122, 123
No Connect	NC			1–3, 36–38, 46

PIN CONFIGURATION



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Pin Name	Function
INPUTS	
R_{AIN} G_{AIN} B_{AIN}	Analog Input for RED Channel Analog Input for GREEN Channel Analog Input for BLUE Channel High impedance inputs that accepts the RED, GREEN, and BLUE channel graphics signals, respectively. The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference. They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.
HSYNC	Horizontal Sync Input This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by HSPOL. Only the *leading* edge of HSYNC is active. When HSPOL = 0, the falling edge of HSYNC is used. When HSPOL = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V. Electrostatic Discharge (ESD) protection diodes will conduct heavily if this pin is driven more than 0.5 V above the 3.3 V power supply (or more than 0.5 V below ground). If a 5 V signal source is driving this pin, the signal should be clamped or current limited.
COAST	Clock Generator Coast Input (optional) This input may be used to cause the pixel clock generator to stop synchronizing with HSYNC and continue producing a clock at its present frequency and phase. This is useful when processing sources that fail to produce horizontal sync pulses when in the vertical interval. The COAST signal is generally NOT required for PC-generated signals. The logic sense of this pin is controlled by CSTPOL. COAST may be asserted at any time. When not used, this pin must be grounded and CSTPOL programmed to 1. CSTPOL defaults to 1 at power-up.
CLAMP	External Clamp Input (optional) This logic input may be used to define the time during which the input signal is clamped to ground, establishing a black reference. It should be exercised when a black signal is known to be present on the analog input channels, typically during the back porch period of the graphics signal. The CLAMP pin is enabled by setting control bit EXTCLMP to 1 (default power-up is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the HSYNC input. The logic sense of this pin is controlled by CLAMPOL. When not used, this pin must be grounded and EXTCLMP programmed to 0.
SOGIN	Sync On Green Slicer Input (optional) This input is provided to assist in processing signals with embedded sync, typically on the GREEN channel. The pin is connected to a high speed comparator with an internally-generated threshold of 0.15 V. When connected to a dc-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT that changes state whenever the input signal crosses 0.15 V. This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal to HSYNC. The SOG slicer comparator continues to operate when the AD9884A is put into a power-down state. When not used, this input should be grounded.
CKEXT	External Clock Input (optional) This pin may be used to provide an external clock to the AD9884A, in place of the clock internally-generated from HSYNC. This input is enabled by programming EXTCLK to 1. When an external clock is used, all other internal functions operate normally. When unused, this pin should be tied through a 10 kΩ resistor to GROUND, and EXTCLK programmed to 0. The clock phase adjustment still operates when an external clock source is used.
CKINV	Sampling Clock Inversion (optional) This pin may be used to invert the pixel sampling clock, which has the effect of shifting the sampling phase 180 degrees. This is in support of Alternate Pixel Sampling mode, wherein higher frequency input signals (up to 280 Mpps) may be captured by first sampling the odd pixels, then capturing the even pixels on the subsequent frame. This pin should be exercised only during blanking intervals (typically vertical blanking) as it may produce several samples of corrupted data during the phase shift. CKINV should be grounded when not used.

PIN FUNCTION DESCRIPTIONS (continued)

Pin Name	Function
OUTPUTS	
D_RA_{7-0}	Data Output, Red Channel, Port A
D_RB_{7-0}	Data Output, Red Channel, Port B
D_GA_{7-0}	Data Output, Green Channel, Port A
D_GB_{7-0}	Data Output, Green Channel, Port B
D_BA_{7-0}	Data Output, Blue Channel, Port A
D_BB_{7-0}	Data Output, Blue Channel, Port B The main data outputs. Bit 7 is the MSB. Each channel has two ports. When the part is operated in Single Channel mode (DEMUX = 0), all data are presented to Port A, and Port B is placed in a high impedance state. Programming DEMUX to 1 establishes Dual Channel mode, wherein alternate pixels are presented to Port A and Port B of each channel. These will appear simultaneously, two pixels presented at the time of every second input pixel, when PAR is set to 1 (parallel mode). When PAR = 0, pixel data appear alternately on the two ports, one new sample with each incoming pixel (interleaved mode). In Dual Channel mode, the first pixel sampled after HSYNC is routed to Port A. The second pixel goes to Port B, the third to A, etc. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK, $\overline{\text{DATACK}}$ and HSOUT outputs are also moved, so the timing relationship among the signals is maintained.
DATACK	Data Output Clock
$\overline{\text{DATACK}}$	Data Output Clock Complement Differential data clock output signals to be used to strobe the output data and HSOUT into external logic. They are produced by the internal clock generator and are synchronous with the internal pixel sampling clock. When the AD9884A is operated in Single Channel mode, the output frequency is equal to the pixel sampling frequency. When operating in Dual Channel mode, the Data Output Clock and the Output Data are presented at one-half the pixel rate. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, $\overline{\text{DATACK}}$ and HSOUT outputs are all moved, so the timing relationship among the signals is maintained. Either or both signals may be used, depending on the timing mode and interface design employed.
HSOUT	Horizontal Sync Output A reconstructed and phase-aligned version of the HSYNC input. This signal is always active HIGH. By maintaining alignment with DATACK, $\overline{\text{DATACK}}$, and Data, data timing with respect to horizontal sync can always be clearly determined.
SOGOUT	Sync On Green Slicer Output The output of the Sync On Green slicer comparator. When SOGIN is presented with a dc-coupled ground-referenced analog graphics signal containing composite sync, SOGOUT will produce a digital composite sync signal. This signal gets no other processing on the AD9884A. The SOG slicer comparator continues to operate when the AD9884A is put into a power-down state.
CONTROL	
SDA	Serial Data I/O Bidirectional data port for the serial interface port.
SCL	Serial Interface Clock Clock input for the serial interface port.
A_{1-0}	Serial Port Address LSBs The two least significant bits of the serial port address are set by the logic levels on these pins. Connect a pin to ground to set the address bit to 0. Tie it HIGH (to V_D through 10 kΩ) to set the address bit to 1. Using these pins, the serial address may be set to any value from 98h to 9Fh. Up to four AD9884As may be used on the same serial bus by appropriately setting these bits. They can also be used to change the AD9884A address if a conflict is found with another device on the bus.
$\overline{\text{PWRDN}}$	Power-Down Control Input Bringing this pin LOW puts the AD9884A into a very low power dissipation mode. The output buffers are placed in a high impedance state. The clock generator is stopped. The control register contents are maintained. The Sync On Green Slicer (SOGOUT) and internal reference continue to function.

PIN FUNCTION DESCRIPTIONS (continued)

Pin Name	Function
ANALOG INTERFACE	
REFOUT	Internal Reference Output Output from the internal 1.25 V bandgap reference. This output is intended to drive relatively light loads. It can drive the AD9884A Reference input directly, but should be externally buffered if it is used to drive other loads as well. The absolute accuracy of this output is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9884A applications. If higher accuracy is required, an external reference may be employed. If an external reference is used, tie this pin to ground through a 0.1 µF capacitor.
REFIN	Reference Input The reference input accepts the master reference voltage for all AD9884A internal circuitry (+1.25 V ± 10%). It may be driven directly by the REFOUT pin. Its high impedance presents a very light load to the reference source. This pin should be bypassed to Ground with a 0.1 µF capacitor.
FILT	External Filter Connection For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in *Figure* 10 to this pin. For optimal performance, minimize noise and parasitics on this node.
POWER SUPPLY	
V_D	Main Power Supply These pins supply power to the main elements of the circuit. It should be as quiet and filtered as possible.
V_{DD}	Digital Output Power Supply A large number of output pins (up to 52) switching at high speed (up to 140 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the V_D pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9884A is interfacing with lower-voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 2.5 V) for compatibility.
PV_D	Clock Generator Power Supply The most sensitive portion of the AD9884A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide "quiet," noise-free power to these pins.
GND	Ground The ground return for all circuitry on chip. It is recommended that the AD9884A be assembled on a single solid ground plane, with careful attention to ground current paths. See the Design Guide for details.

CONTROL REGISTER MAP

The AD9884A is initialized and controlled by a set of registers that determine the operating modes. An external controller is employed to write and read the control registers through the 2-line serial interface port.

Table II. Control Register Map

Reg	Bit	Default	Mnemonic	Function
PLL Divider Control				
00	7–0	01101001	PLLDIVM	PLL Divide Ratio MSBs
01	7–4	1101••••	PLLDIVL	PLL Divide Ratio LSBs
01	3–0	••••0000		Reserved, Set to Zero
Input Gain				
02	7–0	10000000	REDGAIN	Red Channel Gain Adjust
03	7–0	10000000	GRNGAIN	Green Channel Gain Adjust
04	7–0	10000000	BLUGAIN	Blue Channel Gain Adjust
Input Offset				
05	7–2	100000••	REDOFST	Red Channel Offset Adjust
05	1–0	••••••00		Reserved, Set to Zero
06	7–2	100000••	GRNOFST	Green Channel Offset Adjust
06	1–0	••••••00		Reserved, Set to Zero
07	7–2	100000••	BLUOFST	Blue Channel Offset Adjust
07	1–0	••••••00		Reserved, Set to Zero
Clamp Timing				
08	7–0	10000000	CLPLACE	Clamp Placement
09	7–0	10000000	CLDUR	Clamp Duration
General Control 1				
0A	7	1•••••••	DEMUX	Output Port Select
0A	6	•1••••••	PAR	Output Timing Select
0A	5	••1•••••	HSPOL	HSYNC Polarity
0A	4	•••1••••	CSTPOL	COAST Polarity
0A	3	••••0•••	EXTCLMP	Clamp Signal Source
0A	2	•••••1••	CLAMPOL	Clamp Signal Polarity
0A	1	••••••0•	EXTCLK	External Clock Select
0A	0	•••••••0		Reserved, Set to Zero
Clock Generator Control				
0B	7–3	10000•••	PHASE	Clock Phase Adjust
0B	2–0	•••••000		Reserved, Set to Zero
0C	7	0•••••••		Reserved, Set to Zero
0C	6–5	•01•••••	VCORNGE	VCO Range Select
0C	4–2	•••001••	CURRENT	Charge Pump Current
0C	1–0	••••••00		Reserved, Set to Zero
General Control 2				
0D	7–5	000•••••		Reserved, Set to Zero
0D	4	•••0••••	OUTPHASE	Output Port Phase
0D	3–1	••••000•	REVID	Die Revision ID
0D	0	•••••••0		Reserved, Set to Zero
0E	7–0	00000000		Reserved, Set to Zero

Table III. Default Register Values

Reg	Value		Reg	Value	
00	01101001	69h	08	10000000	80h
01	1101 0000	D0h	09	10000000	80h
02	10000000	80h	0A	11110100	F4h
03	10000000	80h	0B	10000 000	80h
04	10000000	80h	0C	0 01 001 00	24h
05	100000 00	80h	0D	00000000	00h
06	100000 00	80h	0E	0000xxx0	0xh
07	100000 00	80h	0F	00000000	00h

CONTROL REGISTER DETAIL

PLL DIVIDER CONTROL

00	7–0	PLLDIVM	PLL Divide Ratio MSBs

The eight most significant bits of the 12-bit PLL divide ratio PLLDIV. *The operational divide ratio is PLLDIV* + 1.

The PLL derives a master clock from an incoming HSYNC signal. The master clock frequency is then divided by an integer value, and the divider's output is phase-locked to HSYNC. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of PLLDIV supports divide ratios from 2 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed HSYNC frequency.

VESA has established some standard timing specifications, which will assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table VII). However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

01	7–4	PLLDIVL	PLL Divide Ratio LSBs

The four least significant bits of the 12-bit PLL divide ratio PLLDIV. *The operational divide ratio is PLLDIV* + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

INPUT GAIN

02	7–0	REDGAIN	Red Channel Gain Adjust

An 8-bit word that sets the gain of the RED channel. The AD9884A can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting REDGAIN to 255 corresponds to an input range of 1.0 V. A REDGAIN of 0 establishes an input range of 0.5 V. Note that *increasing* REDGAIN results in the picture having *less* contrast (the input signal uses fewer of the available converter codes). See Figure 8.

The power-up default value is REDGAIN = 80h.

03	7–0	GRNGAIN	Green Channel Gain Adjust

An 8-bit word that sets the gain of the GREEN channel. See REDGAIN (02).

The power-up default value is GRNGAIN = 80h.

04	7–0	BLUGAIN	Blue Channel Gain Adjust

An 8-bit word that sets the gain of the BLUE channel. See REDGAIN (02).

The power-up default value is BLUGAIN = 80h.

INPUT OFFSET

05	7–2	REDOFST	Red Channel Offset Adjust

A six-bit offset binary word that sets the dc offset of the RED channel.

One LSB of offset adjustment equals approximately one LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel is changed (Figure 9). A nominal setting of 31 results in the channel nominally clamping the back porch (during the clamping interval) to code 00. An offset setting of 63 results in the channel clamping to code 31 of the ADC. An offset setting of 0 clamps to code –31 (off the bottom of the range). Increasing the value of REDOFST decreases the brightness of the channel.

The power-up default value is REDOFST = 80h.

06	7–2	GRNOFST	Green Channel Offset Adjust

A six-bit offset binary word that sets the dc offset of the GREEN channel. See REDOFST (05).

The power-up default value is GRNOFST = 80h.

07	7–2	BLUOFST	Blue Channel Offset Adjust

A six-bit offset binary word that sets the DC offset of the GREEN channel. See REDOFST (05).

The power-up default value is BLUOFST = 80h.

CLAMP TIMING

08	7–0	CLPLACE	Clamp Placement

An 8-bit register that sets the position of the internally generated clamp.

When EXTCLMP = 0, a clamp signal is generated internally, at a position established by CLPLACE and for a duration set by CLDUR. Clamping is started CLPLACE pixel periods after the trailing edge of HSYNC. CLPLACE may be programmed to any value between 1 and 255. CLPLACE = 0 is not supported.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between HSYNC and the image. A value of 08h will usually work.

When EXTCLMP = 1, this register is ignored.

The power-up default value is CLPLACE = 80h.

09	7–0	CLDUR	Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp.

When EXTCLMP = 0, a clamp signal is generated internally, at a position established by CLPLACE and for a duration set by CLDUR. Clamping is started CLPLACE pixel periods after the trailing edge of HSYNC, and continues for CLDUR pixel periods. CLDUR may be programmed to any value between 1 and 255. CLDUR = 0 is not supported.

For the best results, the clamp duration should be set to include the majority of the black reference signal time found following the HSYNC signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the Average Picture Level (APL), or brightness. A value of 10h to 20h works with most standard signals.

When EXTCLMP = 1, this register is ignored.

The power-up default value is CLDUR = 80h.

GENERAL CONTROL

0A	7	DEMUX	Output Port Select

A bit that determines whether all pixels are presented to a single port (A), or alternating pixels are demultiplexed to Ports A and B.

DEMUX	Function
0	All Data Goes to Port A
1	Alternate Pixels Go to Port A and Port B

When DEMUX = 0, Port B outputs are in a high impedance state.

The power-up default value is DEMUX = 1.

0A	6	PARALLEL	Output Timing Select

Setting this bit to a Logic 1 delays data on Port A and the DATACK output by one-half DATACK period so that the rising edge of DATACK may be used to externally latch data from both Port A and Port B. When this bit is set to a Logic 0, the rising edge of DATACK may be used to externally latch data from Port A only, and the $\overline{\text{DATACK}}$ rising edge may be used to externally latch data from Port B.

PARALLEL	Function
0	Data Alternates Between Ports
1	Simultaneous Data on Alternate DATACKs

When in single port mode (DEMUX = 0), this bit is ignored.

The power-up default value is PARALLEL = 1.

0A	5	HSPOL	HSYNC Polarity

A bit that must be set to indicate the polarity of the HSYNC signal that is applied to the HSYNC input.

HSPOL	Function
0	Active LOW
1	Active HIGH

Active LOW is the traditional negative-going HSYNC pulse. Sampling timing is based on the leading edge of HSYNC, which is the FALLING edge. The Clamp Position, as determined by CLPLACE, is measured from the trailing edge.

Active HIGH is inverted from the traditional HSYNC, with a positive-going pulse. This means that sampling timing will be based on the leading edge of HSYNC, which is now the RISING edge, and clamp placement will count from the FALLING edge.

The device will operate more-or-less properly if this bit is set incorrectly, but the internally generated clamp position, as established by CLPOS, will not be placed as expected, which may generate clamping errors.

The power-up default value is HSPOL = 1.

0A	4	CSTPOL	COAST Polarity

A bit that must be set to indicate the polarity of the COAST signal that is applied to the COAST input.

CSTPOL	Function
0	Active LOW
1	Active HIGH

Active LOW means that the clock generator will ignore HSYNC inputs when COAST is LOW, and continue operating at the same nominal frequency until COAST goes HIGH.

Active HIGH means that the clock generator will ignore HSYNC inputs when COAST is HIGH, and continue operating at the same nominal frequency until COAST goes LOW.

The power-up default value is CSTPOL = 1.

0A	3	EXTCLMP	Clamp Signal Source

A bit that determines the source of clamp timing.

EXTCLMP	Function
0	Internally-generated clamp
1	Externally-provided clamp signal

A 0 enables the clamp timing circuitry controlled by CLPLACE and CLDUR. The clamp position and duration is counted from the trailing edge of HSYNC.

A 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the CLAMPOL bit.

The power-up default value is EXTCLMP = 0.

0A	2	CLAMPOL	Clamp Signal Polarity

A bit that determines the polarity of the externally provided CLAMP signal.

CLAMPOL	Function
0	Active LOW
1	Active HIGH

A 0 means that the circuit will clamp when CLAMP is LOW, and it will pass the signal to the ADC when CLAMP is HIGH.

A 1 means that the circuit will clamp when CLAMP is HIGH, and it will pass the signal to the ADC when CLAMP is LOW.

The power-up default value is CLAMPOL = 1.

0A	1	EXTCLK	External Clock Select

A bit that determines the source of the pixel clock.

EXTCLK	Function
0	Internally generated clock
1	Externally provided clock signal

A 0 enables the internal PLL that generates the pixel clock from an externally-provided HSYNC.

A 1 enables the external CKEXT input pin. In this mode, the PLL Divide Ratio (PLLDIV) is ignored. The clock phase adjust (PHASE) is still functional.

The power-up default value is EXTCLK = 0.

CLOCK GENERATOR CONTROL

0B	7–3	PHASE	Clock Phase Adjust

A five-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25 degree shift in sampling phase.

The power-up default value is PHASE = 16.

0C	6–5	VCORNGE	VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE	Range (MHz)
00	20-60
01	50-90
10	80-120
11	110-140

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The power-up default value is VCORNGE = 01.

0C	4–2	CURRENT	Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

CURRENT	Current (μA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

CURRENT must be set to correspond with the desired operating frequency (incoming pixel rate).

The power-up default value is CURRENT = 001.

0D	4	OUTPHASE	Output Port Phase

One bit that determines whether even pixels or odd pixels go to Port A.

OUTPHASE	First Pixel After HSYNC
0	Port A
1	Port B

In normal operation (OUTPHASE = 0), when operating in Dual Channel output mode (DEMUX = 1), the first sample after the HSYNC leading edge is presented at Port A. Every subsequent ODD sample appears at Port A. All EVEN samples go to Port B.

When OUTPHASE = 1, these ports are reversed and the first sample goes to Port B.

When DEMUX = 0, this bit is ignored.

When reading back the value of OUTPHASE, the bit appears at register 0D, Bit 7.

0D	3–1	REVID	Silicon Revision ID

The die revision of the AD9884A can be determined by reading these three bits.

Serial Control Port

A 2-wire serial control interface is provided. Up to four AD9884A devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The Analog Flat Panel Interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is LOW. If SDA changes state while SCL is HIGH, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte to Read or Write
- Stop Signal

When the serial interface is inactive (SCL and SDA are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprising a seven bit slave address (the first seven bits) and a single R/$\overline{W}$ bit (the eighth bit). The R/$\overline{W}$ bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{1-0} input pins in *Table IV*), the AD9884A acknowledges by bringing SDA LOW on the ninth SCL pulse. If the addresses do not match, the AD9884A does not acknowledge.

Table IV. Serial Port Addresses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A_6 (MSB)	A_5	A_4	A_3	A_2	A_1	A_0 (LSB)	R/$\overline{W}$
1	0	0	1	1	0	0	
1	0	0	1	1	0	1	
1	0	0	1	1	1	0	
1	0	0	1	1	1	1	

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9884A does not acknowledge the master device during a write sequence, the SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the AD9884A during a read sequence, the AD9884A interprets this as "end of data." The SDA remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the AD9884A requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 0Eh. Any base address higher than 0Eh will not produce an ACKnowledge signal.

Data are read from the control registers of the AD9884A in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/$\overline{W}$ bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/$\overline{W}$ bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9884A, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to One Control Register

- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Stop Signal

Write to Four Consecutive Control Registers

- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- Data Byte to (Base Address + 3)
- Stop Signal

Read from One Control Register

- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = HIGH)
- Data Byte from Base Address
- Stop Signal

Read from Four Consecutive Control Registers

- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = HIGH)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- Data Byte from (Base Address + 3)
- Stop Signal

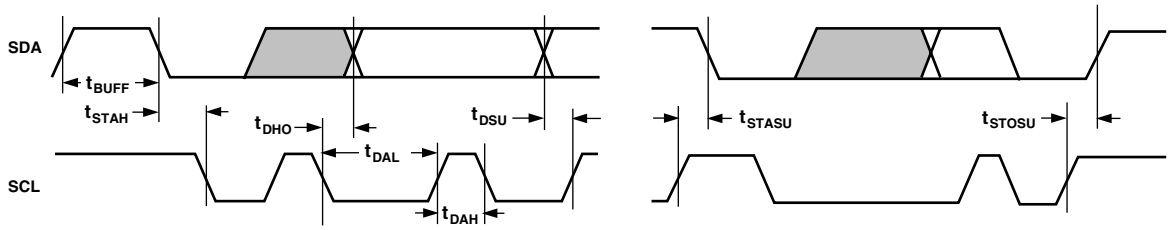


Figure 1. Serial Port Read/Write Timing

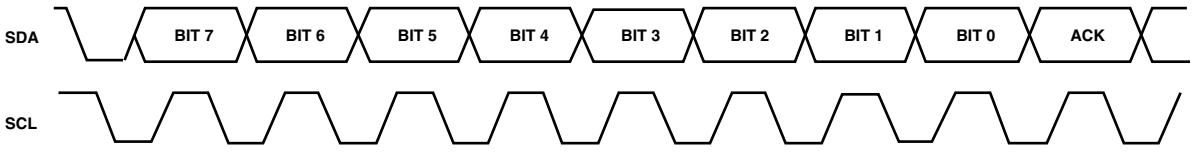


Figure 2. Serial Interface—Typical Byte Transfer

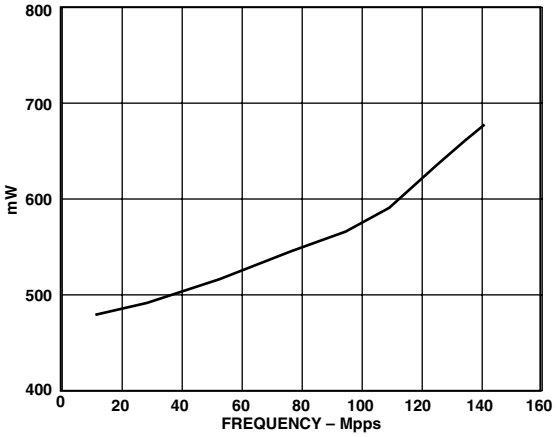


Figure 3. Power Dissipation vs. Frequency

DESIGN GUIDE

GENERAL DESCRIPTION

The AD9884A is a fully-integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is also ideal for providing a computer interface for HDTV monitors or as the front-end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 140 MegaPixels Per Second (Mpps), and with an Alternate Pixel Sampling mode, up to 280 Mpps.

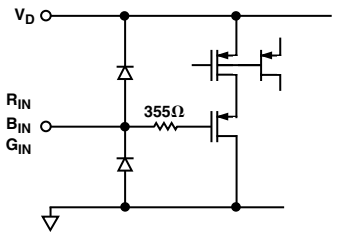


Figure 4. Equivalent Analog Input Circuit

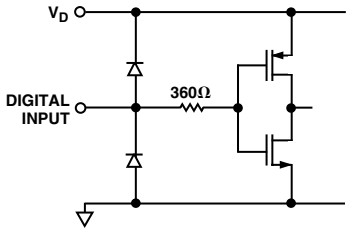


Figure 5. Equivalent Digital Input Circuit

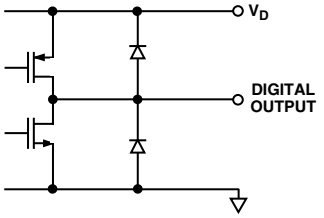


Figure 6. Equivalent Digital Output Circuit

The AD9884A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 570 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

INPUT SIGNAL HANDLING

Analog Inputs

The AD9884A has three high impedance analog input pins for the red, green, and blue channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a 15-pin D connector, a VESA P&D connector, a DDWG DVI connector, or via BNC connectors. The AD9884A should be located as close as practical to the input connector. Signals should be routed via matched- impedance traces (normally 75 Ω) to the IC input pins.

At that point the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9884A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The ultrawide bandwidth inputs of the AD9884A (500 MHz) can track the input signal continuously as it moves from one pixel level to the next, and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly, and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 High-Speed Signal Chip Bead inductor in the circuit of Figure 7 gives good results in most applications.

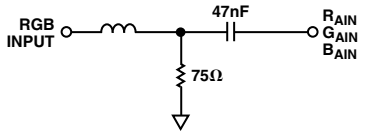


Figure 7. Analog Input Interface Circuit

HSYNC, VSYNC Inputs

The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. It is possible to operate the AD9884A without applying HSYNC (using an external clock, external clamp, and single port output mode) but a number of features of the chip will be unavailable, so it is recommended that HSYNC be provided. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal. The HSYNC input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times.

In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. Since the AD9884A operates from a 3.3 V power supply, and TTL sources may drive a high level to 5 V or more, it is recommended that a 1 kΩ series current-limiting resistor be placed in series with HSYNC and COAST. If these pins are driven more than 0.5 V outside the power supply voltages, internal ESD protection diodes will conduct, and may dissipate considerable power if the sync source is of particularly low impedance. If a signal is applied to the AD9884A when the IC's power is off, then even a 1 V signal can turn on the ESD protection diodes. The 1 kΩ series resistor will protect the device from overstress in this situation as well.

Serial Control Port

The serial control port (SDA, SCL) is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150 Ω series resistors.

OUTPUT SIGNAL HANDLING

The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5 V for compatibility with other 2.5 V logic.

CLAMPING

To properly digitize the incoming signal, the dc offset of the input signal must be adjusted to fit the range of the on-board A/D converters.

Most graphic systems produce RGB signals with black at ground and white at approximately +0.75 V. However, if sync signals are embedded in the graphics, then the sync tip is often at ground potential, and black is at +300 mV. Then white is at approximately +1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal which must be removed for proper capture by the AD9884A.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the A/D converters producing a black output (code 00h) when the known black input is present. That offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most graphic systems, black is transmitted between active video lines. Going back to CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (HSYNC) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of HSYNC. Fortunately, there is virtually always a period following HSYNC called the back porch where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with EXTCLMP = 1). The polarity of this signal is set by the CLAMPOL bit.

A simpler method of clamp timing employs the AD9884A internal clamp timing generator. Register CLPLACE is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (CLDUR) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of HSYNC because, though HSYNC duration can vary widely, the back porch (black reference) always follows HSYNC. A good starting point for establishing clamping is to set CLPLACE to 08h (providing 8 pixel periods for the graphics signal to stabilize after sync) and set CLDUR to 14h (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp circuit to recover from a large change in incoming signal offset. The recommended value results in recovering from a step error of 100 mV to within 1/2 LSB in 10 lines with a clamp duration of 20 pixels on a 60 Hz SXGA signal.

GAIN AND OFFSET CONTROL

The AD9884A can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (REDGAIN, GRNGAIN, BLUGAIN).

A code of 0 in a gain register establishes a minimum input range of 0.5 V; 255 corresponds with the maximum range of 1.0 V. Note that INCREASING the gain setting results in an image with LESS contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 6-bit registers (REDOFST, GRNOFST, BLUOFST) provide independent settings for each channel.

The offset controls provide a ±31 LSB adjustment range. This range is connected with the full-scale range, so if the input range is doubled (from 0.5 V to 1.0 V) then the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 8 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale *range* is not affected, but the full-scale *level* is shifted by the same amount as the zero scale level.

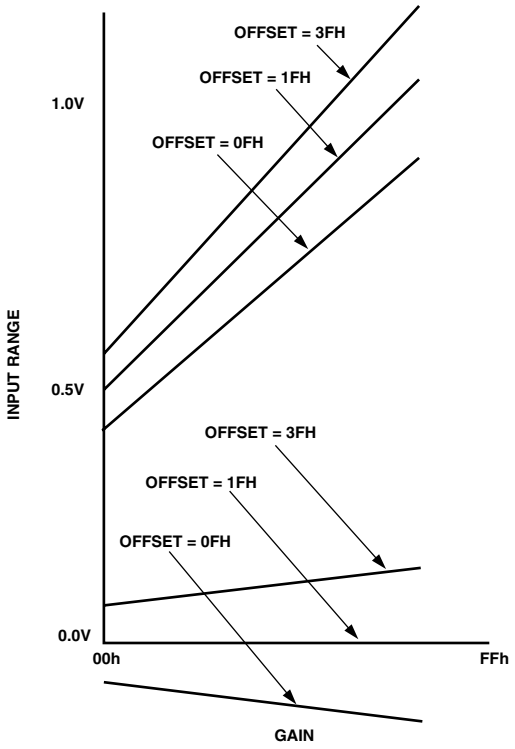


Figure 8. Gain and Offset Control

CLOCK GENERATION

A Phase Locked Loop (PLL) is employed to generate the pixel clock. In this PLL, the HSYNC input provides a reference frequency. A Voltage Controlled Oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the value PLLDIV programmed into the AD9884A, and phase compared with the HSYNC input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 9). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

Any jitter in the pixel clock reduces the precision with which the sampling time can be determined, and must also be subtracted from the stable pixel time.

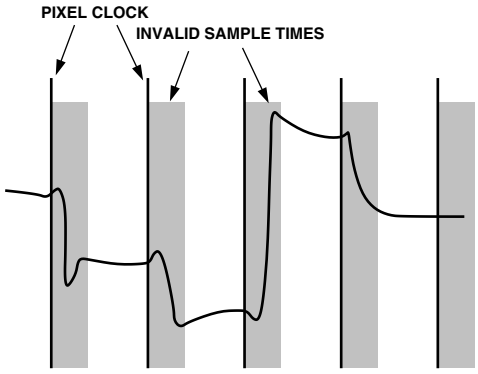


Figure 9. Pixel Sampling Times

Considerable care has been taken in the design of the AD9884A's clock generation circuit to minimize jitter. As indicated in Figure 11 and Table VI, the clock jitter of the AD9884A is less than 5% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

The PLL characteristics are determined by the loop filter design, by the PLL Charge Pump Current (CURRENT), and by the VCO Range setting (VCORNGE). The loop filter design is illustrated in Figure 10. Recommended settings of VCORNGE and CURRENT for VESA standard display modes are listed in Table VII.

Table V. Typical K_{VCO} Derived From VCORNGE

Pixel Rate (MHz)	VCORNGE	K_{VCO} (MHz/V)
20–60	00	100
50–90	01	100
80–120	10	150
110–140	11	180

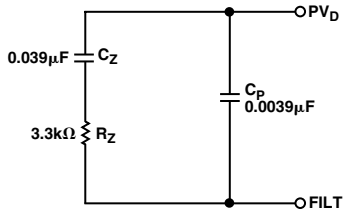


Figure 10. PLL Loop Filter Detail

Table VI. Pixel Clock Jitter vs Frequency

Pixel Rate (MSPS)	Jitter p-p (ps)	Jitter p-p (% of Pixel Time)
135	350	4.7%
108	400	4.3%
94	400	3.4%
75	450	3.4%
65	600	3.9%
50	500*	2.4%
40	500*	2.0%
36	550*	1.8%
25	1000*	2.5%

*AD9884A in oversampled mode.

Table VII. Recommended VCORNGE and CURRENT Settings for Standard Display Formats

Standard	Resolution	Refresh Rate	Horizontal Frequency	Pixel Rate	VCORNGE	CURRENT
VGA	640 × 480	60 Hz	31.5 kHz	25.175 MHz	00	000
		72 Hz	37.7 kHz	31.500 MHz	00	000
		75 Hz	37.5 kHz	31.500 MHz	00	000
		85 Hz	43.3 kHz	36.000 MHz	00	001
SVGA	800 × 600	56 Hz	35.1 kHz	36.000 MHz	00	001
		60 Hz	37.9 kHz	40.000 MHz	00	001
		72 Hz	48.1 kHz	50.000 MHz	00	010
		75 Hz	46.9 kHz	49.500 MHz	00	001
		85 Hz	53.7 kHz	56.250 MHz	01	010
XGA	1024 × 768	60 Hz	48.4 kHz	65.000 MHz	01	010
		70 Hz	56.5 kHz	75.000 MHz	01	011
		75 Hz	60.0 kHz	78.750 MHz	01	011
		80 Hz	64.0 kHz	85.500 MHz	10	011
		85 Hz	68.3 kHz	94.500 MHz	10	011
SXGA	1280 × 1024	60 Hz	64.0 kHz	108.000 MHz	10	011
		75 Hz	80.0 kHz	135.000 MHz	11	100
		85 Hz	91.1 kHz	157.500 MHz*	01	100
UXGA	1600 × 1200	60 Hz	75.0 kHz	162.000 MHz*	01	100
		65 Hz	81.3 kHz	175.500 MHz*	10	100
		70 Hz	87.5 kHz	189.000 MHz*	10	101
		75 Hz	93.8 kHz	202.500 MHz*	10	101
		85 Hz	106.3 kHz	229.500 MHz*	10	110

VESA Monitor Timing Standards and Guidelines, September 17, 1998
*Graphics sampled at 1/2 incoming pixel rate using Alternate Pixel Sampling mode.

Figure 11 illustrates the AD9884A's jitter as a percentage of the total clock period over the range of operating frequencies. Though the jitter is very low over most of the range (less than 5% of the pixel period), the jitter increases at clock rates below 40 MHz. At lower frequencies, the jitter can be reduced by operating the AD9884A at twice the desired frequency, and using only every other data sample produced. This can be easily implemented by placing the part in Dual Channel mode (for example, as in Figure 21), and reading the data from only one of the output ports. The DATACK and $\overline{\text{DATACK}}$ outputs will run at the desired, lower, sample rate.

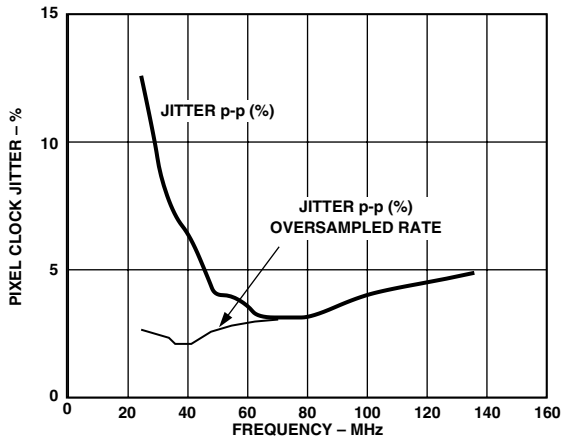


Figure 11. Pixel Clock Jitter vs. Frequency

TIMING

The following timing diagrams show the operation of the AD9884A in all clock modes. The part establishes timing by having the sample that corresponds to the pixel digitized when the leading edge of HSYNC occurs sent to the "A" data port (to the B data port if 0Dh, Bit 4 = 1). In Dual Channel mode, the next sample is sent to the "B" port (to the A data port if 0Dh, Bit 4 = 1). Subsequent samples are alternated between the "A" and "B" data ports. In Single Channel mode, data is only sent to the "A" data port, and the "B" port is placed in a high impedance state.

When operating in Dual Channel mode, since the first pixel after HSYNC is always sent to the A port, there are situations where the first DESIRED pixel (the first active pixel of a line) may appear on the B port. If the graphics controller or memory buffer requires that the first pixel appear on the A port, the OUTPHASE control bit will swap the data to the A and B ports.

The Output Data Clock signal is created so that its rising edge always occurs between "A" data transitions, and can be used to latch the output data externally. The HSYNC output is pipelined with the data in a fixed timing relationship between the two in all Single Channel modes.

There is a pipeline in the AD9884A, which must be flushed before valid data becomes available. In all single channel modes, four data sets are presented before valid data is available. In all dual channel modes, two data sets are presented before valid "A" port data is available.

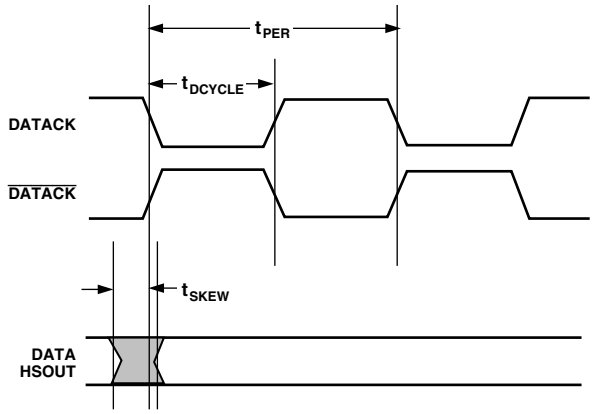


Figure 12. Output Timing

Horizontal Sync Timing

Horizontal Sync is processed in the AD9884A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The HSYNC input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to HSYNC, through a full 360° in 32 steps via the PHASE register (to optimize the pixel sampling time). Display systems use HSYNC to align memory and display write cycles, so it is important to have a stable timing relationship between HSOUT and DATACK.

Two things happen to Horizontal Sync in the AD9884A. First, HSOUT is always produced in an active HIGH state: that is, the leading edge of HSOUT is always a RISING edge. Then, HSOUT is aligned with DATACK and the data outputs. This is the sync signal that should be used to drive the rest of the display system.

The trailing edge of HSOUT is NOT time-aligned: it remains linked to the incoming HSYNC. Refer to the timing diagrams for HSOUT leading edge placement. HSOUT trailing edge is coincident with HSYNC input trailing edge. There can be no guarantee of the timing relationship between the HSOUT trailing edge and DATACK. Therefore, the leading edge of HSOUT should be used for all display system timing.

HSOUT is forced LOW at midline, whether or not the incoming HSYNC trailing edge has arrived. If HSOUT exhibits a 50% duty cycle (while HSYNC input does not) it is an indication that the HSPOL bit is incorrectly set. This characteristic can be used to produce an HSOUT with synchronous leading and trailing edges by programming HSPOL to use the trailing edge of HSYNC instead of the leading edge. In this case, if the internal clamp function is used, be aware that the clamp position is now measured from the LEADING edge of HSYNC, and program it accordingly.

COAST Timing

In most computer systems, the HSYNC signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary, and should not be used.

In some systems, however, HSYNC is disturbed during the Vertical Sync period (VSYNC). In some cases, HSYNC pulses disappear. In other systems, such as those that employ Composite Sync (CSYNC) signals or embed Sync On Green (SOG), HSYNC includes equalization pulses or other distortions during VSYNC. To avoid upsetting the clock generator during VSYNC, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency, and will have changed frequency by the end of the VSYNC period. It then will take a few lines of correct HSYNC timing to recover at the beginning of a new frame, resulting in a "tearing" of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

COAST can be driven directly from a VSYNC input, or it can be provided by the graphics controller.

ALTERNATE PIXEL SAMPLING MODE

A Logic 1 input on CKINV (Pin 27) shifts the sampling phase 180 degrees. CKINV can be switched between frames to implement the alternate pixel sampling mode. This allows higher effective image resolution to be achieved at lower pixel rates, but with lower frame rates.

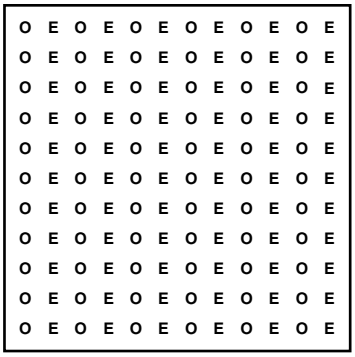


Figure 13. Odd and Even Pixels in a Frame

On one frame, only even pixels are digitized. On the subsequent frame, odd pixels are sampled. By reconstructing the entire frame in the graphics controller, a complete image can be reconstructed. This is very similar to the interlacing process that is employed in broadcast television systems, but the interlacing is vertical instead of horizontal. The frame data is still presented to the display at the full desired refresh rate (usually 60 Hz) so there are no flicker artifacts added.

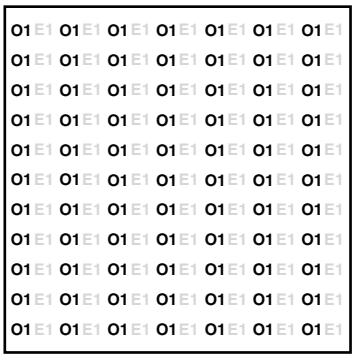


Figure 14. Odd Pixels from Frame 1

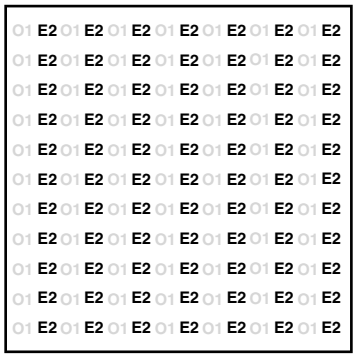


Figure 15. Even Pixels from Frame 2

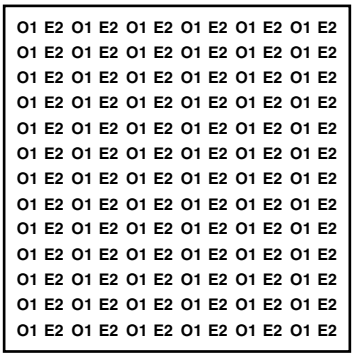


Figure 16. Combined Frame Output from Graphics Controller

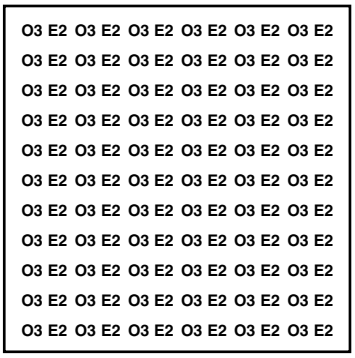


Figure 17. Subsequent Frame from Controller

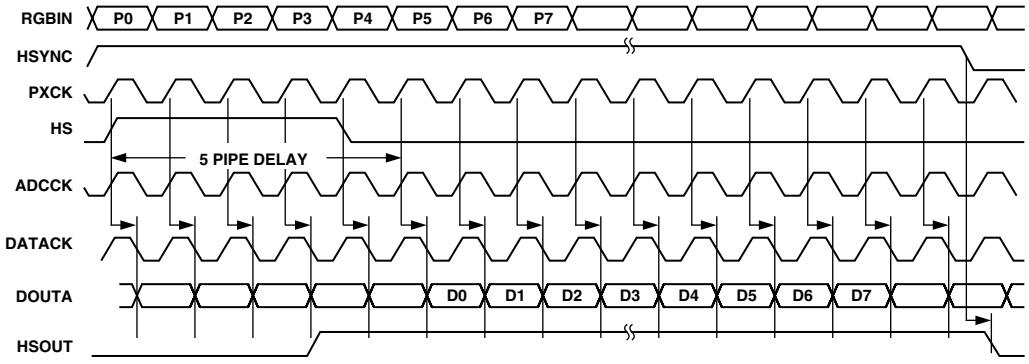


Figure 18. Single Channel Mode

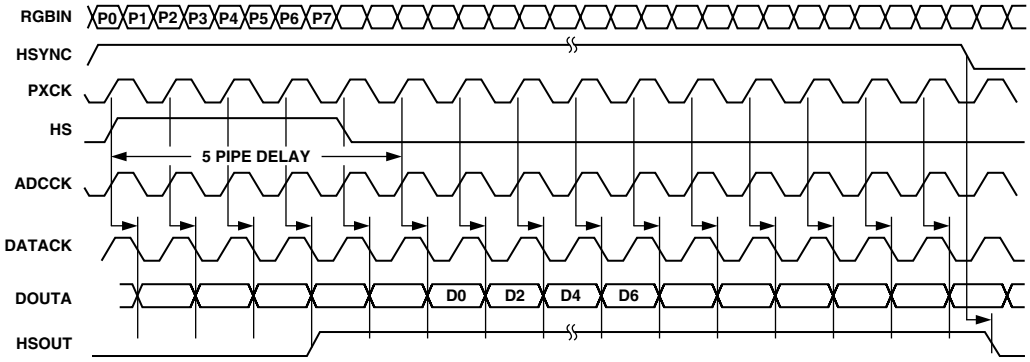


Figure 19. Single Channel Mode, Alternate Pixel Sampling (Even Pixels)

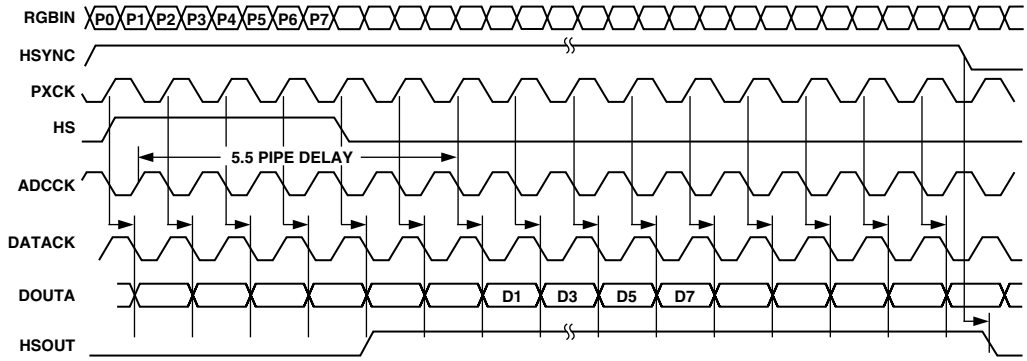


Figure 20. Single Channel Mode, Alternate Pixel Sampling (Odd Pixels)

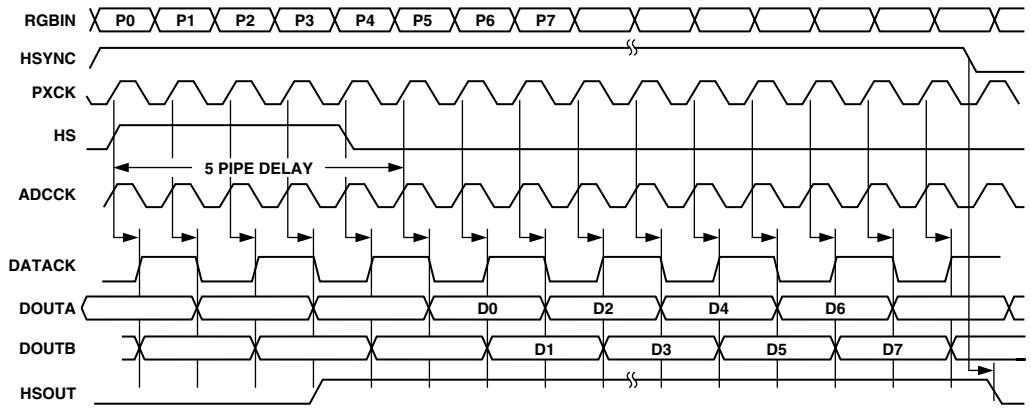


Figure 21. Dual Channel Mode, Interleaved Outputs

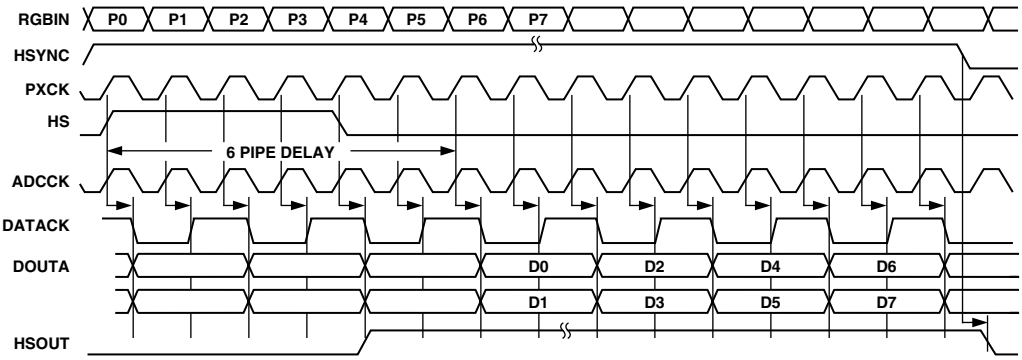


Figure 22. Dual Channel Mode, Parallel Outputs

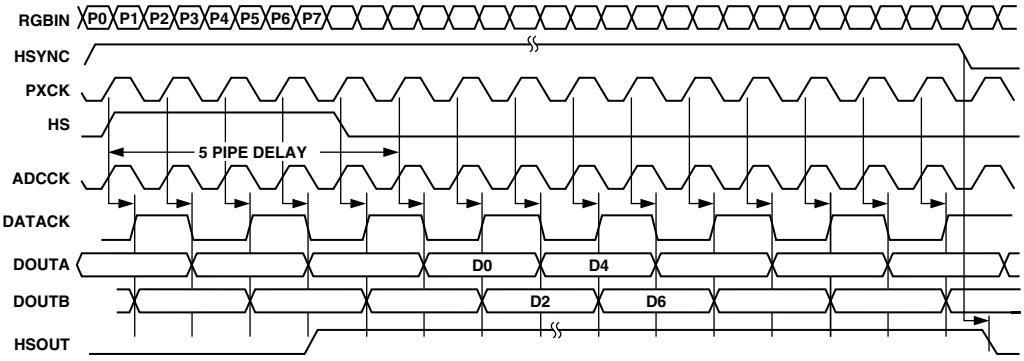


Figure 23. Dual Channel Mode, Interleaved Outputs, Alternate Pixel Sampling (Even Pixels)

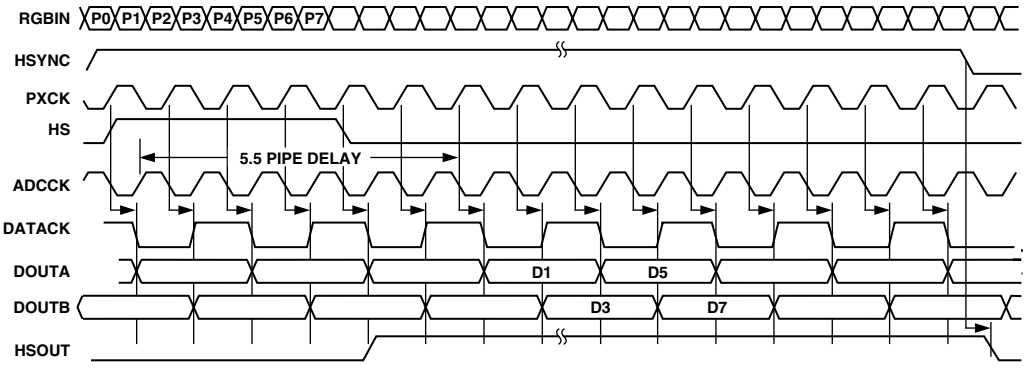


Figure 24. Dual Channel Mode, Interleaved Outputs, Alternate Pixel Sampling (Odd Pixels)

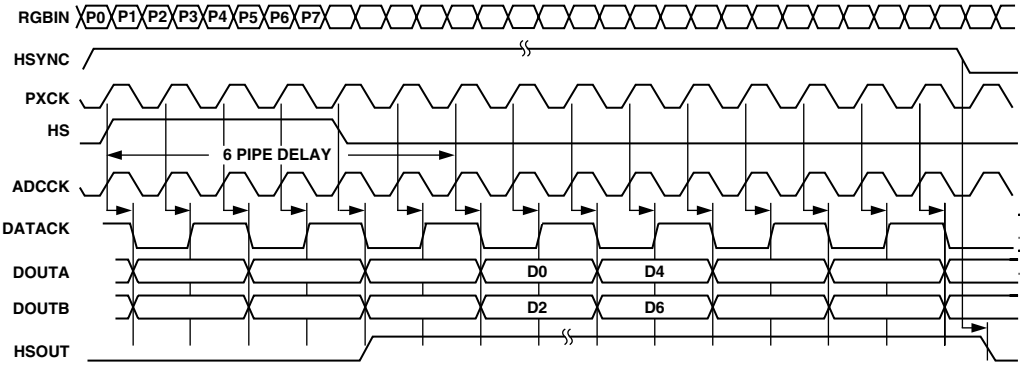


Figure 25. Dual Channel Mode, Parallel Outputs, Alternate Pixel Sampling (Even Pixels)

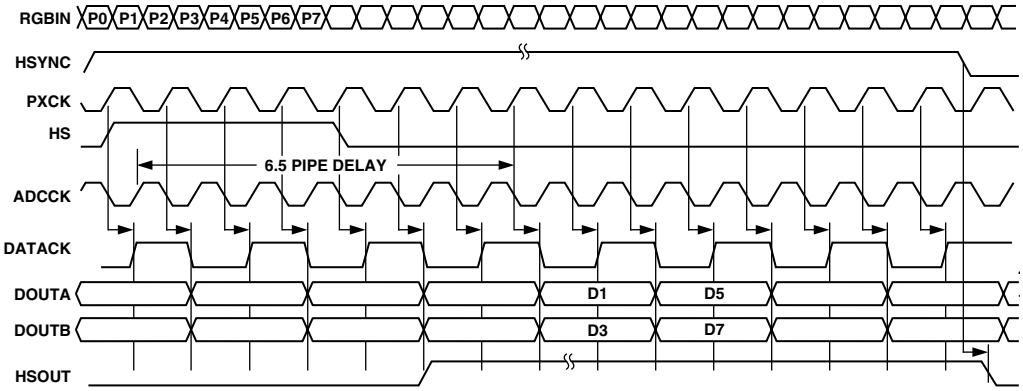


Figure 26. Dual Channel Mode, Parallel Outputs, Alternate Pixel Sampling (Odd Pixels)

PCB LAYOUT RECOMMENDATIONS

The AD9884A is a high precision, high speed analog device. As such, to get the maximum performance out of the part it is important to have a well laid-out board.

Inputs

Using the following layout techniques on the graphics inputs is extremely important:

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9884A as close as possible to the input connector. Long input trace lengths are undesirable because they will pick up more noise from the board and other external sources.

Place the 75 Ω termination resistors as close to the AD9884A as possible. Any additional trace length between the termination resistors and the input of the AD9884A increases the magnitude of reflections, which will corrupt the graphics signal.

Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω will also increase the magnitude of reflections.

The AD9884A has very high input bandwidth (500 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it will also capture any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9884A, sometimes low-pass filtering the analog inputs can help to reduce noise. (For many applications, filtering is unnecessary.) Our experiments have shown that placing a series ferrite bead prior to the 75 Ω termination resistor is helpful in filtering out excess noise. Specifically, we used the Part #2508051217Z0 from Fair-Rite, but each application may work best with a different bead value.

Power Supply Bypassing

We recommend you bypass each power supply pin with a 0.1 µF capacitor. The exception is in the case where two or more supply pins are adjacent. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9884A, as that interposes resistive vias in the path.

The bypass capacitors should be connected between the power plane and the power pin. Current should flow from the power plane → capacitor → power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide a separately regulated supply for the analog circuitry (V_D and P_{VD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during Horizontal and Vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog voltage. This can be mitigated by regulating the analog supply, or at least P_{VD}, from a different, cleaner, power source (for example, from a 12 V supply).

We also recommend that you use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is better, or at least the same, with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, we recommend to at least place a single ground plane under the AD9884A. The location of the split should be at the receiver of the digital outputs. For this case it is even more important to place components wisely because the current loops will be much longer, (current takes the path of least resistance). An example of a current loop:

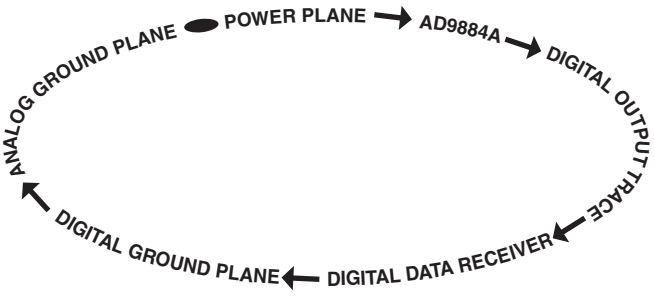


Figure 27. Current Loop

PLL
Place the PLL loop filter components as close to the AD9884A pins as possible.

Do not place any digital or other high frequency traces near these components.

Use the values suggested in the data sheet with 5% tolerance or less.

Outputs (Both Data and Clocks)
Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which requires more current, which causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 50 Ω–200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9884A. If series resistors are used, place them as close to the AD9884A pins as possible, (although try not to add vias or extra length to the output trace in order to get the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance will increase the current transients inside of the AD9884A, and create more digital noise on its power supplies.

Digital Inputs
The digital inputs on the AD9884A were designed to work with 3.3 V signals. Connecting 5 V digital signals to the part may cause damage. To accommodate 5 V digital signals, we recommend adding a series resistor at the AD9884A pin of 1 kΩ. The only exception is the two serial interface pins, SDA and SCL. On these two pins, a resistor value of 150 Ω should be used and it should be placed between the AD9884A pin and the pull-up resistors.

Any noise that gets onto the HSYNC input trace will add jitter to the system, so, try to minimize the trace length and try not to run any digital or other high frequency traces near it.

Voltage Reference
Bypass with a 0.1 µF capacitor. Place it as close to the AD9884A pin as possible. Make the ground connection as short as possible.

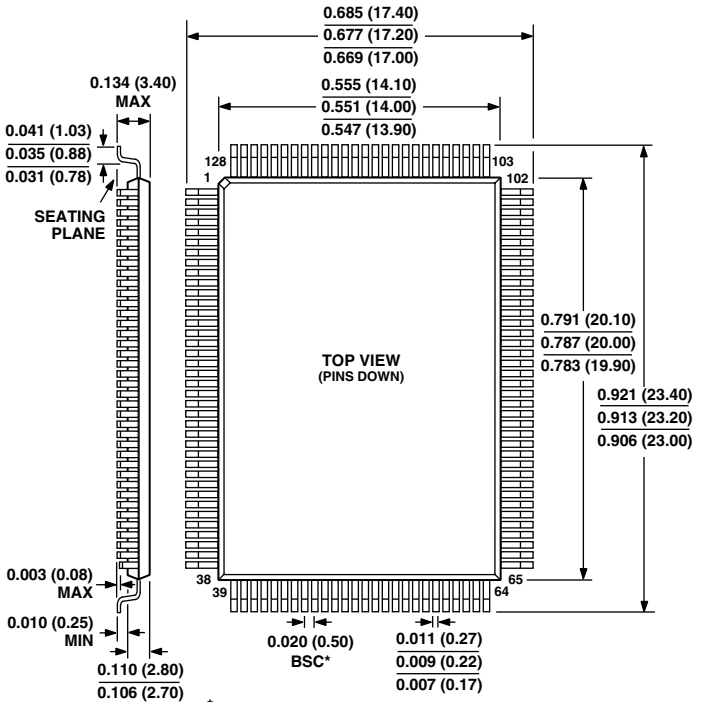
REFOUT is easily connected to REFIN with a short trace. Avoid making this trace any longer than it needs to be.

When using an external reference, the REFOUT output, while unused, still needs to be bypassed to ground with a 0.1 µF capacitor to avoid ringing.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

128-Lead Plastic Quad Flatpack (MQFP)
(S-128)



* THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.00315 (0.08) FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.
CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
THE CONTROLLING DIMENSIONS ARE IN MM.

C00639a–0–10/01(C)

Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Edit to ABSOLUTE MAXIMUM RATINGS	3

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