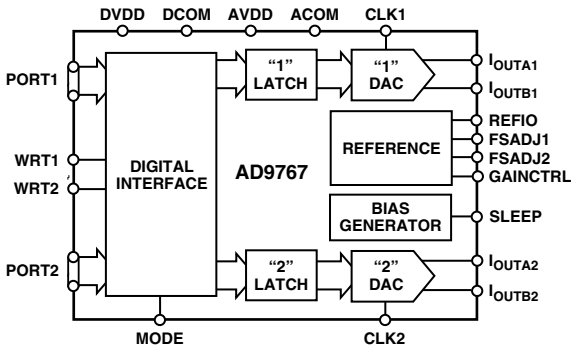
14-Bit, 125 MSPS Dual TxDAC+® D/A Converter

AD9767*

FEATURES
14-Bit Dual Transmit DAC
125 MSPS Update Rate
Excellent SFDR and IMD: 82 dBc
Excellent Gain and Offset Matching: 0.1%
Fully Independent or Single Resistor Gain Control
Dual Port or Interleaved Data
On-Chip 1.2 V Reference
Single 5 V or 3 V Supply Operation
Power Dissipation: 380 mW @ 5 V
Power-Down Mode: 50 mW @ 5 V
48-Lead LQFP

APPLICATIONS
Communications
Base Stations
Digital Synthesis
Quadrature Modulation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9767 is a dual port, high speed, two channel, 14-bit CMOS DAC. It integrates two high quality 14-bit TxDAC+ cores, a voltage reference and digital interface circuitry into a small 48-lead LQFP package. The AD9767 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9767 has been optimized for processing I and Q data in communications applications. The digital interface consists of two double-buffered latches as well as control logic. Separate write inputs allow data to be written to the two DAC ports independent of one another. Separate clocks control the update rate of the DACs.

A mode control pin allows the AD9767 to interface to two separate data ports, or to a single interleaved high speed data port. In interleaving mode the input data stream is demuxed into its original I and Q data and then latched. The I and Q data is then converted by the two DACs and updated at half the input data rate.

The GAINCTRL pin allows two modes for setting the full-scale current (I_{OUTFS}) of the two DACs. I_{OUTFS} for each DAC can be set independently using two external resistors, or I_{OUTFS} for both DACs can be set by using a single external resistor.**

The DACs utilize a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and to maximize dynamic accuracy. Each DAC provides differential current output thus supporting single-ended or differential applications. Both DACs can be simultaneously updated and provide a nominal full-scale current of 20 mA. The full-scale currents between each DAC are matched to within 0.1%.

The AD9767 is manufactured on an advanced low cost CMOS process. It operates from a single supply of 3.0 V to 5.0 V and consumes 380 mW of power.

PRODUCT HIGHLIGHTS

1. The AD9767 is a member of a pin-compatible family of dual TxDACs providing 8-, 10-, 12- and 14-bit resolution.
2. Dual 14-Bit, 125 MSPS DACs: A pair of high performance DACs optimized for low distortion performance provide for flexible transmission of I and Q information.
3. Matching: Gain matching is typically 0.1% of full scale, and offset error is better than 0.02%.
4. Low Power: Complete CMOS Dual DAC function operates on 380 mW from a 3.0 V to 5.0 V single supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low power idle periods.
5. On-Chip Voltage Reference: The AD9767 includes a 1.20 V temperature-compensated bandgap voltage reference.
6. Dual 14-Bit Inputs: The AD9767 features a flexible dual-port interface allowing dual or interleaved input data.

TxDAC+ is a registered trademark of Analog Devices, Inc.
*Patent pending.
**Please see GAINCTRL Mode section, for important date code information on this feature.

REV. B

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AD9767–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Units
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)				
T_A = +25°C	–3.5	±1.5	+3.5	LSB
T_{MIN} to T_{MAX}	–4.0		+4.0	LSB
Differential Nonlinearity (DNL)				
T_A = +25°C	–2.5	±1.0	+2.5	LSB
T_{MIN} to T_{MAX}	–3.0		+3.0	LSB
ANALOG OUTPUT				
Offset Error	–0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	–2	±0.25	+2	% of FSR
Gain Error (With Internal Reference)	–5	±1	+5	% of FSR
Gain Match	–1.6	0.1	+1.6	% of FSR
	–0.14		+0.14	dB
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	3	5	5.5	V
DVDD	2.7	5	5.5	V
Analog Supply Current (I_{AVDD})		71	75	mA
Digital Supply Current (I_{DVDD})[4]		5	7	mA
Digital Supply Current (I_{DVDD})[5]			15	mA
Supply Current Sleep Mode (I_{AVDD})		8	12	mA
Power Dissipation[4] (5 V, I_{OUTFS} = 20 mA)		380	410	mW
Power Dissipation[5] (5 V, I_{OUTFS} = 20 mA)		420	450	mW
Power Dissipation[6] (5 V, I_{OUTFS} = 20 mA)		450		mW
Power Supply Rejection Ratio[7]—AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio[7]—DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES

[1]Measured at I_{OUTA}, driving a virtual ground.

[2]Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.

[3]An external buffer amplifier with input bias current <100 nA should be used to drive any external load.

[4]Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 1.0 MHz.

[5]Measured at f_{CLOCK} = 100 MSPS and f_{OUT} = 1 MHz.

[6]Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and 50 Ω R_{LOAD} at I_{OUTA} and I_{OUTB}, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.

[7]±10% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	125			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (90% to 10%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 100 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output	71	82		dBc
–6 dBFS Output		77		dBc
–12 dBFS Output		73		dBc
–18 dBFS Output		70		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 1.00 MHz		82		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.51 MHz		80		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 5.02 MHz		79		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 14.02 MHz		70		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 25 MHz		55		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 25 MHz		67		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 40 MHz		70		dBc
Spurious-Free Dynamic Range Within a Window				
f_{CLOCK} = 100 MSPS; f_{OUT} = 1.00 MHz; 2 MHz Span	82	91		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 10 MHz Span		88		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 5.03 MHz; 10 MHz Span		88		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 5.04 MHz; 10 MHz Span		88		dBc
Total Harmonic Distortion				
f_{CLOCK} = 100 MSPS; f_{OUT} = 1.00 MHz		–81	–71	dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.00 MHz		–79		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 4.00 MHz		–83		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 10.00 MHz		–80		dBc
Multitone Power Ratio (Eight Tones at 110 kHz Spacing)				
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.00 MHz to 2.99 MHz				
0 dBFS Output		80		dBc
–6 dBFS Output		79		dBc
–12 dBFS Output		78		dBc
–18 dBFS Output		76		dBc
Channel Isolation				
f_{CLOCK} = 125 MSPS; f_{OUT} = 10 MHz		85		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 40 MHz		77		dBc

NOTES

[1]Measured single-ended into 50 Ω load.

Specifications subject to change without notice.

AD9767–SPECIFICATIONS

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V	3.5	5		V
Logic "1" @ DVDD = 3	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V		0	1.3	V
Logic "0" @ DVDD = 3	0		0.9	V
Logic "1" Current	–10		+10	μA
Logic "0" Current	–10		+10	μA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW}, t_{CPW})	3.5			ns

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+6.5	V
DVDD	DCOM	–0.3	+6.5	V
ACOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
MODE, CLK1, CLK2, WRT1, WRT2	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
I_{OUTA1}/I_{OUTA2}, I_{OUTB1}/I_{OUTB2}	ACOM	–1.0	AVDD + 0.3	V
REFIO, FSADJ1, FSADJ2	ACOM	–0.3	AVDD + 0.3	V
GAINCTRL, SLEEP	ACOM	–0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9767AST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9767-EB		Evaluation Board	

*ST = Thin Plastic Quad Flatpack.

THERMAL CHARACTERISTICS

Thermal Resistance

48-Lead LQFP

θ_{JA} = 91°C/W

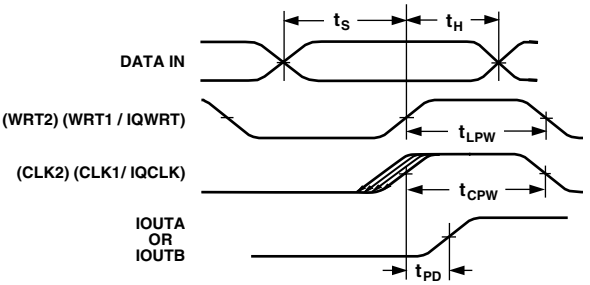


Figure 1. Timing Diagram for Dual and Interleaved Modes

See Dynamic and Digital sections for timing specifications.

CAUTION

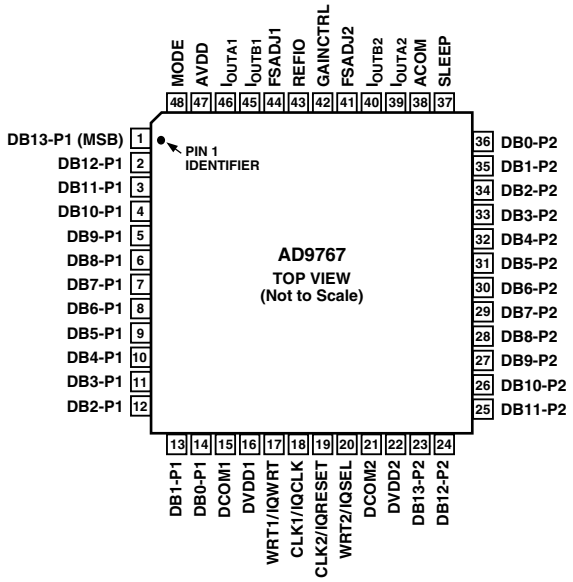
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9767 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1–14	PORT1	Data Bits DB13–P1 to DB0–P1.
15, 21	DCOM1, DCOM2	Digital Common.
16, 22	DVDD1, DVDD2	Digital Supply Voltage.
17	WRT1/IQWRT	Input write signal for PORT 1 (IQWRT in interleaving mode).
18	CLK1/IQCLK	Clock input for DAC1 (IQCLK in interleaving mode).
19	CLK2/IQRESET	Clock input for DAC2 (IQRESET in interleaving mode).
20	WRT2/IQSEL	Input write signal for PORT 2 (IQSEL in interleaving mode).
23–36	PORT2	Data Bits DB13–P2 to DB0–P2.
37	SLEEP	Power-Down Control Input.
38	ACOM	Analog Common.
39, 40	I_{OUTA2}, I_{OUTB2}	"PORT 2" differential DAC current outputs.
41	FSADJ2	Full-scale current output adjust for DAC2.
42	GAINCTRL	GAINCTRL Mode (0 = 2 resistor, 1 = 1 resistor.)
43	REFIO	Reference Input/Output.
44	FSADJ1	Full-scale current output adjust for DAC1.
45, 46	I_{OUTB1}, I_{OUTA1}	"PORT 1" differential DAC current outputs.
47	AVDD	Analog Supply Voltage.
48	MODE	Mode Select (1 = Dual Port, 0 = Interleaved).

PIN CONFIGURATION



DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C (ppm/°C).

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

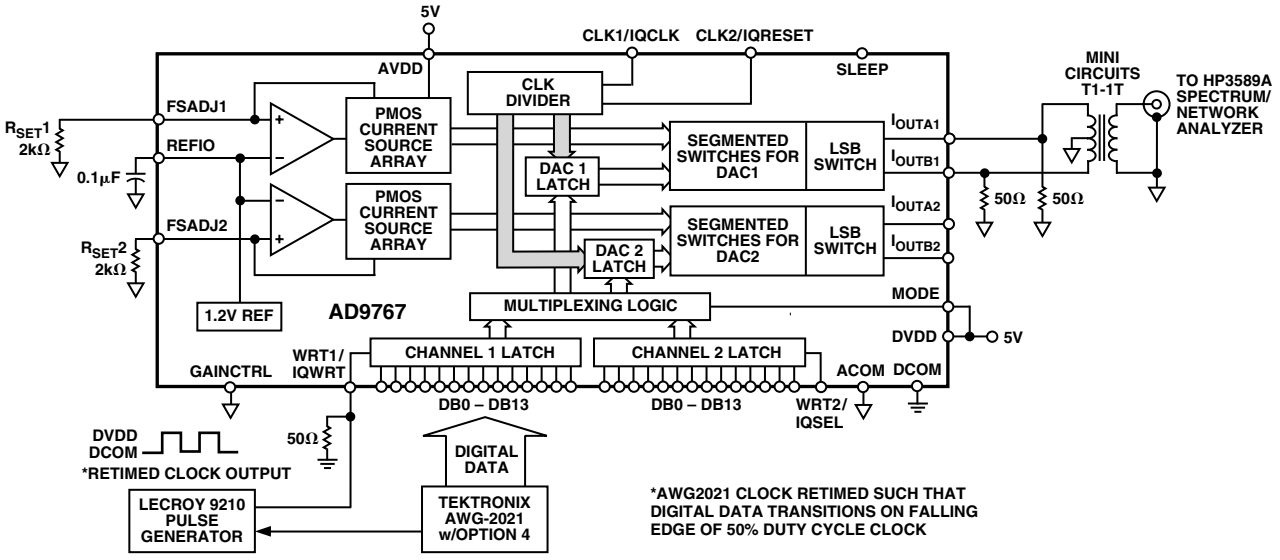


Figure 2. Basic AC Characterization Test Setup for AD9767, Testing Port 1 in Dual Port Mode, Using Independent GAINCTRL Resistors on FSADJ1 and FSADJ2

Typical Characterization Curves

(AVDD = +5 V, DVDD = +3.3 V, I_{OUTFS} = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, T_A = +25°C, SFDR up to Nyquist, unless otherwise noted.)

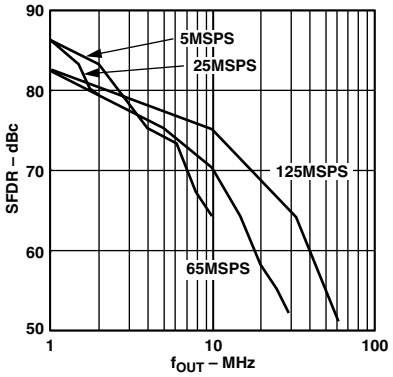


Figure 3. SFDR vs. f_{OUT} @ 0 dBFS

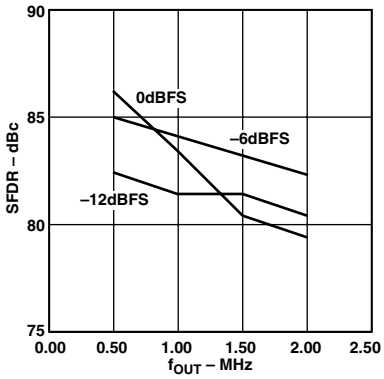


Figure 4. SFDR vs. f_{OUT} @ 5 MSPS

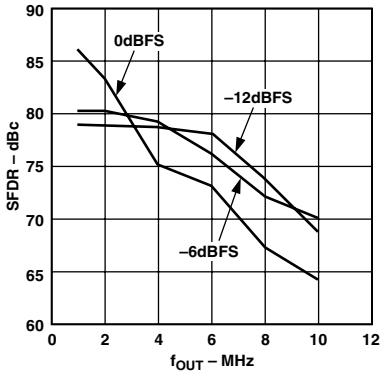


Figure 5. SFDR vs. f_{OUT} @ 25 MSPS

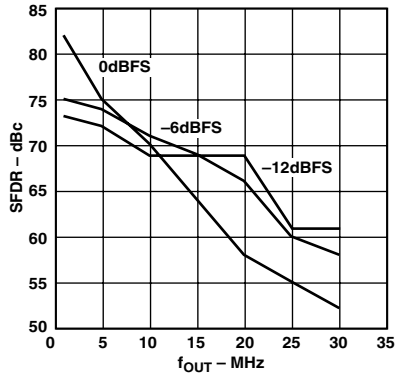


Figure 6. SFDR vs. f_{OUT} @ 65 MSPS

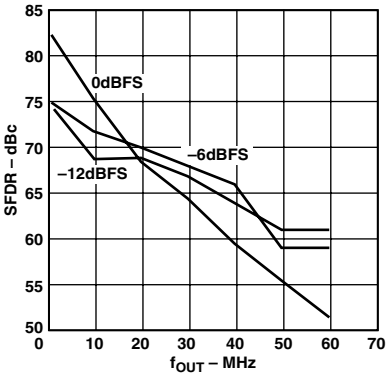


Figure 7. SFDR vs. f_{OUT} @ 125 MSPS

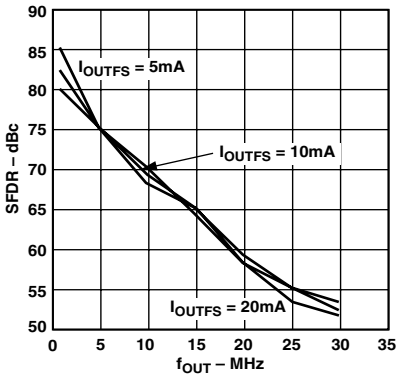


Figure 8. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS and 0 dBFS

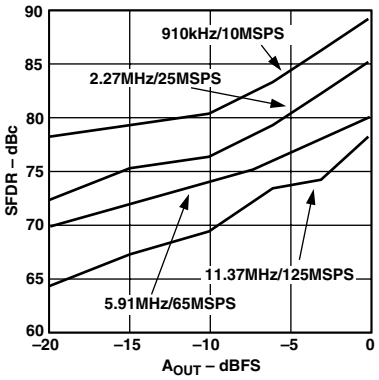


Figure 9. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/11$

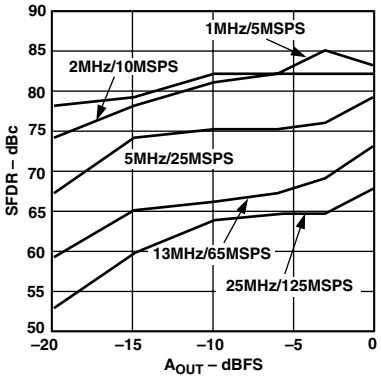


Figure 10. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

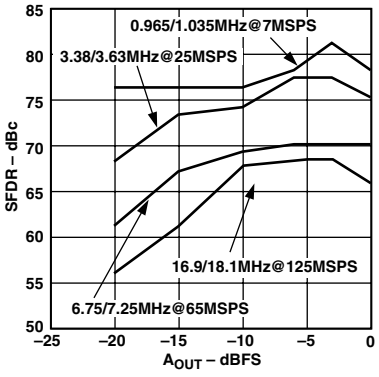


Figure 11. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/7$

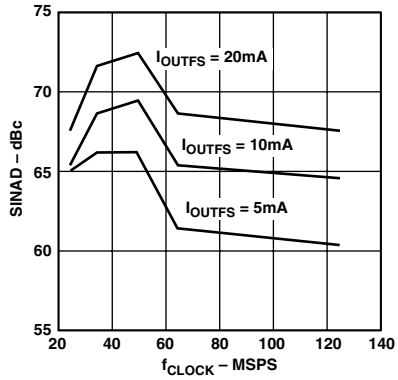


Figure 12. SINAD vs. f_{CLOCK} and I_{OUTFS} @ f_{OUT} = 5 MHz and 0 dBFS

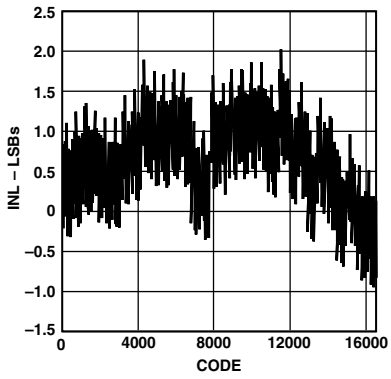


Figure 13. Typical INL

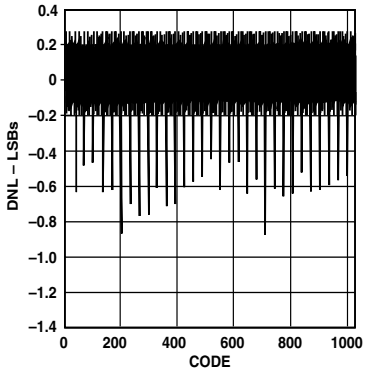


Figure 14. Typical DNL

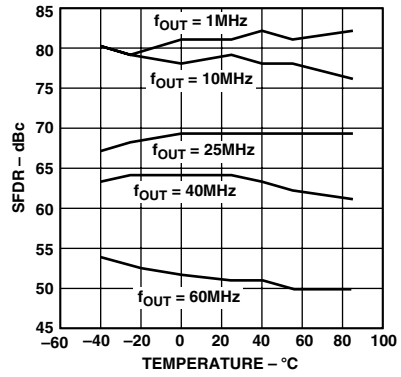


Figure 15. SFDR vs. Temperature @ 125 MSPS, 0 dBFS

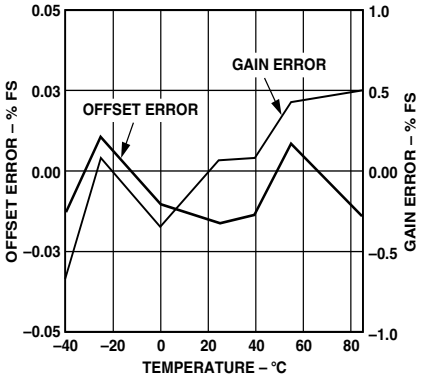


Figure 16. Reference Voltage Drift vs. Temperature

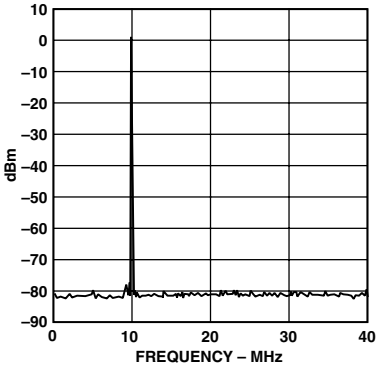


Figure 17. Single-Tone SFDR @ f_{CLK} = 125 MSPS

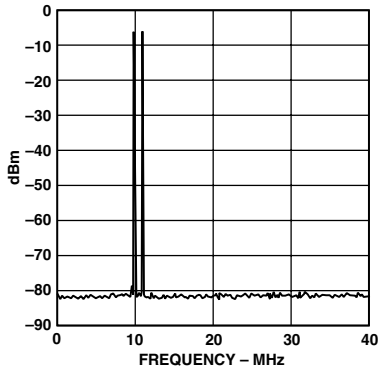


Figure 18. Dual-Tone SFDR @ f_{CLK} = 125 MSPS

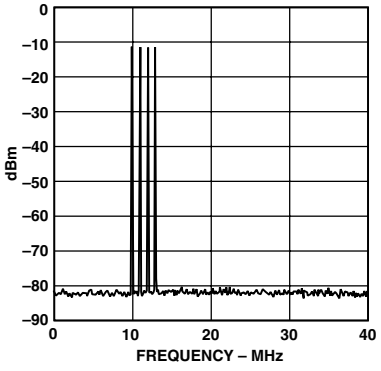


Figure 19. Four-Tone SFDR @ f_{CLK} = 125 MSPS

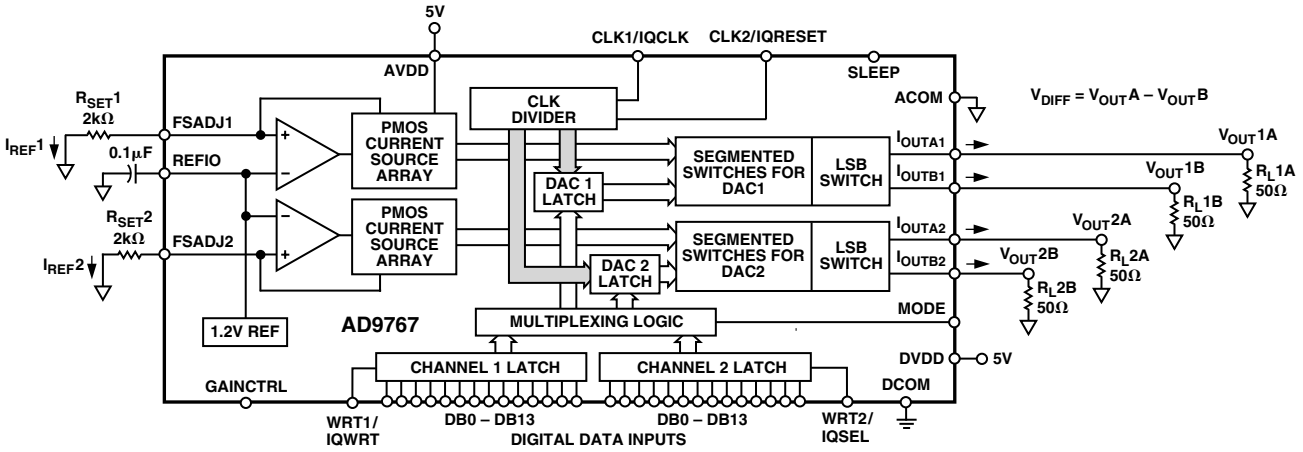


Figure 20. Simplified Block Diagram

FUNCTIONAL DESCRIPTION

Figure 20 shows a simplified block diagram of the AD9767. The AD9767 consists of two DACs, each with its own independent digital control logic and full-scale output current control. Each DAC contains a PMOS current source array capable of providing up to 20 mA of full-scale current (I_{OUTFS}). The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSB is a binary weighted fraction of the middle bit current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances the dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9767 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 3 V to 5.5 V range. The digital section, which is capable of operating up to a 125 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and two reference control amplifiers.

The full-scale output current of each DAC is regulated by separate reference control amplifiers and can be set from 2 mA to 20 mA via an external resistor, R_{SET}, connected to the Full Scale Adjust (FSADJ) pin. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is $32 \times I_{REF}$.

REFERENCE OPERATION

The AD9767 contains an internal 1.20 V bandgap reference. This can easily be overridden by an external reference with no effect on performance. REFIO serves as either an *input* or *output*, depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1 μF capacitor. The internal reference voltage will be present at REFIO. If the voltage at REFIO is to be used elsewhere in the circuit, an external buffer amplifier with an input bias current of less than 100 nA should be used. An example of the use of the internal reference is shown in Figure 21.

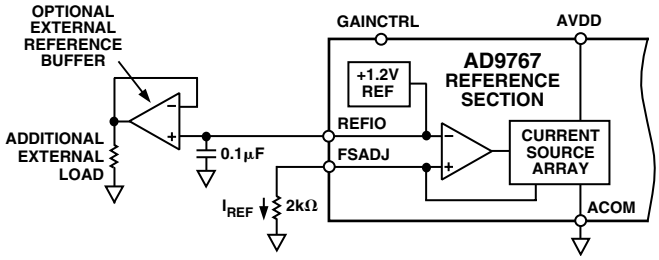


Figure 21. Internal Reference Configuration

An external reference can be applied to REFIO as shown in Figure 22. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 μF compensation capacitor is not required since the internal reference is overridden, and the relatively high input impedance of REFIO minimizes any loading of the external reference.

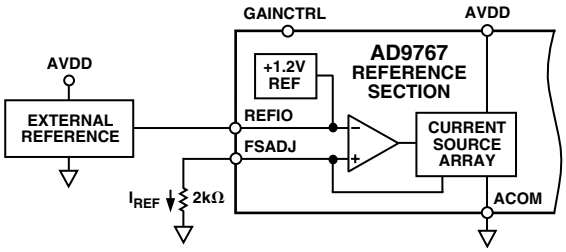


Figure 22. External Reference Configuration

GAINCTRL MODE

The AD9767 allows the gain of each channel to be independently set by connecting one R_{SET} resistor to FSADJ1 and another R_{SET} resistor to FSADJ2. To add flexibility and reduce system cost, a single R_{SET} resistor can be used to set the gain of both channels simultaneously.

When GAINCTRL is low (i.e., connected to AGND), the independent channel gain control mode using two resistors is enabled. In this mode, individual R_{SET} resistors should be connected to FSADJ1 and FSADJ2. When GAINCTRL is high (i.e., connected to AVDD), the master/slave channel gain control mode using one resistor is enabled. In this mode, a single R_{SET} resistor is connected to FSADJ1 and the resistor on FSADJ2 must be removed.

NOTE: Only parts with date code of 9930 or later have the Master/Slave GAINCTRL function. For parts with a date code before 9930, Pin 42 must be connected to AGND, and the part will operate in the two resistor, independent gain control mode.

REFERENCE CONTROL AMPLIFIER

Both of the DACs in the AD9767 contain a control amplifier that is used to regulate the full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter as shown in Figure 21, so that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied to the segmented current sources with the proper scale factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} from 2 mA to 20 mA by setting I_{REF} between 62.5 μA and 625 μA. The wide adjustment range of I_{OUTFS} provides several benefits. The first relates directly to the power dissipation of the AD9767, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500 kHz and can be used for low frequency, small signal multiplying applications.

DAC TRANSFER FUNCTION

Both DACs in the AD9767 provide complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 16383) while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA} = (DAC\ CODE\ /16384) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (16383 - DAC\ CODE)/16384) \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 16383 (i.e., Decimal Representation).

As previously mentioned, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage, V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply:

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB} and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2 \times DAC\ CODE - 16383)/16384\} \times (32 \times R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9767 differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9767 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

ANALOG OUTPUTS

The complementary current outputs in each DAC, I_{OUTA} and I_{OUTB}, may be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9767 is optimum and specified using a differential transformer coupled output in which the voltage swing at I_{OUTA} and I_{OUTB} is limited to ±0.5 V. If a single-ended unipolar output is desirable, I_{OUTA} should be selected.

The distortion and noise performance of the AD9767 can be enhanced when it is configured for differential operation. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (i.e., assuming no source termination). Since the output currents of I_{OUTA} and I_{OUTB} are complementary, they become additive when processed differentially. A properly selected transformer will allow the AD9767 to provide the required power and voltage levels to different loads.

The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 kΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground via an I-V op amp configuration will result in the optimum dc linearity. Note the INL/DNL specifications for the AD9767 are measured with I_{OUTA} maintained at a virtual ground via an op amp.

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9767.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed 0.5 V. Applications requiring the AD9767's output (i.e., V_{OUTA} and/or V_{OUTB}) to extend its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range will adversely affect the AD9767's linearity performance and subsequently degrade its distortion performance.

DIGITAL INPUTS

The AD9767's digital inputs consist of two channels. For the dual port mode, each DAC has its own dedicated 14-bit data port, WRT line and CLK line. In the interleaved timing mode, the function of the digital control pins changes as described in the Interleaved Mode Timing section. The 14-bit parallel data inputs follow straight binary coding where DB13 is the Most Significant Bit (MSB) and DB0 is the Least Significant Bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. The DAC outputs are updated following either the rising edge, or every other rising edge of the clock, depending on whether dual or interleaved mode is being used. The DAC outputs are designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

DAC TIMING

The AD9767 can operate in two timing modes, dual and interleaved, which are described below. The block diagram in Figure 25 represents the latch architecture in the interleaved timing mode.

DUAL PORT MODE TIMING

For the following section, refer to Figure 2.

When the mode pin is at Logic 1, the AD9767 operates in dual port mode. The AD9767 functions as two distinct DACs. Each DAC has its own completely independent digital input and control lines.

The AD9767 features a double buffered data path. Data enters the device through the channel input latches. This data is then transferred to the DAC latch in each signal path. Once the data is loaded into the DAC latch, the analog output will settle to its new value.

For general consideration, the WRT lines control the channel input latches and the CLK lines control the DAC latches. Both sets of latches are updated on the rising edge of their respective control signals.

The rising edge of CLK should occur before or simultaneously with the rising edge of WRT. Should the rising edge of CLK occur after the rising edge of WRT, a 2 ns minimum delay should be maintained from the rising edge of WRT to the rising edge of CLK.

Timing specifications for dual port mode are given in Figures 23 and 24.

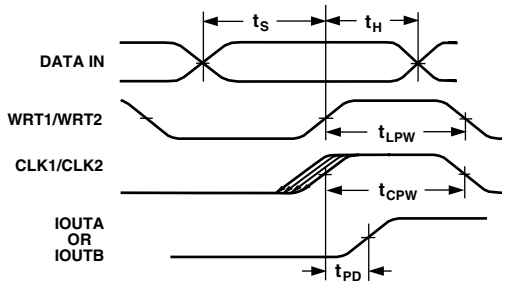


Figure 23. Dual Mode Timing

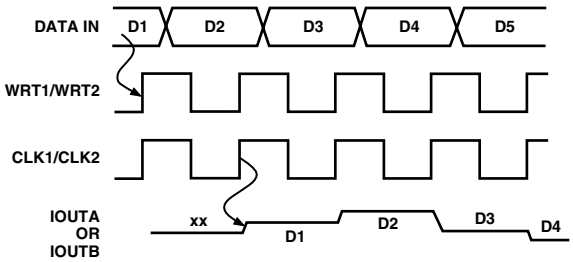


Figure 24. Dual Mode Timing

INTERLEAVED MODE TIMING

For the following section, refer to Figure 25.

When the mode pin is at Logic 0, the AD9767 operates in interleaved mode. WRT1 now functions as IQWRT and CLK1 functions as IQCLK. WRT2 functions as IQSEL and CLK2 functions as IQRESET.

Data enters the device on the rising edge of IQWRT. The logic level of IQSEL will steer the data to either Channel Latch 1 (IQSEL = 1) or to Channel Latch 2 (IQSEL = 0).

When IQRESET is high, IQCLK is disabled. When IQRESET goes low, the following rising edge on IQCLK will update both DAC latches with the data present at their inputs. In the interleaved mode IQCLK is divided by 2 internally. Following this first rising edge, the DAC latches will only be updated on every other rising edge of IQCLK. In this way, IQRESET can be used to synchronize the routing of the data to the DACs.

As with the dual port mode, IQCLK should occur before or simultaneously with IQWRT.

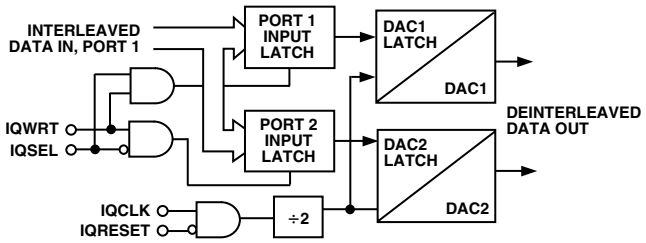


Figure 25. Latch Structure Interleaved Mode

Timing specifications for interleaved mode are given in Figures 26 and 27.

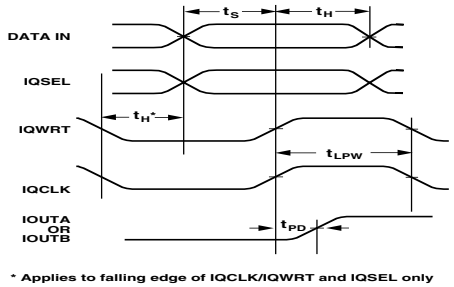


Figure 26. Interleaved Mode Timing

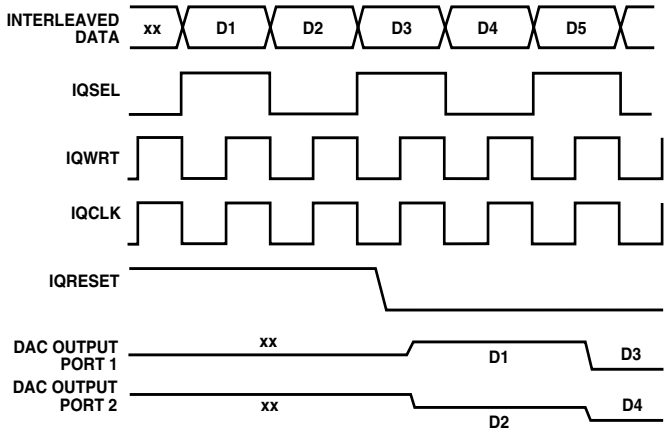


Figure 27. Interleaved Mode Timing

The digital inputs are CMOS-compatible with logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (DVDD) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9767 is capable of operating over a digital supply range of 3 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers V_{OH}(MAX). A DVDD of 3 V to 3.3 V will typically ensure proper compatibility with most TTL logic families. Figure 28 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar with the exception that it contains an active pull-down circuit, thus ensuring that the AD9767 remains enabled if this input is left disconnected.

Since the AD9767 is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. Operating the AD9767 with reduced logic swings and a corresponding digital supply (DVDD) will result in the lowest data feedthrough and on-chip digital noise. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the AD9767 as well as its required min/max input logic level thresholds.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9767 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to digital feedthrough. For longer board traces and high data update rates, stripline techniques with proper impedance and termination resistors should be considered to maintain "clean" digital inputs.

The external clock driver circuitry should provide the AD9767 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

Note that the clock input could also be driven via a sine wave, which is centered around the digital threshold (i.e., DVDD/2) and meets the min/max logic threshold. This will typically result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Also, at higher sampling rates, the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and, subsequently, cut into the required data setup and hold times.

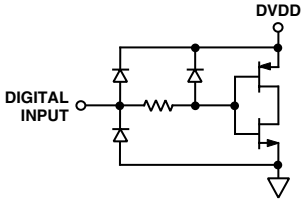


Figure 28. Equivalent Digital Input

INPUT CLOCK AND DATA TIMING RELATIONSHIP

SNR in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9767 is rising edge triggered, and so exhibits SNR sensitivity when the data transition is close to this edge. In general, the goal when applying the AD9767 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 29 shows the relationship of SNR to clock placement with different sample rates. Note that at the lower sample rates, much more tolerance is allowed in clock placement, while much more care must be taken at higher rates.

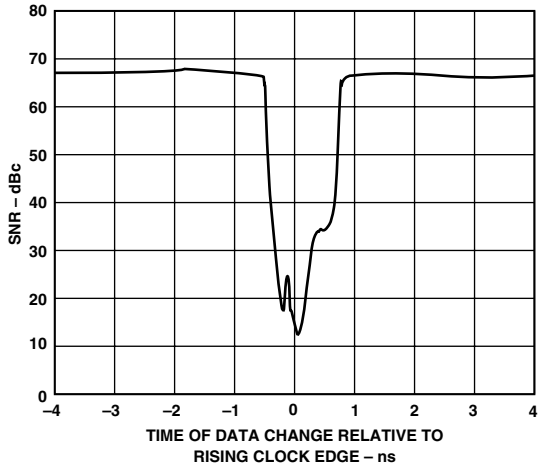


Figure 29. SNR vs. Clock Placement @ f_{OUT} = 20 MHz and f_{CLK} = 125 MSPS

SLEEP MODE OPERATION

The AD9767 has a power-down function that turns off the output current and reduces the supply current to less than 8.5 mA over the specified supply range of 3.0 V to 5.5 V and temperature range. This mode can be activated by applying a Logic Level "1" to the SLEEP pin. The SLEEP pin logic threshold is equal to 0.5 × AVDD. This digital input also contains an active pull-down circuit that ensures the AD9767 remains enabled if this input is left disconnected. The AD9767 takes less than 50 ns to power down and approximately 5 µs to power back up.

POWER DISSIPATION

The power dissipation, P_D, of the AD9767 is dependent on several factors that include: (1) The power supply voltages (AVDD and DVDD), (2) the full-scale current output I_{OUTFS}, (3) the update rate f_{CLOCK}, (4) and the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS} as shown in Figure 30 and is insensitive to f_{CLOCK}.

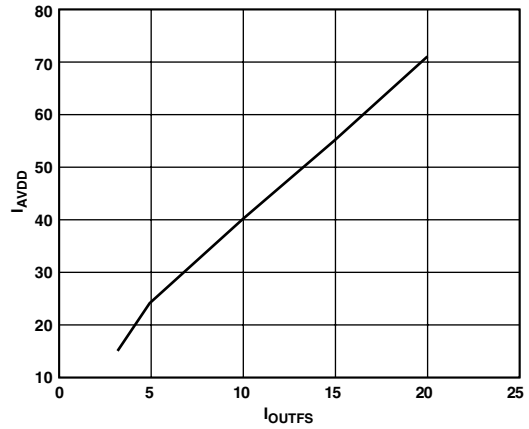


Figure 30. I_{AVDD} vs. I_{OUTFS}

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figures 31 and 32 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 5 V and DVDD = 3 V, respectively. Note how I_{DVDD} is reduced by more than a factor of 2 when DVDD is reduced from 5 V to 3 V.

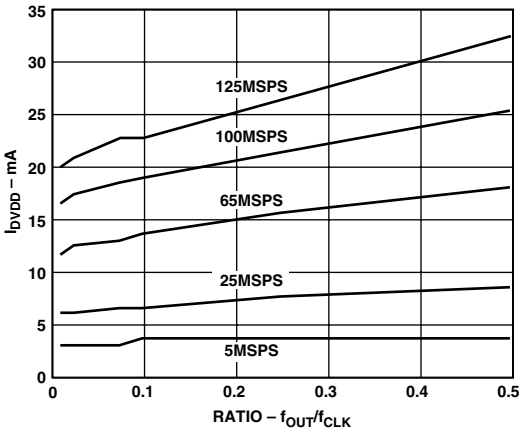


Figure 31. I_{DVDD} vs. Ratio @ DVDD = 5 V

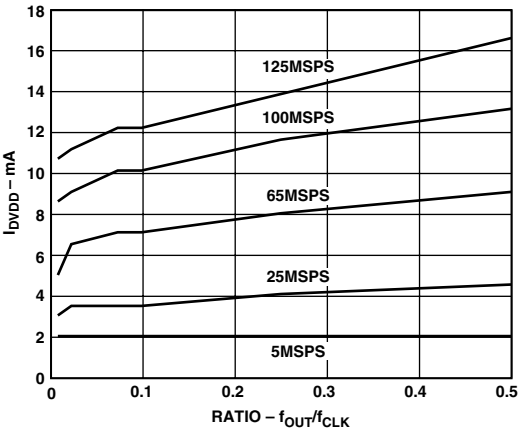


Figure 32. I_{DVDD} vs. Ratio @ DVDD = 3 V

APPLYING THE AD9767

Output Configurations

The following sections illustrate some typical output configurations for the AD9767. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level-shifting, within the bandwidth of the chosen op amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if I_{OUTA} and/or I_{OUTB} is connected to an appropriately-sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note that I_{OUTA} provides slightly better performance than I_{OUTB}.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 33. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9767. A differential resistor, R_{DIFF}, may be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

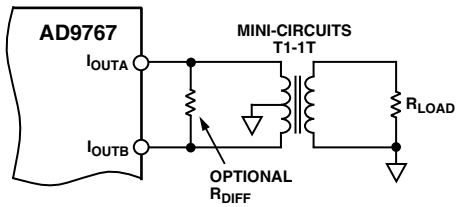


Figure 33. Differential Output Using a Transformer

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion as shown in Figure 34. The AD9767 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate from a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9767, while meeting other system level objectives (i.e., cost, power), should be selected. The op amp's differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

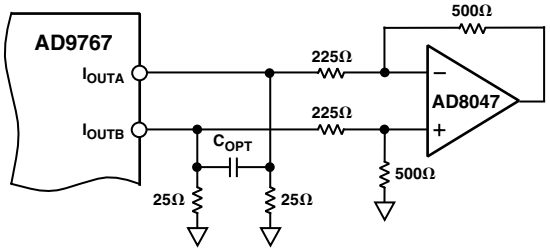


Figure 34. DC Differential Coupling Using an Op Amp

The differential circuit shown in Figure 35 provides the necessary level-shifting required in a single supply system. In this case AVDD, which is the positive analog supply for both the AD9767 and the op amp, is also used to level-shift the differential output of the AD9767 to midsupply (i.e., AVDD/2). The AD8055 is a suitable op amp for this application.

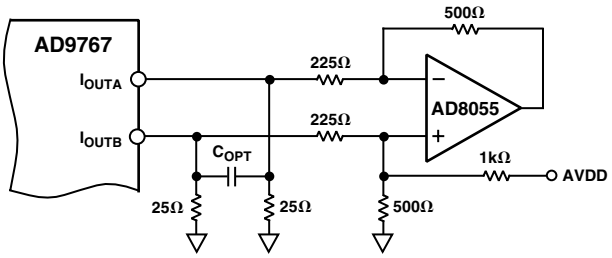


Figure 35. Single Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 36 shows the AD9767 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB}. The unused output (I_{OUTA} or I_{OUTB}) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of

I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the Analog Output section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

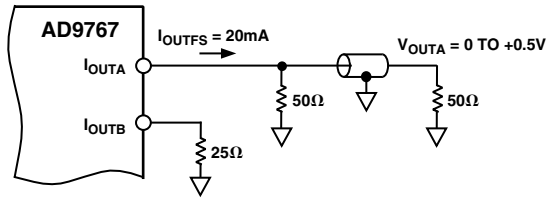


Figure 36. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 37 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9767 output current. U1 maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Output section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

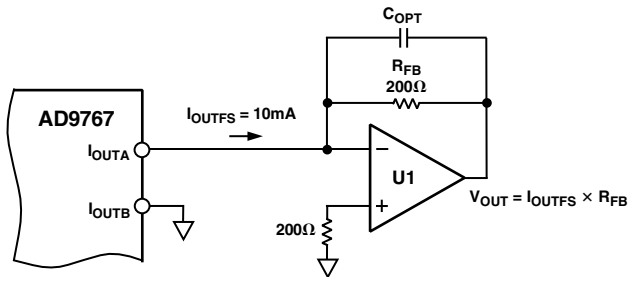


Figure 37. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION

Many applications seek high speed and high performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the printed circuit board is as important as the circuit design. Proper RF techniques must be used for device selection, placement and routing, as well as power supply bypassing and grounding to ensure optimum performance. Figures 43 to 50 illustrate the recommended printed circuit board ground, power and signal plane layouts which are implemented on the AD9767 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution. This is referred to as the Power Supply Rejection Ratio. For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full-scale current, I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise will occur over the spectrum from tens of kHz to several MHz. The PSRR vs. frequency of the AD9767 AVDD supply over this frequency range is shown in Figure 38.

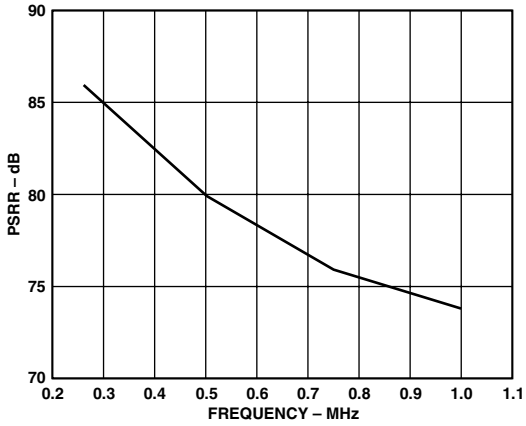


Figure 38. Power Supply Rejection Ratio of AD9767

Note that the units in Figure 38 are given in units of (amps out/volts in). Noise on the analog power supply has the effect of modulating the internal current sources, and therefore the output current. The voltage noise on AVDD, therefore, will be added in a nonlinear manner to the desired I_{OUT}. PSRR is very code-dependent thus producing mixing effects which can modulate low frequency power supply noise to higher frequencies. Worst case PSRR for either one of the differential DAC outputs will occur when the full-scale current is directed towards that output. As a result, the PSRR measurement in Figure 38 represents a worst case condition in which the digital inputs remain static and the full-scale output current of 20 mA is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV of noise and, for simplicity sake (i.e., ignore harmonics), all of this noise is concentrated at 250 kHz. To calculate how much of this undesired noise will appear as current noise superimposed on the DAC's full-scale current, I_{OUTFS}, one must determine the PSRR in dB using Figure 38 at 250 kHz. To calculate the PSRR for a given R_{LOAD}, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 38 by the scaling factor $20 \times \text{Log}(R_{LOAD})$. For instance, if R_{LOAD} is 50 Ω, the PSRR is reduced by 34 dB (i.e., PSRR of the DAC at 250 kHz, which is 85 dB in Figure 38, becomes 51 dB V_{OUT}/V_{IN}).

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9767 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close to the chip as physically possible.

For those applications that require a single +5 V or +3 V supply for both the analog and digital supplies, a clean analog supply may be generated using the circuit shown in Figure 39. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained by using low ESR type electrolytic and tantalum capacitors.

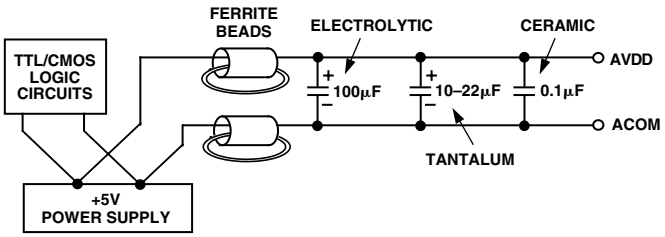


Figure 39. Differential LC Filter for Single +5 V and +3 V Applications

APPLICATION

VDSL Applications Using the AD9767

Very High Frequency Digital Subscriber Line (VDSL) technology is growing rapidly in applications requiring data transfer over relatively short distances. By using QAM modulation and transmitting the data in Discrete Multiple Tones (DMT), high data rates can be achieved.

As with other multitone applications, each VDSL tone is capable of transmitting a given number of bits, depending on the signal-to-noise ratio (SNR) in a narrow band around that tone. For a typical VDSL application, the tones are evenly spaced over the range of several kHz to 10 MHz. At the high frequency end of this range, performance is generally limited by cable characteristics and environmental factors, such as external interferers. Performance at the lower frequencies is much more dependent on the performance of the components in the signal chain. In addition to in-band noise, intermodulation from other tones can also potentially interfere with the data recovery for a given tone. The two graphs in Figure 40 represent a 500 tone missing bin test vector, with frequencies evenly spaced from 400 Hz to 10 MHz. This test is very commonly done to determine if distortion will limit the number of bits which can be transmitted in a tone. The test vector has a series of missing tones around 750 kHz, which is represented in Figure 40a, and a series of missing tones around 5 MHz, which is represented in Figure 40b. In both cases, the spurious free dynamic range (SFDR) between the transmitted tones and the empty bins is greater than 60 dB.

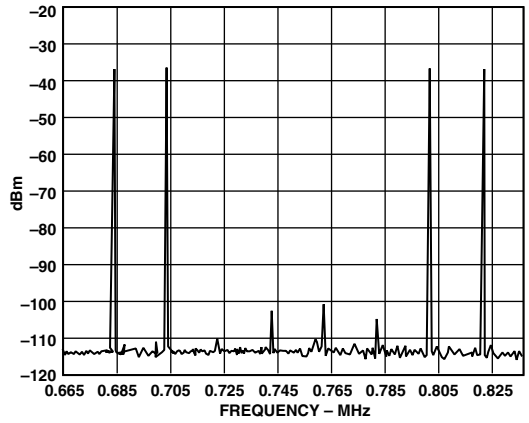


Figure 40a. Notch in Missing Bin at 750 kHz Is Down >60 dB (Peak Amplitude = 0 dBm)

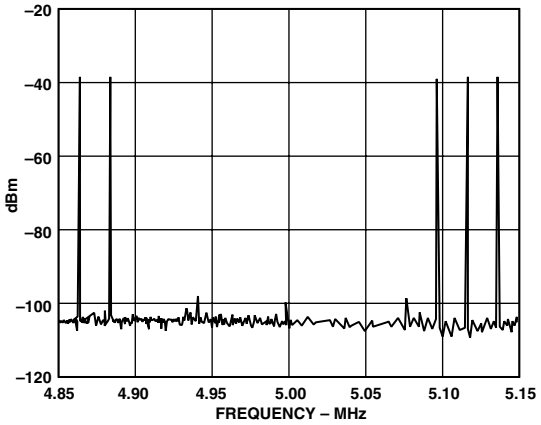


Figure 40b. Notch in Missing Bin at 5 MHz Is Down >60 dB (Peak Amplitude = 0 dBm)

CDMA

Carrier Division Multiple Access, or CDMA, is an air transmit/receive scheme where the signal in the transmit path is modulated with a pseudorandom digital code (sometimes referred to as the spreading code). The effect of this is to spread the transmitted signal across a wide spectrum. Similar to a DMT waveform, a CDMA waveform containing multiple subscribers can be characterized as having a high peak to average ratio (i.e., crest factor), thus demanding highly linear components in the transmit signal path. The bandwidth of the spectrum is defined by the CDMA standard being used, and in operation is implemented by using a spreading code with particular characteristics.

Distortion in the transmit path can lead to power being transmitted out of the defined band. The ratio of power transmitted in-band to out-of-band is often referred to as Adjacent Channel Power (ACP). This is a regulatory issue due to the possibility of interference with other signals being transmitted by air. Regulatory bodies define a spectral mask outside of the transmit band, and the ACP must fall under this mask. If distortion in the transmit path causes the ACP to be above the spectral mask, then filtering, or different component selection, is needed to meet the mask requirements.

Figure 41 shows the AD9767, when used with the AD8346, reconstructing a wideband CDMA signal at 2.4 GHz. The baseband signal is being sampled at 65 MSPS and has a chip rate of 8M chips.

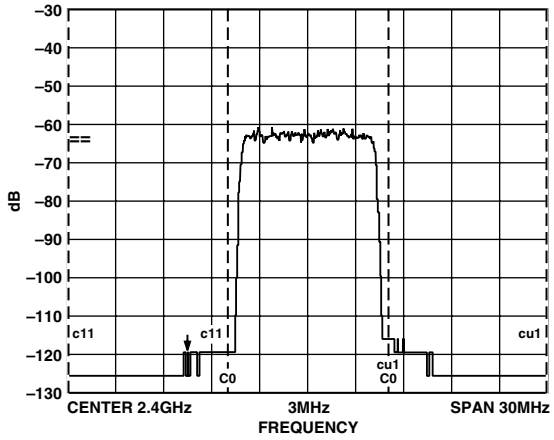


Figure 41. CDMA Signal, 8 M Chips Sampled at 65 MSPS, Recreated at 2.4 GHz Adjacent Channel Power > 60 dBm

Figure 42 shows an example of the AD9767 used in a W-CDMA transmitter application using the AD6122 CDMA 3 V IF subsystem. The AD6122 has functions, such as external gain control and low distortion characteristics, needed for the superior Adjacent Channel Power (ACP) requirements of W-CDMA.

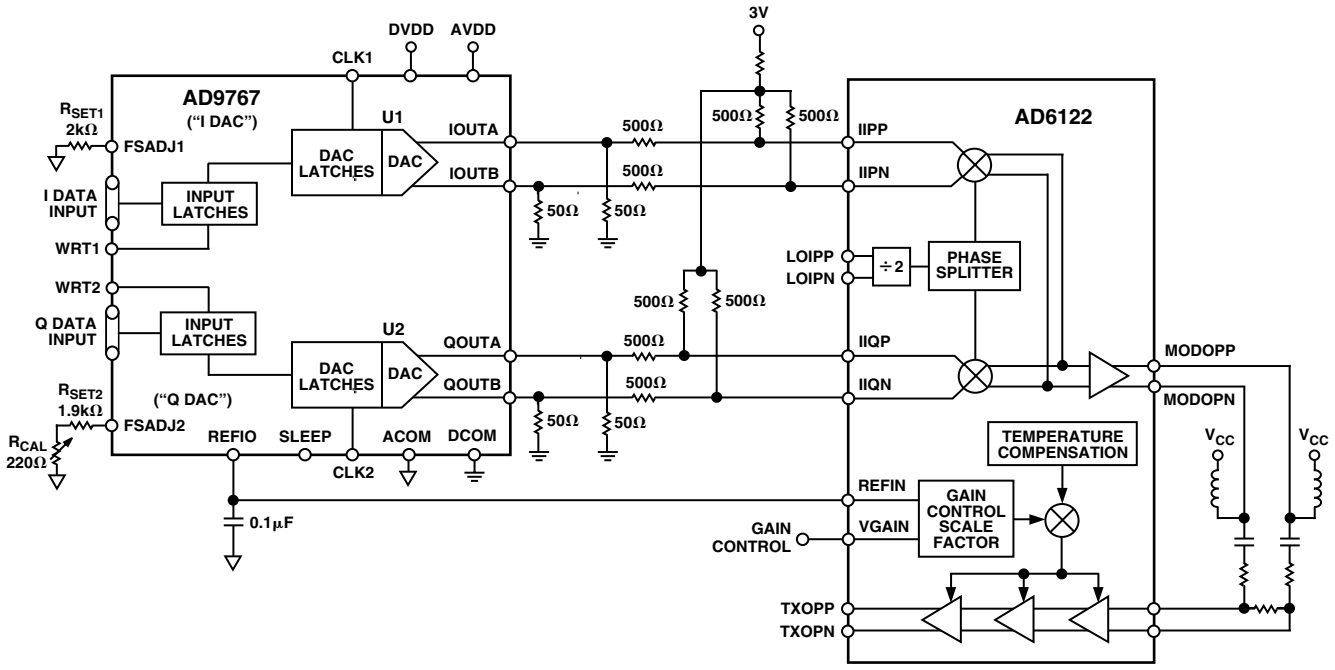


Figure 42. CDMA Transmit Application Using AD9767 and AD6122

EVALUATION BOARD

General Description

The AD9767-EB is an evaluation board for the AD9767 14-bit dual D/A converter. Careful attention to layout and circuit design, combined with a prototyping area, allow the user to easily and effectively evaluate the AD9767 in any application where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9767 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single and differential outputs. The digital inputs can be used in dual port or interleaved mode, and are designed to be driven from various word generators, with the on-board option to add a resistor network for proper load termination. When operating the AD9767, best performance is obtained by running the Digital Supply (DVDD) at +3 V and the Analog Supply (AVDD) at +5 V.

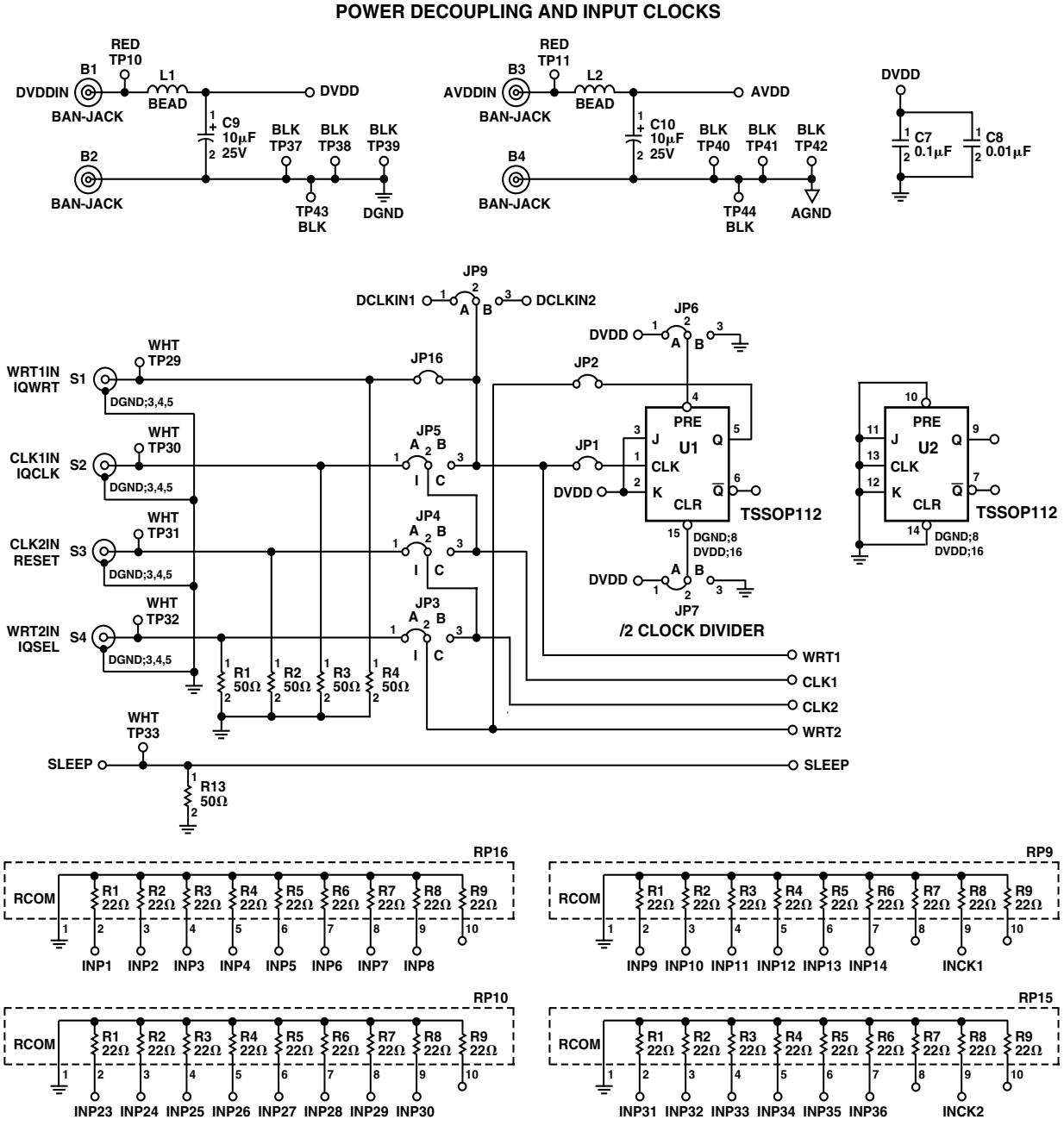


Figure 43. Power Decoupling and Clocks on AD9767 Evaluation Board

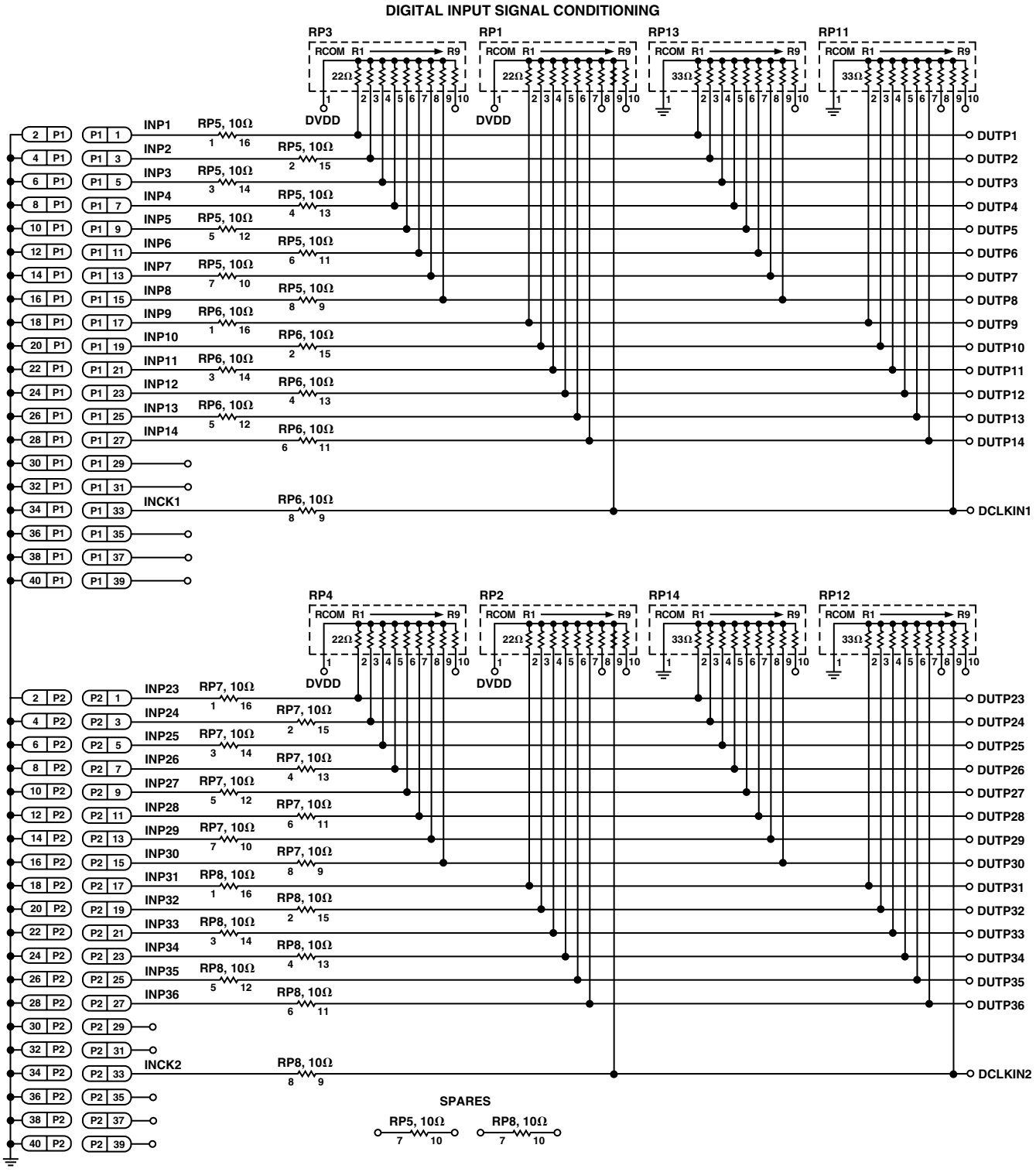


Figure 44. Digital Input Signal Conditioning

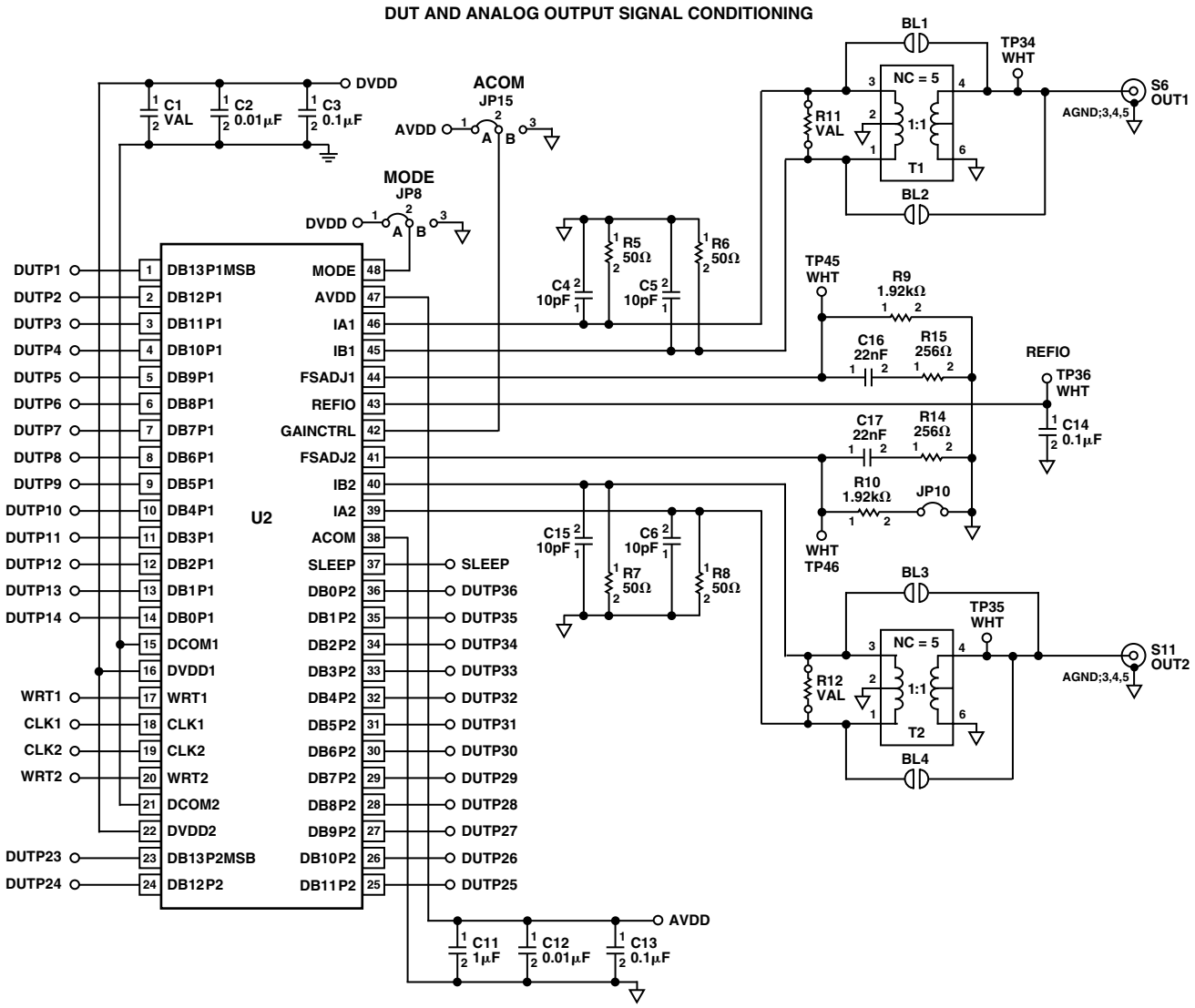


Figure 45. AD9767 and Output Signal Conditioning

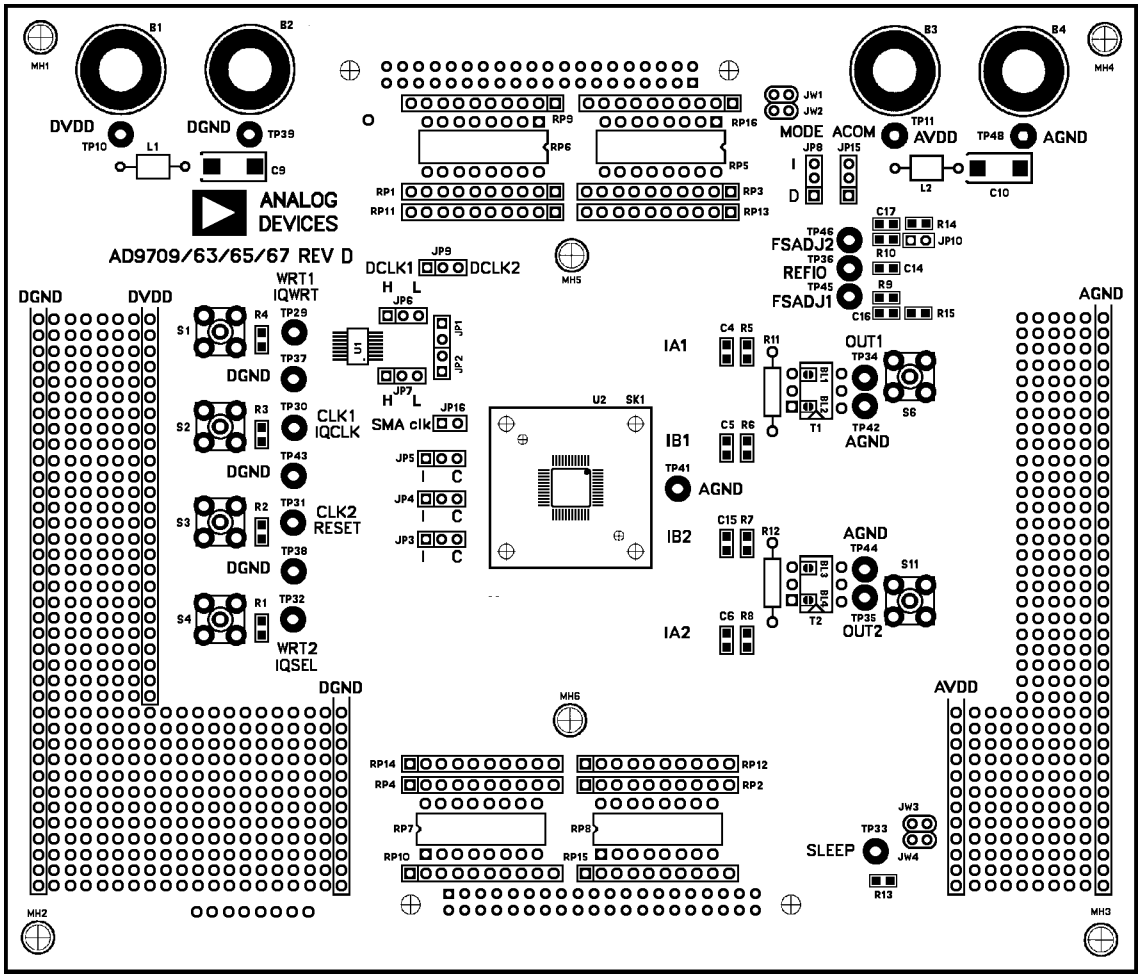


Figure 46. Assembly, Top Side

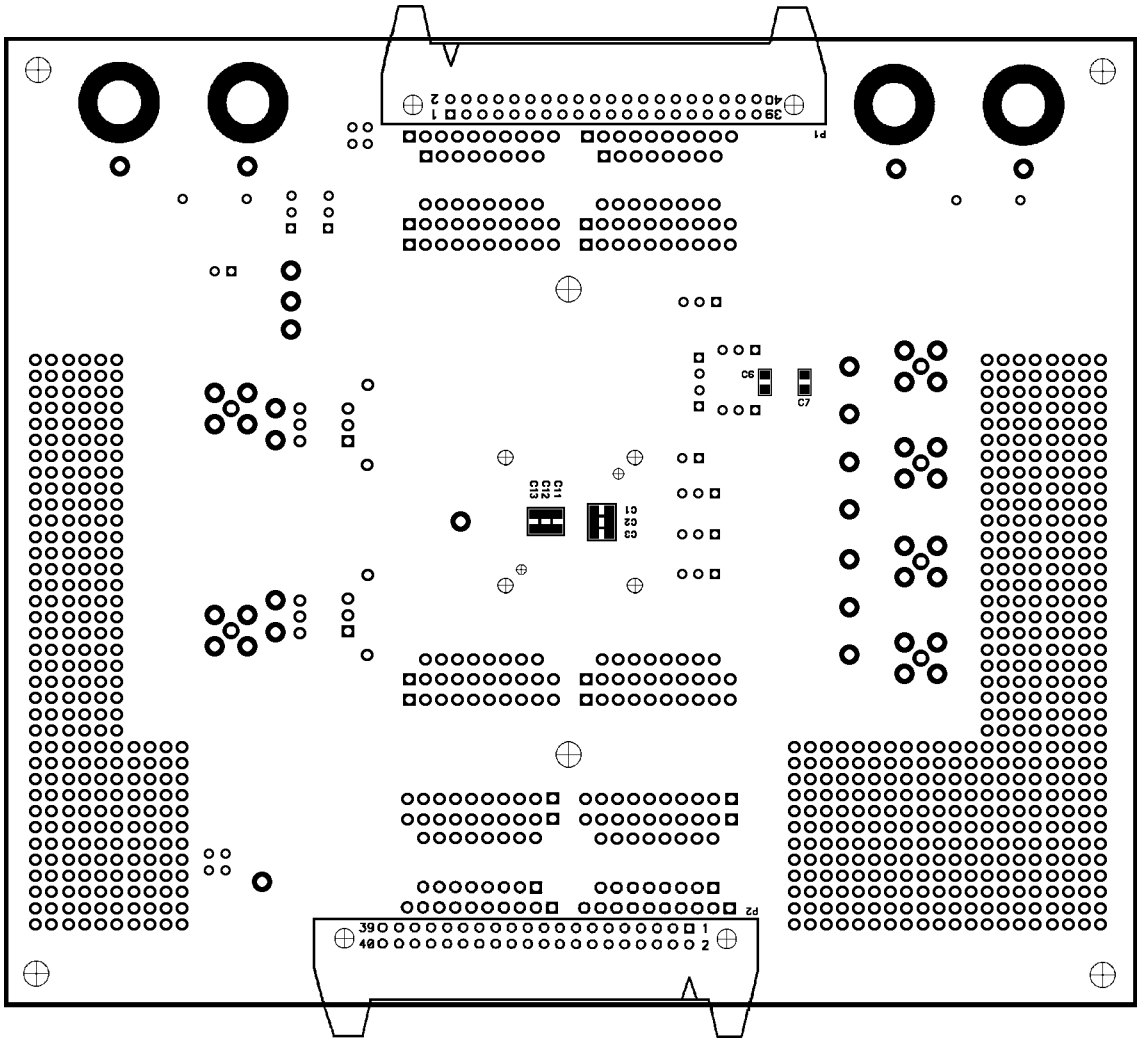


Figure 47. Assembly, Bottom Side

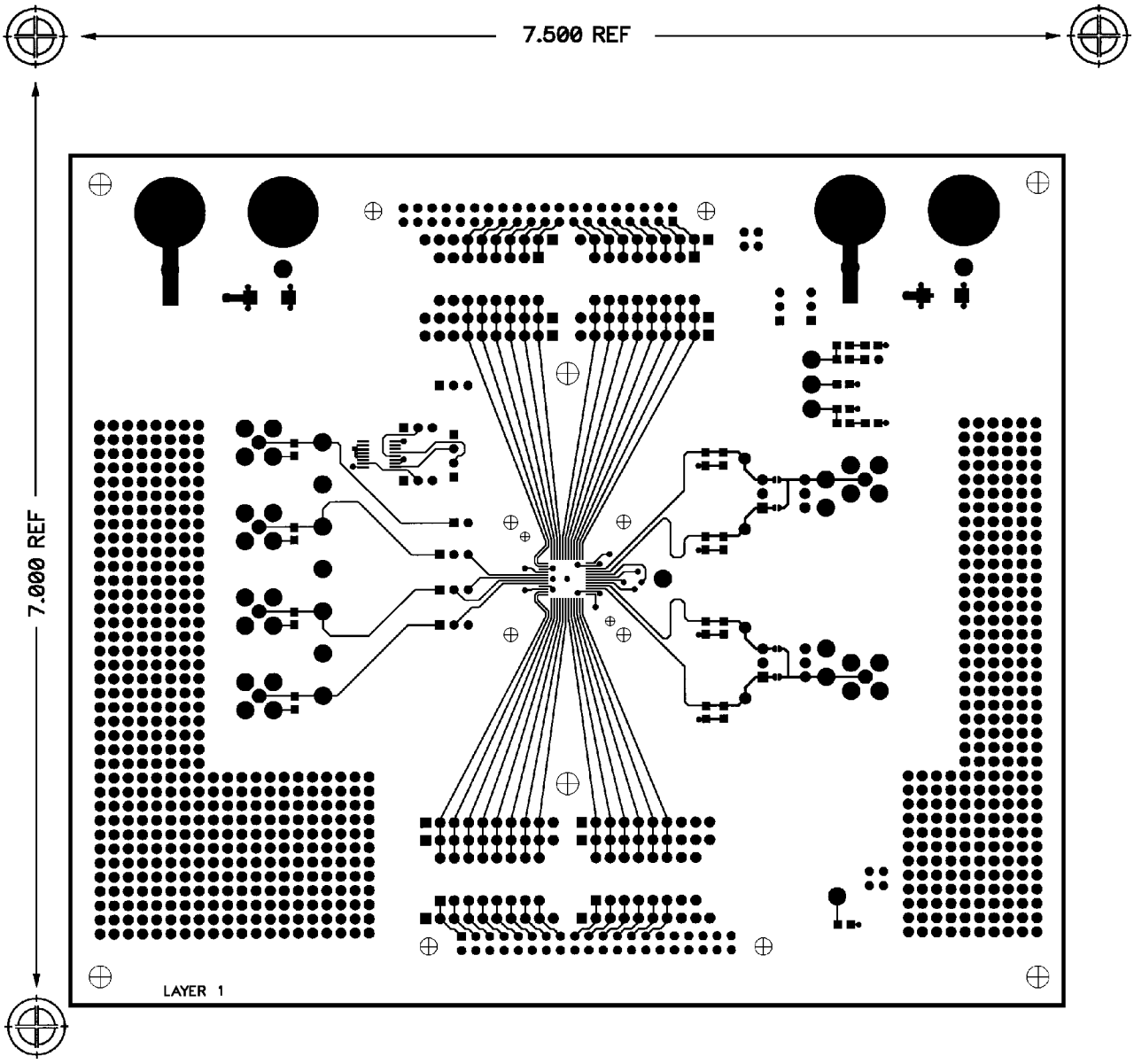


Figure 48. Layer 1, Top Side

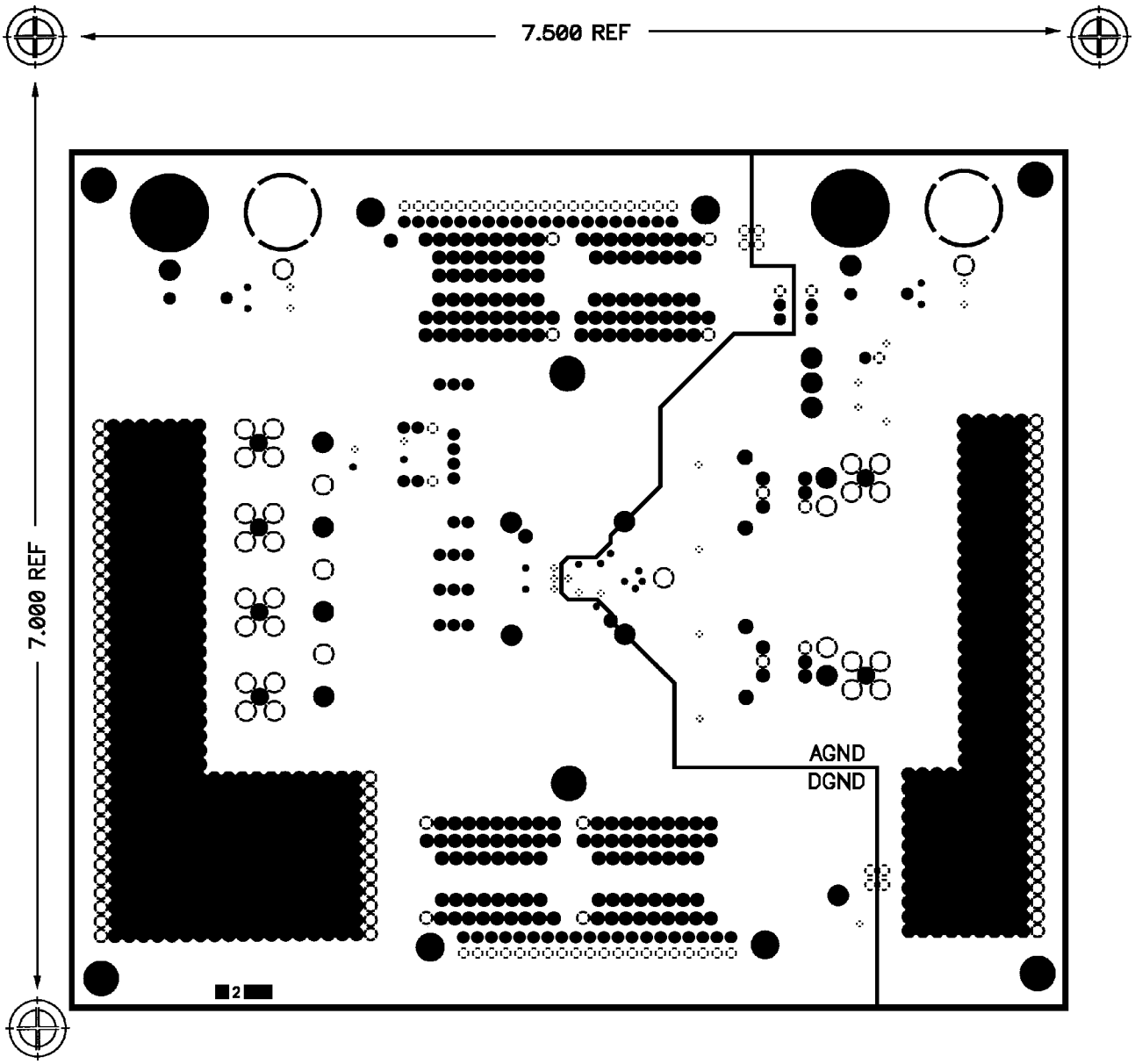


Figure 49. Layer 2, Ground Plane

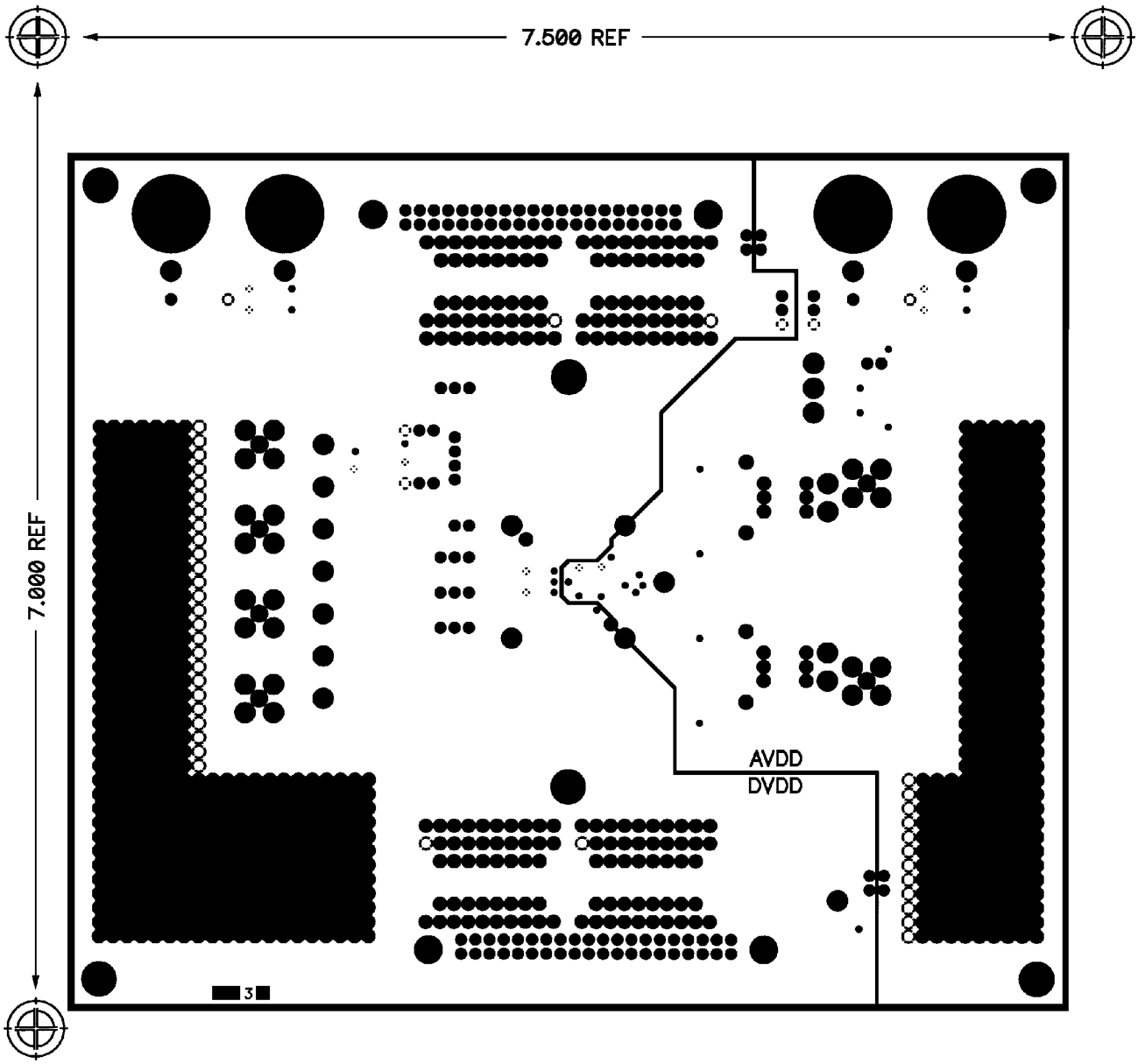


Figure 50. Layer 3, Power Plane

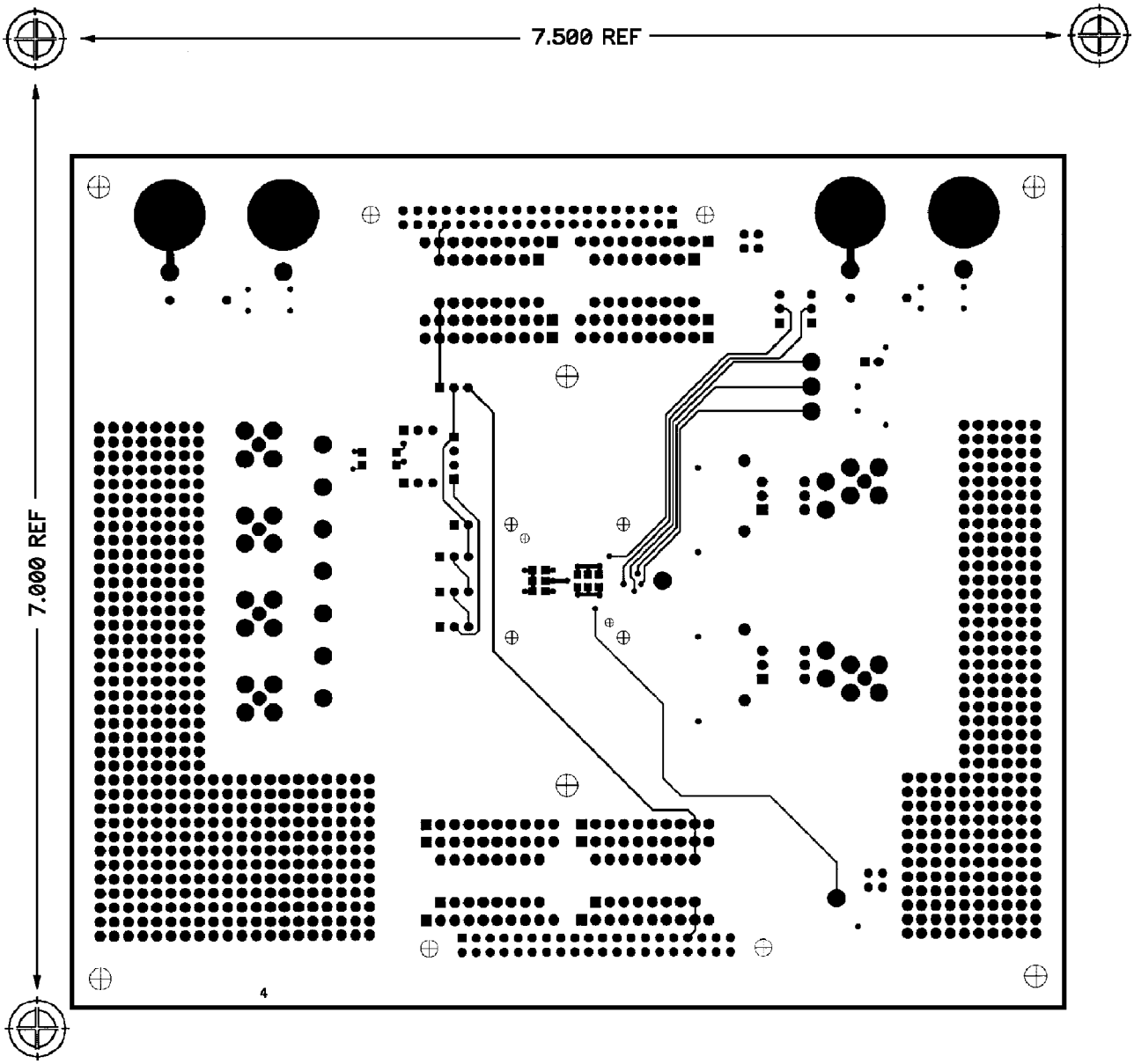
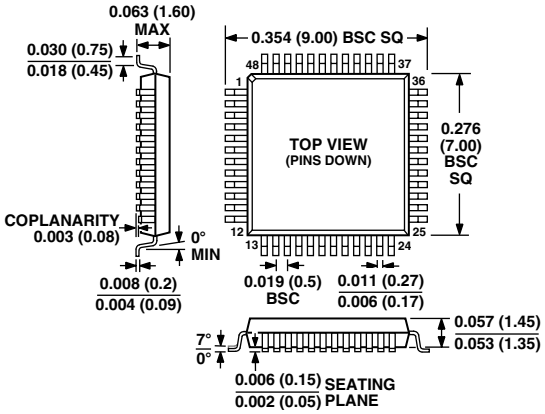


Figure 51. Layer 4, Bottom Side

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Thin Plastic Quad Flatpack (ST-48)



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