12-Bit, 300 MSPS High Speed TxDAC+® D/A Converter

AD9753*

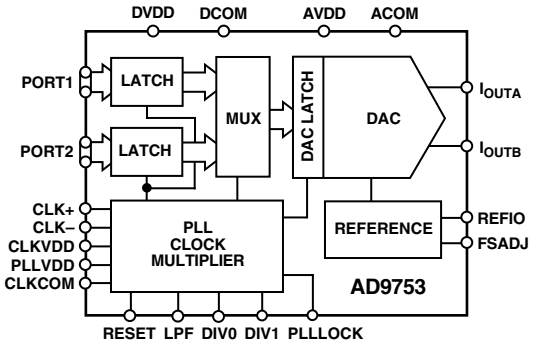
FEATURES

12-Bit Dual Muxed Port DAC
300 MSPS Output Update Rate
Excellent SFDR and IMD Performance
SFDR to Nyquist @ 25 MHz Output: 69 dB
Internal Clock Doubling PLL
Differential or Single-Ended Clock Input
On-Chip 1.2 V Reference
Single 3.3 V Supply Operation
Power Dissipation: 155 mW @ 3.3 V
48-Lead LQFP

APPLICATIONS

Communications: LMDS, LMCS, MMDS
Base Stations
Digital Synthesis
QAM and OFDM

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9753 is a dual, muxed port, ultrahigh speed, single-channel, 12-bit CMOS DAC. It integrates a high quality 12-bit TxDAC+ core, a voltage reference, and digital interface circuitry into a small 48-lead LQFP package. The AD9753 offers exceptional ac and dc performance while supporting update rates up to 300 MSPS.

The AD9753 has been optimized for ultrahigh speed applications up to 300 MSPS where data rates exceed those possible on a single data interface port DAC. The digital interface consists of two buffered latches as well as control logic. These latches can be time multiplexed to the high speed DAC in several ways. This PLL drives the DAC latch at twice the speed of the externally applied clock and is able to interleave the data from the two input channels. The resulting output data rate is twice that of the two input channels. With the PLL disabled, an external 2× clock may be supplied and divided by two internally.

The CLK inputs (CLK+/CLK–) can be driven either differentially or single-ended, with a signal swing as low as 1 V p-p.

The DAC utilizes a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and to maximize dynamic accuracy. Differential current outputs support single-ended or differential applications. The differential outputs each provide a nominal full-scale current from 2 mA to 20 mA.

The AD9753 is manufactured on an advanced low cost 0.35 µm CMOS process. It operates from a single supply of 3.0 V to 3.6 V and consumes 155 mW of power.

PRODUCT HIGHLIGHTS

1. The AD9753 is a member of a pin compatible family of high speed TxDAC+s providing 10-, 12-, and 14-bit resolution.
2. Ultrahigh Speed 300 MSPS Conversion Rate.
3. Dual 12-Bit Latched, Multiplexed Input Ports. The AD9753 features a flexible digital interface allowing high speed data conversion through either a single or dual port input.
4. Low Power. Complete CMOS DAC function operates on 155 mW from a 3.0 V to 3.6 V single supply. The DAC full-scale current can be reduced for lower power operation.
5. On-Chip Voltage Reference. The AD9753 includes a 1.20 V temperature-compensated band gap voltage reference.

*Protected by U.S. Patent numbers 5450084, 5568145, 5689257, and 5703519.

REV. B

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AD9753–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, PLLVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
RESOLUTION	12			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)	–1.5	±0.5	+1.5	LSB
Differential Nonlinearity (DNL)	–1	±0.4	+1	LSB
ANALOG OUTPUT				
Offset Error	–0.025	±0.01	+0.025	% of FSR
Gain Error (Without Internal Reference)	–2	±0.5	+2	% of FSR
Gain Error (With Internal Reference)	–2	±0.25	+2	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	3.0	3.3	3.6	V
DVDD	3.0	3.3	3.6	V
PLLVDD	3.0	3.3	3.6	V
CLKVDD	3.0	3.3	3.6	V
Analog Supply Current (I_{AVDD})[4]		33	36	mA
Digital Supply Current (I_{DVDD})[4]		3.5	4.5	mA
PLL Supply Current (I_{PLLVDD})[4]		4.5	5.1	mA
Clock Supply Current (I_{CLKVDD})[4]		10.0	11.5	mA
Power Dissipation[4] (3 V, I_{OUTFS} = 20 mA)		155	165	mW
Power Dissipation[5] (3 V, I_{OUTFS} = 20 mA)		216		mW
Power Supply Rejection Ratio[6]—AVDD	–1		+1	% of FSR/V
Power Supply Rejection Ratio[6]—DVDD	–0.04		+0.04	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at I_{OUTA}, driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3]An external buffer amplifier is recommended to drive any external load.
[4]100 MSPS f_{DAC} with PLL on, f_{OUT} = 1 MHz, all supplies = 3.0 V.
[5]300 MSPS f_{DAC}.
[6]±5% power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, PLLVDD = 0 V, CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, Differential Transformer-Coupled Output, 50 V Doubly Terminated, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{DAC})	300			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		11		ns
Output Propagation Delay (t_{PD})[1]		1		ns
Glitch Impulse[1]		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/$\sqrt{\text{Hz}}$
Output Noise (I_{OUTFS} = 2 mA)		30		pA/$\sqrt{\text{Hz}}$
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{DAC} = 100 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output	72	82		dBc
–6 dBFS Output		76		dBc
–12 dBFS Output		76		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 1.1 MHz[2]		77		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 5.1 MHz[2]		77		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 10.1 MHz[2]		76		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 20.1 MHz[2]		72		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 30.1 MHz[2]		68		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 1.1 MHz		78		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 11.1 MHz		75		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 31.1 MHz		70		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 51.1 MHz		70		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 71.1 MHz		67		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 1.1 MHz		78		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 26.1 MHz		69		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 51.1 MHz		65		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 101.1 MHz		59		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 141.1 MHz		58		dBc
Spurious-Free Dynamic Range within a Window				
f_{DAC} = 100 MSPS; f_{OUT} = 1 MHz; 2 MHz Span				
0 dBFS Output	82.5	92		dBc
f_{DAC} = 65 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		85		dBc
f_{DAC} = 150 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		85		dBc
Total Harmonic Distortion				
f_{DAC} = 100 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS		–82	–71	dBc
f_{DAC} = 65 MHz; f_{OUT} = 2.00 MHz		–76		dBc
f_{DAC} = 160 MHz; f_{OUT} = 2.00 MHz		–76		dBc
Multitone Power Ratio (Eight Tones at 110 kHz Spacing)				
f_{DAC} = 65 MSPS; f_{OUT} = 2.00 MHz to 2.77 MHz				
0 dBFS Output		73		dBc
–6 dBFS Output		71		dBc
–12 dBFS Output		69		dBc

NOTES
[1]Measured single-ended into 50 Ω load.
[2]Single-Port Mode (PLL disabled, DIV0 = 1, DIV1 = 0, data on Port 1).

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = PLLVDD = CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic 1	2.1	3		V
Logic 0		0	0.9	V
Logic 1 Current	–10		+10	μA
Logic 0 Current	–10		+10	μA
Input Capacitance		5		pF
Input Setup Time (t_S), T_A = 25°C	1.0	0.5		ns
Input Hold Time (t_H), T_A = 25°C	1.0	0.5		ns
Latch Pulsewidth (t_{LPW}), T_A = 25°C	1.5			ns
Input Setup Time (t_S, PLLVDD = 0 V), T_A = 25°C	–1.0	–1.5		ns
Input Hold Time (t_H, PLLVDD = 0 V), T_A = 25°C	2.5	1.7		ns
CLK to PLLLOCK Delay (t_D, PLLVDD = 0 V), T_A = 25°C	3.5		4.0	ns
Latch Pulsewidth (t_{LPW} PLLVDD = 0 V), T_A = 25°C	1.5			ns
PLLOCK (V_{OH})	3.0			V
PLLOCK (V_{OL})			0.3	V
CLK INPUTS				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V
Min CLK Frequency*		6.25		MHz

*Min CLK Frequency applies only when using internal PLL. When PLL is disabled, there is no minimum CLK frequency.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
AVDD, DVDD, CLKVDD, PLLVDD	ACOM, DCOM, CLKCOM, PLLCOM	–0.3	+3.9	V
AVDD, DVDD, CLKVDD, PLLVDD	AVDD, DVDD, CLKVDD, PLLVDD	–3.9	+3.9	V
ACOM, DCOM, CLKCOM, PLLCOM	ACOM, DCOM, CLKCOM, PLLCOM	–0.3	+0.3	V
REFIO, REFLO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
I_{OUTA}, I_{OUTB}	ACOM	–1.0	AVDD + 0.3	V
Digital Data Inputs (DB13 to DB0)	DCOM	–0.3	DVDD + 0.3	V
CLK+/CLK–, PLLLOCK	CLKCOM	–0.3	CLKVDD + 0.3	V
DIV0, DIV1, RESET	CLKCOM	–0.3	CLKVDD + 0.3	V
LPF	PLLCOM	–0.3	PLLVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

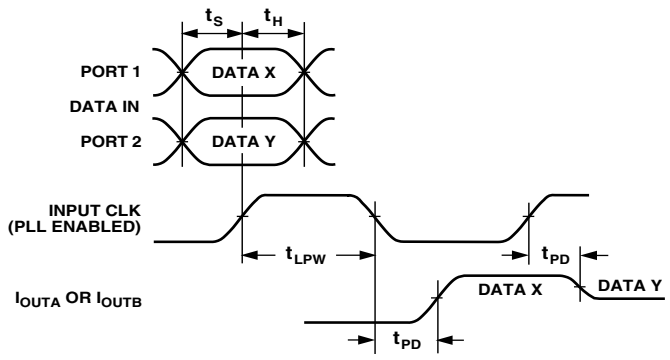


Figure 1. I/O Timing

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9753AST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9753ASTRL	–40°C to +85°C	48-Lead LQFP	ST-48
AD9753-EB			Evaluation Board

THERMAL CHARACTERISTIC

Thermal Resistance

48-Lead LQFP

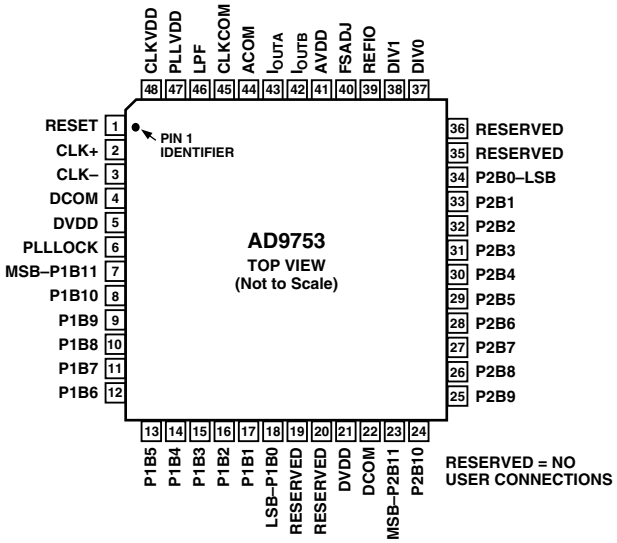
θ_{JA} = 91°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9753 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	RESET	Internal Clock Divider Reset
2	CLK+	Differential Clock Input
3	CLK–	Differential Clock Input
4, 22	DCOM	Digital Common
5, 21	DVDD	Digital Supply Voltage
6	PLLLOCK	Phase-Locked Loop Lock Indicator Output
7–18	P1B11–P1B0	Data Bits DB11 to DB0, Port 1
19–20, 35–36	RESERVED	
23–34	P2B11–P2B0	Data Bits DB11 to DB0, Port 2
37, 38	DIV0, DIV1	Control Inputs for PLL and Input Port Selector Mode. See Tables I and II for details.
39	REFIO	Reference Input/Output
40	FSADJ	Full-Scale Current Output Adjust
41	AVDD	Analog Supply Voltage
42	I_{OUTB}	Differential DAC Current Output
43	I_{OUTA}	Differential DAC Current Output
44	ACOM	Analog Common
45	CLKCOM	Clock and Phase-Locked Loop Common
46	LPF	Phase-Locked Loop Filter
47	PLLVDD	Phase-Locked Loop Supply Voltage
48	CLKVDD	Clock Supply Voltage

TERMINOLOGY

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s, minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels (dB).

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Adjacent Channel Power Ratio (ACPR)
A ratio in dBc between the measured power within a channel relative to its adjacent channel.

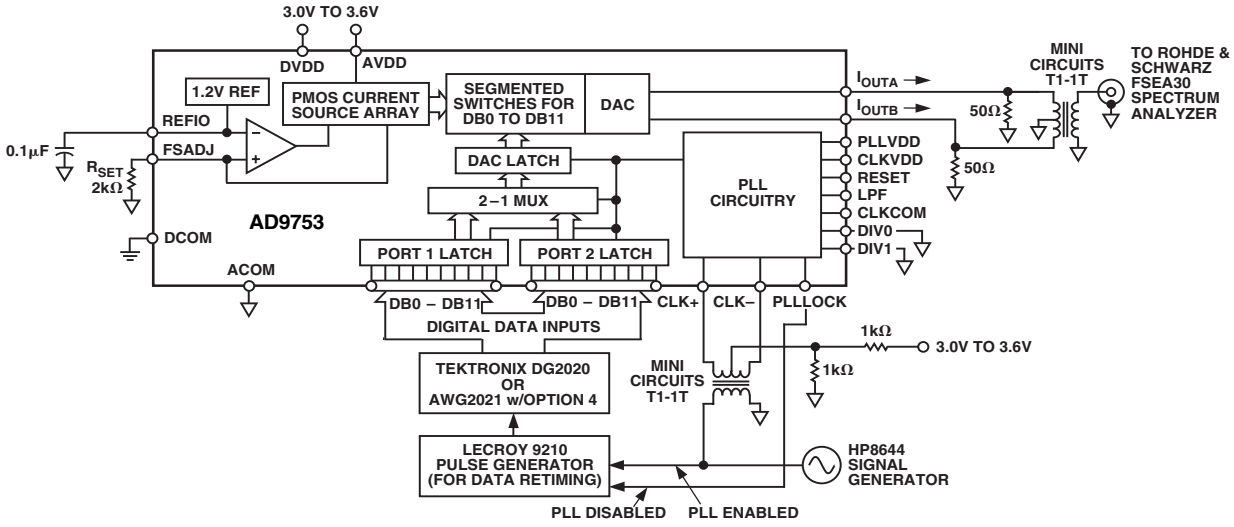
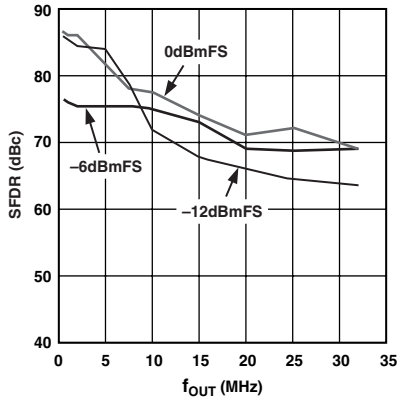
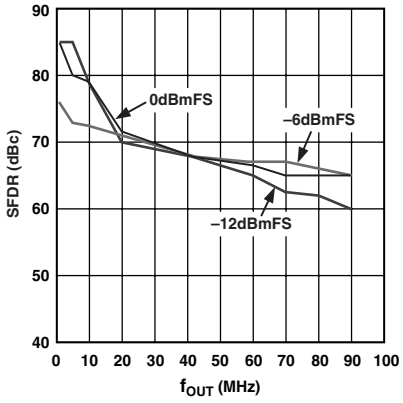


Figure 2. Basic AC Characterization Test Setup

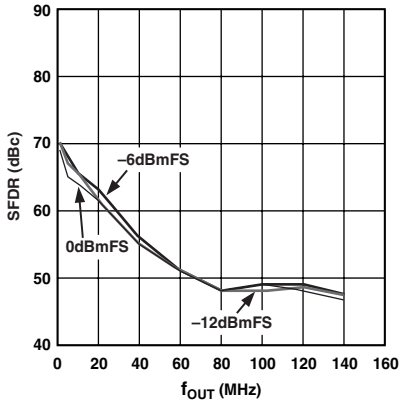
AD9753–Typical Performance Characteristics



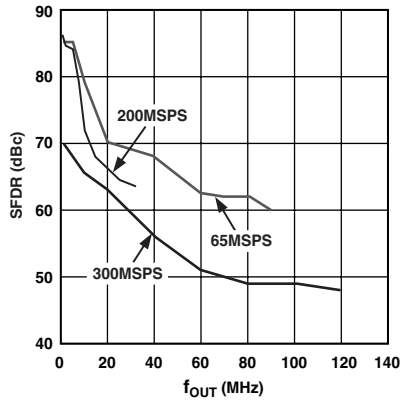
TPC 1. Single-Tone SFDR vs. f_{OUT} @ f_{DAC} = 65 MSPS, Single-Port Mode



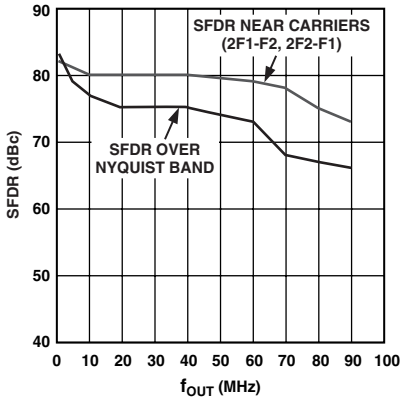
TPC 2. Single-Tone SFDR vs. f_{OUT} @ f_{DAC} = 200 MSPS



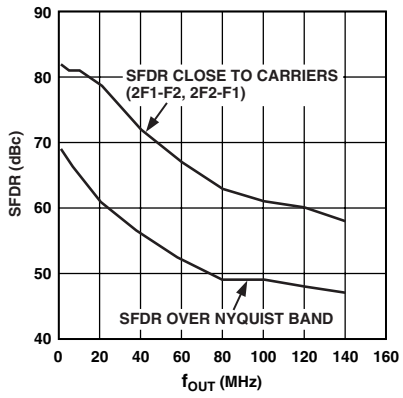
TPC 3. Single-Tone SFDR vs. f_{OUT} @ f_{DAC} = 300 MSPS



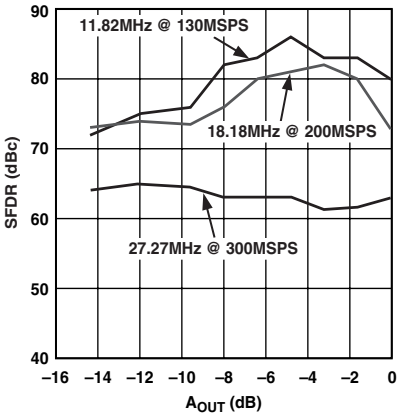
TPC 4. SFDR vs. f_{OUT} @ 0 dBFS



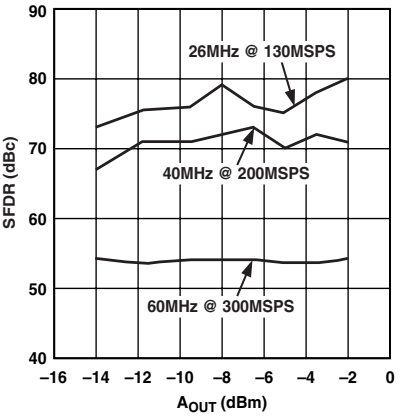
TPC 5. Two-Tone IMD vs. f_{OUT} @ f_{DAC} = 200 MSPS, 1 MHz Spacing between Tones, 0 dBFS



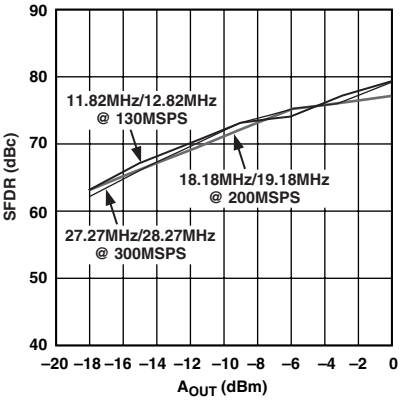
TPC 6. Two-Tone IMD vs. f_{OUT} @ f_{DAC} = 300 MSPS, 1 MHz Spacing between Tones, 0 dBFS



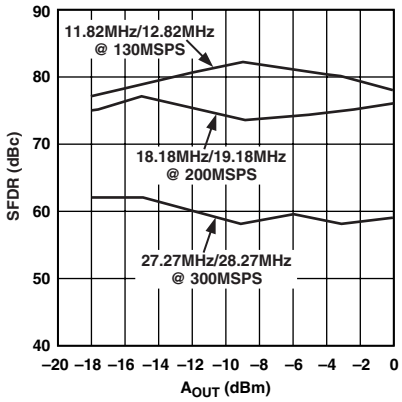
TPC 7. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{DAC}/11$



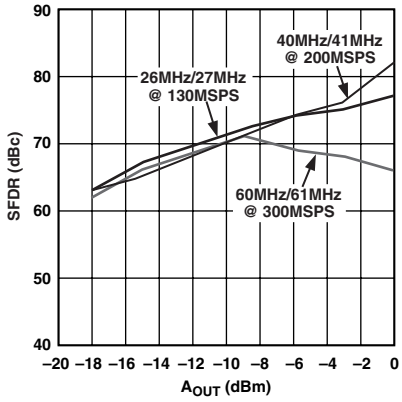
TPC 8. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{DAC}/5$



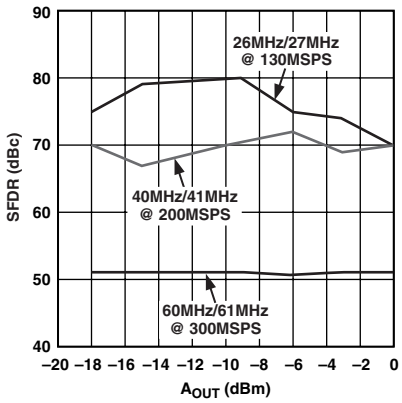
TPC 9. Two-Tone IMD (Third Order Products) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/11$



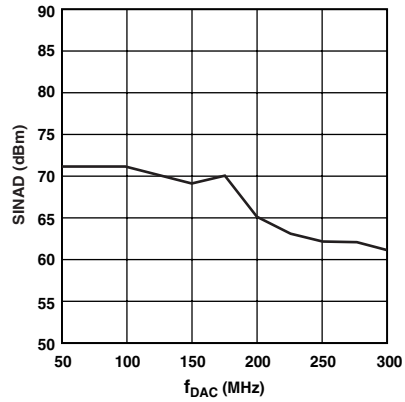
TPC 10. Two-Tone IMD (to Nyquist) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/11$



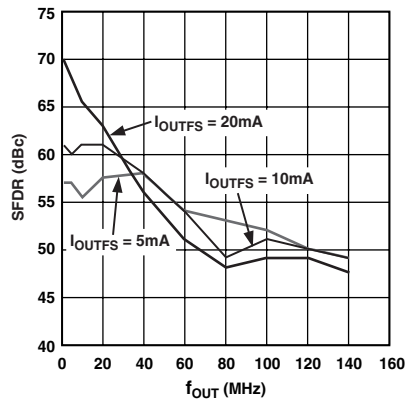
TPC 11. Two-Tone IMD (Third Order Products) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/5$



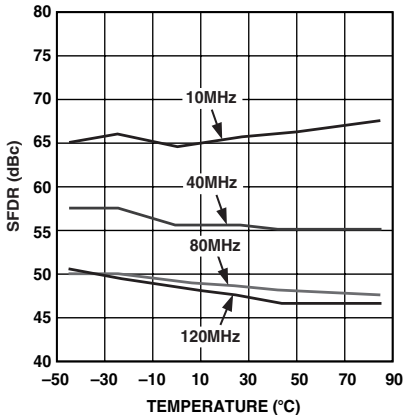
TPC 12. Two-Tone IMD (to Nyquist) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/5$



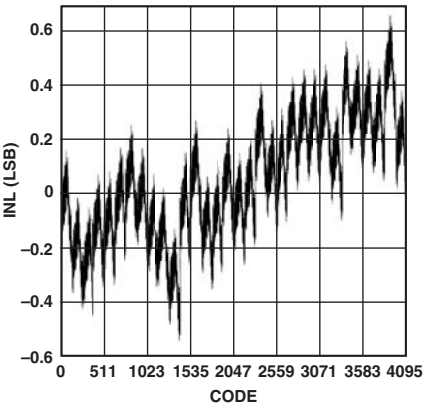
TPC 13. SINAD vs. f_{DAC} @ f_{OUT} = 10 MHz, 0 dBFS



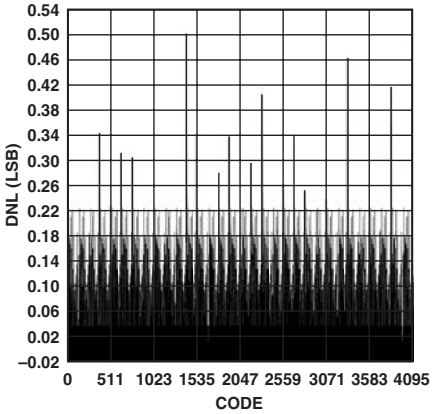
TPC 14. SFDR vs. I_{OUTFS}, f_{DAC} = 300 MSPS @ 0 dBFS



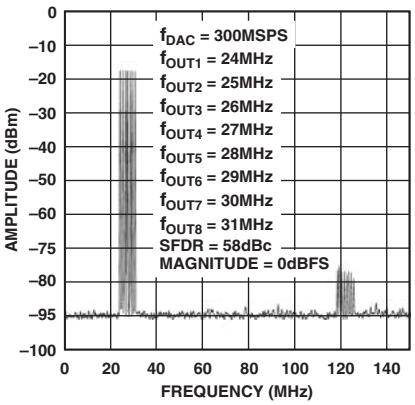
TPC 15. SFDR vs. Temperature, f_{DAC} = 300 MSPS @ 0 dBFS



TPC 16. Typical INL



TPC 17. Typical DNL



TPC 18. Eight-Tone SFDR @ $f_{OUT} \approx f_{DAC}/11$, f_{DAC} = 300 MSPS

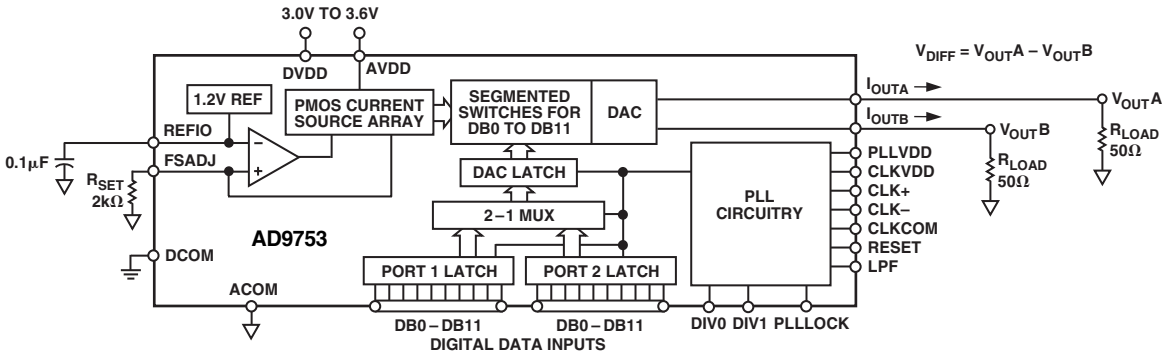


Figure 3. Simplified Block Diagram

FUNCTIONAL DESCRIPTION

Figure 3 shows a simplified block diagram of the AD9753. The AD9753 consists of a PMOS current source array capable of providing up to 20 mA of full-scale current, I_{OUTFS}. The array is divided into 31 equal sources that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are a binary weighted fraction of the middle bit current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of the current sources are switched to one of the two outputs (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9753 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 3.0 V to 3.6 V range. The digital section, which is capable of operating at a 300 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V band gap voltage reference, and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is 32 times the value of I_{REF}.

REFERENCE OPERATION

The AD9753 contains an internal 1.20 V band gap reference. This can easily be overdriven by an external reference with no effect on performance. REFIO serves as either an input or output, depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1 µF capacitor. The internal reference voltage will be present at REFIO. If the voltage at REFIO is to be used elsewhere in the circuit, an external buffer amplifier with an input bias current less than 100 nA should be used. An example of the use of the internal reference is given in Figure 4.

A low impedance external reference can be applied to REFIO, as shown in Figure 5. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is overdriven, and the relatively high input impedance of REFIO minimizes any loading of the external reference.

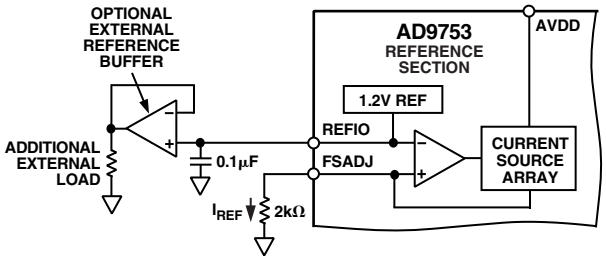


Figure 4. Internal Reference Configuration

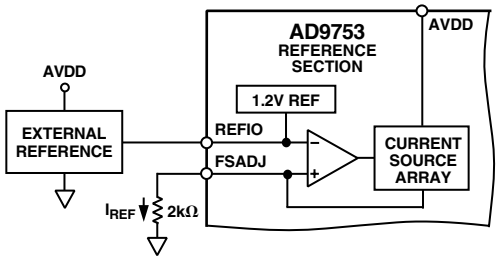


Figure 5. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9753 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a voltage-to-current converter as shown in Figure 4, so that its current output, I_{REF}, is determined by the ratio of V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is applied to the segmented current sources with the proper scaling factor to set I_{OUTFS}, as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 μA and 625 μA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9753, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500 kHz and can be used for low frequency, small signal multiplying applications.

PLL CLOCK MULTIPLIER OPERATION

The Phase-Locked Loop (PLL) is intrinsic to the operation of the AD9753 in that it produces the necessary internally synchronized 2× clock for the edge-triggered latches, multiplexer, and DAC.

With PLLVDD connected to its supply voltage, the AD9753 is in PLL mode. Figure 6 shows a functional block diagram of the AD9753 clock control circuitry with PLL active. The circuitry consists of a phase detector, charge pump, voltage controlled oscillator (VCO), input data rate range control, clock logic circuitry, and control input/outputs. The ÷2 logic in the feedback loop allows the PLL to generate the 2× clock needed for the DAC output latch.

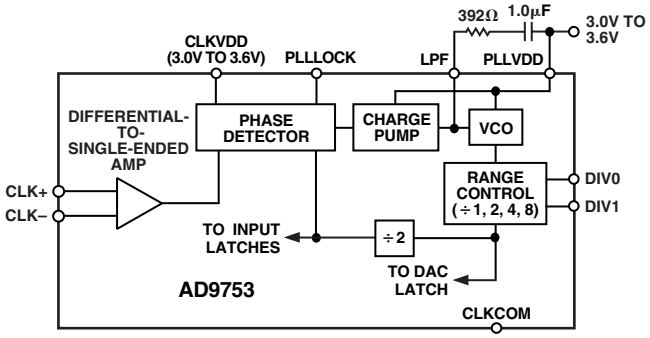


Figure 6. Clock Circuitry with PLL Active

Figure 7 defines the input and output timing for the AD9753 with the PLL active. CLK in Figure 7 represents the clock that is generated external to the AD9753. The input data at both Ports 1 and 2 is latched on the same CLK rising edge. CLK may be applied as a single-ended signal by tying CLK– to midsupply and applying CLK to CLK+, or as a differential signal applied to CLK+ and CLK–.

RESET has no purpose when using the internal PLL and should be grounded. When the AD9753 is in PLL mode, PLLLOCK is the output of the internal phase detector. When locked, the lock output in this mode will be a Logic 1.

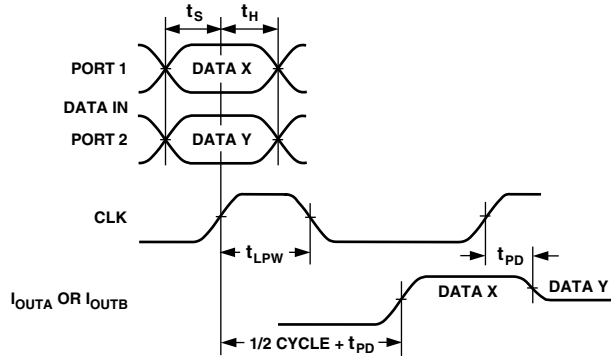


Figure 7a. DAC Input Timing Requirements with PLL Active, Single Clock Cycle

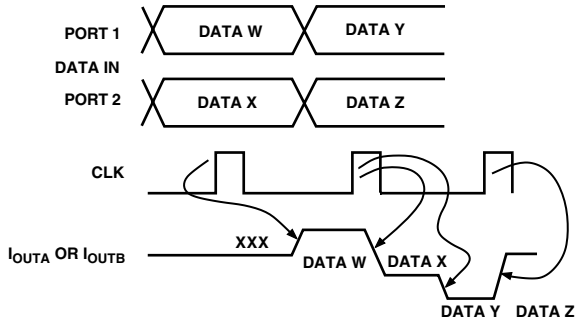


Figure 7b. DAC Input Timing Requirements with PLL Active, Multiple Clock Cycles

Typically, the VCO can generate outputs of 100 MHz to 400 MHz. The range control is used to keep the VCO operating within its designed range, while allowing input clocks as low as 6.25 MHz. With the PLL active, logic levels at DIV0 and DIV1 determine the divide (prescaler) ratio of the range controller. Table I gives the frequency range of the input clock for the different states of DIV0 and DIV1.

Table I. CLK Rates for DIV0, DIV1 Levels with PLL Active

CLK Frequency	DIV1	DIV0	Range Controller
50 MHz–150 MHz	0	0	÷1
25 MHz–100 MHz	0	1	÷2
12.5 MHz–50 MHz	1	0	÷4
6.25 MHz–25 MHz	1	1	÷8

A 392 Ω resistor and 1.0 μF capacitor connected in series from LPF to PLLVDD are required to optimize the phase noise versus the settling/acquisition time characteristics of the PLL. To obtain optimum noise and distortion performance, PLLVDD should be set to a voltage level similar to DVDD and CLKVDD.

In general, the best phase noise performance for any PLL range control setting is achieved with the VCO operating near its maximum output frequency of 400 MHz.

As stated earlier, applications requiring input data rates below 6.25 MSPS must disable the PLL clock multiplier and provide an external 2× reference clock. At higher data rates however, applications already containing a low phase noise (i.e., jitter)

reference clock that is twice the input data rate should consider disabling the PLL clock multiplier to achieve the best SNR performance from the AD9753. Note, the SFDR performance of the AD9753 remains unaffected with or without the PLL clock multiplier enabled.

The effects of phase noise on the AD9753's SNR performance become more noticeable at higher reconstructed output frequencies and signal levels. Figure 8 compares the phase noise of a full-scale sine wave at exactly $f_{DATA}/4$ at different data rates (thus carrier frequency) with the optimum DIV1, DIV0 setting.

SNR is partly a function of the jitter generated by the clock circuitry. As a result, any noise on PLLVDD or CLKVDD may decrease the SNR at the output of the DAC. To minimize this potential problem, PLLVDD and CLKVDD can be connected to DVDD using an LC filter network similar to the one shown in Figure 9.

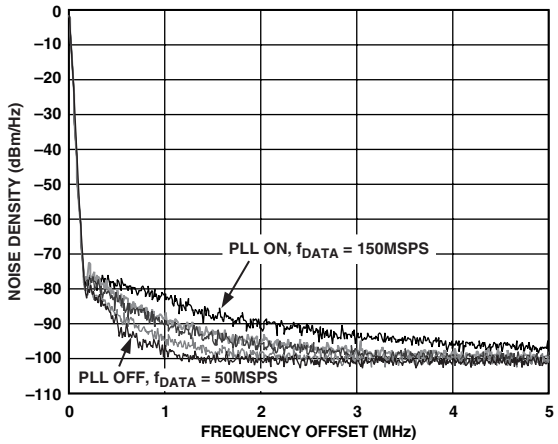


Figure 8. Phase Noise of PLL Clock Multiplier at $f_{OUT} = f_{DATA}/4$ at Different f_{DATA} Settings with DIV0/DIV1 Optimized, Using R&S FSEA30 Spectrum Analyzer

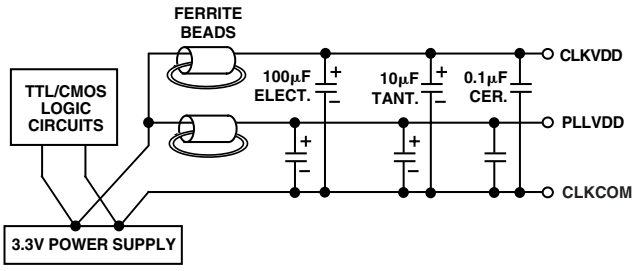


Figure 9. LC Network for Power Filtering

DAC TIMING WITH PLL ACTIVE

As described in Figure 7, in PLL active mode, Port 1 and Port 2 input latches are updated on the rising edge of CLK. On the same rising edge, data previously present in the input Port 2 latch is written to the DAC output latch. The DAC output will update after a short propagation delay (t_{PD}).

Following the rising edge of CLK at a time equal to half of its period, the data in the Port 1 latch will be written to the DAC output latch, again with a corresponding change in the DAC output. Due to the internal PLL, the time at which the data in the Port 1 and Port 2 input latches is written to the DAC latch is independent of the duty cycle of CLK. When using the PLL, the external clock can be operated at any duty cycle that meets the specified input pulsewidth.

On the next rising edge of CLK, the cycle begins again with the two input port latches being updated, and the DAC output latch being updated with the current data in the Port 2 input latch.

PLL DISABLED MODE

When PLLVDD is grounded, the PLL is disabled. An external clock must now drive the CLK inputs at the desired DAC output update rate. The speed and timing of the data present at input Ports 1 and 2 are now dependent on whether or not the AD9753 is interleaving the digital input data or only responding to data on a single port. Figure 10 is a functional block diagram of the AD9753 clock control circuitry with the PLL disabled.

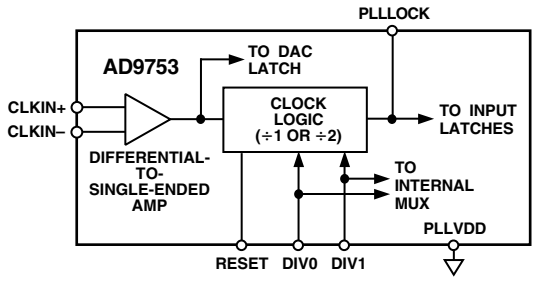


Figure 10. Clock Circuitry with PLL Disabled

DIV0 and DIV1 no longer control the PLL but are used to set the control on the input mux for either interleaving or non-interleaving the input data. The different modes for states of DIV0 and DIV1 are given in Table II.

Table II. Input Mode for DIV0, DIV1 Levels with PLL Disabled

Input Mode	DIV1	DIV0
Interleaved (2×)	0	0
Noninterleaved		
Port 1 Selected	0	1
Port 2 Selected	1	0
Not Allowed	1	1

INTERLEAVED (2×) MODE WITH PLL DISABLED

The relationship between the internal and external clocks in this mode is shown in Figure 11. A clock at the output update data rate (2× the input data rate) must be applied to the CLK inputs. Internal dividers then create the internal 1× clock necessary for the input latches. Although the input latches are updated on the rising edge of the delayed internal 1× clock, the setup-and-hold times given in the Digital Specifications table are with respect to the rising edge of the external 2× clock. With the PLL disabled, a load-dependent delayed version of the 1× clock is present at the PLLLOCK pin. This signal can be used to synchronize the external data.

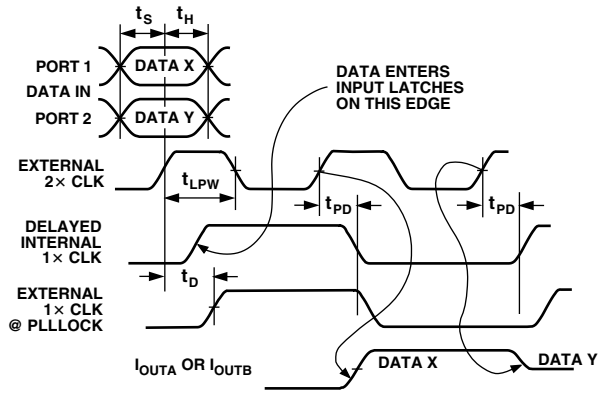


Figure 11. Timing Requirements, Interleaved (2×) Mode with PLL Disabled

Updates to the data at input Ports 1 and 2 should be synchronized to the specific rising edge of the external 2× clock that corresponds to the rising edge of the 1× internal clock, as shown in Figure 11. To ensure synchronization, a Logic 1 must be momentarily applied to the RESET pin. Doing this and returning RESET to Logic 0 brings the 1× clock at PLLLOCK to a Logic 1. On the next rising edge of the 2× clock, the 1× clock will go to Logic 0. On the second rising edge of the 2× clock, the 1× clock (PLLLOCK) will again go to Logic 1, as well as update the data in both of the input latches. The details of this are shown in Figure 12.

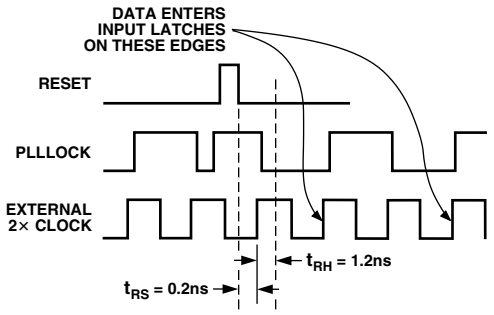


Figure 12. RESET Function Timing with PLL Disabled

For proper synchronization, sufficient delay must be present between the time RESET goes low and the rising edge of the 2× clock. RESET going low must occur either at least t_{RS} ns before the rising edge of the 2× clock, or t_{RH} ns afterwards. In the first case, the immediately occurring CLK rising edge will cause PLLLOCK to go low. In the second case, the next CLK rising edge will toggle PLLLOCK.

NONINTERLEAVED MODE WITH PLL DISABLED

If the data at only one port is required, the AD9753 interface can operate as a simple double buffered latch with no interleaving. On the rising edge of the 1× clock, input latch 1 or 2 is updated with the present input data (depending on the state of DIV0/DIV1). On the next rising edge, the DAC latch is updated and a time t_{PD} later, the DAC output reflects this change. Figure 13 represents the AD9753 timing in this mode.

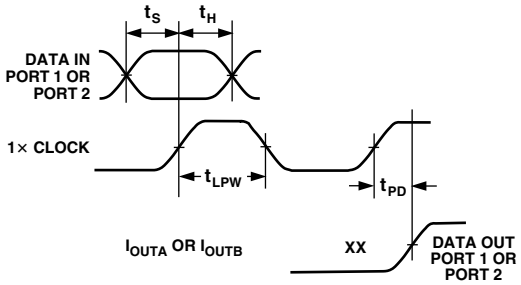


Figure 13. Timing Requirements, Noninterleaved Mode with PLL Disabled

DAC TRANSFER FUNCTION

The AD9753 provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 4095), while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as

$$I_{OUTA} = (DAC\ CODE/4096) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (4095 - DAC\ CODE)/4096 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 4095 (i.e., decimal representation).

As mentioned previously, I_{OUTFS} is a function of the reference current, I_{REF}, which is nominally set by a reference voltage, V_{REFIO}, and an external resistor R_{SET}. It can be expressed as

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note that R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note that the full-scale values of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, $I_{OUTB,}$ and I_{REF}, V_{DIFF} can be expressed as

$$V_{DIFF} = \{(2\ DAC\ CODE - 4095)/4096\} \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9753 differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion, and dc offsets. Second, the differential code-dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9753 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship, as shown in Equation 8.

ANALOG OUTPUTS

The AD9753 produces two complementary current outputs, I_{OUTA} and I_{OUTB}, that may be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described by Equations 5 through 8 in the DAC Transfer Function section. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB}, can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9753 is optimum and specified using a differential transformer-coupled output in which the voltage swing at I_{OUTA} and I_{OUTB} is limited to ±0.5 V. If a single-ended unipolar output is desirable, I_{OUTA} should be selected as the output, with I_{OUTB} grounded.

The distortion and noise performance of the AD9753 can be enhanced when it is configured for differential operation. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (i.e., assuming no source termination). Since the output currents of I_{OUTA} and I_{OUTB} are complementary, they become additive when processed differentially. A properly selected transformer will allow the AD9753 to provide the required power and voltage levels to different loads. Refer to the Applying the AD9753 Output Configurations section for examples of various output configurations.

The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 kΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground via an I–V op amp configuration will result in the optimum dc linearity. Note that the INL/DNL specifications for the AD9753 are measured with I_{OUTA} and I_{OUTB} maintained at virtual ground via an op amp.

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9753.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed 0.5 V. Applications requiring the AD9753's output (i.e., V_{OUTA} and/or V_{OUTB}) to extend its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range will adversely affect the AD9753's linearity performance and subsequently degrade its distortion performance.

DIGITAL INPUTS

The AD9753's digital inputs consist of two channels of 14 data input pins each and a pair of differential clock input pins. The 12-bit parallel data inputs follow standard straight binary coding where DB13 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. With the PLL active or disabled, the DAC output is updated twice for every input latch rising edge, as shown in Figures 7 and 11. The AD9753 is designed to support an input data rate as high as 150 MSPS, giving a DAC output update rate of 300 MSPS. The setup-and-hold times can also be varied within the clock cycle as long as the specified minimum times are met. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (*DVDD*) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9753 is capable of operating over a digital supply range of 3.0 V to 3.6 V. As a result, the digital inputs can also accommodate TTL levels when *DVDD* is set to accommodate the maximum high level voltage of the TTL drivers V_{OH}(max). A *DVDD* of 3.0 V to 3.6 V typically ensures proper compatibility with most TTL logic families. Figure 14 shows the equivalent digital input circuit for the data and clock inputs.

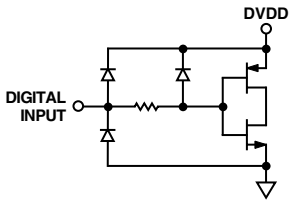


Figure 14. Equivalent Digital Input

The AD9753 features a flexible differential clock input operating from separate supplies (i.e., CLKVDD, CLKCOM) to achieve optimum jitter performance. The two clock inputs, CLK+ and CLK–, can be driven from a single-ended or differential clock source. For single-ended operation, CLK+ should be driven by a logic source while CLK– should be set to the threshold voltage of the logic source. This can be done via a resistor divider/capacitor network, as shown in Figure 15a. For differential operation, both CLK+ and CLK– should be biased to CLKVDD/2 via a resistor divider network, as shown in Figure 15b.

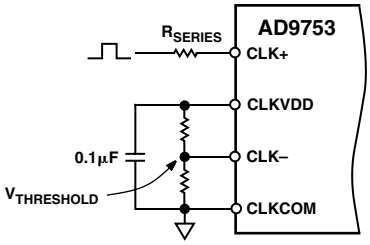


Figure 15a. Single-Ended Clock Interface

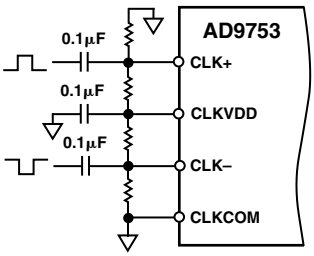


Figure 15b. Differential Clock Interface

Because the output of the AD9753 can be updated at up to 300 MSPS, the quality of the clock and data input signals is important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum setup-and-hold times of the AD9753 as well as its required min/max input logic level thresholds.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. Inserting a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9753 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs.

The external clock driver circuitry should provide the AD9753 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

Note that the clock input could also be driven via a sine wave that is centered around the digital threshold (i.e., DVDD/2) and meets the min/max logic threshold. This typically results in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Also, at higher sampling rates, the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and, subsequently, cut into the required data setup-and-hold times.

INPUT CLOCK AND DATA TIMING RELATIONSHIP

SNR in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9753 is rising edge triggered, and so exhibits SNR sensitivity when the data transition is close to this edge. In general, the goal when applying the AD9753 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 16 shows the relationship of SNR to clock placement with different sample rates. Note that the setup-and-hold times implied in Figure 16 appear to violate the maximums stated in the Digital Specifications of this data sheet. The variation in Figure 16 is due to the skew present between data bits inherent in the digital data generator used to perform these tests. Figure 16 is presented to show the effects of violating setup-and-hold times and to show the insensitivity of the AD9753 to clock placement when data transitions fall outside of the so-called "bad window." The setup-and-hold times stated in the Digital Specifications table were measured on a bit-by-bit basis, therefore eliminating the skew present in the digital data generator. At higher data rates, it becomes very important to account for the skew in the input digital data when defining timing specifications.

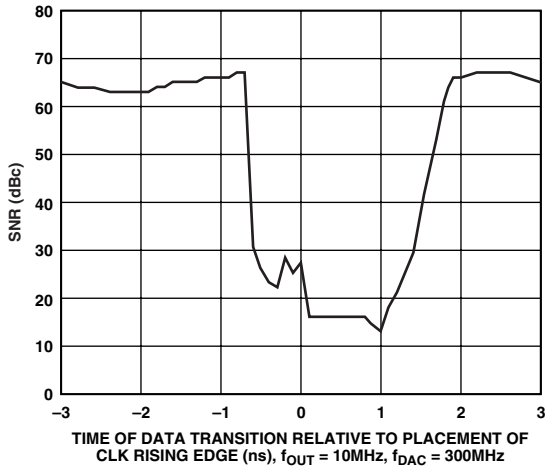


Figure 16. SNR vs. Time of Data Transition Relative to Clock Rising Edge

POWER DISSIPATION

The power dissipation, P_D, of the AD9753 is dependent on several factors that include the power supply voltages (AVDD and DVDD), the full-scale current output I_{OUTFS}, the update rate f_{CLOCK}, and the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 17,

and is insensitive to f_{CLOCK}. Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply, DVDD. Figure 18 shows I_{DVDD} as a function of the ratio (f_{OUT}/f_{DAC}) for various update rates. In addition, Figure 19 shows the effect that the speed of f_{DAC} has on the PLLVDD current, given the PLL divider ratio.

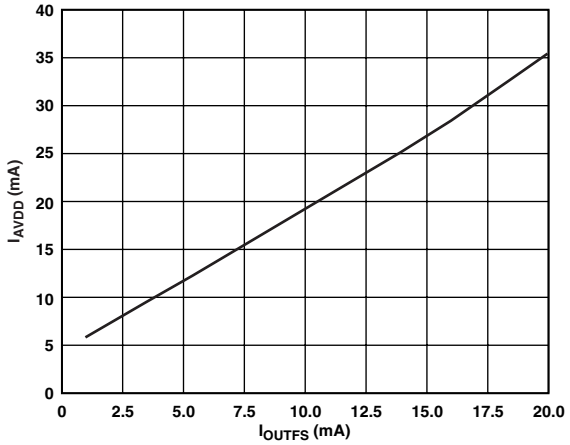


Figure 17. I_{AVDD} vs. I_{OUTFS}

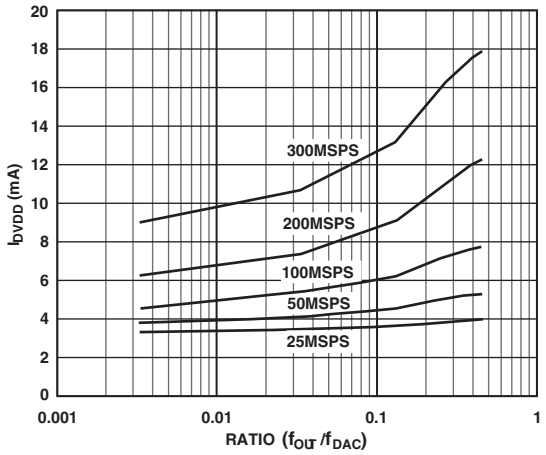


Figure 18. I_{DVDD} vs. f_{OUT}/f_{DAC} Ratio

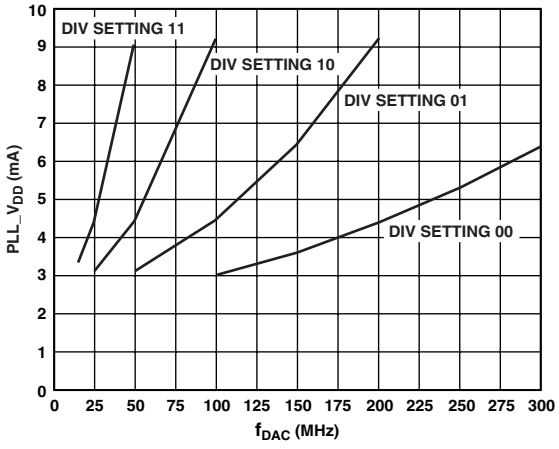


Figure 19. PLLVDD vs. f_{DAC}

APPLYING THE AD9753 OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9753. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level shifting, within the bandwidth of the chosen op amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc-coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note that I_{OUTA} provides slightly better performance than I_{OUTB}.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion, as shown in Figure 20. A differentially-coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's pass band. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. When I_{OUTA} and I_{OUTB} are terminated to ground with 50 Ω, this configuration provides 0 dBm power to a 50 Ω load on the secondary with a DAC full-scale current of 20 mA. A 2:1 transformer, such as the Coilcraft WB2040-PC, can also be used in a configuration in which I_{OUTA} and I_{OUTB} are terminated to ground with 75 Ω. This configuration improves load matching and increases power to 2 dBm into a 50 Ω load on the secondary. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

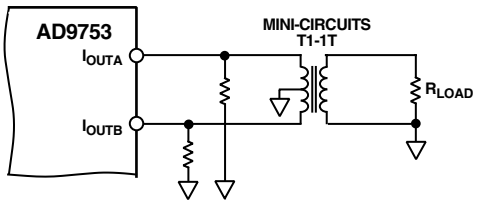


Figure 20. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9753. A differential resistor, R_{DIFF}, may be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a

passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR.

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion, as shown in Figure 21. The AD9753 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DAC's high slewing output from overloading the op amp's input.

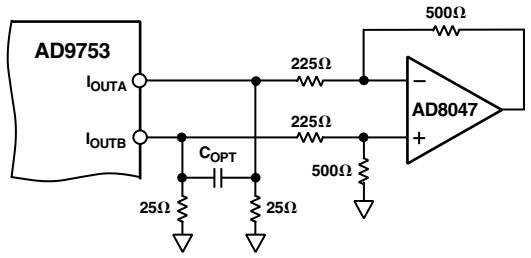


Figure 21. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate from a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9753, while meeting other system level objectives (i.e., cost, power), should be selected. The op amp's differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 22 provides the necessary level-shifting required in a single-supply system. In this case, AVDD, which is the positive analog supply for both the AD9753 and the op amp, is also used to level-shift the differential output of the AD9753 to midsupply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.

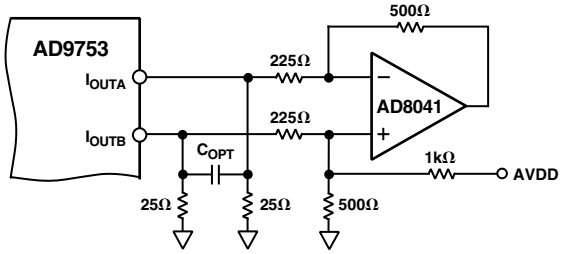


Figure 22. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 23 shows the AD9753 configured to provide a unipolar output range of approximately 0 V to 0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB}. The unused output (I_{OUTA} or I_{OUTB}) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL), as discussed in the Analog Outputs section. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

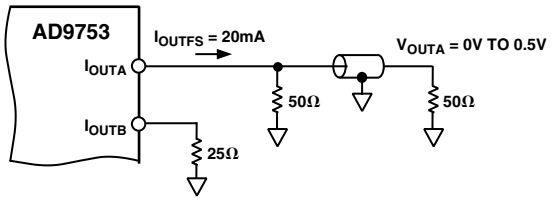


Figure 23. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED BUFFERED VOLTAGE OUTPUT

Figure 24 shows a buffered single-ended output configuration in which the op amp performs an I–V conversion on the AD9753 output current. The op amp maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Outputs section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by the op amp's slewing capabilities. The op amp provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within the op amp's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS}, since the signal current the op amp will be required to sink will subsequently be reduced.

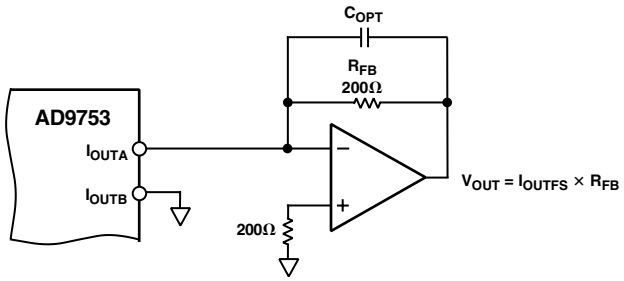


Figure 24. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION

Many applications seek high speed and high performance under less than ideal operating conditions. In these applications, the implementation and construction of the printed circuit board is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as power supply bypassing and grounding, to ensure optimum performance. Figures 34 to 41 illustrate the recommended printed circuit board ground, power, and signal plane layouts that are implemented on the AD9753 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution.

This is referred to as the Power Supply Rejection Ratio. For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full-scale current, I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise will occur over the spectrum from tens of kHz to several MHz. The PSRR versus the frequency of the AD9753 AVDD supply over this frequency range is shown in Figure 25.

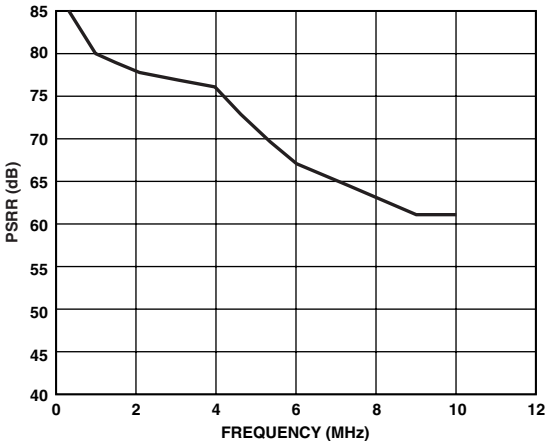


Figure 25. Power Supply Rejection Ratio

Note that the units in Figure 25 are given in units of (amps out/volts in). Noise on the analog power supply has the effect of modulating the internal switches, and therefore the output current. The voltage noise on AVDD will thus be added in a nonlinear manner to the desired I_{OUT}. Due to the relative different size of these switches, PSRR is very code-dependent. This can produce a mixing effect that can modulate low frequency power supply noise to higher frequencies. Worst-case PSRR for either one of the differential DAC outputs will occur when the full-scale current is directed toward that output. As a result, the PSRR measurement in Figure 25 represents a worst-case condition in which the digital inputs remain static and the full-scale output current of 20 mA is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV rms of noise and, for simplicity sake (i.e., ignore harmonics), all of this noise is concentrated at 250 kHz. To calculate how much of this undesired noise will appear as current noise superimposed on the DAC's full-scale current, I_{OUTFS}, one must determine the PSRR in dB using Figure 25 at 250 kHz. To calculate the PSRR for a given R_{LOAD}, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 25 by the scaling factor $20 \times \text{Log}(R_{LOAD})$. For instance, if R_{LOAD} is 50 Ω, the PSRR is reduced by 34 dB, i.e., PSRR of the DAC at 250 kHz, which is 85 dB in Figure 25, becomes 51 dB V_{OUT}/V_{IN}.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9753 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close to the chip as physically possible.

For those applications that require a single 3.3 V supply for both the analog and digital supplies, a clean analog supply may be generated using the circuit shown in Figure 26. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained by using low ESR type electrolytic and tantalum capacitors.

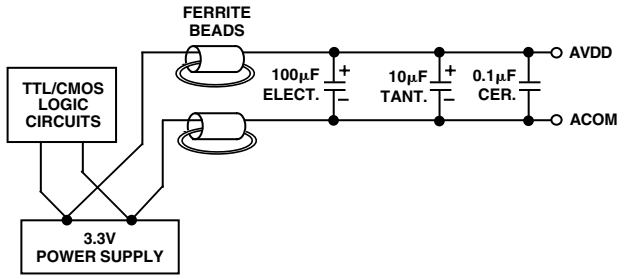


Figure 26. Differential LC Filter for a Single 3.3 V Application

APPLICATIONS

QAM/PSK Synthesis

Quadrature modulation (QAM or PSK) consists of two baseband PAM (Pulse Amplitude Modulated) data channels. Both channels are modulated by a common frequency carrier. However, the carriers for each channel are phase-shifted 90° from each other. This orthogonality allows twice the spectral efficiency (data for a given bandwidth) of digital data transmitted via AM. Receivers can be designed to selectively choose the "in phase" and "quadrature" carriers, and then recombine the data. The recombination of the QAM data can be mapped as points representing digital words in a two dimensional constellation as shown in Figure 27. Each point, or symbol, represents the transmission of multiple bits in one symbol period.

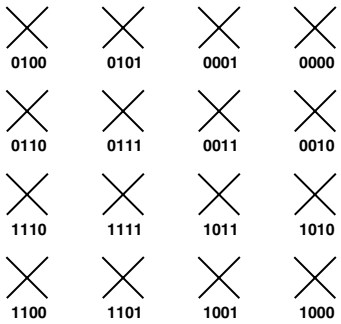


Figure 27. 16 QAM Constellation, Gray Coded (Two 4-Level PAM Signals with Orthogonal Carriers)

Typically, the I and Q data channels are quadrature-modulated in the digital domain. The high data rate of the AD9753 allows extremely wideband (>10 MHz) quadrature carriers to be synthesized. Figure 28 shows an example of a 25 MSymbol/S QAM signal, oversampled by 8 at a data rate of 200 MSPS, modulated onto a 25 MHz carrier and reconstructed using the AD9753. The power in the reconstructed signal is measured to be –11.92 dBm. In the first adjacent band, the power is –76.86 dBm, while in the second adjacent band, the power is –80.96 dBm.

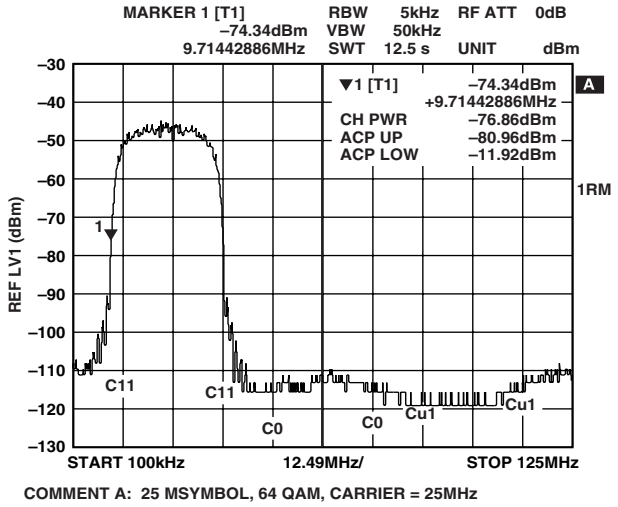


Figure 28. Reconstructed 64-QAM Signal at a 25 MHz IF

A figure of merit for wideband signal synthesis is the ratio of signal power in the transmitted band to the power in an adjacent channel. In Figure 28, the adjacent channel power ratio (ACPR) at the output of the AD9753 is measured to be 65 dB. The limitation on making a measurement of this type is often not the DAC but the noise inherent in creating the digital data record using computer tools. To find how much this is limiting the perceived DAC performance, the signal amplitude can be reduced, as is shown in Figure 29. The noise contributed by the DAC will remain constant as the signal amplitude is reduced. When the signal amplitude is reduced to the level where the noise floor drops below that of the spectrum analyzer, the ACPR will fall off at the same rate that the signal level is being reduced. Under the conditions measured in Figure 28, this point occurs in Figure 29 at –10 dBFS. This shows that the data record is actually degrading the measured ACPR by up to 10 dB.

A single-channel active mixer such as the Analog Devices AD8343 can then be used for the hop to the transmit frequency. Figure 30 shows an applications circuit using the AD9753 and the AD8343. The AD8343 is capable of mixing carriers from dc to 2.5 GHz. Figure 31 shows the result of mixing the signal in Figure 28 up to a carrier frequency of 800 MHz. ACPR measured at the output of the AD8343 is shown in Figure 31 to be 59 dB.

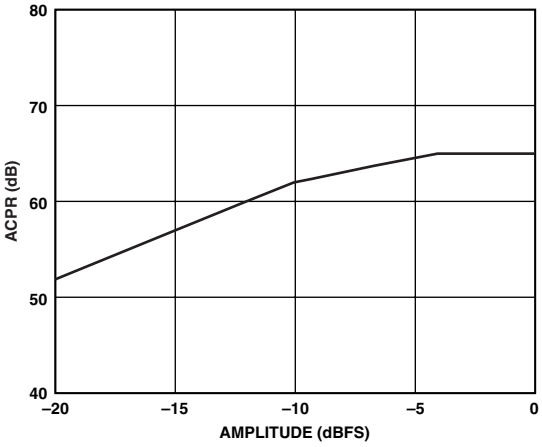


Figure 29. ACPR vs. Amplitude for QAM Carrier

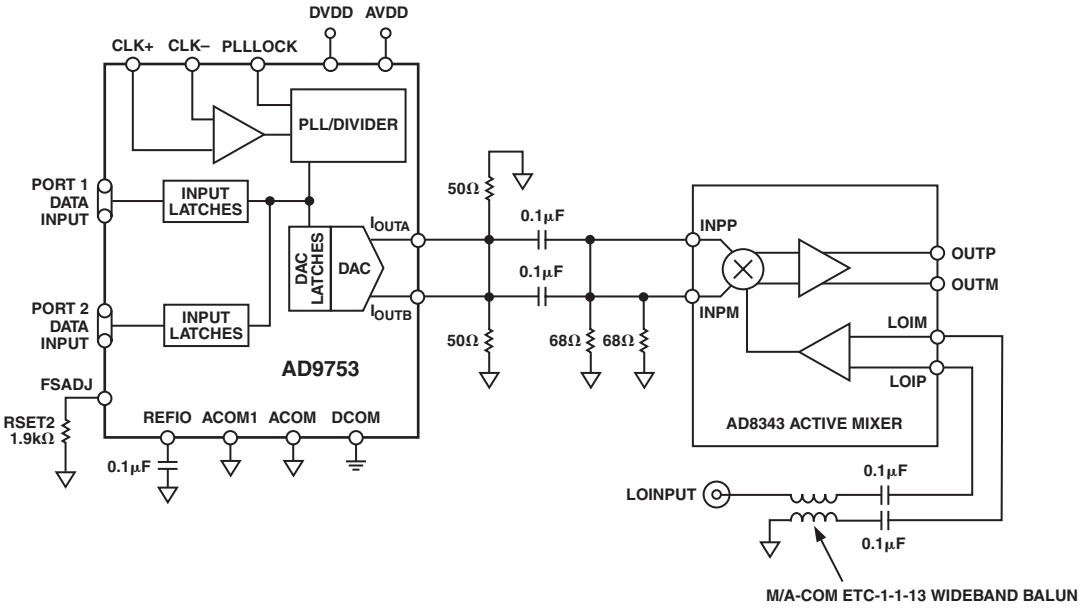


Figure 30. QAM Transmitter Architecture Using AD9753 and AD8343 Active Mixer

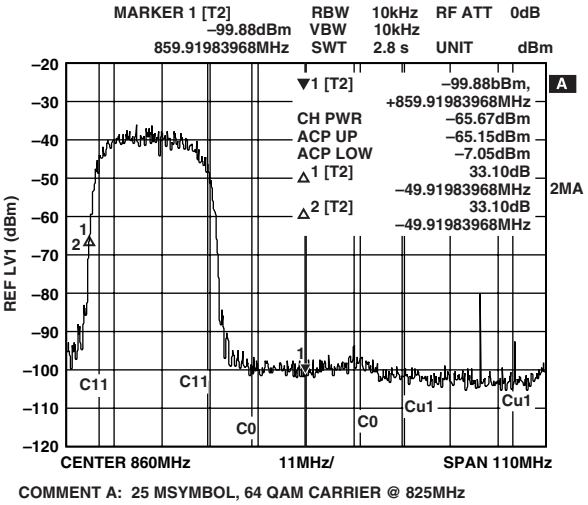


Figure 31. Signal of Figure 28 Mixed to Carrier Frequency of 800 MHz

Effects of Noise and Distortion on Bit Error Rate (BER)

Textbook analyses of Bit Error Rate (BER) performance are generally stated in terms of E (energy in watts-per-symbol or watts-per-bit) and NO (spectral noise density in watts/Hz). For QAM signals, this performance is shown graphically in Figure 32. M represents the number of levels in each quadrature PAM signal (i.e., M = 8 for 64 QAM, M = 16 for 256 QAM). Figure 32 implies gray coding in the QAM constellation, as well as the use of matched filters at the receiver, which is typical. The horizontal axis of Figure 32 can be converted to units of energy/symbol by adding to the horizontal axis 10 log of the number of bits in the desired curve. For instance, to achieve a BER of 1e-6 with 64 QAM, an energy per bit of 20 dB is necessary. To calculate energy per symbol, we add 10 log(6), or 7.8 dB. 64 QAM with a BER of 1e-6 (assuming no source or channel coding) can therefore theoretically be achieved with an energy/symbol-to-noise (E/NO) ratio of 27.8 dB. Due to the loss and interferers inherent in the wireless path, this signal-to-noise ratio must be realized at the receiver to achieve the given bit error rate.

Distortion effects on BER are much more difficult to determine accurately. Most often in simulation, the energies of the strongest distortion components are root-sum-squared with the noise, and the result is treated as if it were all noise. That being said, if the example above of 64 QAM with the BER of 1e-6, using the E/NO ratio is much greater than the worst-case SFDR, the noise will dominate the BER calculation.

The AD9753 has a worst-case in-band SFDR of 47 dB at the upper end of its frequency spectrum (see TPCs 4 and 7). When used to synthesize high level QAM signals as described above, noise, as opposed to distortion, will dominate its performance in these applications.

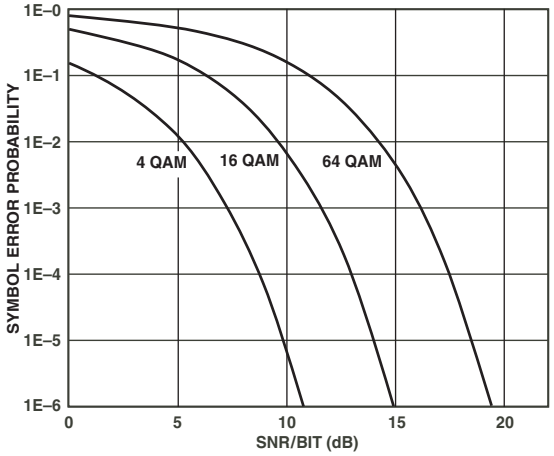


Figure 32. Probability of a Symbol Error for QAM

Pseudo Zero Stuffing/IF Mode

The excellent dynamic range of the AD9753 allows its use in applications where synthesis of multiple carriers is desired. In addition, the AD9753 can be used in a pseudo zero stuffing mode that improves dynamic range at IF frequencies. In this mode, data from the two input channels is interleaved to the DAC, which is running at twice the speed of either of the input ports. However, the data at Port 2 is held constant at midscale. The effect of this is shown in Figure 33. The IF signal is the image, with respect to the input data rate, of the fundamental. Normally, the sinx/x response of the DAC will attenuate this image. Zero stuffing improves the pass-band flatness so that the image amplitude is closer to that of the fundamental signal. Zero stuffing can be an especially useful technique in the synthesis of IF signals.

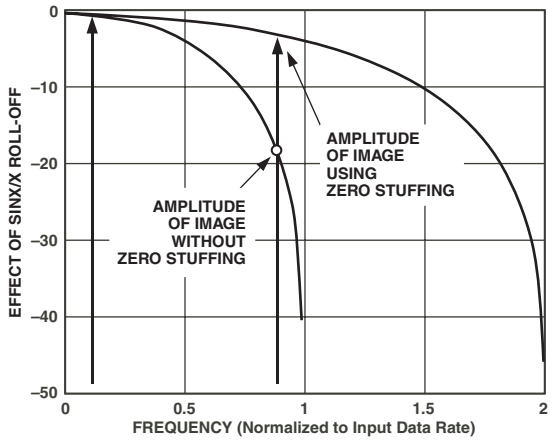


Figure 33. Effects of Pseudo Zero Stuffing on Spectrum of AD9753

EVALUATION BOARD

The AD9753-EB is an evaluation board for the AD9753 TxDAC. Careful attention to layout and circuit design, combined with prototyping area, allows the user to easily and effectively evaluate the AD9753 in different modes of operation.

Referring to Figures 34 and 35, the AD9753's performance can be evaluated differentially or single-ended either using a transformer, or directly coupling the output. To evaluate the output differentially using the transformer, it is recommended that either the Mini-Circuits T1-1T (through-hole) or the Coilcraft TTWB-1-B (SMT) be placed in the position of T1 on the evaluation board. To evaluate the output either single-ended or direct-coupled, remove the transformer and bridge either BL1 or BL2.

The digital data to the AD9753 comes from two ribbon cables that interface to the 40-lead IDC connectors P1 and P2. Proper termination or voltage scaling can be accomplished by installing the resistor pack networks RN1–RN12. RN1, 4, 7, and 10 are 22 Ω DIP resistor packs and should be installed as they help reduce the digital edge rates and therefore peak current on the inputs.

A single-ended clock can be applied via J3. By setting the SE/DIFF labeled jumpers J2, 3, 4, and 6, the input clock can be directed to the CLK+/CLK– inputs of the AD9753 in either a single-ended or differential manner. If a differentially applied clock is desired, a Mini-Circuits T1-1T transformer should be used in the position of T2. Note that with a single-ended square wave clock input, T2 must be removed. A clock can also be applied via the ribbon cable on Port 1 (P1), Pin 33. By inserting the EDGE jumper (JP1), this clock will be applied to the CLK+ input of the AD9753. JP3 should be set in its SE position in this application to bias CLK– to 1/2 the supply voltage.

The AD9753's PLL clock multiplier can be enabled by inserting JP7 in the IN position. As described in the Typical Performance Characteristics and Functional Description sections, with the PLL enabled, a clock at 1/2 the output data rate should be applied as described in the last paragraph. The PLL takes care of the internal 2× frequency multiplication and all internal timing requirements. In this application, the PLLLOCK output indicates when lock is achieved on the PLL. With the PLL enabled, the DIV0 and DIV1 jumpers (JP8 and JP9) provide the PLL divider ratio as described in Table I.

The PLL is disabled when JP7 is in the EX setting. In this mode, a clock at the speed of the output data rate must be applied to the clock inputs. Internally, the clock is divided by 2. For data synchronization, a 1× clock is provided on the PLLLOCK pin in this application. Care should be taken to read the timing requirements described earlier in the data sheet for optimum performance. With the PLL disabled, the DIV0 and DIV1 jumpers define the mode (interleaved, noninterleaved) as described in Table II.

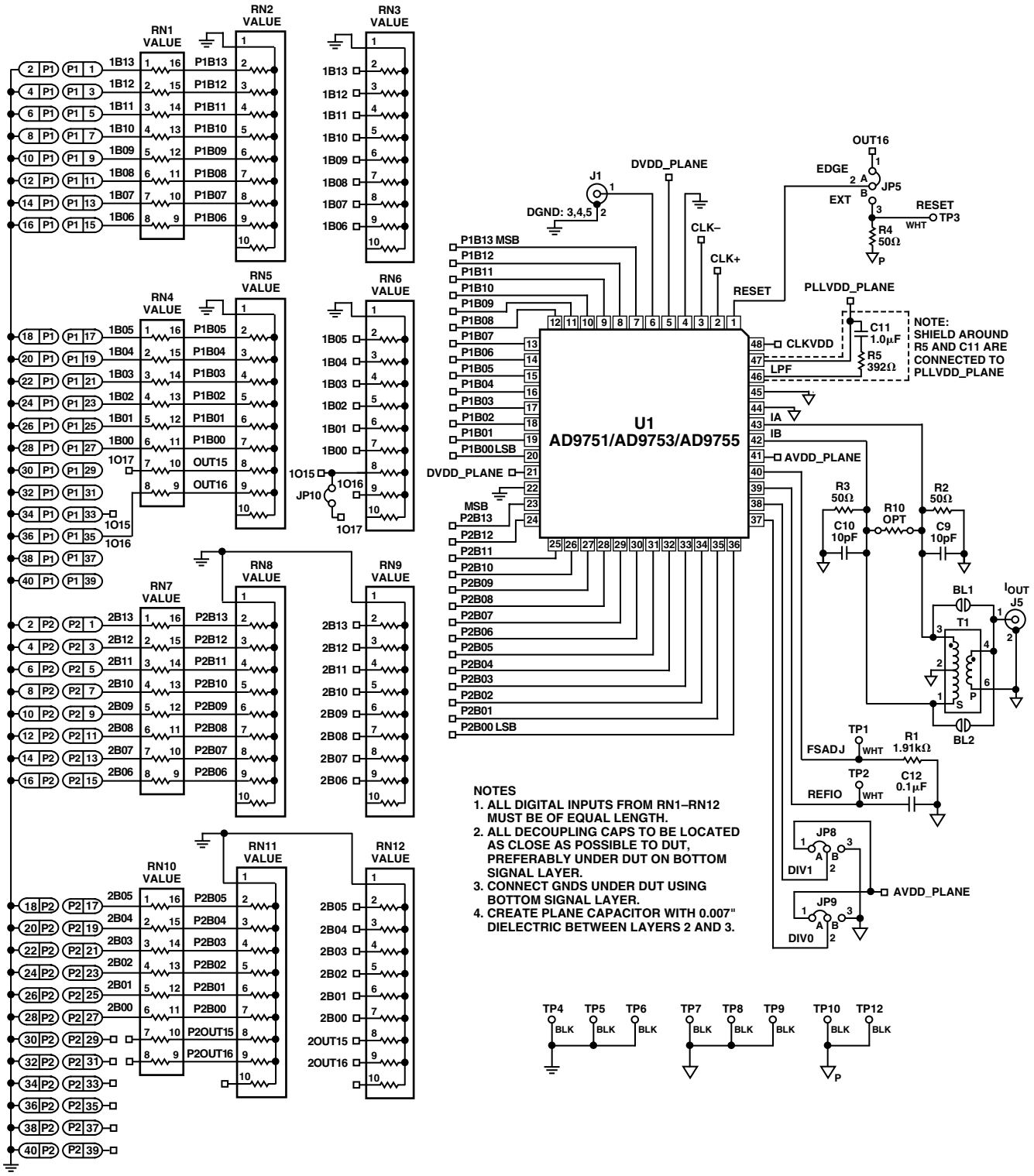


Figure 34. Evaluation Board Circuitry

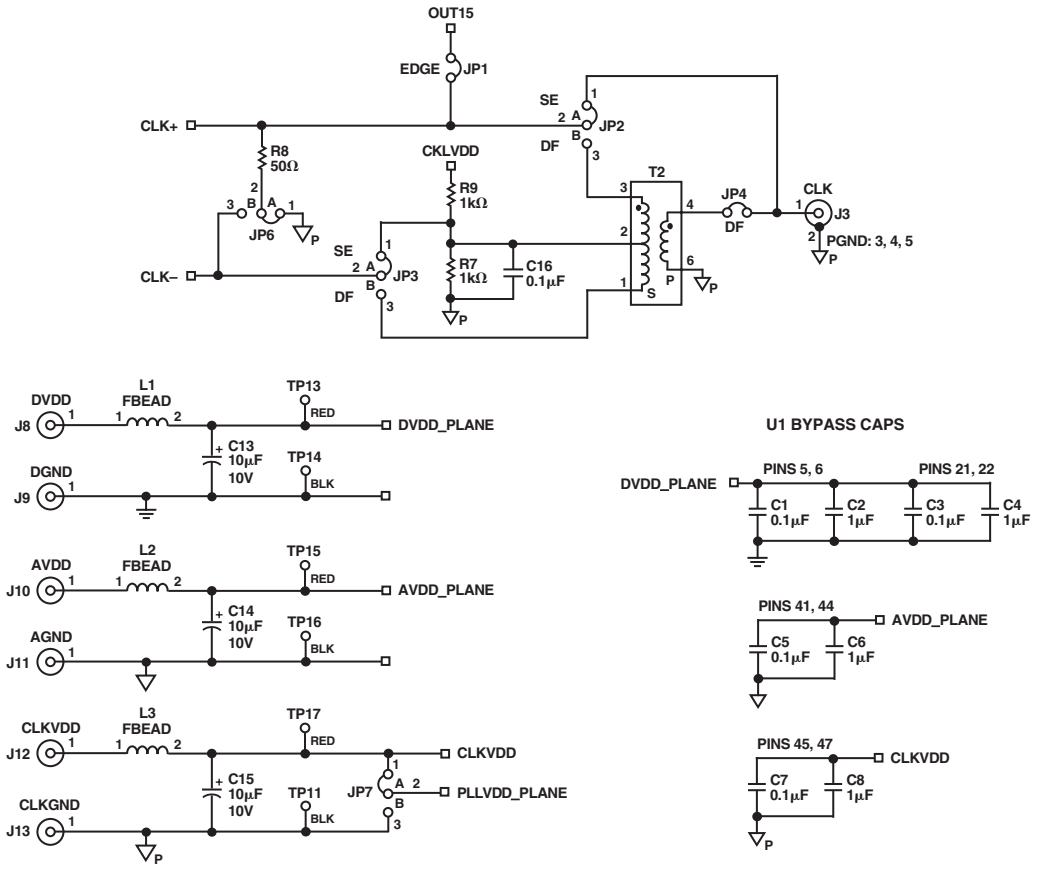


Figure 35. Evaluation Board Clock Circuitry

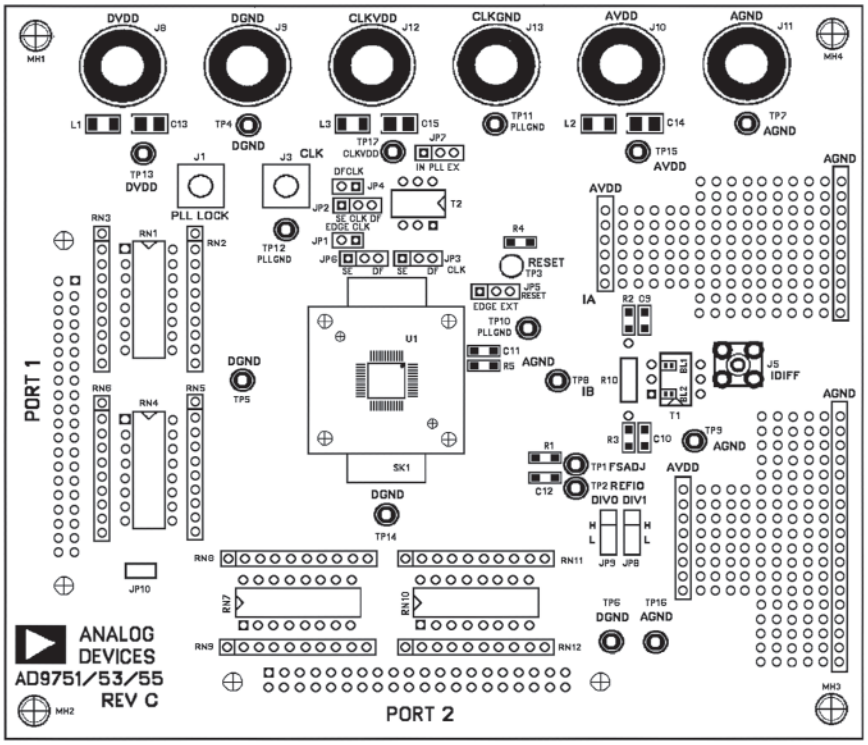


Figure 36. Evaluation Board, Assembly—Top

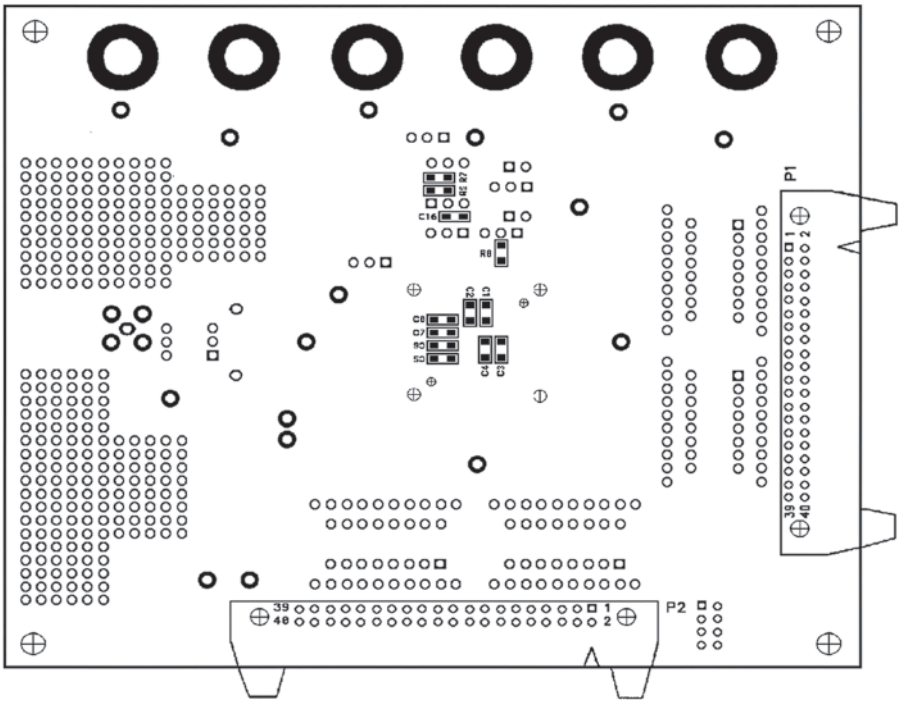


Figure 37. Evaluation Board, Assembly—Bottom

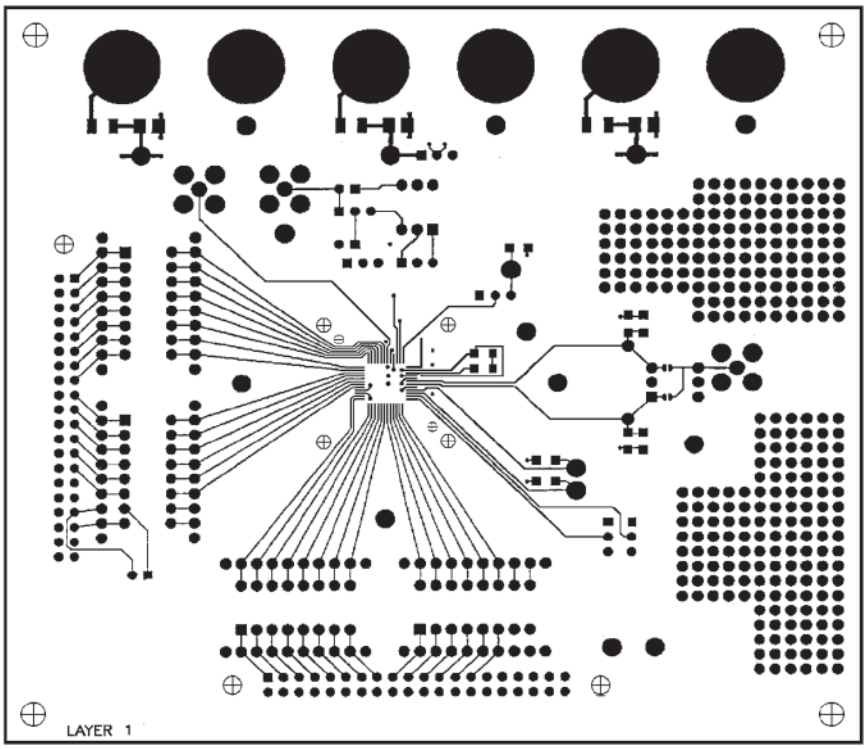


Figure 38. Evaluation Board, Top Layer

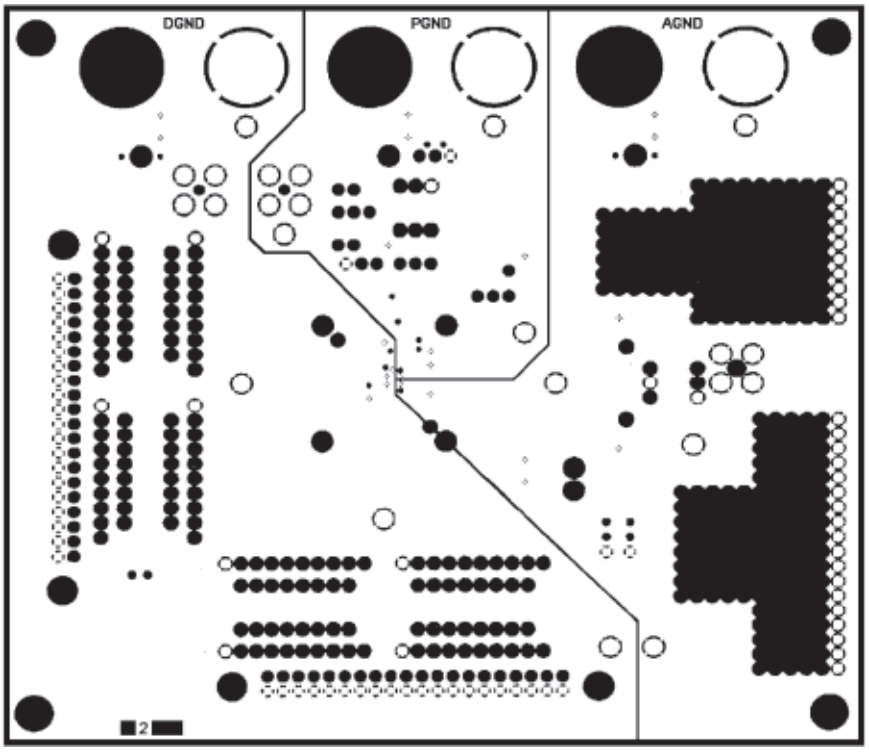


Figure 39. Evaluation Board, Layer 2, Ground Plane

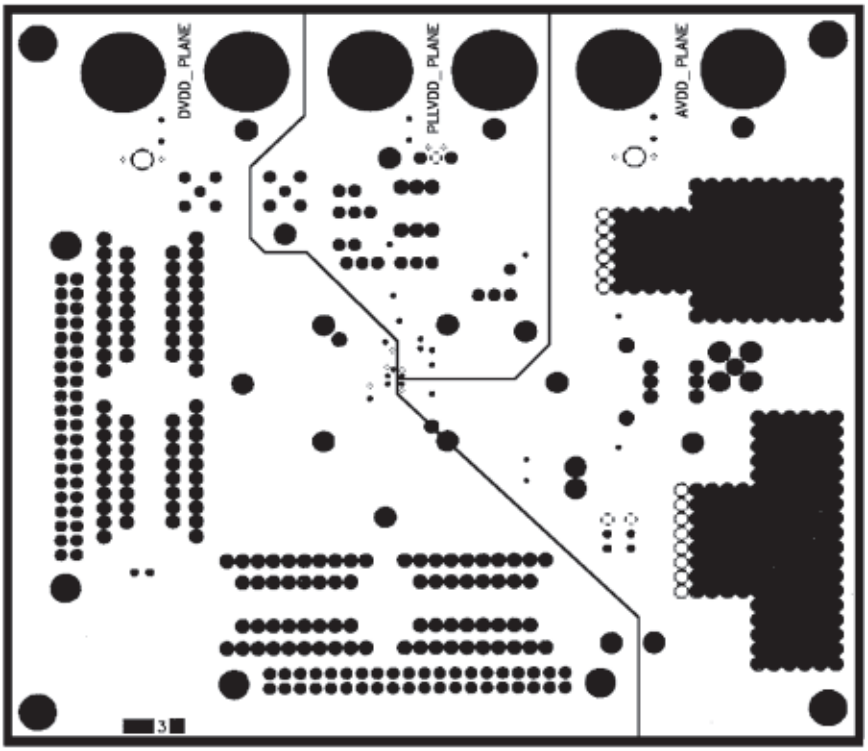


Figure 40. Evaluation Board, Layer 3, Power Plane

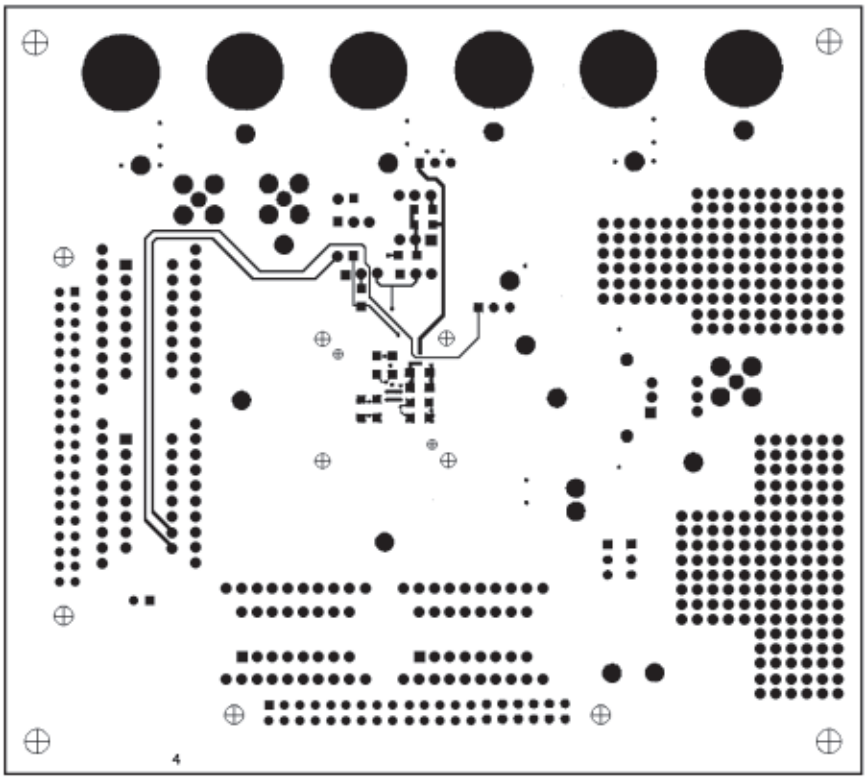
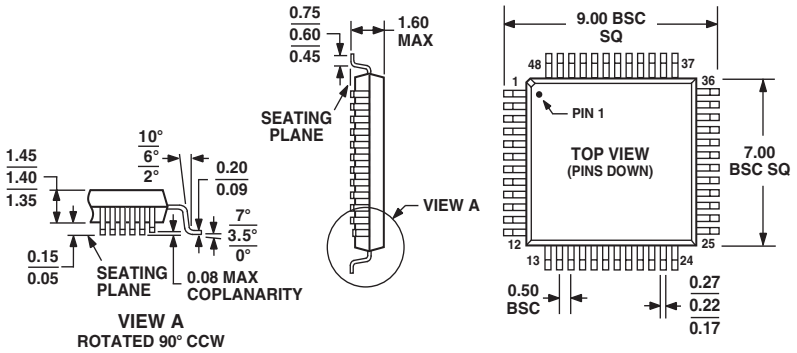


Figure 41. Evaluation Board, Bottom Layer

OUTLINE DIMENSIONS

48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Revision History

Location	Page
9/03—Data Sheet changed from REV. A to REV. B.	
Changes to GENERAL DESCRIPTION	1
Changes to PRODUCT HIGHLIGHTS	1
Changes to DIGITAL SPECIFICATIONS	4
Changes to ORDERING GUIDE	5
Changes to Figure 2	7
Changes to Figure 3	10
Changes to FUNCTIONAL DESCRIPTION section	10
Changes to Figure 6	11
Changes to Figure 9	12
Changes to Figure DIGITAL INPUTS section	14
Changes to Figure 34	22
1/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to DIGITAL SPECIFICATIONS	4
Changes to Figure 1	5
Changes to Figure 2	7
Changes to Figure 11	13
Updated OUTLINE DIMENSIONS	27

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