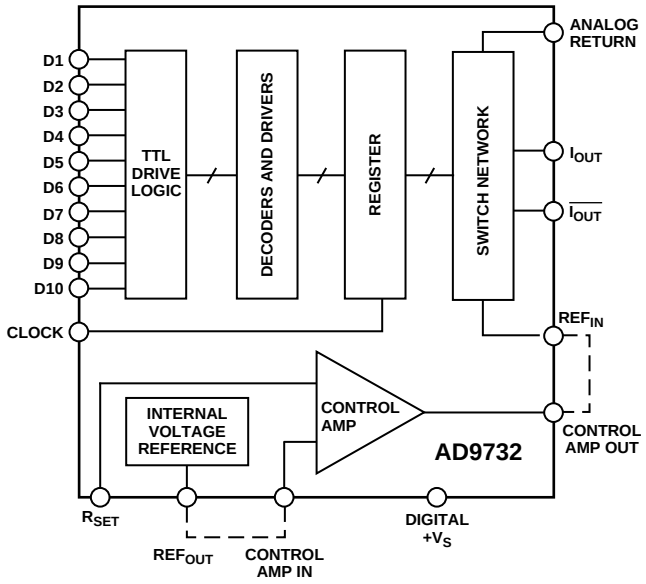
10-Bit, 200 MSPS D/A Converter

AD9732

FEATURES
200 MSPS Throughput Rate
3.3 V PECL Digital Input
65 dB SFDR @ 2 MHz A_{OUT}, 200 MSPS/54 dB @ 40 MHz A_{OUT}, 200 MSPS
Low Power: 305 mW
Fast Settling: 5 ns to 1/2 LSB
Low Glitch Energy: 6 pVs
Internal Reference
28-Lead SSOP Packaging

APPLICATIONS
Digital Communications
Direct Digital Synthesis
Waveform Reconstruction
High Speed Imaging

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9732 is a 10-bit, 200 MSPS, bipolar D/A converter that is optimized to provide high dynamic performance, yet offers lower power dissipation and a more economical price than previous high speed DAC solutions. The AD9732 was primarily designed for demanding communications systems applications where maximum spurious-free dynamic range (SFDR) is required at high throughput rates. The proliferation of digital communications into base station and high volume subscriber-end markets has created a demand for high performance bipolar DACs delivered at CMOS associated levels of power dissipation and cost. The AD9732 is the answer to that demand.

Optimized for direct digital synthesis (DDS) and digital modulator waveform reconstruction, the AD9732 provides >50 dB of wideband harmonic suppression over the dc to 80 MHz analog output bandwidth. This signal bandwidth addresses the transmit spectrum in many of the emerging digital communications applications where signal purity is critical. Narrowband (±1 MHz window), the AD9732 provides an SFDR of greater than 75 dB. This level of wideband and narrowband ac performance, coupled with its 200 MSPS throughput rate, enables the AD9732 to present outstanding value in the high speed DAC function.

The AD9732 is packaged in a 28-lead SSOP and is specified to operate over the extended industrial temperature range of –40°C to +85°C. Digital inputs and clock are positive-ECL compatible.

REV. A

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AD9732–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V, ENCODE = 125 MSPS, R_{SET} = 1.95 kΩ (for 20 mA I_{OUT}) unless otherwise noted)

Parameter	Temp	Test Level	AD9732BRS Min	Typ	Max	Units
THROUGHPUT RATE	+25°C	IV	165	200		MHz
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.25	1	LSB
	Full	VI		0.36	1	LSB
Integral Nonlinearity	+25°C	I		0.6	1.5	LSB
	Full	VI		0.7	1.5	LSB
INITIAL OFFSET ERROR						
Zero-Scale Offset Error	+25°C	I		35	70	µA
	Full	VI		40	100	µA
Full-Scale Gain Error[1]	+25°C	I		2.5	5	% FS
	Full	VI		2.5	5	% FS
Offset Drift Coefficient		V		0.04		µA/°C
REFERENCE/CONTROL AMP						
Internal Reference Voltage[2]	+25°C	I	3.65	3.75	3.85	V
Internal Reference Voltage Drift	Full	IV		150		µV/°C
Internal Reference Output Current[3]	Full	VI	–50		+500	µA
Amplifier Input Impedance	+25°C	I		50		kΩ
Amplifier Bandwidth	+25°C	I		2.5		MHz
REFERENCE INPUT[4]						
Reference Input Impedance	+25°C	V		4.6		kΩ
Reference Multiplying Bandwidth[5]	+25°C	V		75		MHz
OUTPUT PERFORMANCE						
Output Current[4, 6]	Full	V		20		mA
Output Compliance	Full	IV	2		5.75	V
Output Resistance	+25°C	V		240		Ω
Output Capacitance	+25°C	V		5		pF
Voltage Settling Time to 1/2 LSB (t_{ST})[7]	+25°C	V		4.75		ns
Propagation Delay (t_{PD})[8]	+25°C	V		2.7		ns
Glitch Impulse[9]	Full	V		5.9		pVs
Output Slew Rate[10]	Full	V		450		V/µs
Output Rise Time[10]	Full	V		1		ns
Output Fall Time[10]	Full	V		1		ns
DIGITAL INPUTS						
Logic “1” Voltage	Full	VI	2.4			V
Logic “0” Voltage	Full	VI			1.6	V
Logic “1” Current	+25°C	I		1.7	10	µA
Logic “0” Current	+25°C	I	–1	0.01	1	µA
Input Capacitance	Full	V		2		pF
Minimum Data Setup Time (t_S)[11]	+25°C	IV		0.7	1.5	ns
	Full	IV		1	1.5	ns
Minimum Data Hold Time (t_H)[12]	+25°C	IV		0.7	1.5	ns
	Full	IV		1	1.5	ns
Clock Pulsewidth Low (pw_{MIN})	+25°C	IV	2			ns
Clock Pulsewidth High (pw_{MAX})	+25°C	IV	2			ns
POWER SUPPLY[13]						
Digital +V Supply Current	+25°C	I	15	25	35	mA
	Full	VI	10		40	mA
Analog +V Supply Current	+25°C	I	10	20	30	mA
	Full	VI	10		30	mA
Power Dissipation[14]	+25°C	V		305		mW
	Full	V		350		mW
Power Supply Rejection Ratio (PSRR)	+25°C	V		200		µA/V

Parameter	Temp	Test Level	AD9732BRS Min	Typ	Max	Units
SFDR PERFORMANCE (Wideband)[15]						
2 MHz A_{OUT}	+25°C	V		66		dB
10 MHz A_{OUT}	+25°C	V		63		dB
20 MHz A_{OUT}	+25°C	V		57		dB
40 MHz A_{OUT}	+25°C	V		52		dB
2 MHz A_{OUT} (Clock = 165 MHz)	+25°C	V		63		dB
10 MHz A_{OUT} (Clock = 165 MHz)	+25°C	V		62		dB
20 MHz A_{OUT} (Clock = 165 MHz)	+25°C	V		56		dB
40 MHz A_{OUT} (Clock = 165 MHz)	+25°C	V		51		dB
65 MHz A_{OUT} (Clock = 165 MHz)	+25°C	V		48		dB
65 MHz A_{OUT} (Clock = 200 MHz)	+25°C	V		45		dB
80 MHz A_{OUT} (Clock = 200 MHz)	+25°C	V		43		dB
SFDR PERFORMANCE (Narrowband)[15]						
2 MHz; 2 MHz Span	+25°C	V		77		dB
25 MHz; 2 MHz Span	+25°C	V		65		dB
10 MHz; 5 MHz Span (Clock = 200 MHz)	+25°C	V		70		dB
INTERMODULATION DISTORTION[16]						
F1 = 800 kHz, F2 = 900 kHz to Nyquist	+25°C	V		69		dB
F1 = 800 kHz, F2 = 900 kHz, Narrowband (2 MHz)	+25°C	V		61		dB

NOTES

[1]Measured as an error in ratio of full-scale current to current through R_{SET} (640 μA nominal); ratio is nominally 32. DAC load is virtual ground.

[2]Internal reference voltage is tested under load conditions specified in Internal Reference Output Current specification.

[3]Internal reference output current defines load conditions applied during Internal Reference Voltage test.

[4]Full-scale current variations among devices are higher when driving REFERENCE IN directly.

[5]Frequency at which a 3 dB change in output of DAC is observed; R_L = 50 Ω; 100 mV modulation at midscale.

[6]Based on I_{FS} = 32 ([CONTROL AMP IN – $(+V_S)$]/R_{SET}) when using internal control amplifier. DAC load is virtual ground.

[7]Measured as voltage settling at midscale transition to 0.1%; R_L = 50 Ω.

[8]Measured from 50% point of rising edge of CLOCK signal to 1/2 LSB change in output signal.

[9]Peak glitch impulse is measured as the largest area under a single positive or negative transient.

[10]Measured with R_L = 50 Ω and DAC operating in latched mode.

[11]Data must remain stable for a specified time prior to rising edge of CLOCK.

[12]Data must remain stable for a specified time after rising edge of CLOCK.

[13]Supply voltages should remain stable with ±5% for nominal operation.

[14]Power dissipation calculation includes current through a 50 Ω load.

[15]SFDR is defined as the difference in signal energy between the full-scale fundamental signal and worst case spurious frequencies in the output spectrum window. The frequency span dc to Nyquist unless otherwise noted.

[16]Intermodulation distortion is the measure of the sum and difference products produced when a two-tone input is driven into the DAC. The distortion products created will manifest themselves at sum and difference frequencies of the two tones.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range.

ORDERING GUIDE

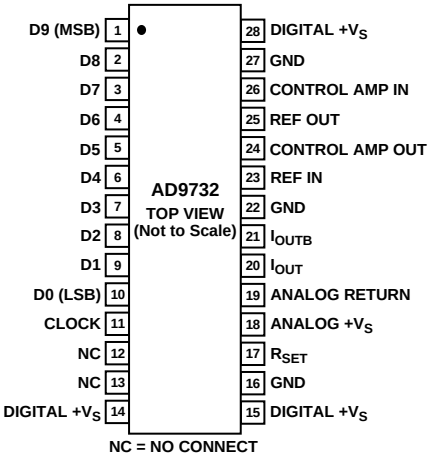
Model	Temperature Range	Package Description	Package Option
AD9732BRS	–40°C to +85°C	28-Lead Small Outline (SSOP)	RS-28
AD9732/PCB	+25°C	Evaluation Board	

ABSOLUTE MAXIMUM RATINGS*

Analog Output . . . . . $+V_S$
$+V_S$ . . . . . +6 V
Digital Inputs . . . . . –0.7 V to $+V_S$
Analog Output Current . . . . . 30 mA
Control Amplifier Input Voltage Range . . . . . 0 V to $+V_S$
Reference Input Voltage Range . . . . . 0 V to $+V_S$
Internal Reference Output Current . . . . . 500 μA
Control Amplifier Output Current . . . . . ±2.5 mA
Operating Temperature . . . . . –40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Lead Temperature (10 sec) Soldering . . . . . +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

PIN CONFIGURATION



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Pin Number	Name	Function
1	D9 (MSB)	Most significant data bit of digital input word.
2–9	D8–D1	Eight bits of 10-bit digital input word.
10	D0 (LSB)	Least significant data bit of digital input word.
11	CLOCK	TTL-compatible edge-triggered latch enable signal for on-board registers.
12, 13	NC	No internal connection to this pin. Recommend tie to ground.
14, 15, 28	DIGITAL $+V_S$	+5 V supply voltage for digital circuitry.
16, 22, 27	GND	Converter Ground.
18	ANALOG $+V_S$	+5 V supply voltage for analog circuitry.
17	R_{SET}	Connection for external reference set resistor; nominal 1.96 kΩ. Full-scale output current = 32 [Control Amp + V_S] (Reset).
19	ANALOG RETURN	Analog Return. This point and the reference side of the DAC load resistors should be connected to the same potential (Analog $+V_S$).
20	I_{OUT}	Analog current output; full-scale current occurs with a digital word input of all "1s" with external load resistor, output voltage = I_{OUT} ($R_{LOAD} \| R_{INTERNAL}$). $R_{INTERNAL}$ is nominally 240 Ω.
21	I_{OUTB}	Complementary analog current output; full-scale current occurs with a digital word input of all "0s."
23	REF IN	Normally connected to CONTROL AMP OUT (Pin 24). Direct line to DAC current source network. Voltage changes (noise) at this point have a direct effect on the full-scale output current of the DAC. Full-scale current output = 32 (CONTROL AMP IN/ R_{SET}) when using internal amplifier. DAC load is virtual ground.
24	CONTROL AMP OUT	Normally connected to REF IN (Pin 23). Output of internal control amplifier, which provides a reference for the current switch network.
25	REF OUT	Normally connected to CONTROL AMP IN (Pin 26). Internal voltage reference, nominally 3.75 V.
26	CONTROL AMP IN	Normally connected to REF OUT (Pin 25) if not connected to external reference.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9732 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



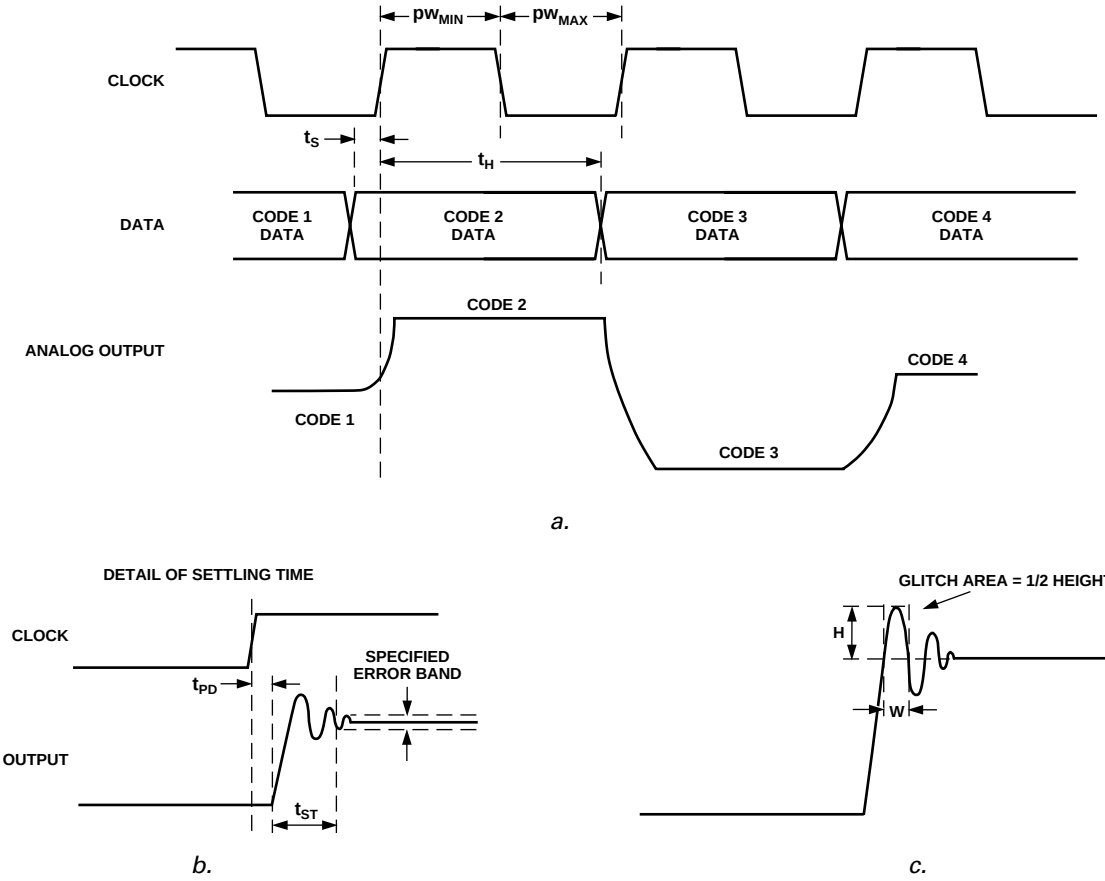


Figure 1. Timing Diagrams

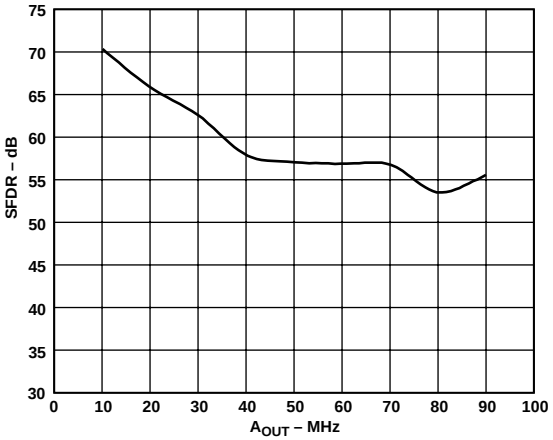


Figure 2. Narrowband SFDR (Clock = 200 MHz) vs. A_{OUT} Frequency

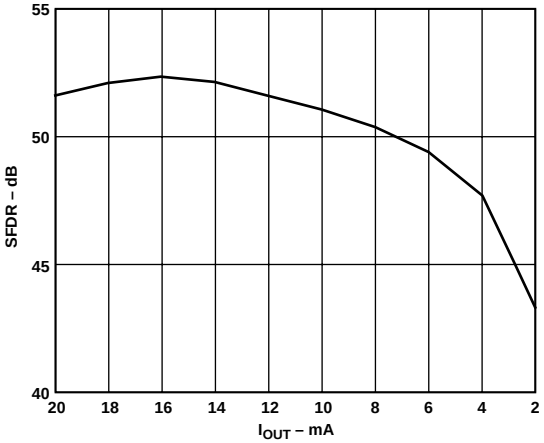


Figure 5. SFDR vs. I_{OUT}

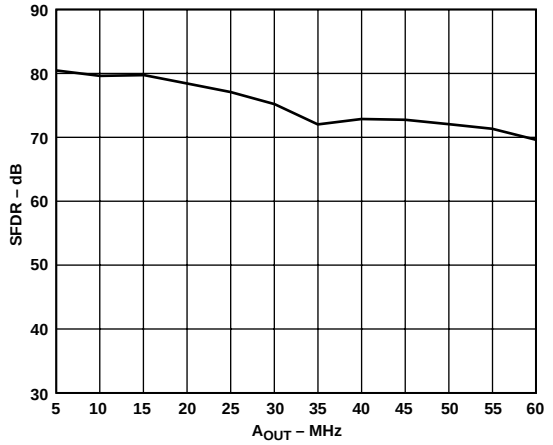


Figure 3. Narrowband SFDR (Clock = 125 MHz) vs. A_{OUT} Frequency

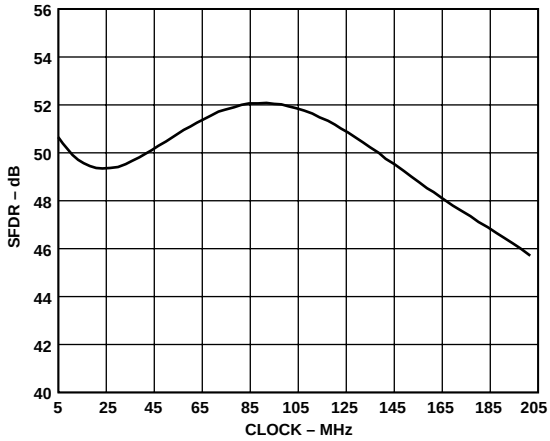


Figure 6. SFDR vs. Clock for $f_{CLK}/A_{OUT} = 3.125$

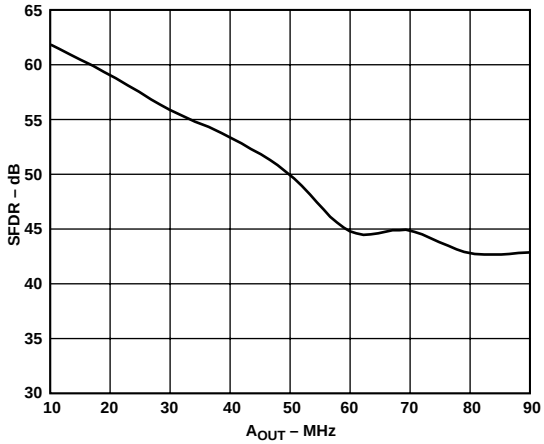


Figure 4. Wideband SFDR (200 MHz Clock) vs. A_{OUT}

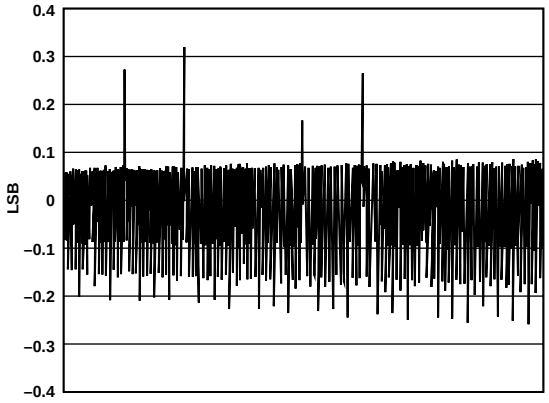


Figure 7. Typical Differential Nonlinearity Performance (DNL)

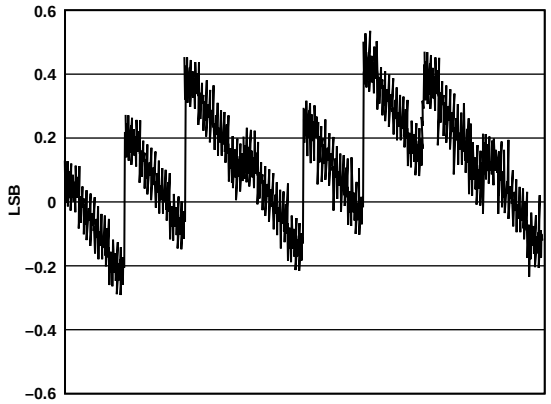


Figure 8. Typical Integral Nonlinearity Performance (INL)

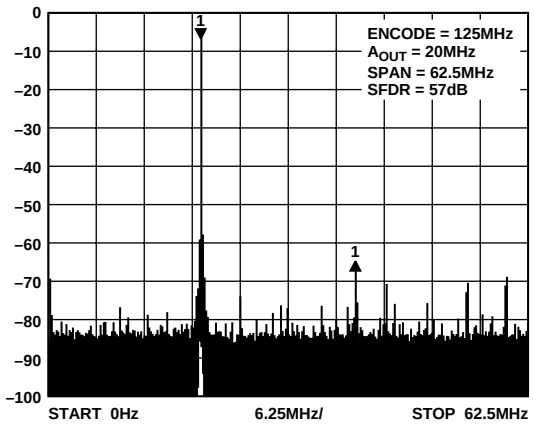


Figure 11. Wideband SFDR 20 MHz A_{OUT}; 125 MHz Clock

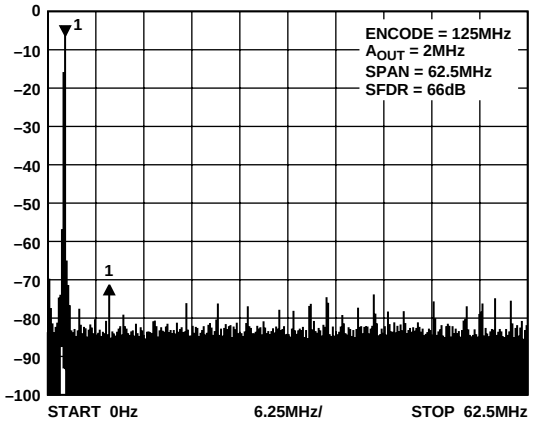


Figure 9. Wideband SFDR 2 MHz A_{OUT}; 125 MHz Clock

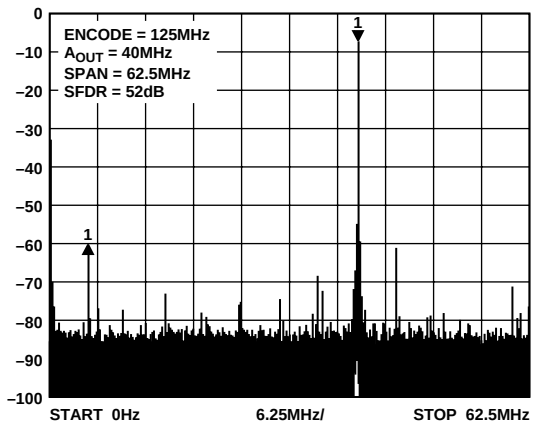


Figure 12. Wideband SFDR 40 MHz A_{OUT}; 125 MHz Clock

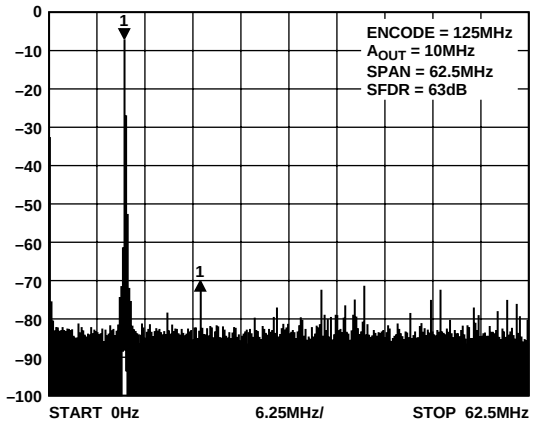


Figure 10. Wideband SFDR 10 MHz A_{OUT}; 125 MHz Clock

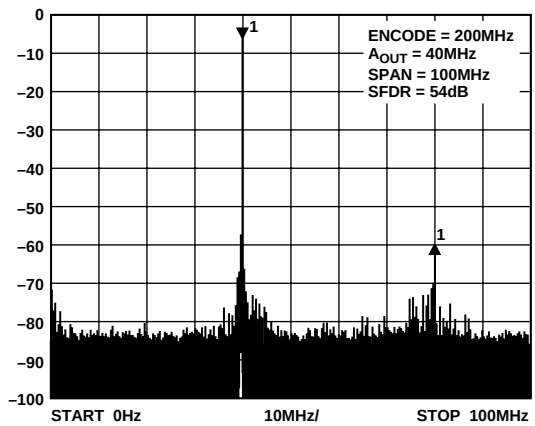


Figure 13. Wideband SFDR 40 MHz A_{OUT}; 200 MHz Clock

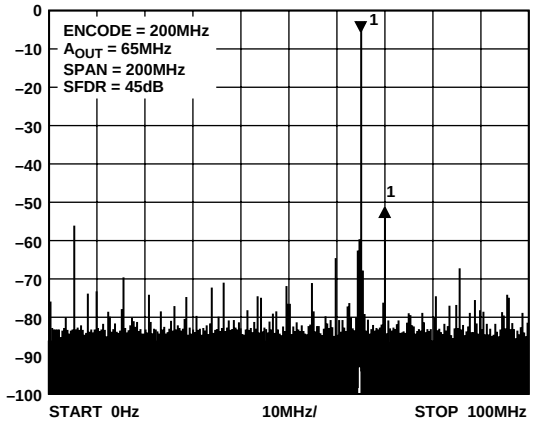


Figure 14. Wideband SFDR 65 MHz A_{OUT}; 200 MHz Clock

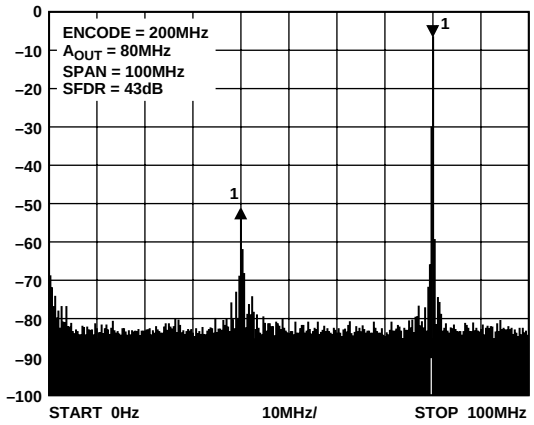


Figure 15. Wideband SFDR 80 MHz A_{OUT}; 200 MHz Clock

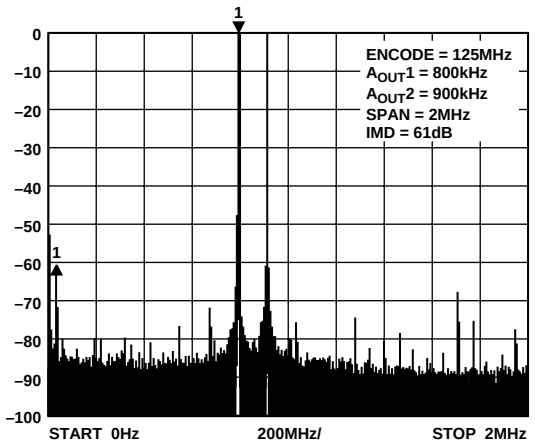


Figure 16. Wideband Intermodulation Distortion F1 = 800 kHz; F2 = 900 kHz; 125 MHz Clock; Span = 2 MHz

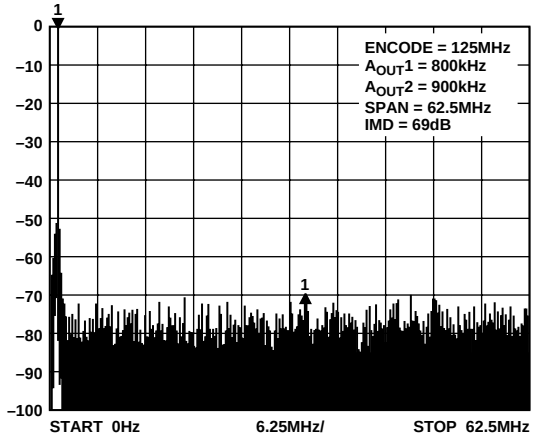


Figure 17. Wideband Intermodulation Distortion F1 = 800 kHz; F2 = 900 kHz; 125 MHz Clock; Span = 62.5 MHz

APPLICATION NOTES

THEORY OF OPERATION

The AD9732 high speed digital-to-analog converter utilizes most significant bit decoding and segmentation techniques to reduce glitch impulse and deliver high dynamic performance on lower power consumption than previous bipolar DAC technologies.

The design is based on four main subsections: the decode/driver circuits, the edge-triggered data register, the switch network and the control amplifier. An internal bandgap reference is included to allow operation of the device with minimum external support components.

Digital Inputs/Timing

The AD9732 has PECL high speed single-ended inputs for data inputs and clock. The switching threshold is +2.0 V.

In the decode/driver section, the three MSBs are decoded to seven "thermometer code" lines. An equalizing delay is included for the seven least significant bits and the clock signals. This delay minimizes data skew and data setup-and-hold times at the register inputs.

The on-board register is rising-edge triggered and should be used to synchronize data to the current switches by applying a pulse with proper data setup-and-hold times as shown in the timing diagram. Although the AD9732 is designed to provide isolation of the digital inputs to the analog output, some coupling of digital transitions is inevitable. Digital feedthrough can be minimized by forming a low-pass filter at the digital input by using a resistor in series with the capacitance of each digital input. This common high speed DAC application technique has the effect of isolating digital input noise from the analog output.

References

The internal bandgap reference, control amplifier and reference input are pinned out to provide maximum user flexibility in configuring the reference circuitry for the AD9732. When using the internal reference, REF OUT (Pin 25) should be connected to CONTROL AMP IN (Pin 26). CONTROL AMP OUT (Pin 24) should be connected to REF IN (Pin 23). A 0.1 μF ceramic capacitor connected from Pin 23 to GND improves settling time by decoupling switching noise from the current sink baseline. A reference current cell provides feedback to the control amplifier by sinking current through R_{SET} (Pin 17).

Full-scale current is determined by CONTROL AMP IN and R_{SET} according to the following equation:

$$I_{OUT}(FS) = 32\ ([CONTROL\ AMP\ IN - (+V_S)]/R_{SET})$$

The internal reference is nominally –1.25 V (referenced to Analog $+V_S$), with a tolerance of ±8% and typical drift over temperature of 150 ppm/°C. If greater accuracy or temperature stability is required, an external reference can be used. The AD589 reference features 10 ppm/°C drift over the 0°C to +70°C temperature range.

Two modes of multiplying operation are possible with the AD9732. Signals with bandwidths up to 2.5 MHz and input swings from 3.8 V to 4.4 V can be applied to the CONTROL AMP IN pin as shown in Figure 18. Because the control amplifier is internally compensated, the 0.1 μF capacitor discussed above can be reduced to maximize the multiplying bandwidth. However, it should be noted that output settling time, for changes in the digital word, will be degraded.

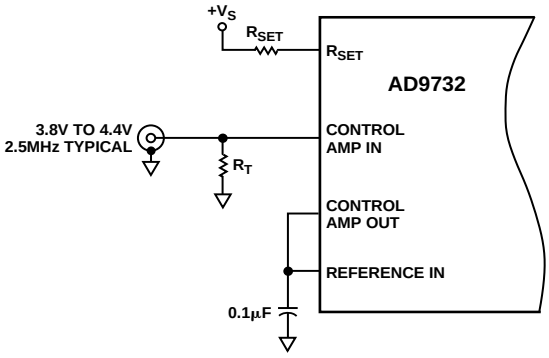


Figure 18. Lower Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of 0.95 V to 1.9 V. This can be implemented by capacitively coupling into REFERENCE IN a signal with a dc bias of 1.9 V (I_{OUT} = 22.5 mA) to 0.95 V (I_{OUT} = 3 mA), as shown in Figure 19, or by dividing REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

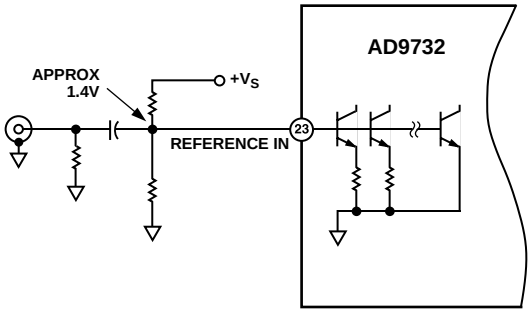


Figure 19. Wideband Multiplying Circuit

Analog Output

The switch network provides complementary current outputs I_{OUT} and I_{OUTB}. The design of the AD9732 is based on statistical current source matching, which provides a 10-bit linearity without trim. Current is steered to either I_{OUT} or I_{OUTB} in proportion to the digital input word. The sum of the two currents is always equal to the full-scale output current. The current can be converted to a voltage by resistive loading as shown in Figure 20. Both I_{OUT} and I_{OUTB} should be equally loaded for best overall performance. The voltage that is developed is the product of the output current and the value of the load resistor.

EVALUATION BOARD

The performance characteristics of the AD9732 make it ideally suited for direct digital synthesis (DDS) and other waveform synthesis applications. The AD9732 evaluation board provides a platform for analyzing performance under optimum layout conditions. The AD9732 also provides a reference for high speed circuit board layout techniques.

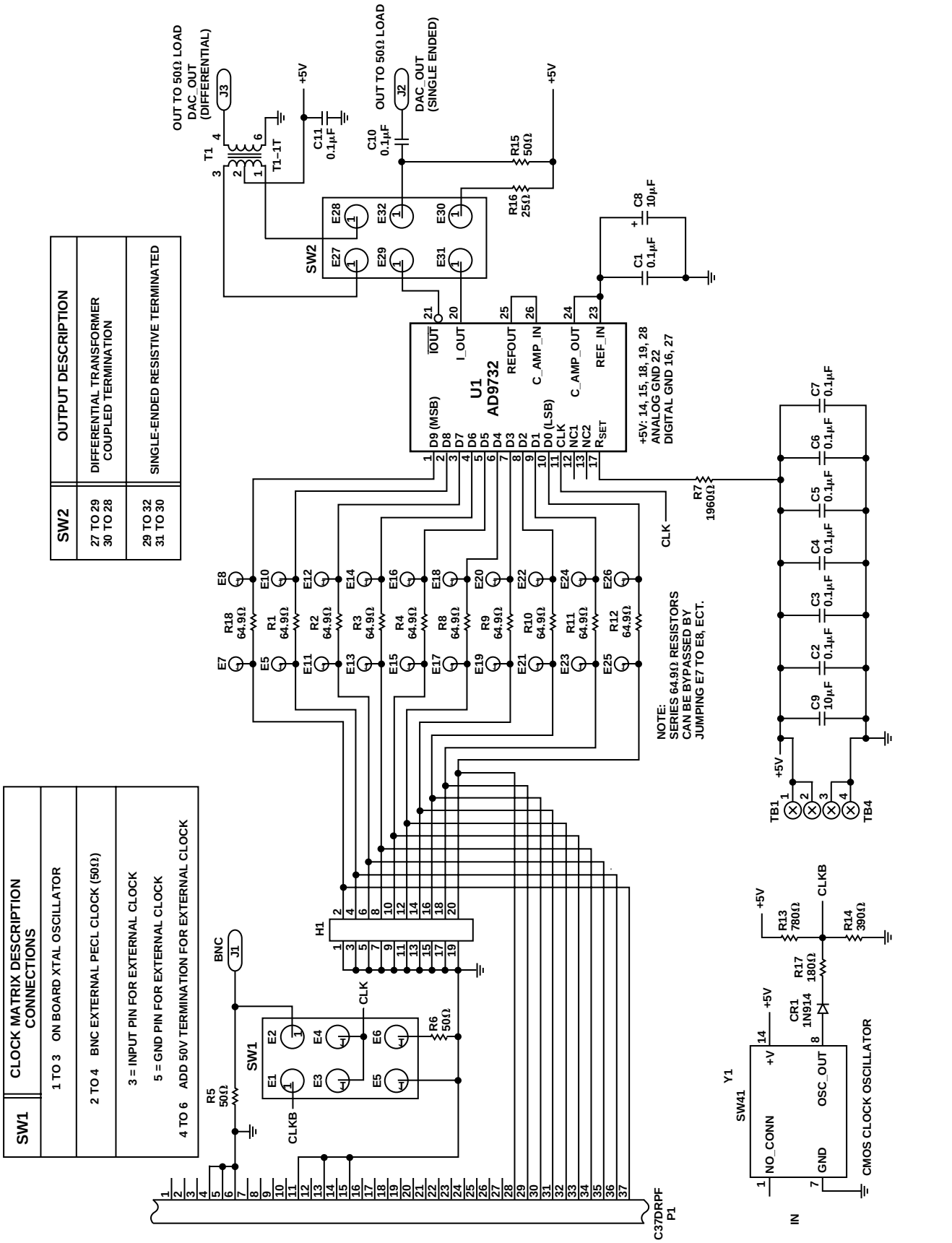
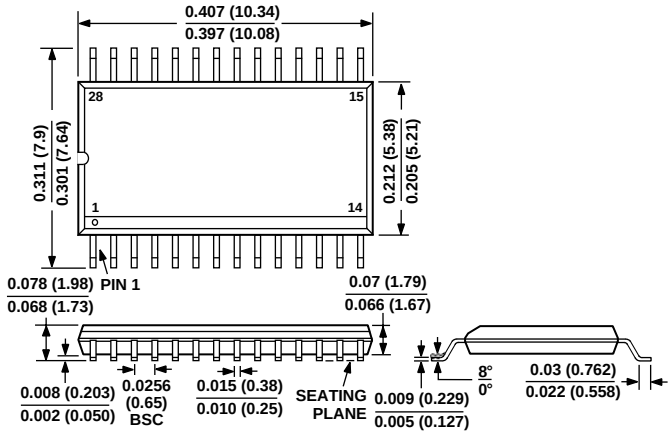


Figure 20. Evaluation Board

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead SSOP
(RS-28)



C3365a–0–4/99

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