Dual 16-Bit, 105 MSPS, 1.8 V Analog-to-Digital Converter

Data Sheet

AD9650-EP

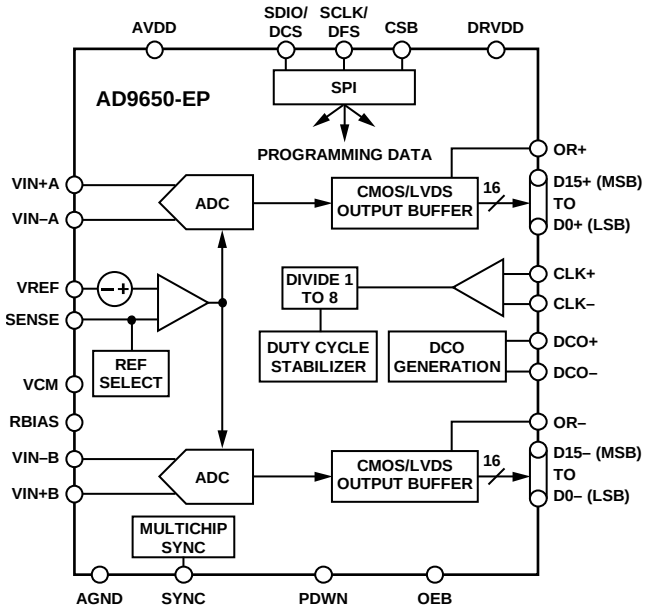
FEATURES

- Dual 16-bit ADC in enhanced package for extended temperature range of −55°C to +85°C
- 1.8 V analog supply operation
- LVDS output
- SNR: 80.5 dBFS at 30 MHz input and 105 MSPS data rate
- SFDR: 93 dBc at 30 MHz input and 105 MSPS data rate
- Low power: 328 mW per channel at 105 MSPS
- Integer 1-to-8 input clock divider
- IF sampling frequencies up to 300 MHz
- Analog input range of 2.7 V p-p
- Optional on-chip dither
- Integrated ADC sample-and-hold inputs
- Differential analog inputs with 500 MHz bandwidth
- ADC clock duty cycle stabilizer (DCS)

APPLICATIONS

- Radar
- Electronic warfare (EW) systems
- Joint tactical radio system (JTRS) and other COMSEC
- Industrial instrumentation
- X-ray, MRI, and ultrasound equipment
- High speed pulse acquisition
- Chemical and spectrum analysis
- General-purpose software radios

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. PIN NAMES ARE FOR THE LVDS PIN CONFIGURATION ONLY.

11312-001

Figure 1.

GENERAL DESCRIPTION

The AD9650-EP is a dual 16-bit, 105 MSPS analog-to-digital converter (ADC) designed for digitizing high frequency, wide dynamic range signals with input frequencies of up to 300 MHz.

The dual ADC core features a multistage differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth, differential sample-and-hold analog input amplifiers, and a shared integrated voltage reference, which eases design considerations. A duty cycle stabilizer (DCS) is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC output data can be routed directly to the two external 16-bit output ports or multiplexed on a single 16-bit bus. These outputs can be set to either 1.8 V CMOS or LVDS.

Flexible power-down options allow significant power savings, when desired. Programming for setup and control is accomplished using a 3-wire, SPI-compatible serial interface.

The AD9650-EP is available in an 80-lead TQFP and is specified over the extended temperature range of −55°C to +85°C.

Additional application and technical information can be found in the AD9650 data sheet.

PRODUCT HIGHLIGHTS

1. On-chip dither option for improved SFDR performance with low power analog input.
2. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 300 MHz.
3. Operation from a single 1.8 V supply with a separate digital output driver supply that accommodates 1.8 V CMOS or LVDS outputs.
4. Standard serial port interface (SPI) that supports various product features and functions such as data formatting (offset binary, twos complement, or Gray coding), enabling the clock DCS, power-down, and test modes.
5. 12 mm × 12 mm, 80-lead TQFP with an exposed pad (7.5 mm × 7.5 mm).

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REVISION HISTORY

5/13—Revision 0: Initial Version

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS disabled, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full		16		Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±0.4	±0.7	% FSR
Gain Error	Full		±0.4	±2.5	% FSR
Differential Nonlinearity (DNL)[1]	Full	−1		+1.3	LSB
	25°C		±0.7		LSB
Integral Nonlinearity (INL)[1]	Full			±6	LSB
	25°C		±3		LSB
MATCHING CHARACTERISTIC					
Offset Error	Full		±0.1	±0.4	% FSR
Gain Error	Full		±0.5	±1.3	% FSR
TEMPERATURE DRIFT					
Offset Error	Full		±2		ppm/°C
Gain Error	Full		±15		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage Error (1.35 V Mode)	Full		±7	±14	mV
Load Regulation at 1.0 mA	Full		10		mV
INPUT REFERRED NOISE					
VREF = 1.35 V	25°C		1.5		LSB rms
ANALOG INPUT					
Input Span, VREF = 1.35 V	Full		2.7		V p-p
Input Capacitance[2]	Full		11		pF
Input Common-Mode Voltage	Full		0.9		V
REFERENCE INPUT RESISTANCE	Full		6		kΩ
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current[1]					
I_{AVDD}	Full		332	340	mA
I_{DRVDD} (1.8 V CMOS)	Full		36		mA
I_{DRVDD} (1.8 V LVDS)	Full		100		mA
POWER CONSUMPTION					
DC Input	Full		656	675	mW
Sine Wave Input[1] (DRVDD = 1.8 V)					
CMOS Output Mode	Full		663		mW
LVDS Output Mode	Full		778		mW
Standby Power[3]	Full		50		mW
Power-Down Power	Full		0.25	2.5	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK+ and CLK− pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS disabled, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 30 MHz	25°C		80.5		dBFS
	Full	78.4			dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)					
f_{IN} = 30 MHz	25°C		80.2		dBFS
	Full	77.9			dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 30 MHz	25°C		13		Bits
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25°C		−93		dBc
	Full			−87	dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25°C		93		dBc
	Full	87			dBc
WORST OTHER (HARMONIC OR SPUR)					
f_{IN} = 30 MHz	25°C		−101		dBc
	Full			−94	dBc
CROSSTALK[2]	Full		−105		dBFS
ANALOG INPUT BANDWIDTH	25°C		500		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured with a 170 MHz tone at −1 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		9		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (V_{IN} = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO/DCS)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (V_{IN} = 1.8 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD})					
ANSI Mode	Full	290	345	400	mV
Reduced Swing Mode	Full	160	200	230	mV
Output Offset Voltage (V_{OS})					
ANSI Mode	Full	1.15	1.25	1.35	V
Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			640	MHz
Conversion Rate[1]					
DCS Enabled	Full	20		105	MSPS
DCS Disabled	Full	10		105	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	9.5			ns
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	2.85	4.75	6.65	ns
Divide-by-1 Mode, DCS Disabled	Full	4.5	4.75	5.0	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			ns
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.075		ps rms
DATA OUTPUT PARAMETERS					
CMOS Mode					
Data Propagation Delay (t_{PD})	Full	2.8	3.5	4.2	ns
DCO Propagation Delay (t_{DCO})[2]	Full		3.1		ns
DCO to Data Skew (t_{SKEW})	Full	−0.6	−0.4	0	ns
LVDS Mode					
Data Propagation Delay (t_{PD})	Full	2.9	3.7	4.5	ns
DCO Propagation Delay (t_{DCO})[2]	Full		3.9		ns
DCO to Data Skew (t_{SKEW})	Full	−0.1	+0.2	+0.5	ns
CMOS Mode Pipeline Delay (Latency)	Full		12		Cycles
LVDS Mode Pipeline Delay (Latency), Channel A/Channel B	Full		12/12.5		Cycles
Wake-Up Time[3]	Full		500		µs
Out-of-Range Recovery Time	Full		2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Additional DCO delay can be added by writing to Bit 0 through Bit 4 in SPI Register 0x17.
[3] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.3	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.4	ns typ
SPI TIMING REQUIREMENTS			
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

Timing Diagrams

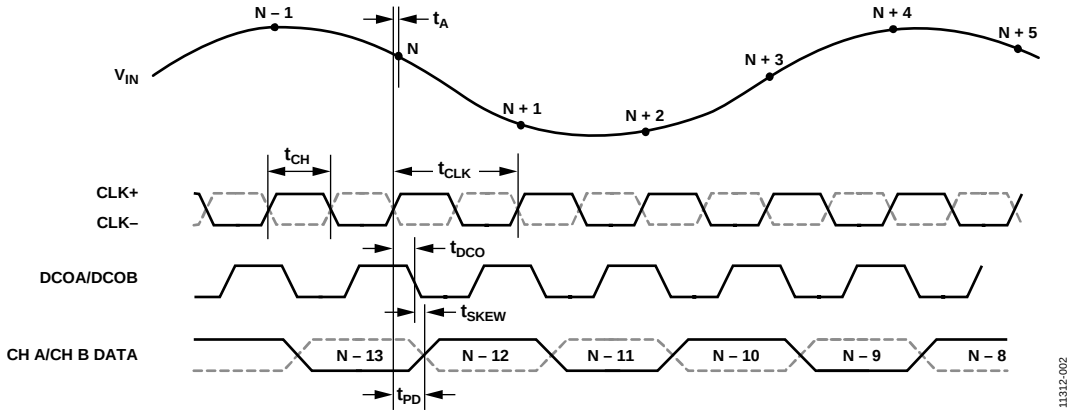


Figure 2. CMOS Default Output Mode Data Output Timing

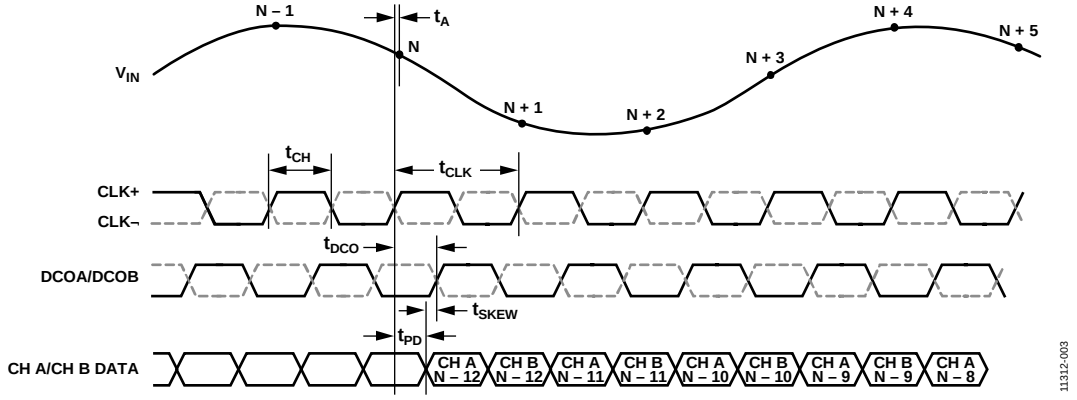


Figure 3. CMOS Interleaved Output Mode Data Output Timing

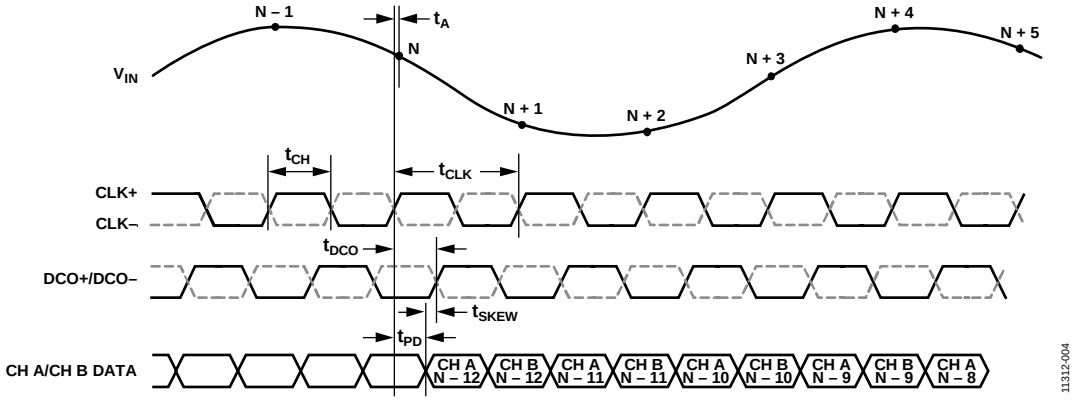


Figure 4. LVDS Mode Data Output Timing

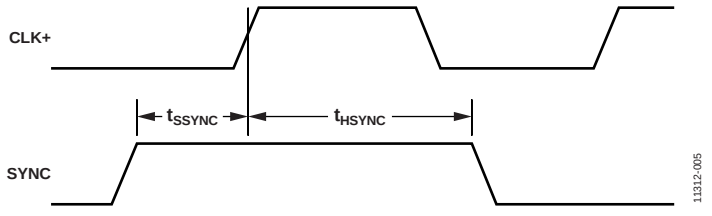


Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical[1]	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.2 V
SDIO/DCS to AGND	−0.3 V to DRVDD + 0.2 V
OEB	−0.3 V to DRVDD + 0.2 V
PDWN	−0.3 V to DRVDD + 0.2 V
D0+/D0− Through D15+/D15− to AGND	−0.3 V to DRVDD + 0.2 V
DCO+/DCO− to AGND	−0.3 V to DRVDD + 0.2 V
Environmental	
Operating Temperature Range (Ambient)	−55°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

[1] The inputs and outputs are rated to the supply voltage (AVDD + 0.2 V or DRVDD + 0.2 V), but they should not exceed 2.1 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed pad on the underside of the TQFP package must be soldered to the ground plane for the package. Soldering the exposed pad to the PCB increases the reliability of the solder joints and maximizes the thermal capability of the package.

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. Airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2, 4]	θ_{JC}[1, 3, 4]	Unit
80-Lead TQFP_EP	0	22.48	4.67	°C/W

[1] Per JEDEC JESD51-7, plus JEDEC JESD25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD-883, Method 1012.1.
[4] Per JEDEC STD, a 7 × 7 via array should be used to achieve this value.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

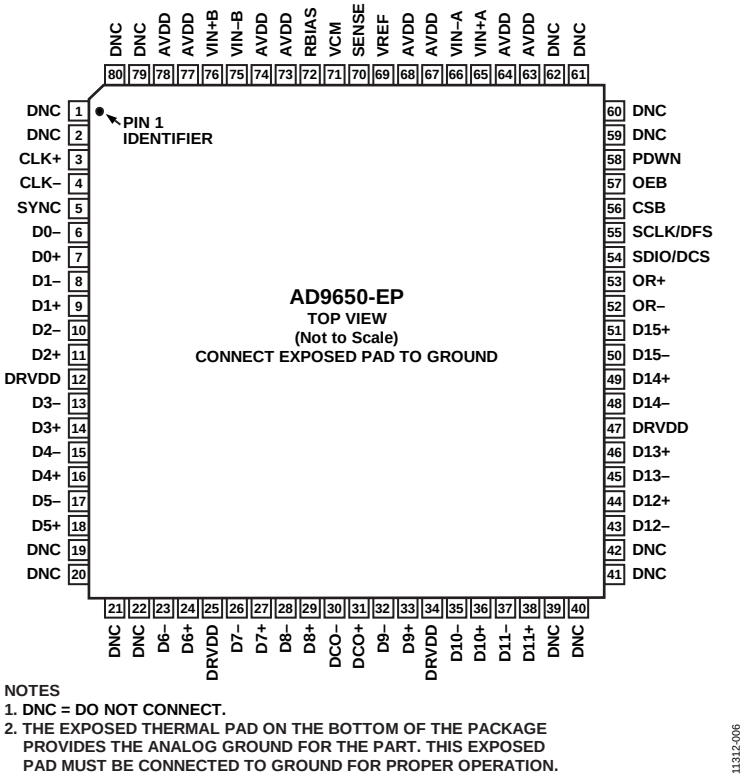


Figure 6. Interleaved Parallel LVDS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
12, 25, 34, 47	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
63, 64, 67, 68, 73, 74, 77, 78	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
65	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
66	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
76	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
75	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
69	VREF	Input/output	Voltage Reference Input/Output.
70	SENSE	Input	Voltage Reference Mode Select.
72	RBIAS	Input/output	External Reference Bias Resistor.
71	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
3	CLK+	Input	ADC Clock Input—True.
4	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
5	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
7	D0+	Output	Channel A/Channel B LVDS Output Data 0—True (LSB).
6	D0−	Output	Channel A/Channel B LVDS Output Data 0—Complement (LSB).
9	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
8	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
11	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
10	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
14	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
13	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
16	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
15	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
18	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
17	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
24	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
23	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
27	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
26	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
29	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
28	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
33	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
32	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
36	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
35	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
38	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
37	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
44	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
43	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
46	D13+	Output	Channel A/Channel B LVDS Output Data 13—True.
45	D13−	Output	Channel A/Channel B LVDS Output Data 13—Complement.
49	D14+	Output	Channel A/Channel B LVDS Output Data 14—True.
48	D14−	Output	Channel A/Channel B LVDS Output Data 14—Complement.
51	D15+	Output	Channel A/Channel B LVDS Output Data 15—True (MSB).
50	D15−	Output	Channel A/Channel B LVDS Output Data 15—Complement (MSB).
53	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
52	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
31	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
30	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
55	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
54	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
56	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
57	OEB	Input	Output Enable Input (Active Low) in External Pin Mode.
58	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.
Do Not Connect			
1, 2, 19, 20, 21, 22, 39, 40, 41, 42, 59, 60, 61, 62, 79, 80	DNC	N/A	Do Not Connect.

OUTLINE DIMENSIONS

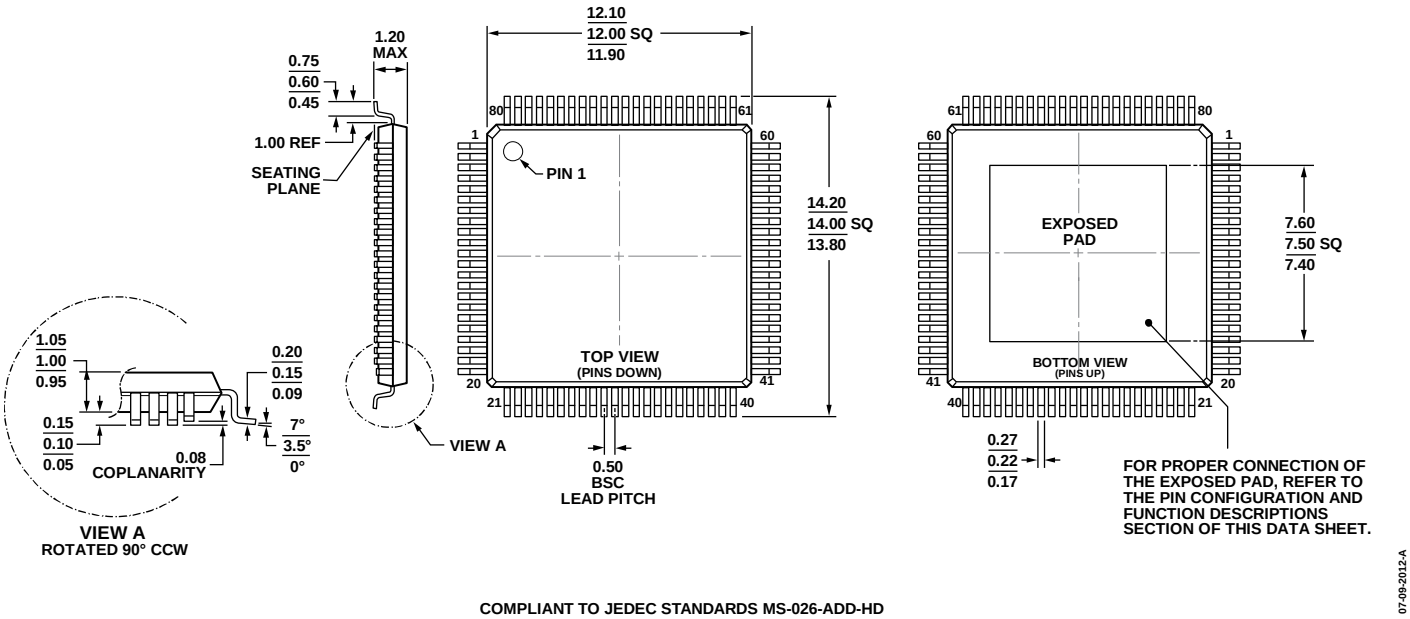


Figure 7. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
12 mm × 12 mm (SV-80-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9650USVZ-105EP	−55°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-6
AD9650USVZR7-105EP	−55°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-6

[1] Z = RoHS Compliant Part.

NOTES

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