Dual PLL, Asynchronous Clock Generator

Data Sheet **AD9576**

FEATURES

- Single, low phase noise, fully integrated VCO/fractional-N PLL core
  - VCO range: 2375 MHz to 2725 MHz
  - Integrated loop filter (requires a single external capacitor)
  - 2 differential, XTAL, or single-ended reference inputs
  - Reference monitoring capability
  - Automatic redundant XTAL switchover
  - Minimal transient, smooth switching
  - Typical RMS jitter
    - <0.3 ps (12 kHz to 20 MHz), integer-N translations
    - <0.5 ps (12 kHz to 20 MHz), fractional-N translations
  - Input frequency
    - 8 kHz, 1.544 MHz, 2.048 MHz, and 10 MHz to 325 MHz
  - Preset frequency translations via pin strapping (PPRx)
    - Using a 25 MHz input reference
      - 24.576 MHz, 25 MHz, 33.33 MHz, 50 MHz, 70.656 MHz, 100 MHz, 125 MHz, 148.5 MHz, 156.25 MHz, 161.1328 MHz, 312.5 MHz, 322.2656 MHz, 625 MHz, or 644.5313 MHz
    - Using a 19.44 MHz input reference
      - 50 MHz, 100 MHz, 125 MHz, 156.25 MHz, 161.1328 MHz, or 644.5313 MHz
    - Using a 30.72 MHz input reference
      - 25 MHz, 50 MHz, 100 MHz, 125 MHz, or 156.25 MHz
- Single, general-purpose, fully integrated VCO/integer-N PLL core
  - VCO range: 750 MHz to 825 MHz
  - Integrated loop filter
  - Independent, duplicate reference input or operation from the fractional-N PLL active reference input
  - Input frequency: 25 MHz
  - Preset frequency translations via pin strapping (PPRx)
    - 25 MHz, 33.33 MHz, 50 MHz, 66.67 MHz, 100 MHz, 133.33 MHz, 200 MHz, or 400 MHz
  - Up to 3 copies of reference clock output
- 11 pairs of configurable differential outputs
  - Output drive formats
    - 3 outputs: HSTL, LVDS, HCSL, 1.8 V CMOS, 2.5 V/3.3 V CMOS
    - 8 outputs: HSTL, LVDS, or 1.8 V CMOS
- 2.5 V or 3.3 V single-supply operation

APPLICATIONS

- Ethernet line cards, switches, and routers
- Baseband units
- SATA and PCI express
- Low jitter, low phase noise clock generation
- Asynchronous clock generation

FUNCTIONAL BLOCK DIAGRAM

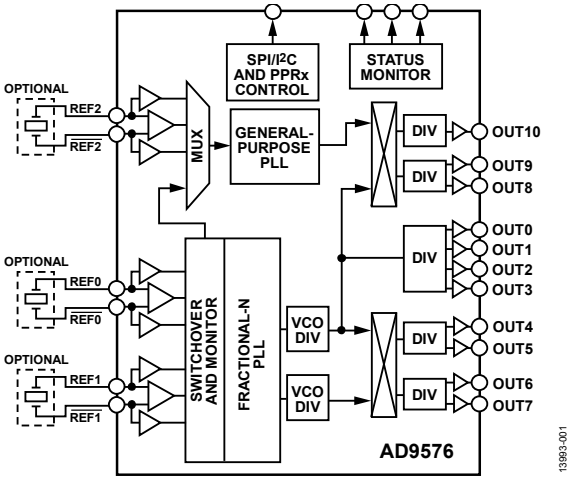


Figure 1.

GENERAL DESCRIPTION

The AD9576 provides a multiple output clock generator function comprising two dedicated phase-locked loop (PLL) cores with flexible frequency translation capability, optimized to serve as a robust source of asynchronous clocks for an entire system, providing extended operating life within frequency tolerance through monitoring of and automatic switchover between redundant crystal (XTAL) inputs with minimized switching, induced transients. The fractional-N PLL design is based on the Analog Devices, Inc., proven portfolio of high performance, low jitter frequency synthesizers to maximize network performance, whereas the integer-N PLL provides general-purpose clocks for use as CPU and field-programmable gate array (FPGA) reference clocks.

The AD9576 uses pin strapping to select among a multitude of power-on ready configurations for its 11 output clocks, which require only the connection of external pull-up or pull-down resistors to the appropriate pin program reader pins (PPRx). These pins provide control of the internal dividers for establishing the desired frequency translations, clock output functionality, and input reference functionality. These parameters can also be manually configured through a serial port interface (SPI).

The AD9576 is packaged in a 64-lead, 9 mm × 9 mm LFCSP, requiring only a single 2.5 V or 3.3 V supply. The operating temperature range is −40°C to +85°C.

Each $\overline{\text{OUTx}}$ output is differential and contains two pins: OUTx and $\overline{\text{OUTx}}$. For simplicity, the term OUTx refers to the functional output block containing these two pins.

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REVISION HISTORY

9/2018—Rev. 0 to Rev. A

Change to Table 47, Address 0x103, Bits[5:3], Reset Column.....55
Updated Outline Dimensions.....65

7/2016—Revision 0: Initial Version

SPECIFICATIONS

Typical values are given for V_{DD_x} = 2.5 V, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full V_{DD_x} and T_A (−40°C to +85°C) range.

VDD_x and V_{DD_x} refer to the following pins, and to the voltage on any of the following pins, respectively: VDD_REFMON, VDD_REF0, VDD_REF1, VDD_IO, VDD_PLL0, VDD_VCO0, VDD_M0, VDD_M1, VDD_OUT67, VDD_OUT45, VDD_OUT23, VDD_OUT01, VDD_OUT89, VDD_OUT10, VDD_VCO1, VDD_PLL1, and VDD_REF2.

Note that throughout this data sheet, multifunction pins, such as SCLK/SCL, are referred to either by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY VOLTAGE (V_{DD_x})					Applies to all VDD_x pins; 2.5 V and 3.3 V nominal supplies are supported on all specifications, unless otherwise noted
	2.38		2.63	V	2.5 V ± 5%
	2.97		3.63	V	3.3 V ± 10%

SUPPLY CURRENT SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLIES OTHER THAN CLOCK OUTPUT DRIVERS					All blocks running (excludes clock distribution section); REF0 (differential) and REF1 (differential) at 300 MHz; PLL0 locked at 2500 MHz with a 100 MHz phase frequency detector (PFD) rate; Divider M0 set to 2 and Divider M1 disabled; REF2 (XTAL) at 25 MHz, configured as PLL1 input; PLL1 locked to 800 MHz with input doubler enabled
VDD_REFMON and VDD_REFx (Pin 4, Pin 9, Pin 10, and Pin 64)		35.6	39.2	mA	Cumulative current draw from all listed supply pins
VDD_IO and VDD_PLL0 (Pin 16 and Pin 18)		26.5	29.5	mA	Cumulative current draw from all listed supply pins
VDD_VCO0 (Pin 21)		33.8	36.9	mA	
VDD_Mx (Pin 23 and Pin 25)		81.0	88.7	mA	Cumulative current draw from all listed supply pins
VDD_VCO1 (Pin 60)		19.2	21.8	mA	
VDD_PLL1 (Pin 61)		20.4	23.7	mA	
SUPPLY CURRENT FOR EACH CLOCK DISTRIBUTION SUPPLY					Output driver supplies power both the output driver and output divider
High Speed Transceiver Logic (HSTL)					
VDD_OUT67 (Pin 29)		59.8	69.7	mA	Output at 1250 MHz
VDD_OUT45 (Pin 35)		59.8	69.7	mA	Output at 1250 MHz
VDD_OUT23 (Pin 41)		46.7	53.8	mA	Output at 625 MHz
VDD_OUT01(Pin 46)		36.4	42.6	mA	Output at 625 MHz
VDD_OUT89 (Pin 52)		57.4	67.1	mA	Output at 400 MHz
VDD_OUT10 (Pin 57)		34.2	39.5	mA	Output at 400 MHz
Low Voltage Differential Signaling (LVDS)					
VDD_OUT67 (Pin 29)		41.3	49.2	mA	Output at 1250 MHz
VDD_OUT45 (Pin 35)		41.3	49.2	mA	Output at 1250 MHz
VDD_OUT23 (Pin 41)		31.1	34.9	mA	Output at 625 MHz
VDD_OUT01(Pin 46)		20.8	23.6	mA	Output at 625 MHz
VDD_OUT89 (Pin 52)		37.5	43.6	mA	Output at 400 MHz
VDD_OUT10 (Pin 57)		24.1	27.7	mA	Output at 400 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1.8 V CMOS					All outputs at 100 MHz with a 10 pF load
VDD_OUT67 (Pin 29)		27.2	34.7	mA	
VDD_OUT45 (Pin 35)		27.2	34.7	mA	
VDD_OUT23 (Pin 41)		28.2	31.7	mA	
VDD_OUT01(Pin 46)		17.4	21.9	mA	
VDD_OUT89 (Pin 52)		32.7	42.5	mA	
VDD_OUT10 (Pin 57)		21.4	26.8	mA	
2.5 V CMOS					V_{DD_x} set to 2.5 V, output at 100 MHz with a 10 pF load; not available on OUT0 to OUT7
VDD_OUT89 (Pin 52)		38.5	48.8	mA	
VDD_OUT10 (Pin 57)		24.4	30.1	mA	
3.3 V CMOS					V_{DD_x} set to 3.3 V, all outputs at 100 MHz with a 10 pF load; not available on OUT0 to OUT7
VDD_OUT89 (Pin 52)		48.5	60.4	mA	
VDD_OUT10 (Pin 57)		29.1	36.2	mA	
High Speed Current Sinking Logic (HCSL)					All outputs at 400 MHz; not available on OUT0 to OUT7
VDD_OUT89 (Pin 52)		30.7	41.4	mA	
VDD_OUT10 (Pin 57)		20.8	26.6	mA	

POWER DISSIPATION SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					All supplies set to 2.5 V nominal; specifications do not include power dissipated by external terminations
Typical Configuration 1		680	1168	mW	Asynchronous operation; PPR0 = State 0, PPR1 = State 0, PPR2 = State 3, PPR3 = State 3; REF 0 and REF1 = 25 MHz XTAL, doubler enabled; OUT10 = 25 MHz CMOS; OUT0 to OUT3 = 100 MHz LVDS; OUT4 to OUT5 = 312.5 MHz LVDS, OUT6 to OUT7 = 156.25 MHz LVDS, OUT8 to OUT9 = 125 MHz LVDS
Typical Configuration 2		619	974	mW	Synchronous operation; REF0 (differential) at 100 MHz, REF1 disabled, and REF2 (XTAL) at 25 MHz; PLL1 disabled and PLL0 locked at 2500 MHz using R divider of 2 and PLL0 feedback divider (N0) set to 50; M0 and M1 set to divide by 2; Output 0 set to 625 MHz HSTL; Output 1 to Output 3 disabled; Output 4 to Output 7 set to 125 MHz LVDS; Output 8 to Output 9 set to 156.25 MHz LVDS
All Blocks Running		979	1520	mW	All blocks running; REF0 (differential) and REF1 (differential) at 300 MHz; PLL0 locked at 2500 MHz with a 100 MHz PFD rate; M0 set to 2 and enabled to Q0, Q1, and Q2; OUT0 to OUT3 = 625 MHz LVDS; OUT4 to OUT 7 = 1250 MHz LVDS; REF2 (XTAL) at 25 MHz, configured as PLL1 input; PLL1 locked to 800 MHz with input doubler enabled; Divider Q3 and Divider Q4 set to 2 and OUT8 to OUT10 = 400 MHz, HCSL
Minimal Power Configuration		145	179	mW	PPR0 = State 0, PPR1 = State 0, PPR2 = State 0, PPR3 = State 0
INCREMENTAL POWER DISSIPATION					Typical configuration; values show the change in power due to the indicated operation
Input Reference On/Off					Applies to one reference clock input at 25 MHz
Single-Ended		2.5	10	mW	
Differential		27.5	33.7	mW	
Output Driver On/Off					
LVDS at 156.25 MHz		47.6	66.1	mW	
HSTL at 156.25 MHz		51.3	80.8	mW	
1.8 V CMOS at 100 MHz		64.6	74.1	mW	A single 1.8 V CMOS output with a 10 pF load
2.5 V CMOS at 100 MHz		88.4	102.5	mW	A single 2.5 V CMOS output with a 10 pF load

REFERENCE INPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL INPUT MODE					
Input Frequency			325	MHz	
Input Sensitivity	100			mV p-p	
Minimum Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance (when using a sinusoidal source)
Minimum Pulse Width	1.38			ns	Applies to both low and high pulses
Common-Mode Internally Generated Bias Voltage		1.24		V	
Common-Mode Voltage Tolerance	0.83		1.675	V	The acceptable common-mode range for a 200 mV p-p, dc-coupled input signal
Differential Input Capacitance		2		pF	
Differential Input Resistance		4.3		kΩ	
SINGLE-ENDED INPUT CMOS MODE					
Input Frequency			200	MHz	
Minimum Pulse Width	2			ns	Applies to both low and high pulses
Hysteresis		240		mV	
Input Leakage		2		nA	
Input Capacitance		2		pF	
Input Voltage					
High	1.93			V	
Low			1.04	V	
CRYSTAL RESONATOR MODE					Fundamental mode quartz resonator
Input Frequency					
Reference of PLL0 or Buffered Output	19.44		30.72	MHz	
Reference of PLL1		25		MHz	REF2
Effective Series Resistance (ESR)			80	Ω	
Input Capacitance		3		pF	

REFERENCE SWITCHOVER OUTPUT DISTURBANCE SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INSTANTANEOUS FREQUENCY (dθ/dt) DISTURBANCE DUE TO REFERENCE SWITCHOVER		350		ppm peak	Applies only to PLL0 outputs; 1 ppm frequency offset between the REF0 and REF1 channels; 400 kHz loop bandwidth; smooth switchover enabled
INSTANTANEOUS PHASE DISTURBANCE DUE TO REFERENCE SWITCHOVER		220		ps	Applies only to the active reference of PLL0; smooth switchover enabled

PLL0 CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT PATH					
Input Frequency					
Divider			325	MHz	
Doubler			145	MHz	
PHASE FREQUENCY DETECTOR (PFD)					
Frequency Range					
Integer Mode			290	MHz	
Fractional Mode	9.4		170	MHz	
Lock Detect Window		±16		ppm	
INPUT FREQUENCY OF FEEDBACK DIVIDERS					
N0			2725	MHz	
N0A			156	MHz	
Q_{ZD}			1250	MHz	
VOLTAGE CONTROLLED OSCILLATOR (VCO)					
Frequency Range	2375		2725	MHz	
Gain		64		MHz/V	
VCO DIVIDER (M0 AND M1) OUTPUT FREQUENCY			1250	MHz	

PLL1 CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT PATH					
Input Frequency					
Divider		25		MHz	
Doubler		25		MHz	
PFD FREQUENCY					
Frequency Range	25		50	MHz	
Lock Detector Window		2		UI	
VCO					
Frequency Range	750		825	MHz	
Gain		750		MHz/V	

CLOCK DISTRIBUTION OUTPUTS SPECIFICATIONS

Rise and fall time measurement thresholds are 20% and 80% of the nominal low and high amplitude of the waveform.

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL (OUT0 TO OUT7)					100 Ω termination (differential)
Output Frequency					
OUT0 to OUT3			1000	MHz	
OUT4 to OUT7			1250	MHz	
Output Rise Time, t_{RL}	108	136	163	ps	Measured differentially; output at 100 MHz
Output Fall Time, t_{FL}	108	136	161	ps	Measured differentially; output at 100 MHz
Duty Cycle	45		55	%	
Differential Output Voltage Swing	861	1080	1374	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	840	940	1034	mV	Output driver static

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS (OUT0 TO OUT7)					100 Ω termination (differential)
Output Frequency					
OUT0 to OUT3			1000	MHz	
OUT4 to OUT7			1250	MHz	
Output Rise Time, t_{RL}	139	158	181	ps	Measured differentially; output at 100 MHz
Output Fall Time, t_{FL}	141	159	181	ps	Measured differentially; output at 100 MHz
Duty Cycle	45		55	%	
Differential Output Voltage, V_{OD}	276	375	490	mV	Magnitude of voltage across pins; output driver static
Delta V_{OD}			22	mV	
Output Offset Voltage, V_{OS}	1.18	1.275	1.36	V	
Delta V_{OS}			26	mV	
Short-Circuit Current (I_{SA}, I_{SB})			25	mA	Output shorted to GND; value represents the magnitude of current draw
1.8 V CMOS (OUT0 TO OUT7)					C_{LOAD} = 10 pF
Output Frequency			200	MHz	
Output Rise Time, t_{RC}	0.84	1.19	1.54	ns	Output at 25 MHz
Output Fall Time, t_{FC}	1.04	1.25	1.49	ns	Output at 25 MHz
Duty Cycle	45		55	%	
Output Voltage					
High (V_{OH})	1.74			V	I_{LOAD} = −1 mA
Low (V_{OL})			0.065	V	I_{LOAD} = 1 mA
HSTL (OUT8 TO OUT10)					100 Ω termination (differential)
Output Frequency			1000	MHz	
Output Rise Time, t_{RL}	124	144	170	ps	Measured differentially; output at 100 MHz
Output Fall Time, t_{FL}	125	144	170	ps	Measured differentially; output at 100 MHz
Duty Cycle	45		55	%	Assumes 50% reference input duty cycle
Differential Output Voltage Swing	861	1080	1374	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	840	940	1034	mV	Output driver static
LVDS (OUT8 TO OUT10)					100 Ω termination (differential)
Output Frequency			1000	MHz	
Output Rise Time, t_{RL}	65	85	112	ps	Measured differentially; output at 100 MHz
Output Fall Time, t_{FL}	66	86	113	ps	Measured differentially; output at 100 MHz
Duty Cycle	45		55	%	Assumes 50% reference input duty cycle
Differential Output Voltage, V_{OD}	276	375	490	mV	Magnitude of voltage across pins; output driver static
ΔV_{OD}			22	mV	
Output Offset Voltage, V_{OS}	1.18	1.275	1.36	V	
ΔV_{OS}			26	mV	
Short-Circuit Current (I_{SA}, I_{SB})			25	mA	Output shorted to GND; value represents the magnitude of current draw
1.8 V CMOS (OUT8 TO OUT10)					C_{LOAD} = 10 pF
Output Frequency			200	MHz	
Output Rise Time, t_{RC}		0.49	1.41	ns	Output at 25 MHz
Output Fall Time, t_{FC}		0.59	1.24	ns	Output at 25 MHz
Duty Cycle	45		55	%	Assumes 50% reference input duty cycle
Output Voltage					
High (V_{OH})	1.74			V	I_{LOAD} = −1 mA
Low (V_{OL})			0.065	V	I_{LOAD} = 1 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FULL SWING CMOS (OUT8 TO OUT10)					C_{LOAD} = 10 pF
Output Frequency			250	MHz	
Output Rise Time, t_{RC}		0.50	1.38	ns	Output at 25 MHz
Output Fall Time, t_{FC}		0.57	1.19	ns	Output at 25 MHz
Duty Cycle	45		55	%	Assumes 50% reference input duty cycle
Output Voltage					
High (V_{OH})	V_{DD_x} − 0.33			V	I_{LOAD} = −10 mA
Low (V_{OL})			0.25	V	I_{LOAD} = 10 mA
HCSL (OUT8 to OUT10)					50 Ω from each output pin to GND
Output Frequency			800		
Output Rise Time, t_{RL}	145	174	211	ps	Measured differentially; output at 100 MHz
Output Fall Time, t_{FL}	141	175	209	ps	Measured differentially; output at 100 MHz
Duty Cycle	45		55	%	Assumes 50% reference input duty cycle
Differential Output Voltage Swing	570	770	975	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	295	400	500	mV	Output driver static

Timing Diagrams

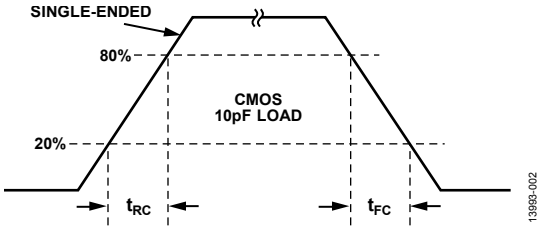


Figure 2. CMOS Timing, Single-Ended, 10 pF Load

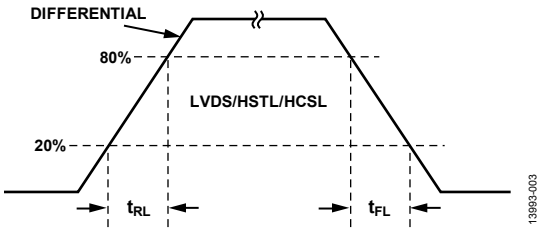


Figure 3. LVDS, HSTL, and HCSL Timing, Differential

OUTPUT ALIGNMENT AND STARTUP SPECIFICATIONS

The indicated times assume the voltage applied to all power supply pins is within specification and stable.

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ZERO DELAY					Timing delay between input clock edge on REF0 or REF1 to any corresponding OUTx clock edge; R divider and doubler are bypassed
OUT0 to OUT7		3.44	3.87	ns	
OUT8 to OUT9		3.82	4.28	ns	
OUTPUT TO OUTPUT SKEW					Deviation between rising edges of outputs of a similar logic type; frequency source to distribution is the output of the M0 divider; all output drivers are configured to the same logic type, unless otherwise noted; all output frequencies are 25 MHz
Between Outputs that Share a Single Qx Divider					
LVDS					
OUT1, OUT2, and OUT3	−36		+29	ps	Relative to OUT0
OUT5	−13		+30	ps	Relative to OUT4
OUT7	−19		+15	ps	Relative to OUT6
OUT9	−22		+20	ps	Relative to OUT8
HSTL					
OUT1, OUT2, and OUT3	−33		+30	ps	Relative to OUT0
OUT5	−16		+37	ps	Relative to OUT4
OUT7	−16		+19	ps	Relative to OUT6
OUT9	−23		+24	ps	Relative to OUT8
Between OUT0 to OUT9					
LVDS					
OUT4	−141		−8	ps	Relative to OUT0
OUT6	−105		+23	ps	Relative to OUT0
OUT8	229		440	ps	Relative to OUT0
HSTL					
OUT4	−149		−12	ps	Relative to OUT0
OUT6	−116		+17	ps	Relative to OUT0
OUT8	271		487	ps	Relative to OUT0
PROPAGATION DELAY		3.88	4.47	ns	Rising edge on REF2 input to OUT8 to OUT10; 25 MHz reference input clock, PLL1 bypassed, and Qx dividers set to 1
OUTPUT READY TIME					25 MHz reference input clocks, input doublers disabled
PLL0		8		ms	Time interval from $\overline{\text{RESET}}$ pin = Logic 1 to LD_0 pin = Logic 1 (PLL0 lock detection)
PLL1		455		µs	Time interval from $\overline{\text{RESET}}$ pin = Logic 1 to LD_1 pin = Logic 1 (PLL1 lock detection)

PLL0 CHANNELS ABSOLUTE CLOCK JITTER SPECIFICATIONS

Reference input frequency source is a 25 MHz Taitien XTAL, and frequency multiplier (×2) at PLL input enabled, unless otherwise noted.

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL INTEGRATED RMS JITTER					
Jitter Integration Bandwidth = 10 kHz to 10 MHz					
Integer-N Translations					
100 MHz Output		0.233		ps	
125 MHz Output		0.218		ps	
156.25 MHz Output		0.218		ps	
625 MHz Output		0.221		ps	
Fractional-N Translations					
70.656 MHz Output		0.291		ps	
148.5 MHz Output		0.307		ps	
153.6 MHz Output		0.292		ps	
644.53125 MHz Output		0.313		ps	
Jitter Integration Bandwidth = 12 kHz to 20 MHz					
Integer-N Translations					
100 MHz Output		0.239		ps	
125 MHz Output		0.222		ps	
156.25 MHz Output		0.221		ps	
625 MHz Output		0.222		ps	
Fractional-N Translations					
70.656 MHz Output		0.298		ps	
148.5 MHz Output		0.310		ps	
153.6 MHz Output		0.296		ps	
644.53125 MHz Output		0.314		ps	
Jitter Integration Bandwidth = 50 kHz to 80 MHz					
312.5 MHz Output		0.237		ps	
Jitter Integration Bandwidth = 1.875 MHz to 20 MHz					
Integer-N Translations					
100 MHz Output		0.088		ps	
125 MHz Output		0.076		ps	
156.25 MHz Output		0.071		ps	
625 MHz Output		0.053		ps	
Fractional-N Translations					
70.656 MHz Output		0.119		ps	
148.5 MHz Output		0.106		ps	
153.6 MHz Output		0.103		ps	
644.53125 MHz Output		0.096		ps	
LVDS INTEGRATED RMS JITTER					
Jitter Integration Bandwidth = 10 kHz to 10 MHz					
Integer-N Translations					
100 MHz Output		0.242		ps	
125 MHz Output		0.227		ps	
156.25 MHz Output		0.250		ps	
625 MHz Output		0.221		ps	
Fractional-N Translations					
70.656 MHz Output		0.351		ps	
148.5 MHz Output		0.329		ps	
153.6 MHz Output		0.327		ps	
644.53125 MHz Output		0.313		ps	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Jitter Integration Bandwidth = 12 kHz to 20 MHz					
Integer-N Translations					
100 MHz Output		0.268		ps	
125 MHz Output		0.240		ps	
156.25 MHz Output		0.257		ps	
625 MHz Output		0.221		ps	
Fractional-N Translations					
70.656 MHz Output		0.412		ps	
148.5 MHz Output		0.336		ps	
153.6 MHz Output		0.334		ps	
644.53125 MHz Output		0.314		ps	
Jitter Integration Bandwidth = 50 kHz to 80 MHz					
312.5 MHz Output		0.246		ps	
Jitter Integration Bandwidth = 1.875 MHz to 20 MHz					
Integer-N Translations					
100 MHz Output		0.161		ps	
125 MHz Output		0.117		ps	
156.25 MHz Output		0.099		ps	
625 MHz Output		0.053		ps	
Fractional-N Translations					
70.656 MHz Output		0.298		ps	
148.5 MHz Output		0.130		ps	
153.6 MHz Output		0.129		ps	
644.53125 MHz Output		0.095		ps	
HCSL INTEGRATED RMS JITTER					OUT8 and OUT9 only
Jitter Integration Bandwidth = 10 kHz to 10 MHz					
Integer-N Translations					
100 MHz Output		0.247		ps	
125 MHz Output		0.250		ps	
156.25 MHz Output		0.273		ps	
625 MHz Output		0.228		ps	
Jitter Integration Bandwidth = 12 kHz to 20 MHz					
100 MHz Output		0.263		ps	
125 MHz Output		0.265		ps	
156.25 MHz Output		0.298		ps	
625 MHz Output		0.229		ps	
Jitter Integration Bandwidth = 50 kHz to 80 MHz					
312.5 MHz Output		0.348		ps	
Jitter Integration Bandwidth = 1.875 MHz to 20 MHz					
100 MHz Output		0.145		ps	
125 MHz Output		0.144		ps	
156.25 MHz Output		0.176		ps	
625 MHz Output		0.063		ps	

PLL1 AND BYPASS CHANNEL ABSOLUTE CLOCK JITTER SPECIFICATIONS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL INTEGRATED RMS JITTER					
25 MHz Output		0.125		ps	Source = 25 MHz Taitien XTAL; jitter integration bandwidth = 12 kHz to 5 MHz
100 MHz Output		1.605		ps	Source = PLL1; Qx divider = 8; jitter integration bandwidth = 12 kHz to 20 MHz
400 MHz Output		1.641		ps	Source = PLL1; Qx divider = 2; jitter integration bandwidth = 12 kHz to 20 MHz
HCSL INTEGRATED RMS JITTER					
25 MHz Output		0.287		ps	Source = 25 MHz Taitien XTAL; jitter integration bandwidth = 12 kHz to 5 MHz
100 MHz Output		1.54		ps	Source = PLL1; Qx divider = 8; jitter integration bandwidth = 12 kHz to 20 MHz
400 MHz Output		1.617		ps	Source = PLL1; Qx divider = 2; jitter integration bandwidth = 12 kHz to 20 MHz
LVDS INTEGRATED RMS JITTER					
25 MHz Output		0.535		ps	Source = 25 MHz Taitien XTAL; jitter integration bandwidth = 12 kHz to 5 MHz
100 MHz Output		1.535		ps	Source = PLL1; Qx divider = 8; jitter integration bandwidth = 12 kHz to 20 MHz
400 MHz Output		1.605		ps	Source = PLL1; Qx divider = 2; jitter integration bandwidth = 12 kHz to 20 MHz
2.5 V CMOS INTEGRATED RMS JITTER					
25 MHz Output		0.17		ps	Source = 25 MHz Taitien XTAL; jitter integration bandwidth = 12 kHz to 5 MHz
100 MHz Output		1.669		ps	Source = PLL1; Qx divider = 8; jitter integration bandwidth = 12 kHz to 20 MHz
400 MHz Output		1.586		ps	Source = PLL1; Qx divider = 2; jitter integration bandwidth = 12 kHz to 20 MHz

OUT8 TO OUT10 CHANNEL CYCLE TO CYCLE CLOCK JITTER SPECIFICATIONS

Frequency multiplier (×2) at PLL input enabled. Cycle to cycle jitter magnitude varies with respect to the clock edge (rising or falling). Table 12 indicates jitter for the worst edge (rising or falling). The better edge typically offers a factor of 2 improvement over the tabulated jitter.

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS CYCLE TO CYCLE JITTER					Peak-to-peak jitter, 10,000 cycles
66.6 MHz Output		43.9		ps	
133.3 MHz Output		30.3		ps	
1.8 V CMOS CYCLE TO CYCLE JITTER					Peak-to-peak jitter, 10,000 cycles
66.6 MHz Output		35.3		ps	
133.3 MHz Output		27.4		ps	
3.3 V CMOS CYCLE TO CYCLE JITTER					Peak-to-peak jitter, 10,000 cycles
33.3 MHz Output		83		ps	
66.6 MHz Output		44.9		ps	
133.3 MHz Output		65.4		ps	

LOGIC INPUT PINS CHARACTERISTICS—REF_SEL, $\overline{\text{RESET}}$, SPx, PPRx

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT STATIC CHARACTERISTICS					
REF_SEL Pin					Internal 30 kΩ pull-down resistor
Logic 1 Voltage (V_{IH})	2.11			V	
Logic 0 Voltage (V_{IL})			1.0	V	
Logic 1 Current (I_{IH})			195	µA	$V_{IH} = V_{DD_x}$; value represents the magnitude of current draw
Logic 0 Current (I_{IL})			0.25	µA	V_{IL} = GND; value represents the magnitude of current draw
$\overline{\text{RESET}}$ Pin					Internal 30 kΩ pull-up resistor
Logic 1 Voltage (V_{IH})	1.9			V	
Logic 0 Voltage (V_{IL})			0.9	V	
Logic 1 Current (I_{IH})			0.04	µA	$V_{IH} = V_{DD_x}$; value represents the magnitude of current draw
Logic 0 Current (I_{IL})			260	µA	V_{IL} = GND; value represents the magnitude of current draw
SPx Pins					
Logic 1 Voltage (V_{IH})	V_{DD_x} – 0.5			V	
Logic 0 Voltage (V_{IL})			0.28	V	
Logic 1 Current (I_{IH})			95	µA	$V_{IH} = V_{DD_x}$; value represents the magnitude of current draw
Logic 0 Current (I_{IL})			0.04	µA	V_{IL} = GND; value represents the magnitude of current draw
RESET TIMING					
Pule Width Low	1.25			ns	
$\overline{\text{RESET}}$ Inactive to Start of Register Programming	1.25			ns	
PPR0 TO PPR3 PINS EXTERNAL TERMINATION					Maximum resistor tolerance = 10%
State 0		820		Ω	Pull-down to GND
State 1		1800		Ω	Pull-down to GND
State 2		3900		Ω	Pull-down to GND
State 3		8200		Ω	Pull-down to GND
State 4		820		Ω	Pull-up to V_{DD_x}
State 5		1800		Ω	Pull-up to V_{DD_x}
State 6		3900		Ω	Pull-up to V_{DD_x}
State 7		8200		Ω	Pull-up to V_{DD_x}

STATUS OUTPUT PINS CHARACTERISTICS—LD_0, LD_1, REF_SW, REF_STATUS, REF_ACT

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					I_{LOAD} = 1 mA (source or sink)
Logic 1 Voltage	V_{DD_x} – 0.1			V	
Logic 0 Voltage			0.03	V	

SERIAL CONTROL PORT SPECIFICATIONS

Serial Port Interface (SPI) Mode

Table 15.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)						Input pin
Input Voltage						
Logic 1		V_{DD_x} – 0.3			V	
Logic 0				0.71	V	
Input Current						
Logic 1			–0.2		nA	
Logic 0			–0.3		nA	
Input Capacitance			2		pF	
SCLK (INPUT) IN SPI MODE						
Input Voltage						
Logic 1		V_{DD_x} – 0.3			V	
Logic 0				0.71	V	
Input Current						
Logic 1			–0.7		nA	
Logic 0			–0.6		nA	
Input Capacitance			2		pF	
SDIO (INPUT)						Pin is bidirectional
Input Voltage						
Logic 1		V_{DD_x} – 0.3			V	
Logic 0				0.71	V	
Input Current						
Logic 1			0.7		nA	
Logic 0			–0.8		nA	
Input Capacitance			2		pF	
SDIO (OUTPUT)						Pin is bidirectional
Output Voltage						
Logic 1		V_{DD_x} – 0.1			V	
Logic 0				0.05	V	
TIMING						
Clock Rate (SCLK, $1/t_{SCLK}$)				50	MHz	
Pulse Width High	t_{HIGH}	4			ns	
Pulse Width Low	t_{LOW}	2.2			ns	
SDIO to SCLK Setup	t_{DS}	2.5			ns	
SCLK to SDIO Hold	t_{DH}	2.7			ns	
SCLK to Valid SDIO and SDO	t_{DV}			6.44	ns	
$\overline{CS}$ to SCLK Setup	t_S	0			ns	
$\overline{CS}$ to SCLK Hold	t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High	t_{PWH}	2.7			ns	

I²C Mode

Table 16.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL VOLTAGE						When inputting data
Input Logic 1		$0.7 \times V_{DD_x}$			V	
Input Logic 0				$0.3 \times V_{DD_x}$	V	
Input Current		−10		+10	µA	Input voltage between $0.1 \times V_{DD_x}$ and $0.9 \times V_{DD_x}$
Hysteresis of Schmitt Trigger Inputs		$0.015 \times V_{DD_x}$			V	
SDA						When outputting data
Output Logic 0 Voltage at 3 mA Sink Current				0.2	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX}		$20 + 0.1\ C_B$[1]		250	ns	Bus capacitance from 10 pF to 400 pF
TIMING						All I²C timing values are referred to VIH_{MIN} ($0.3 \times V_{DD}$) and VIL_{MAX} levels ($0.7 \times V_{DD}$)
Clock Rate (SCL, f_{I2C})				400	kHz	
Bus Free Time Between a Stop and Start Condition	t_{BUF}	1.3			µs	
Setup Time for a Repeated Start Condition	$t_{SU;\ STA}$	0.6			µs	
Hold Time (Repeated) Start Condition	$t_{HD;\ STA}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for a Stop Condition	$t_{SU;\ STO}$	0.6			µs	
Low Period of the SCL Clock	t_{LOW}	1.3			µs	
High Period of the SCL Clock	t_{HIGH}	0.6			µs	
SCL, SDA Rise Time	t_R	$20 + 0.1\ C_B$[1]		300	ns	
SCL, SDA Fall Time	t_F	$20 + 0.1\ C_B$[1]		300	ns	
Data Setup Time	$t_{SU;\ DAT}$	100			ns	
Data Hold Time	$t_{HD;\ DAT}$	0			ns	
Capacitive Load for Each Bus Line	C_B[1]			400	pF	

[1] C_B is the capacitance of one bus line in picofarads (pF).

ABSOLUTE MAXIMUM RATINGS

Table 17.

Parameter	Rating
V_{DD_x} to GND	−0.3 V to +3.6 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C

[1] See Table 18 for θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 18. Thermal Resistance

Package Type	θ_{JA}	Unit
CP-64-17[1]	22.7	°C/W

[1] Thermal impedance is based on a 4-layer board in still air in accordance with a JEDEC JESD51-7 plus JEDEC JESD51-5 2S2P test board and in accordance with JEDEC JESD51-2 (still air).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

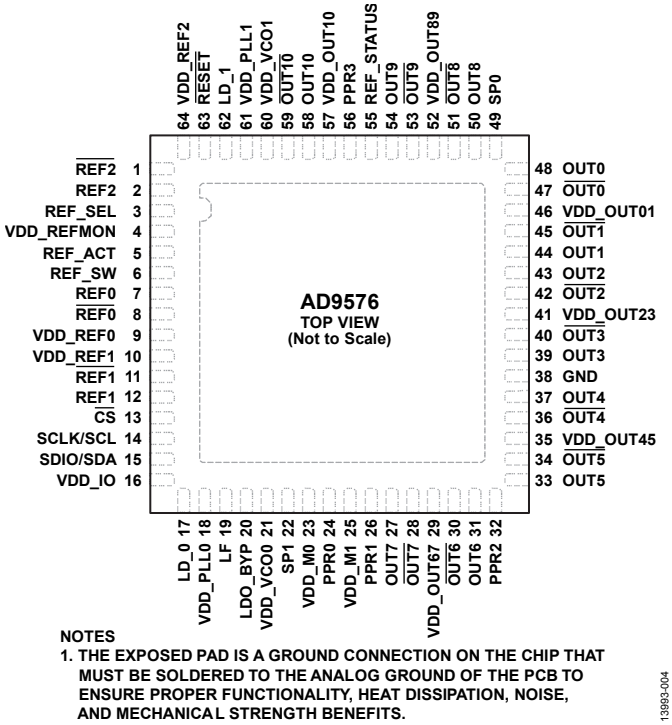


Figure 4. Pin Configuration

Table 19. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1	$\overline{\text{REF2}}$	Input	Configurable clock input	Complimentary Reference Clock Input 2. This pin is the complimentary signal to the input on Pin 2 (REF2). When REF2 is configured as 2.5 V/3.3 V, dc-coupled, single-ended LVCMOS, leave this pin floating. When REF2 is configured as 1.8 V, ac-coupled, single-ended LVCMOS, this pin must be ac grounded via a 100 nF capacitor.
2	REF2	Input	Configurable clock input	Reference Clock Input 2. This clock can serve as the stable clock input to the reference monitor, as well as an input to PLL1. Its format can be configured as 2.5 V/3.3 V, dc-coupled, single-ended LVCMOS, or 1.8 V, ac-coupled, single-ended LVCMOS, differential input (with a complimentary signal on $\overline{\text{REF2}}$, Pin 1, or as an XTAL input. The receiver format is power-on configurable via PPR0 (Pin 24) and is independently configurable via the serial port.
3	REF_SEL	Input	2.5 V/3.3 V CMOS control	Reference Clock Select. This pin selects the output clock of the reference selection mux, which can be either Reference Clock Input 0 or Reference Clock Input 1 (Logic 0 or Logic 1, respectively). For this pin to function, automatic reference switching and soft REF_SEL must be disabled (Register 0x082, Bits[2:1] = 00). This pin has an internal 30 kΩ pull-down resistor.
4	VDD_REFMON	Input	Power	2.5 V or 3.3 V Power Supply.
5	REF_ACT	Output	2.5 V/3.3 V CMOS	Currently Selected, Active Reference Indicator. This status signal represents the output of the reference selector mux. Logic 0 means that REF0 is the currently selected reference, Logic 1 means that REF1 is the currently selected reference. This pin is on the VDD_REFMON power domain.
6	REF_SW	Output	2.5 V/3.3 V CMOS	Reference Switchover Status Indicator. Logic 0 = normal operation, Logic 1 means reference switch in progress. This pin is on the VDD_REFMON power domain.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
7	REF0	Input	Configurable clock input	Reference Clock Input 0. This clock is an input to the reference selection mux. The clock format can be configured as 2.5 V/3.3 V, dc-coupled, single-ended LVCMOS, or 1.8 V, ac-coupled, single-ended LVCMOS, differential input (with a complimentary signal on $\overline{\text{REF0}}$, Pin 8), or as an XTAL input. The receiver format is power-on configurable via PPR0 (Pin 24) and is independently configurable via the serial port.
8	$\overline{\text{REF0}}$	Input	Configurable clock input	Complimentary Reference Clock Input 0. Complimentary signal to the input on Pin 7 (REF0). When REF0 is configured as 2.5 V/3.3 V, dc-coupled, single-ended LVCMOS, leave this pin floating. When REF0 is configured as 1.8 V, ac-coupled, single-ended LVCMOS, this pin must be ac grounded via a 100 nF capacitor.
9	VDD_REF0	Input	Power	2.5 V or 3.3 V Power Supply. Configure this supply to set the full swing CMOS logic high level of Reference Input 0, REF0.
10	VDD_REF1	Input	Power	2.5 V or 3.3 V Power Supply. Configure this supply to set the full swing CMOS logic high level of Reference Input 1, REF1.
11	$\overline{\text{REF1}}$	Input	Configurable clock input	Complimentary Reference Clock Input 1. Complimentary signal to the input on Pin 12 (REF1). When REF1 is configured as 2.5 V/3.3 V, dc-coupled, single-ended LVCMOS, leave this pin floating. When REF1 is configured as 1.8 V, ac-coupled, single-ended LVCMOS, this pin must be ac grounded via a 100 nF capacitor.
12	REF1	Input	Configurable clock output	Reference Clock Input 1. This clock is an input to the reference selection mux. The clock format can be configured as 2.5 V/3.3 V, dc-coupled, single-ended LVCMOS, or 1.8 V, ac-coupled, single-ended LVCMOS, differential input (with a complimentary signal on $\overline{\text{REF1}}$, Pin 11), or as an XTAL input. The receiver format is power-on configurable via PPR0 (Pin 24) and is independently configurable via the serial port.
13	$\overline{\text{CS}}$	Input	2.5 V/3.3 V CMOS	Chip Select for SPI Serial Communication (Active Low Input). When programming the device in SPI mode, this pin must be held low, as shown in Figure 32. The logic high level of this pin is determined by VDD_IO.
14	SCLK/SCL	Input	2.5 V/3.3 V CMOS	Serial Control Port Clock Signal for SPI Mode (SCLK) or I^2C Mode (SCL). This pin is the data clock for serial programming. The logic high level of this pin is determined by the VDD_IO pin.
15	SDIO/SDA	Input/ output	2.5 V/3.3 V CMOS	Serial Control Port Bidirectional Serial Data In/Data Out for SPI Mode (SDIO) or I^2C Mode (SDA). The logic high level of this pin is determined by V_{DD_IO}.
16	VDD_IO	Input	Power	2.5 V or 3.3 V Power Supply. Configure this pin to set the logic high level of the serial port interface.
17	LD_0	Output	2.5 V/3.3 V CMOS	PLL0 Lock Detector Status. Logic 0 means unlocked; Logic 1 means locked.
18	VDD_PLL0	Input	Power	2.5 V or 3.3 V Power Supply.
19	LF	Input	Analog	Loop Filter. Connect a 4.7 nF capacitor from this pin to LDO_BYP (Pin 20).
20	LDO_BYP	Input	Analog	LDO Bypass. Connect a 470 nF capacitor from this pin to ground.
21	VDD_VCO0	Input	Power	2.5 V or 3.3 V Power Supply.
22, 49	SP1, SP0	Input/ output	Control	Serial Port Configuration Pins. These pins are latched at power-up and upon release from reset to configure the serial port as well as to determine whether a PPR load is to occur. See Table 35 for a complete decode of configurations. These pins use three-state logic: high, low, and floating.
23	VDD_M0	Input	Power	2.5 V or 3.3 V Power Supply.
24	PPR0	Input	Control	Pin Program Reader 0. Connect a resistor to this pin to configure the reference clock input formats and the PLL1 input source.
25	VDD_M1	Input	Power	2.5 V or 3.3 V Power Supply.
26	PPR1	Input	Control	Pin Program Reader 1. Connect a resistor to this pin to configure the OUT10 frequency, input source, and logic format.
27	OUT7	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 7. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
28	$\overline{\text{OUT7}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 7. This pin is the complimentary signal to the output on Pin 27 (OUT7).
29	VDD_OUT67	Input	Power	2.5 V or 3.3 V Power Supply.
30	$\overline{\text{OUT6}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 6. This pin is the complimentary signal to the output on Pin 31 (OUT6).

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
31	OUT6	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 6. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
32, 56	PPR2, PPR3	Input	Control	Pin Program Reader 2 and Pin Program Reader 3. Connect a resistor to these pins to configure the REF0/REF1 input frequency and OUT0 to OUT9.
33	OUT5	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 5. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
34	$\overline{\text{OUT5}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 5. This pin is the complimentary signal to the output on Pin 33 (OUT5).
35	VDD_OUT45	Input	Power	2.5 V or 3.3 V Power Supply.
36	$\overline{\text{OUT4}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 4. This pin is the complimentary signal to the output on Pin 37 (OUT4).
37	OUT4	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 4. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
38	GND	Input	Ground	Power Supply Common Ground.
39	OUT3	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 3. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
40	$\overline{\text{OUT3}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 3. This pin is the complimentary signal to the output on Pin 39 (OUT3).
41	VDD_OUT23	Input	Power	2.5 V or 3.3 V Power Supply.
42	$\overline{\text{OUT2}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 2. This pin is the complimentary signal to the output on Pin 43 (OUT2).
43	OUT2	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 2. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
44	OUT1	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 1. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
45	$\overline{\text{OUT1}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 1. This pin is the complimentary signal to the output on Pin 44 (OUT1).
46	VDD_OUT01	Input	Power	2.5 V or 3.3 V Power Supply.
47	$\overline{\text{OUT0}}$	Output	HSTL, LVDS, 1.8 V CMOS	Complimentary Clock Output 0. This pin is the complimentary signal to the output on Pin 48 (OUT0).
48	OUT0	Output	HSTL, LVDS, 1.8 V CMOS	Clock Output 0. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
50	OUT8	Output	2.5 V/3.3 V CMOS, 1.8 V CMOS, HSTL, LVDS, HCSL	Clock Output 8. When configured as 2.5 V/3.3 V CMOS, the logic high level is determined by VDD_OUT89. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
51	$\overline{\text{OUT8}}$	Output	2.5 V/3.3 V CMOS, 1.8 V CMOS, HSTL, LVDS, HCSL	Complimentary Clock Output 8. This pin is the complimentary signal to the output on Pin 50 (OUT8).
52	VDD_OUT89	Input	Power	2.5 V or 3.3 V Power Supply. Configure this supply to set the full swing CMOS logic high level of Output 8 and Output 9.
53	$\overline{\text{OUT9}}$	Output	2.5 V/3.3 V CMOS, 1.8 V CMOS, HSTL, LVDS, HCSL	Complimentary Clock Output 9. This pin is the complimentary signal to the output on Pin 54 (OUT9).
54	OUT9	Output	2.5 V/3.3 V CMOS, 1.8 V CMOS, HSTL, LVDS, HCSL	Clock Output 9. When configured as 2.5 V/3.3 V CMOS, the logic high level is determined by VDD_OUT89. The power-on format is determined via PPR2 (Pin 32) and PPR3 (Pin 56). This pin is independently configurable via the serial port.
55	REF_STATUS	Output	2.5 V/3.3 V CMOS	Reference Status Indicator. When the reference monitor is enabled, this pin indicates if the output of the reference selection mux is determined to be within the configured tolerance setting. Logic 0 means the reference is within tolerance; Logic 1 means the reference is outside of tolerance. When the reference monitor is disabled, this pin indicates the loss of reference (LOR) status for the requested reference.
57	VDD_OUT10	Input	Power	2.5 V or 3.3 V Power Supply. Configure this supply to set the full swing CMOS logic high level of Output 10. This pin also serves as the PPRx power supply.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
58	OUT10	Output	2.5 V/3.3 V CMOS, 1.8 V CMOS, HSTL, LVDS, HCSL	Clock Output 10. When configured as 2.5 V/3.3 V CMOS, the logic high level is determined by VDD_OUT10. The power-on format is determined via PPR1 (Pin 26). This pin is independently configurable via the serial port.
59	$\overline{\text{OUT10}}$	Output	2.5 V/3.3 V CMOS, 1.8 V CMOS, HSTL, LVDS, HCSL	Complimentary Clock Output 10. This pin is the complimentary signal to the output on Pin 58 (OUT10).
60	VDD_VCO1	Input	Power	2.5 V or 3.3 V Power Supply.
61	VDD_PLL1	Input	Power	2.5 V or 3.3 V Power Supply.
62	LD_1	Output	2.5 V/3.3 V CMOS	PLL1 Lock Detector Status. Logic 0 means unlocked; Logic 1 means locked.
63	$\overline{\text{RESET}}$	Input	Control	Reset. Logic 0 initializes the device to its default state (see the PPRx Pins section for details). This pin has an internal 30 kΩ pull-up resistor.
64	VDD_REF2	Input	Power	2.5 V or 3.3 V Power Supply. Configure this supply to set the full swing CMOS logic high level of Reference Input 2, REF2.
	EPAD	Input	Ground	Exposed Pad. The exposed pad is a ground connection on the chip that must be soldered to the analog ground of the PCB to ensure proper functionality, heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

PHASE NOISE AND VOLTAGE WAVEFORMS

V_{DD_x} = nominal, T_A = 25°C. The only enabled output channels are those indicated in the figure captions. The phase noise plots (see Figure 5 to Figure 9) show the Taitien XO A0145-L-006-3 (noted as XO in the figures) phase noise normalized to the output frequency. The voltage waveform plots (see Figure 10 to Figure 16) embody ac coupling to the measurement instrument.

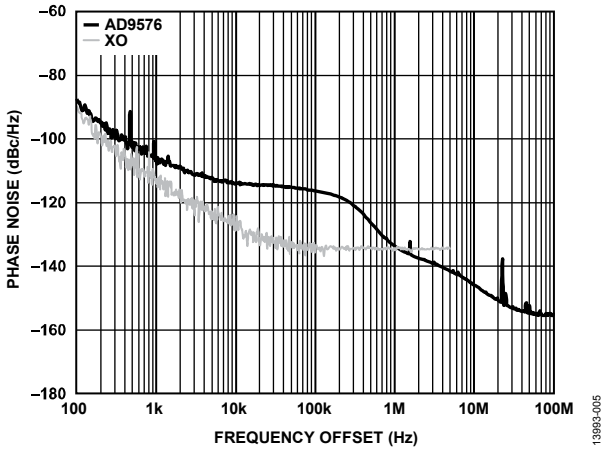


Figure 5. Phase Noise (OUT0)—f_{OUT0} = 644.53125 MHz (HSTL), Fractional

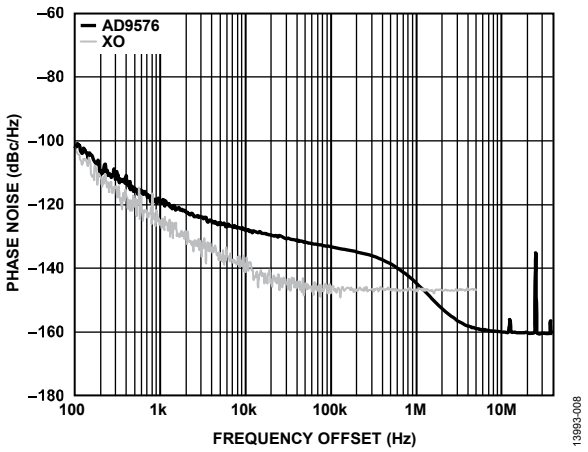


Figure 8. Phase Noise (OUT2)—f_{OUT2} = 156.25 MHz (HSTL)

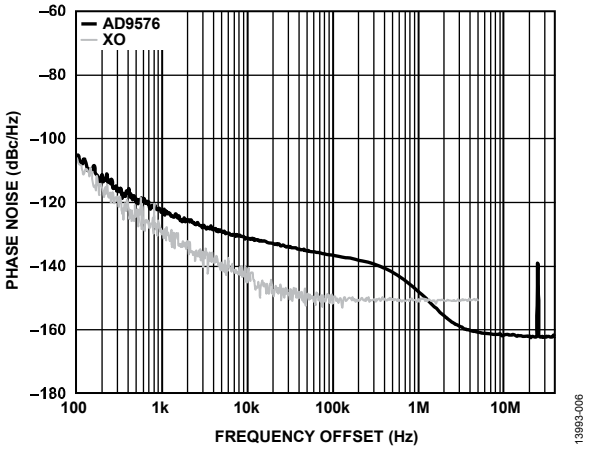


Figure 6. Phase Noise (OUT3)—f_{OUT3} = 100 MHz (HSTL), f_{OUT4} = 125 MHz (HSTL)

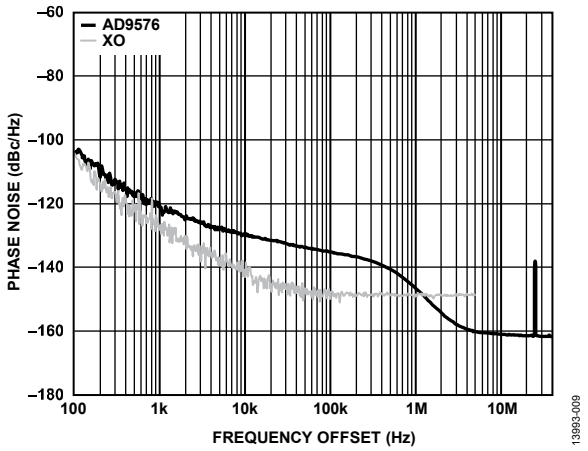


Figure 9. Phase Noise (OUT3)—f_{OUT3} = 125 MHz (HSTL), f_{OUT4} = 100 MHz (HSTL)

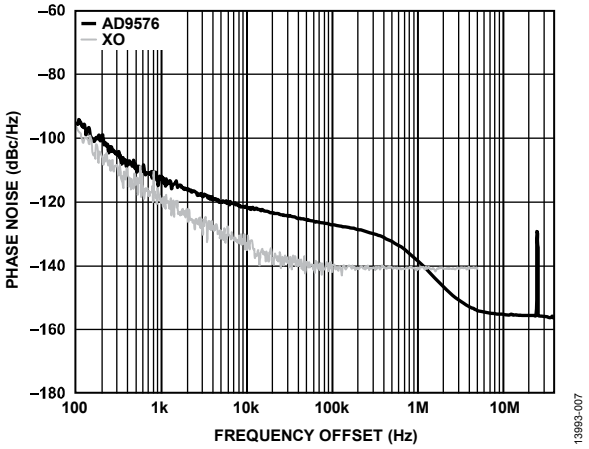


Figure 7. Phase Noise (OUT4)—f_{OUT4} = 312.5 MHz (LVDS)

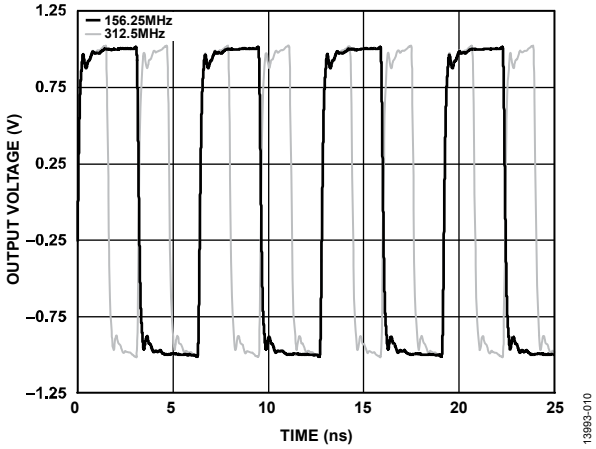


Figure 10. OUT0 Output Waveform, HSTL (156.25 MHz, 312.5 MHz)

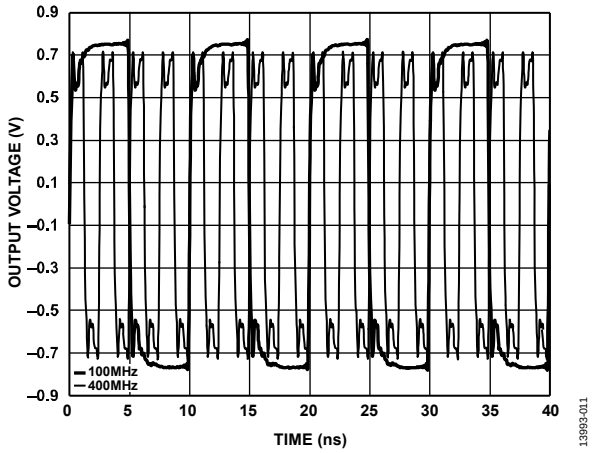


Figure 11. OUT8 Output Waveform, HCSL (100 MHz, 400 MHz)

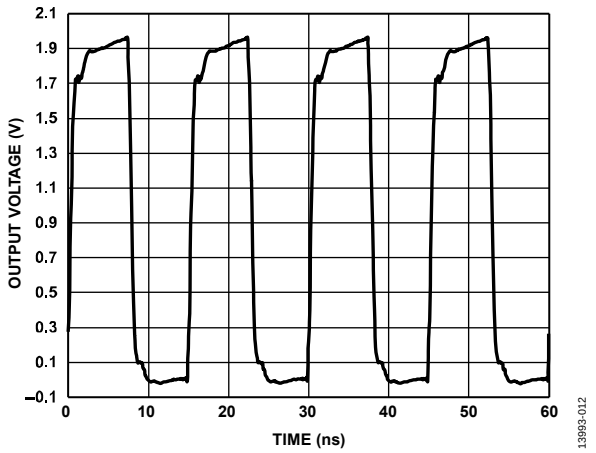


Figure 12. OUT8 Output Waveform, 1.8 V CMOS (66.67 MHz), 10 pF Load

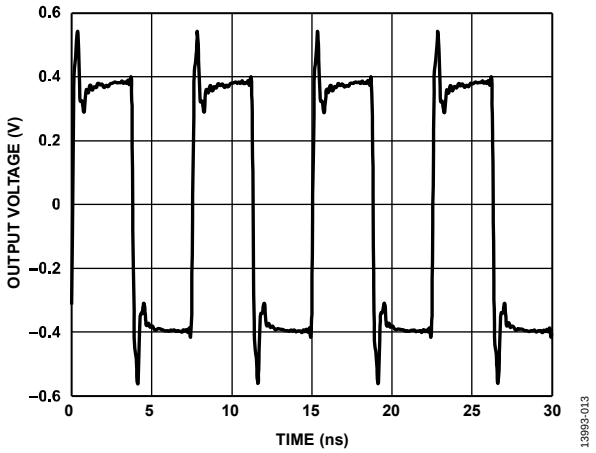


Figure 13. OUT8 Output Waveform, LVDS (133.3 MHz)

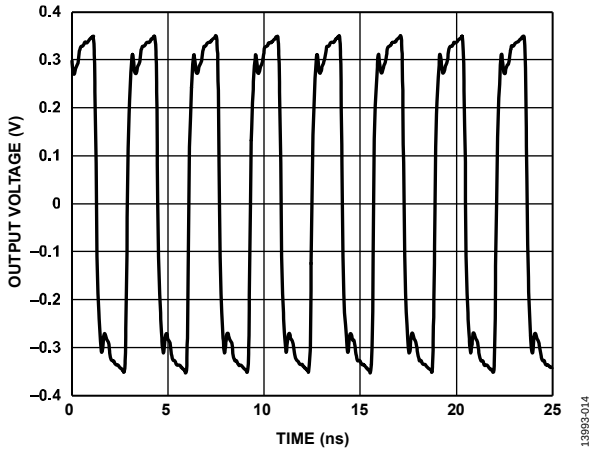


Figure 14. OUT0 Output Waveform, LVDS (312.5 MHz)

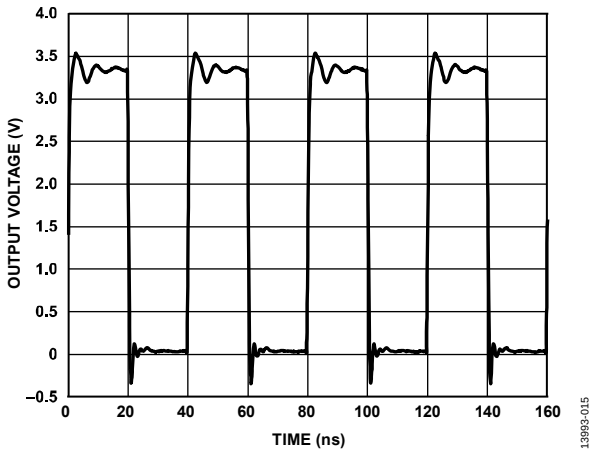


Figure 15. OUT8 Output Waveform, 3.3 V CMOS (25 MHz), 10 pF Load

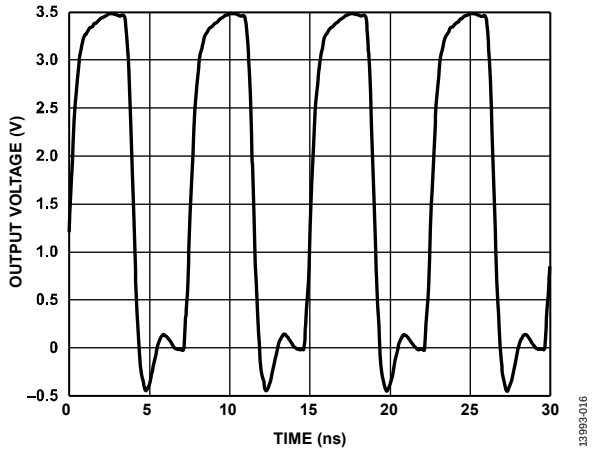


Figure 16. OUT8 Output Waveform, 3.3 V CMOS (133.3 MHz), 10 pF Load

REFERENCE SWITCHING FREQUENCY AND PHASE DISTURBANCE

V_{DD_x} = nominal, T_A = 25°C. The only enabled output channels are those indicated in the figure captions. The reference switchover phase disturbance plots, Figure 17, Figure 18, and Figure 19, each show a collection of output phase variations due to approximately 250 reference switching events between two references with a frequency offset of approximately 2 ppm. Each reference switch event (initiated by toggling the REF_SEL pin) occurs at a random phase offset between the two references. The plots demonstrate the tightly controlled phase disturbance at the output as a result of the reference switching logic seeking the optimal moment to switch references.

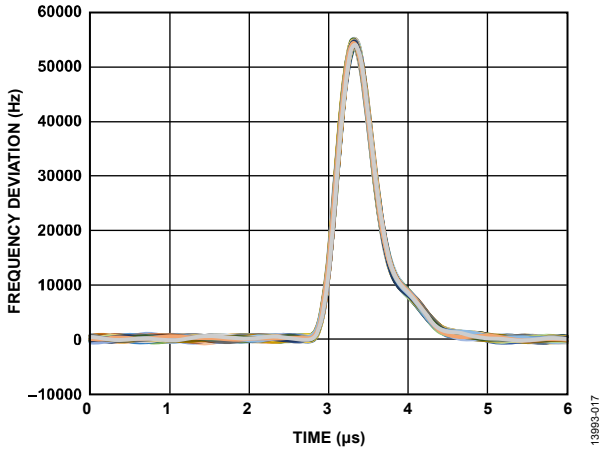


Figure 17. Reference Smooth Switchover Frequency Disturbance for OUT0 at 156.25 MHz (PPR0 = 3, PPR1 = 0, PPR2 = 0, PPR3 = 3)

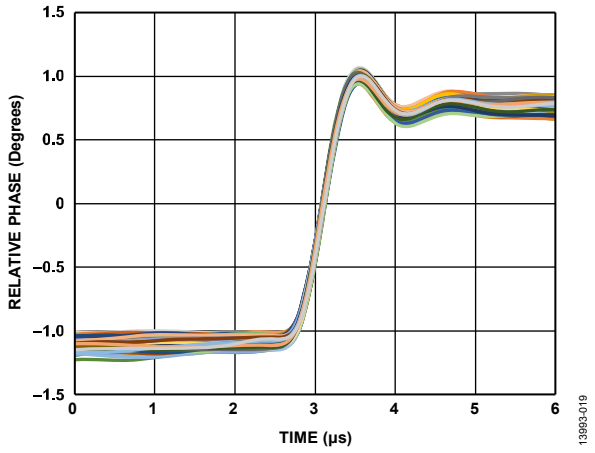


Figure 19. Reference Smooth Switchover Phase Disturbance for OUT8 at 25 MHz (PPR0 = 3, PPR1 = 0, PPR2 = 0, PPR3 = 3)

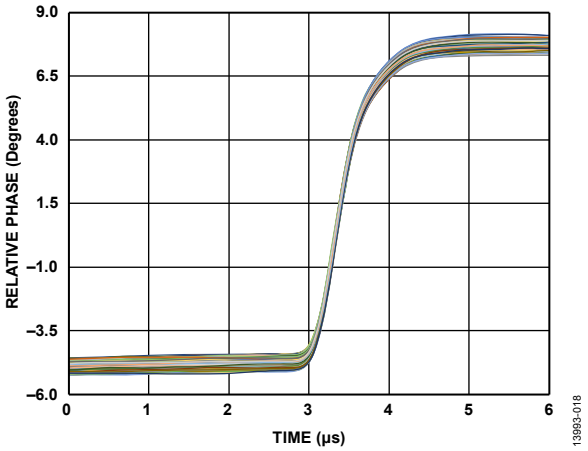


Figure 18. Reference Smooth Switchover Phase Disturbance for OUT0 at 156.25 MHz (PPR0 = 3, PPR1 = 0, PPR2 = 0, PPR3 = 3)

TERMINOLOGY

Phase Jitter
An ideal sine wave has a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is character-ized statistically as Gaussian (normal) in distribution.

This phase jitter leads to the energy of the sine wave spreading out in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Phase Noise
When the total power contained within some interval of offset frequencies (for example, 12 kHz to 20 MHz) is integrated, it is called the integrated phase noise over that frequency offset interval, and it can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on error rate performance by increasing eye closure at the transmitter output and reducing the jitter tolerance/sensitivity of the receiver.

Time Jitter
Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 Σ of the Gaussian distribution.

Additive Phase Noise
Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is sub-tracted, which makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter
Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted, which makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

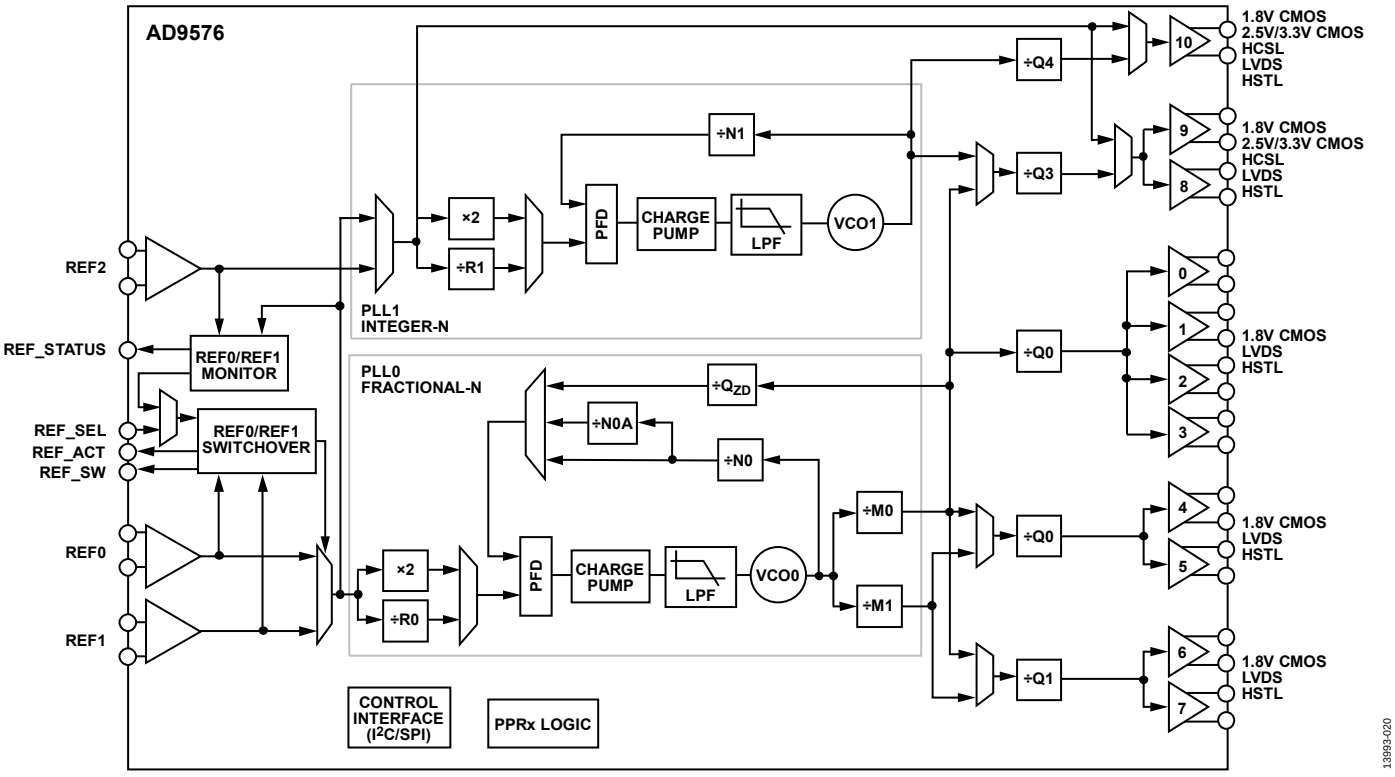


Figure 20. Detailed Functional Block Diagram

OVERVIEW

Figure 20 shows a block diagram of the AD9576. The AD9576 is a 2.5 V or 3.3 V single-supply, pin programmable, power-on ready, dual-channel clock that is fully configurable via a serial port interface (SPI). The two parallel channels consist of a high performance, fractional-N PLL (PLL0) and a general-purpose, integer-N PLL (PLL1).

There are a total of three reference inputs (REF0 to REF2) on the AD9576. Each input receiver provides differential or single-ended input configurations. REF0 and REF1 drive the reference switchover multiplexer (mux). The output of this reference switchover mux drives the input of PLL0 and an input to the PLL1 reference selection mux. REF2 drives the alternate input of the PLL1 reference selection mux and serves as monitor clock to the on-board reference monitor, which monitors the reference switchover mux output clock frequency. REF2 supports frequencies of 8 kHz, 10 MHz, 19.44 MHz, 25 MHz, and 38.88 MHz, while REF0 and REF1 support 8 kHz, 1.544 MHz, 2.048 MHz, and 10 MHz to 325 MHz. However, the PLL1 phase and PFD input rate is limited to 25 MHz or 50 MHz, so only a subset of allowable reference input frequencies are valid for use as an input to PLL1.

The AD9576 provides up to 11 output channel clocks (OUT0 to OUT10). OUT0 to OUT7 are driven by PLL0 exclusively and are comprised of three subgroups of outputs (OUT0 to OUT3, OUT4 and OUT5, and OUT6 and OUT7). Each output within a subgroup is individually configurable, but generates the same output frequency. These outputs support LVDS, HSTL, or 1.8 V LVCMOS output formats.

OUT8 and OUT9 have three potential sources: the output of the PLL1 reference selection mux directly, the output of PLL0, or the output of PLL1. These outputs are individually configurable, but must share the same source and, therefore, the same output frequency. OUT10 is driven by either the output of the PLL1 reference selection mux directly or the output of PLL1. These three outputs support LVDS, HSTL, HCSL, 1.8 V CMOS, and 2.5 V/3.3 V CMOS (the swing is determined by the supply level) output formats.

REFERENCE INPUTS

The AD9576 features a flexible PLL reference input circuit that provides three operating modes: single-ended input, fully differential input, or external crystal input. The operating mode of the REF0, REF1, and REF2 input receivers are selected and controlled by the scanned state of the PPR0 pin or by Register 0x080 and Register 0x081 (see Table 45). Register 0x080 and Register 0x081 allow fully independent control of the operating mode selection for each reference input.

In single-ended CMOS buffer mode, a 2.5 V or 3.3 V clock source is connected directly to the positive reference input pin (for example, REF0). Note that, in single-ended mode, it is best to connect a 0.1 µF capacitor from the negative input pin (for example, $\overline{\text{REF0}}$) to GND. The CMOS swing of the reference input is dependent on V_{DD_x} of said reference input supply and does not exceed V_{DD_x}. The single-ended CMOS receivers are powered down when their individual power-down bits are set in Register 0x080 and Register 0x081, or when operating in differential or external crystal input mode.

In differential mode, a differential clock driver is connected to the two reference input pins (for example, REF0 and $\overline{\text{REF0}}$).

Note that, in differential operating mode, the reference input pins are internally self biased to allow ac coupling. That is, a 0.1 µF capacitor is connected in series from each output of the external differential clock driver to the corresponding reference input pin. This mode also supports a single-ended, 1.8 V CMOS clock source by connecting the source to the positive reference input pins (for example, REF0) with the negative reference input pin (for example, $\overline{\text{REF0}}$) connected to GND via a 0.1 µF capacitor. The differential input receivers are powered down when their individual power-down bits are set in Register 0x080 and Register 0x081, or when operating in single-ended CMOS or external crystal input mode.

External crystal mode is comparable to differential mode, except a fundamental mode AT cut crystal is connected across the two reference input pins (REF0 and $\overline{\text{REF0}}$, for example) and is powered by an internal maintaining amplifier. The external crystal receivers are powered down via the individual power down bits in Register 0x080 and Register 0x081, or when operating in single-ended or differential input mode. The REF0 and REF1 external crystal receivers are also powered down if they are not the currently active/requested reference clock for PLL0.

The reference input format bits, REF0 format (Register 0x080, Bits[1:0]), REF1 format (Register 0x080, Bits[5:4]), and REF2 format (Register 0x081, Bits[1:0]) must be set correctly for the applied input. These bits are set to 00 for 2.5 V and 3.3 V CMOS inputs, 01 for differential inputs and 1.8 V CMOS inputs, and 10 for XTAL inputs. Setting the reference input format bits incorrectly for the applied input may cause undesired results. The input frequency range for the reference inputs is specified in Table 4.

REFERENCE MONITOR

The AD9576 reference monitor function provides the user a means to validate the frequency accuracy of the PLL0 active reference (REF0 or REF1) in real time. When enabled, the reference monitor uses REF2 as the frequency reference to continuously test the frequency accuracy of the active reference. The measured frequency error of the PLL0 active input reference is compared to a user programmable frequency error threshold. The result is reported as being either within or outside the user specified threshold (see Table 20) on both the reference status bits (Register 0x021, Bits[5:4]) and the REF_STATUS pin. To enable the reference monitor, the user must set the enable reference monitor bit (Register 0x083, Bit 7) to Logic 1. Note that the frequency accuracy of the inactive reference channel is not monitored.

Table 20. Reference Monitor Error Window

Frequency Error Threshold (ppm)	Register 0x083, Bits[1:0] Value
±10	00
±25	01
±50	10
±100	11

Reference monitoring is only supported for two input frequencies, 19.44 MHz and 25 MHz. The user must specify which frequency is to be monitored by configuring the monitored frequency bit (Register 0x083, Bit 5). A Logic 0 value indicates that the PLL0 input frequency is 25 MHz, whereas a Logic 1 indicates a frequency of 19.44 MHz. The reference monitor frequency reference, REF2, can be one of five frequencies selectable via two bit fields, as shown in Table 21.

Table 21. REF2 Monitor Frequency Decode

REF2 Input Frequency	Register 0x083, Bit 4 Value	Register 0x083, Bits[3:2] Value
8 kHz	1	Not applicable
10 MHz	0	00
19.44 MHz	0	01
25 MHz	0	10
38.88 MHz	0	11

After comparing the calculated input frequency ppm error to the user specified threshold window, the resulting frequency accuracy is reported on the reference status bits (Register 0x021. Bits[5:4]) and on the REF_STATUS pin. The values of the reference status bits and the respective significance are listed in Table 22. The status indicated on the REF_STATUS pin is the logical OR of the reference status bits.

Table 22. Reference Frequency Monitor Status Decode

Frequency Status	Register 0x021, Bits[5:4] Value
Valid	00
Slow	01
Fast	10
Indeterminate Fault	11

The REF_STATUS pin similarly reports whether the frequency of the active input is within the user specified threshold window. A Logic 0 on this pin indicates the selected input reference frequency is within the tolerance threshold specified by the user, whereas a Logic 1 indicates the selected input reference frequency is outside the tolerance threshold specified by the user. Note that the REF_STATUS pin only specifies whether the selected input reference frequency is within the user specified tolerance threshold. If more detailed information regarding the manifestation of the error is required, refer to the reference status bits.

In addition to the frequency monitoring function, the reference monitor also checks for the presence of a clock signal at the REF0, REF1, and REF2 inputs. The absence of a clock signal results in an internal LOR indication for that particular clock input. A Logic 1 LOR status indicates that the reference is not present,or that the frequency is below approximately 1 MHz. A Logic 0 status indicates that reference input is detected and the frequency is greater than 1 MHz. When REF2 is configured as an 8 kHz reference to be used with the reference monitor, the REF2 LOR circuitry uses the PLL0 active reference to qualify the presence and accuracy of the REF2 input clock. Table 23 defines the REF2 LOR conditions for all valid operating modes.

Table 23. REF2 LOR Status Decode

REF2 Input Frequency	REF0/REF1 Frequency	Reg. 0x021, Bit 2 Value	REF2 LOR Condition
8 kHz	25 MHz	0	>6.1 kHz
		1	< 6.1 kHz
	19.44 MHz	0	>4.7 kHz
		1	<4.7 kHz
10 MHz, 19.44 MHz, 25 MHz, or 38.88 MHz	Not applicable	0	>1 MHz
		1	<1 MHz

A LOR condition for a given reference is reported on its respective status bit in Register 0x021 (see Table 43). Furthermore, when reference frequency monitoring is disabled, the REF_STATUS pin logic state indicates the LOR status for the PLL0 requested reference input.

REFERENCE SWITCHING

The AD9576 provides both manual switchover as well as a single-shot, automatic XTAL redundancy switchover capability. The reference switchover mode is specified through the enable XTAL redundancy switchover bit (Register 0x082, Bit 2). By default, this bit is Logic 0 and manual reference switching is enabled. Setting this bit to a Logic 1 enables automatic XTAL redundancy switchover.

Automatic XTAL redundancy switchover mode can only be used when the following three conditions are met:

- REF0/REF1 are external crystal inputs (Register 0x080, Bits[5:4] and Register 0x080, Bits[1:0] are both set to 10).
- The reference monitoring function is enabled (Register 0x083, Bit 7 is set to 1).
- The REF_SEL pin is held at a static logic state.

The XTAL redundancy switchover is a single use operation per device reset, switching from the initial input reference (for example, REF0) to the alternate input reference (for example, REF1). When the reference monitor determines the selected input frequency accuracy is outside of the specified error window, the alternate input is automatically selected as the new active reference input. Upon completion of the automatic XTAL redundancy switchover, the newly selected alternate reference (for example, REF1) continues to be the input reference source for PLL0, regardless of the accuracy of the frequency. The initial input reference clock is designated by the state of REF_SEL when the enable XTAL redundancy switchover bit is set to Logic 1.

In manual reference switchover mode, the user manually changes the input reference by toggling the state of either the soft reference select bit (Register 0x082, Bit 0) or the REF_SEL pin (Pin 3). The control method of manual reference switchover is determined by the state of the enable soft reference select bit (Register 0x082, Bit 1), as shown in Table 24.

Table 24. PLL0 Active Reference Selection Source Decode

PLL0 Active Reference Selection Source	Register 0x082, Bit 1 Value
REF_SEL (Pin 3)	0
Register 0x082, Bit 0	1

When the REF_SEL pin controls manual reference switchover, a logic signal is supplied to the pin to specify the desired input reference. A Logic 0 on the REF_SEL pin informs the internal reference switching logic to make REF0 the active reference input, whereas a Logic 1 makes REF1 the active reference. When the soft reference select bit controls manual reference switchover, setting this bit to a Logic 0 selects REF0 as the active reference input, whereas setting this bit to a Logic 1 selects REF1 as the active input reference. Note that, with manual switching enabled, the frequency monitoring function of the reference monitor (see the Reference Monitor section) may still be used, but it does not trigger a reference switchover for PLL0.

Both manual and XTAL redundancy reference switchover modes provide the option of using the smooth switchover function. The smooth switchover function is enabled by setting the disable smooth switchover bit (Register 0x082, Bit 3) to Logic 0. The smooth switchover function waits for a minimal phase offset to occur between the REF0 and REF1 reference inputs, prior to physically switching to the newly requested reference. This functionality ensures a minimal frequency and phase disturbance on the output clocks associated with the PLL due to a reference switchover event. Correct operation of the smooth switchover function requires the input references be asynchronous and that a LOR fault condition does not occur on either reference input while the switch is being made. When the smooth switchover function is disabled (Register 0x082, Bit 3 = 1), the switch to the new active reference is instantaneous and the frequency disturbance on the output clocks during reference switchover may increase.

The reference switching logic provides information about which reference channel is the currently active reference, via the REF_ACT pin (Pin 5) and the active reference bit (Register 0x021, Bit 3). The REF_ACT pin and the active reference bit are both Logic 0 when REF0 is the active reference, and are both Logic 1 when REF1 is the active reference. Additionally, the reference switching logic indicates when the device is in the process of performing a smooth reference switchover via the REF_SW pin (Pin 6). The REF_SW pin assumes a Logic 1 state when REF_SEL changes states and returns to a Logic 0 state when the device

completes the reference switchover process. In manual smooth reference switchover mode, confirm that the device has completed the requested switch to the desired reference (REF_SW pin = Logic 0) before initiating a subsequent change of reference request. Changing the state of the REF_SEL pin or the soft reference select bit before the internal state machine completes the previous smooth reference switching process does not result in a subsequent reference switch.

Because the smooth reference switchover function waits for a minimal phase offset between references prior to making a switch, if either of the reference inputs are removed completely and a switchover request is initiated, the internal smooth switching state machine stalls and the device is unable to switch references, thereby retaining the currently active reference. If the current active reference fails, the device loses lock, thereby necessitating a device reset. If the requested reference fails, the device retains the currently active reference, but switches to the requested reference if it becomes available. Note that, as long as a reference remains absent, the state machine remains stalled. Only a device reset makes the state machine disregard the initial request to switch references.

PLL0 INTEGER-N/FRACTIONAL-N PLL

PLL0 is a fractional-N PLL capable of operating in integer mode. It consists of seven functional elements: a reference frequency prescalar, a PFD, a charge pump, a loop filter, a VCO, feedback dividers, and an optional, third-order, Σ-Δ modulator (SDM) that allows fractional divide ratios. PLL0 provides two independent reference clock input signals. The device supports differential, single-ended, and XTAL operation for both reference clocks. PLL0 provides 10 outputs, segregated into four groups. Each group has a dedicated channel divider allowing the device to produce four different output frequencies simultaneously. Note that PLL0 is capable of several different loop configurations, with each described in the following sections. Figure 21 shows the functional block diagram of PLL0.

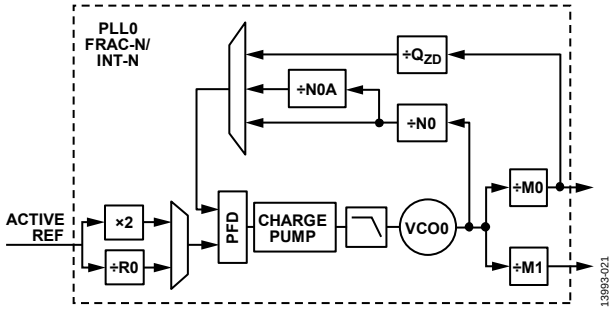


Figure 21. PLL0 Functional Block Diagram

PLL0 Reference Frequency Scaling

The frequency of the active input reference (REF0 or REF1) is scalable via the PLL0 doubler enable bit (Register 0x101, Bit 3) and the R0 divider ratio bits (Register 0x105, Bits[5:0]). This allows the user to scale the input reference frequency to satisfy the input range of the PFD. When the PLL0 doubler enable bit is set to Logic 1, the input frequency to the PFD of PLL0, f_{PFD0}, is twice the active reference input frequency. When the PLL0 doubler enable bit is set to Logic 0, f_{PFD0} is a function of the active reference frequency scaled by the R0 divider ratio bits.

$$f_{PFD0} = \frac{f_{REF}}{R0}$$

where:
f_{REF} is the frequency of the active reference, REF0 or REF1.
$R0$ is the value of the R0 divider ratio bits.

When the PLL0 doubler enable bit is set to Logic 1, the frequency appearing at the input to the PFD of PLL0, f_{PFD0}, is the active reference frequency multiplied by a factor of two.

$$f_{PFD0} = f_{REF} \times 2$$

where f_{REF} is the frequency of the active reference, REF0 or REF1.

Note that, when the ×2 frequency multiplier is in use, the active reference signal must have a duty cycle close to 50%. Otherwise, spurious artifacts (harmonics) may propagate through the signal path and appear at the output of PLL0.

PLL0 Loop Configurations

PLL0 is capable of three different loop configurations. Loop 0 is the fractional translation path, Loop 1 accommodates low frequency reference inputs, and Loop 2 is a zero delay feedback path. The PLL0 loop configuration is selected by programming the PLL0 loop mode bits (Register 0x101, Bits[2:1]) as shown in Table 25.

Table 25. PLL0 Loop Configuration Decode

PLL0 Loop Configuration	Register 0x101, Bits[2:1] Value
Loop 0: Fractional-N/Integer-N	00
Loop 1: Low PFD Frequency	01
Loop 2: Zero Delay	10
Reserved	11

Loop Configuration 0—Fractional-N/Integer-N

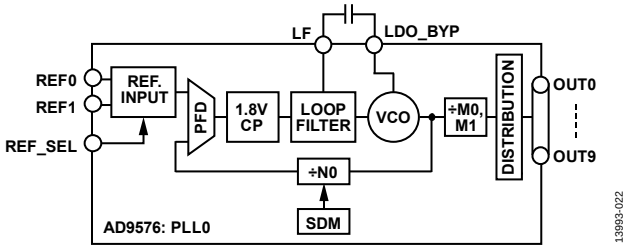


Figure 22. PLL0 Loop Configuration 0

The Loop 0 configuration is the only configuration that supports a fractional-N translation in addition to integer-N translations. This configuration uses a single feedback divider, N0, with an integrated Σ-Δ modulator.

The VCO0 frequency is a function of the PFD input frequency (see the PLL0 Reference Frequency Scaling section) and the values programmed into the registers associated with N0, N0 fraction, and N0 modulus.

$$f_{VCO0} = f_{PFD0} \times \left(N0 + \frac{N0\ \ fraction}{N0\ \ modulus} \right)$$

where:
f_{VCO0} is the frequency of the VCO.
f_{PFD0} is the frequency at the input to the PFD.
N0 is an element of the following set: {N_{MIN}, N_{MIN} + 1, …, 255}, where N_{MIN} = 12 for integer-N operation and N_{MIN} = 15 for fractional-N operation.
N0 fraction is an element of the following set: {0, 1, …, 16,777,214}.
N0 modulus is an element of the following set, but with the constraint of *N0 fraction* < *N0 modulus:* {1, 2, …, 16,777,215}.

Programming the N0 SDM power-down bit (Register 0x101, Bit 0) to Logic 1 disables the SDM, making N0 fraction functionally equivalent to a value of 0, and PLL0 can only be configured as an integer-N PLL. This is also the case if N0 fraction is programmed to 0; however, the SDM circuitry is not placed into a low power state. Integer-N operation yields the best performance in terms of phase noise, spurs, and jitter.

To obtain the best performance in fractional-N operation, configure the N0 modulus value to the largest possible value as allowed by the fractional translation being synthesized. For example, if a 19.44 MHz input is being translated to a 625 MHz output, the required VCO operating frequency is 2500 MHz. Using the input doubler, this requires an N divider value of 64 + 73/243. To make the modulus as large as possible, both the modulus and fraction values must be multiplied by the same scaling value. The scaling value is calculated as follows:

$$Scalar = \text{floor}\left(\frac{2^{24} - 1}{modulus} \right) = \text{floor}\left(\frac{16{,}777{,}215}{243} \right) = 69{,}042$$

The resulting values to be used as the operating N0 fraction and N0 modulus values are as follows:

$$N0\ fraction = scalar \times 73 = 69{,}042 \times 73 = 5{,}040{,}066$$

$$N0\ modulus = scalar \times 243 = 69{,}042 \times 243 = 16{,}777{,}206$$

The overall frequency translation equation for Loop 0 is

$$f_{OUT} = \frac{f_{REF}}{R0} \times \frac{\left(N0 + \frac{N0\ fraction}{N0\ modulus} \right)}{M_Z \times Q_Y}$$

where:
f_{OUT} is the frequency at the output driver, OUTx (OUT0 through OUT9).
f_{REF} is the frequency of the active reference (REF0 or REF1).
M_Z is the VCO divider (M0 or M1) that is the input source of Q_Y.
Q_Y is the channel divider (Q0, Q1, Q2, or Q3) associated with OUTx.
R0 is the divider value used to scale the input reference frequency and is an element of the following set: {½, 1, 2 … 63}. Note the value of ½ is the result of selecting the ×2 reference multiplier (see the PLL0 Reference Frequency Scaling section).

N0 is an element of the set: {N_{MIN}, N_{MIN} + 1, …N_{MAX}} where N_{MIN}, N_{MAX} are 12 and 255, respectively, for integer-N operation and N_{MIN}, N_{MAX} are 15 and 252, respectively, for fractional-N operation.
N0 fraction is an element of the set: {0, 1, …, 16,777,214}.
N0 modulus is an element of the set: {1, 2, …, 16,777,215} with the constraint N0 fraction < N0 modulus.
M_Z is the divide value of the VCO divider and is an element of the set: {2, 3, …, 11}.
Q_Y is the divide value of the channel divider and is an element of the set: {1, 2, …, 64}.

Loop Configuration 1—Low PFD Frequency

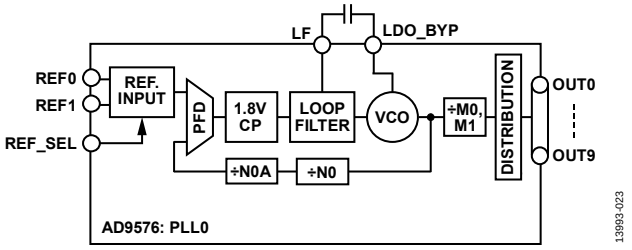


Figure 23. PLL0 Loop Configuration 1

The Loop 1 configuration is an integer-N configuration that uses a cascade of two feedback dividers, N0 and N0A, to operate at much lower PFD frequencies. In this configuration, the charge pump current is internally set to a value of 1024 µA, an internal switch shorts R_{ZERO} in the integrated loop filter and automatically sets the integrated pole capacitor (CPOLE2) to 100 pF. This particular internal loop filter configuration provides the flexibility to set the response zero and the first pole frequency of the loop filter (via an external R-C network) to accommodate a low PFD rate. Note that Loop 1 configures PLL0 as an integer-N PLL only. Therefore, to ensure proper device operation, the N0 SDM

power-down bit must be set to Logic 1, or the N0 fraction value must be set to 0.

The VCO0 frequency is a function of the PFD input frequency (see the PLL0 Reference Frequency Scaling section) and the values programmed into the registers associated with N0 and N0A.

$$f_{VCO0} = f_{PFD0} \times N0 \times N0A$$

The divider value of N0 is set by programming the N0 divider integer value bits to a value between 12 and 255. N0A is a 12-bit divider that is set by programming the N0A Divider Ratio[11:0] bits (Register 0x10E, Bits[7:0] and Register 0x10F, Bits[3:0]) as shown in Table 26.

Table 26. N0A Divider Ratio Decode

N0A Divider Ratio[11:0] Value	Divider Operation
0 to 3	Invalid setting
4 to 4095	Divide by this value

The overall frequency translation equation for Loop 1 is as follows:

$$f_{OUT} = \frac{f_{REF}}{R0} \times \frac{(N0 \times N0A)}{M_Z \times Q_Y}$$

where:
f_{OUT} is the frequency at the output driver, OUTx (OUT0 through OUT9).
f_{REF} is the frequency of the active reference (REF0 or REF1).
M_Z is the VCO divider (M0 or M1) that is the input source of Q_Y.
Q_Y is the channel divider (Q0, Q1, Q2, or Q3) associated with OUTx.

R0 is the divider value used to scale the input reference frequency and is an element of the following set: {½, 1, 2 … 63}. Note that the value of ½ is the result of selecting the ×2 reference multiplier (see the PLL0 Reference Frequency Scaling section).

N0 is an element of the following set: {12, 13 … 255}.

N0A is an element of the following set: {4, 5 … 4095}.

M_Z is the divide value of the VCO divider and is an element of the following set: {2, 3 … 11}.

Q_Y is the divide value of the channel divider and is an element of the following set: {1, 2 … 64}.

Loop Configuration 2—Zero Delay

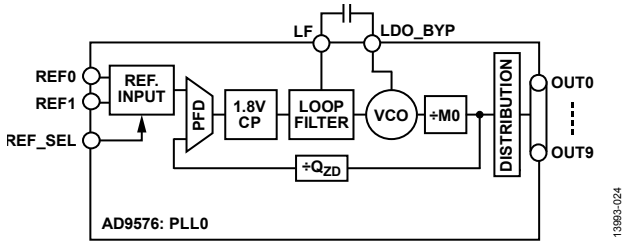


Figure 24. PLL0 Loop Configuration 2

In the Loop 2 configuration, the total feedback division ratio is a cascade of the VCO divider, M0, and the channel divider, Q_{ZD}. The channel divider, Q_{ZD}, operates identically to any other channel divider configured with M0 as an input clock source; however, the output of the divider is not routed to an output driver, but rather to the PLL0 PFD feedback clock input. This feedback scheme, along with Q_{ZD} being synchronized with the other channel dividers (see the Synchronization section) allows the loop to establish a minimal delay between the rising edges of the reference input and the output clocks. See the PLL0 VCO Calibration section for information concerning the impact of the Q_{ZD} synchronization on the VCO0 calibration procedure.

The VCO0 frequency is a function of the PFD input frequency (see the PLL0 Reference Frequency Scaling section) and the values programmed into the registers associated with M0 and Q_{ZD}.

$$f_{VCO0} = f_{PFD0} \times (M0 \times Q_{ZD})$$

M0 is described in detail in the PLL0 VCO Dividers (M0 and M1) section and Q_{ZD} is described in detail in the Channel Dividers section.

The overall frequency translation equation for Loop 2 is as follows:

$$f_{OUT} = \frac{f_{REF}}{R0} \times \frac{M0 \times Q_{ZD}}{M_Z \times Q_Y}$$

where:
f_{OUT} is the frequency at the input to the channel dividers, OUTx (OUT0 through OUT9).
f_{REF} is the frequency of the active reference (REF0 or REF1).
Q_{ZD} is the zero delay feedback divider.
M_Z is the VCO divider (M0 or M1) that is the input source of Q_Y.
Q_Y is the channel divider (Q0, Q1, Q2, or Q3) associated with OUTx.

R0 is the divider value used to scale the input reference frequency and is an element of the following set: {½, 1, 2, …, 63}. Note that the value of ½ is the result of selecting the ×2 reference multiplier (see the PLL0 Reference Frequency Scaling section).

M0 and M_Z are divide values of the VCO dividers and are elements of the following set: {2, 3, …, 11}.

Q_{ZD} and Q_Y are divide values of the channel divider and are elements of the following set: {1, 2, …, 64}.

For deterministic phase alignment through a reference switchover event, configure the output frequency of Q_{ZD} (and, therefore, the PLL0 PFD frequency) such that it is equal to the greatest common denominator (GCD) of all channel divider output frequencies on the PLL0 synchronization domain and the reference input.

In the following example,

- f_{IN} = 25 MHz
- $f_{OUT0_TO_OUT3}$ = 125 MHz
- $f_{OUT4_TO_OUT5}$ = 312.5 MHz
- $f_{OUT6_TO_OUT7}$ = 625 MHz
- $f_{OUT8_TO_OUT10}$ = 25 MHz from the PLL0 active reference input.
- f_{PFD0} = GCD (25, 125, 312.5, 625) = 12.5 MHz
- f_{VCO0} = 625 MHz × 4 = 2500 MHz

Therefore, R0 = 2 and M0 × Q_{ZD} = 2500/12.5 = 200. This requires the following conditions:

- M0 ≥ 4 = ceil(200/64)
- M0 = 4
- Q_{ZD} = 50
- Q0 = 5
- Q1 = 2
- Q1 source = M0
- Q2 = 1
- Q2 source = M0
- N0 = 200

In the following example,

- f_{IN} = 25 MHz
- $f_{OUT0_TO_OUT3}$ = 156.25 MHz
- $f_{OUT4_TO_OUT5}$ = 125 MHz
- $f_{OUT6_TO_OUT7}$ = 625 MHz
- $f_{OUT8_TO_OUT10}$ = 25 MHz from the PLL0 active reference input
- f_{PFD0} = GCD (25, 125, 156.25, 625) = 6.25 MHz
- f_{VCO0} = 625 MHz × 4 = 2500 MHz

Therefore, R0 = 4 and M0 × Q_{ZD} = 2500/6.25 = 400. This requires M0 ≥ 7 = ceil(400/64). M1 must be used to generate all the required frequencies in this configuration, resulting in the following settings:

- M0 = 8
- Q_{ZD} = 50
- Q0 = 2
- M1 = 4
- Q1 = 5
- Q1 source = M1
- Q2 = 1
- Q2 source = M1
- N0 = 400

However, the maximum value for N0 is 255. Therefore, to calibrate the VCO, use Loop Mode 1, which requires N0 = 50 and N0A = 8. See the PLL0 VCO Calibration section for detailed information about calibrating in Loop Mode 2 when M0 × Q_{ZD} > 255.

Note that using smooth switchover minimizes the phase offset between reference inputs for a reference switchover event. Therefore, the use of smooth switching allows deterministic phase alignment to be maintained through a switchover event without the need for the reference input divider.

PLL0 Phase Frequency Detector (PFD) and Charge Pump

The PFD determines the phase difference between the edges of the reference divider output and the feedback divider output. The maximum operating frequency of the PFD depends on the operating mode of the PLL (see Table 6).

The circuit provides two pulse-width modulated output signals: up and down. These up/down pulses drive the charge pump circuit. The instantaneous phase error determines the amount of charge delivered from the charge pump to the loop filter. The closed-loop of the PLL typically drives the frequency and phase difference between the two PFD input signals toward zero.

The 1.8 V charge pump current is user-programmable in increments of 4 µA up to 1.02 mA via the PLL0 charge pump current bits (Register 0x102, Bits[7:0]). The charge pump current is determined by multiplying the bit field value of the PLL0 charge pump current bits by 4 µA. For example, the default setting of 0x8D produces a charge pump current of 141 × 4 µA = 564 µA.

PLL0 Loop Filter

The loop filter affects the dynamic characteristics of a PLL (for example, lock time and stability). The AD9576 provides both internal and external partially integrated loop filter capabilities for VCO0. The loop filter used is specified by the PLL0 loop filter bypass bit (Register 0x104, Bit 0). Setting this bit to Logic 0 uses the internal loop filter, whereas Logic 1 uses an external loop filter for VCO0. For both the external and internal loop filter, the value of CPOLE2 is fixed internally to 16 pF.

Operating VCO0 with the internal loop filter requires a single 4.7 nF external capacitor connected between the LF and LDO_BYP pins. The other loop filter components are internal and can be programmed through the PLL0 loop filter bits (Register 0x103, Bits[7:0]). Note PLL0 uses a static charge pump current; therefore, the nominal bandwidth of 400 kHz varies slightly as the feedback divide ratio deviates from a value of 50.

When VCO0 uses the external loop filter, the value of RPOLE2 is internal and set by the PLL0 loop filter RPOLE2 bits (Register 0x103, Bits[7:6]). The remaining components, R_{ZERO}, C_{ZERO}, and CPOLE1 are external to the AD9576 and are configured by the user.

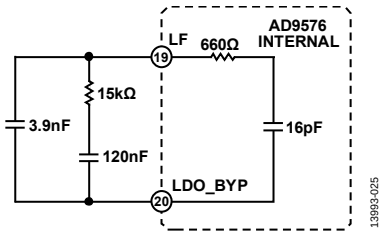


Figure 25. 8 kHz PFD PLL0 External Loop Filter

When using an 8 kHz PFD rate, an external loop filter must be used. Figure 25 shows the recommended external loop filter design for an 8 kHz PFD rate. With a VCO0 frequency of 2500 MHz and a charge pump current of 888 µA (Register 0x102, Bits[7:0] = 0xDE), the loop filter has a bandwidth of 520 Hz with 70° of phase margin.

PLL0 Internal VCO

PLL0 incorporates a low phase noise LC tank VCO0. This VCO has 256 frequency bands spanning from 2.375 GHz to 2.75 GHz. A VCO calibration is required to select the appropriate operating frequency band for the programmed divider configuration (see the PLL0 VCO Calibration section).

VCO0 has an integrated low dropout (LDO) linear voltage regulator that isolates VCO0 from possible external supply voltage variations. The regulated LDO voltage appears at the LDO_BYP pin. To ensure stability, connect a 0.47 µF chip monolithic ceramic capacitor between this pin and ground.

Note that using the LDO_BYP pin to power an external circuit may degrade VCO0 performance.

PLL0 VCO Dividers (M0 and M1)

The internal VCO of PLL0 operates in the 2.5 GHz range, which is too high to clock the output channel dividers directly. The AD9576 has two independent VCO dividers, M0 and M1, used to scale down the internal VCO frequency to an acceptable range for the output channel dividers. Both the M0 and M1 dividers are programmable over the range of 2 to 11 using the M0 divide ratio and M1 divider ratio bits, Register 0x121, Bits[3:0] and Register 0x121, Bits[7:4], respectively. The values of these bits and their corresponding functions are shown in Table 27.

Table 27. VCO Divider Ratio Decode

M0 or M1 Divider Ratio Bit Field Value	Divider Operation
0 to 1	Power down
2 to 11	Divide by this value
12 to 15	Power down

The dual VCO dividers provide flexibility for the output frequencies. VCO Divider M0 drives the Q0, Q1, Q2, Q3, and Q_{ZD} channel output drivers, whereas VCO Divider M1 only drives the Q1 and Q2 channel dividers.

The VCO dividers, M0 and M1, have a synchronous reset function that must be exercised after power-up or a change in divide value to guarantee proper operation. Under normal operation, there is no need for the user to reset the M0 or M1 dividers manually because they are automatically reset by the VCO0 calibration process. However, when the user wants to change the M0 or M1 divider value after the VCO0 calibration, the user must either reissue a VCO0 calibration (see the PLL0 VCO Calibration section) or manually reset the VCO dividers by executing the following sequence:

1. Force a reset on the M0 VCO divider. Set Register 0x120, Bit 0 = 1.
2. Force a reset on the M1 VCO divider. Set Register 0x120, Bit 4 = 1.
3. Issue an input/output (I/O) update. Write Register 0x00F = 0x01.
4. Clear the M0 VCO divider reset state. Set Register 0x120, Bit 0 = 0.
5. Clear the M1 VCO divider reset state. Set Register 0x120, Bit 4 = 0.
6. Issue an I/O update. Write Register 0x00F = 0x01.

Note that, if only a single VCO divider value is changed, only that divider must be reset. However, resetting both dividers simultaneously ensures synchronization between the respective downstream dividers.

PLL0 VCO Calibration

The AD9576 on-chip VCO0 must be calibrated to ensure proper operation over process and temperature. Calibration centers the VCO0 control voltage at the VCO0 frequency established after PLL0 locks, allowing VCO0 a sufficient operating range to maintain lock over extremes of temperature and voltage.

The VCO calibration routine works by comparing the VCO feedback clock to the reference input clock. This requires that a valid reference input clock is present at the time of calibration. Therefore, the LOR status indicator of the PLL0 active reference input is used to gate the VCO calibration operation so that it waits for the presence of a reference input clock. Note that, in Loop Mode 1, the REF0/REF1 frequency may be lower than the detection threshold of the LOR status indicator, causing the LOR status to remain Logic 1 even with a fully valid reference. In this case, the VCO calibration cannot be gated by the PLL0 active reference input LOR status. Therefore, the LOR gating of the calibration is removed when operating in Loop Mode 1 with a total feedback divide value equal to or greater than a value of divide by 512. When these conditions are met, the calibration still waits for the presence of a reference input clock, but no assessment of the frequency accuracy of the signal is made prior to the execution of the calibration.

When a PPR load is executed on power-up, an automatic calibration sequence is issued following the completion of the load. Otherwise, a manual VCO0 calibration must be initiated via the PLL0 calibration bit (Register 0x100, Bit 3). Setting the PLL0 calibration bit to Logic 1 initiates a calibration of VCO0. The PLL0 calibration bit is not a self clearing bit. Therefore, the bit must be reset to Logic 0 before a subsequent manual calibration can be initiated. The PLL0 calibration in progress bit (Register 0x020, Bit 2) indicates when a VCO0 calibration is occurring. A Logic 1 reported on the PLL0 calibration in progress bit indicates a VCO0 calibration is active, whereas a Logic 0 indicates normal PLL0 operation.

After a successful calibration, the VCO operates in a condition with optimal margin to maintain lock in operation across the entire specified temperature range, which includes margin for a deviation in the reference input clock carrier up to ±200 ppm. However, if the active reference clock frequency exceeds this limit, or if the user alters the nominal VCO operating frequency by reconfiguring the reference scaling section or feedback divider, the ability for the PLL to maintain lock over temperature may be compromised. If this occurs, an additional VCO calibration is necessary. To accomplish this, write the following register sequence:

1. Clear the VCO0 calibration bit. Write Register 0x100, Bit 3 = 0.
2. Issue an I/O update. Write Register 0x00F = 0x01.
3. Initiate a manual VCO0 calibration. Write Register 0x100, Bit 3 = 1.
4. Issue an I/O update. Write Register 0x00F = 0x01.

Note that, during the first VCO0 calibration sequence after a PLL0 reset or chip level reset, the calibration controller holds the distribution section in sync mode (the channel dividers are held in reset and the output drivers are static) until the calibration terminates. Therefore, no output signals appear until the VCO0 calibration sequence terminates, as indicated by a Logic 1 to Logic 0 transition of the PLL0 calibration in progress bit (Register 0x020, Bit 2).

The VCO0 calibration process requires approximately 98,500 cycles of the PFD to complete. Therefore, the calibration time (t_{VCO_CAL}) depends on the input frequency to the PFD (f_{PFD}) as follows:

$$t_{VCO_CAL} = \frac{9.85 \times 10^4}{f_{PFD}}$$

Loop Mode 2 Calibration Considerations

When using the PLL0 Loop 2 feedback configuration, the VCO0 calibration requires special treatment because the M0 and Q_{ZD} dividers stop during VCO0 calibration (a result of the automatic synchronization function imposed during calibration), which prevents the calibration circuitry from receiving the required feedback clock edges. Therefore, the calibration controller detects that Loop 2 is in effect and automatically switches to the Loop 0 configuration to perform the VCO0 calibration sequence. Upon completion of the calibration sequence, the calibration controller automatically restores the Loop 2 configuration. Because the calibration controller uses the Loop 0 configuration, the N0 divider is necessarily in the feedback path during the calibration sequence. Therefore, the user must program the value of the N0 divider before initiating a calibration sequence in the Loop 2 configuration, where

$$N0 = M0 \times Q_{ZD}$$

That is, N0 must match the product of the M0 divider and the Q_{ZD} channel divider. The N0 divider is programmed via the N0 divider integer value bits (Register 0x107, Bits[7:0]).

If $M0 \times Q_{ZD} > 255$, the N0 feedback divider alone is not large enough to be used during calibration. To properly calibrate VCO0, manually force the AD9576 to operate in Loop 1 during calibration and, following the completion of the calibration, manually force the AD9576 back to Loop 2. Perform these actions using the following sequence:

5. Clear the VCO0 calibration bit. Write Register 0x100, Bit 3 = 0.
6. Set Loop Mode 1. Write Register 0x101, Bits[2:1] = 1.
7. Issue an I/O update. Write Register 0x00F = 0x01.
8. Initiate a manual VCO0 calibration. Write Register 0x100, Bit 3 = 1.
9. Issue an I/O update. Write Register 0x00F = 0x01.
10. Wait for the calibration to complete, the poll until Register 0x020, Bit 2 = 0.
11. Set Loop Mode 2. Write Register 0x101, Bits[2:1] = 2.
12. Issue an I/O update. Write Register 0x00F = 0x01.

Note that, in this case, the calibration feedback path consists of the cascade of the N0 and N0A dividers. Therefore, the user must program the N0 and N0A dividers such that

$$N0 \times N0A = M0 \times Q_{ZD}$$

PLL0 Lock Detect

The PLL0 lock detector is a frequency detector that evaluates the frequency difference between the feedback and reference inputs to the PFD. A lock condition is indicated when the average difference between the feedback and reference inputs is less than a magnitude of 16 ppm. The PLL0 lock detect process requires approximately 65,500 cycles of the PFD to complete. Therefore, the lock detect time (t_{LDET}) depends on the input frequency to the PFD (f_{PFD}) as follows:

$$t_{LDET} = \frac{6.5 \times 10^4}{f_{PFD}}$$

PLL1 INTEGER-N PLL

PLL1 is a fully integrated integer-N PLL consisting of six functional elements: a reference frequency prescalar, a PFD, a charge pump, an internal loop filter, a VCO, and a feedback divider. PLL1 allows two independent reference clock input signals. PLL1 provides up to three outputs segregated into two groups. Each group has a dedicated channel divider allowing the device to produce two different output frequencies simultaneously. Figure 26 shows the functional block diagram of PLL1.

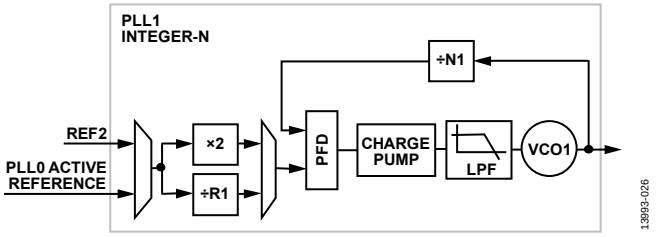


Figure 26. PLL1 Block Diagram

PLL1 Reference Frequency Scaling

The frequency of the active input reference (REF0, REF1, or REF2) is scalable via the PLL1 doubler enable bit (Register 0x202, Bit 0) and the R1 divider ratio bits (Register 0x202, Bits[3:1]). This scaling allows the user to scale the input reference frequency to satisfy the input range of the PFD. When the PLL1 doubler enable bit is set to Logic 0, the frequency appearing at the input to the PFD, f_{PFD1}, is a function of the active reference frequency scaled by the reference input divider.

$$f_{PFD1} = \frac{f_{REF}}{R1}$$

where:
f_{REF} is the frequency of the active reference (REF0, REF1, or REF2).
R1 is the value of the R1 reference input divider value.

When the PLL1 doubler enable bit is set to Logic 1, the frequency appearing at the input to the PFD, f_{PFD1}, is the active reference frequency multiplied by a factor of 2.

$$f_{PFD1} = f_{REF} \times 2$$

where f_{REF} is the frequency of the active reference (REF0, REF1, or REF2).

Note that, when the ×2 frequency multiplier is in use, the active reference signal must have a duty cycle close to 50%. Otherwise, spurious artifacts (harmonics) may propagate through the signal path and appear at the output of PLL1.

PLL1 Loop Configuration

The VCO_1 frequency is a function of the PFD1 input frequency and the values programmed into the registers associated with the N_1 feedback divider.

$$f_{VCO1} = f_{PFD1} \times N_1$$

The divider value of N_1 is set by programming the N1 divider ratio bits (Register 0x201, Bits[7:0]) to a value between 4 and 255.

The overall frequency translation is as follows:

$$f_{OUT} = \frac{f_{REF}}{R1} \times \frac{N_1}{Qx}$$

where:
f_{OUT} is the frequency at the output driver, OUTx (OUT8, OUT9, or OUT10).
f_{REF} is the frequency of the active reference (REF0, REF1, or REF2).
Qx is the channel divider (Q3 or Q4) associated with OUTx.

R1 is the divider value used to scale the input reference frequency and is an element of the following set: {½, 1, 1.5, 2, 3, 4, 6, 8}. Note the value of ½ is the result of selecting the ×2 reference multiplier (see the PLL1 Reference Frequency Scaling section).

N_1 is an element of the following set: {4, 5, …, 255}.

Qx is the divide value of the channel divider and is an element of the following set: {1, 2, …, 64}.

PLL1 PFD, Charge Pump, and Loop Filter

The PFD determines the phase difference between the edges of the reference divider output and the feedback divider output. The circuit provides two pulse-width modulated output signals: up and down. These up/down pulses drive the charge pump circuit. The instantaneous phase error determines the amount of charge delivered from the charge pump to the loop filter. The closed-loop of the PLL typically drives the frequency and phase difference between the two PFD input signals towards zero.

The loop filter affects the dynamic characteristics of a PLL (for example, lock time and stability). PLL1 has a fully integrated internal loop filter that establishes the loop dynamics for a PFD frequency between 10 MHz and 50 MHz. The charge pump current and loop filter components are automatically adjusted based on the programmed N1 feedback divide value to maintain a nearly constant loop bandwidth over a range of feedback dividers values. Table 28 shows the PLL1 closed-loop bandwidth as a function of the N1 divide value.

Table 28. PLL1 Closed-Loop Bandwidth

N1 Divide Value	Nominal Closed Loop Bandwidth (MHz)
4 to 23	3.5
24 to 47	1.75
48 to 255	1

PLL1 Internal VCO

The PLL1 internal VCO has a frequency range of 750 MHz to 825 MHz and a nominal gain of 750 MHz/V, allowing the PLL to support ±3.125% clock margining for an 800 MHz VCO frequency and a 25 MHz PFD frequency by updating the feedback divider on-the-fly.

PLL1 Lock Detect

The PLL1 lock detect is a phase detector that evaluates the phase difference between the feedback and reference inputs to PFD1. The lock detector operates at the PFD rate, which is

$$f_{PFD1} = \frac{f_{VCO1}}{N_1}$$

A lock condition is indicated when the phase error between the feedback and reference inputs to PFD1 is less than 3.25 ns. Typically, a lock condition for PLL1 is declared 420 µs after the release of $\overline{\text{RESET}}$, assuming a valid input clock is available.

OUTPUT DISTRIBUTION

The output distribution is segmented into five groups of outputs (Output Group 0, Output Group 1, Output Group 2, Output Group 3, and Output Group 4) with each group having several output drivers that share a channel divider. The output groups, corresponding channel dividers, output drivers, and input clock source(s) are shown in Table 29.

Table 29. Distribution Output Groups

Output Group	Channel Divider	Output Driver(s)	Frequency Source(s)
0	Q0	OUT0, OUT1, OUT2, OUT3	PLL0 (M0)
1	Q1	OUT4, OUT5	PLL0 (M0 and M1)
2	Q2	OUT6, OUT7	PLL0 (M0 and M1)
3	Q3	OUT8, OUT9	PLL0 (M0), PLL1 output, PLL1 reference
4	Q4	OUT10	PLL1 output, PLL1 reference

Channel Dividers

There are a total of six, 6-bit integer channel dividers: Q0, Q1, Q2, Q3, Q4, and Q_{ZD}. The divider ratio is programmable using the Qx divider ratio bits, Register 0x140, Bits[5:0], Register 0x146, Bits[5:0], Register 0x14A, Bits[5:0], Register 0x240, Bits[5:0], Register 0x244, Bits[5:0], and Register 0x110, Bits[5:0] for Q0, Q1, Q2, Q3, Q4, and Q_{ZD}, respectively. Each channel divider can operate in divide ratios of 1 to 64. The default divide ratio for each channel divider is divide by 4, with the exception of Q_{ZD}, which has a default value of 1.

The initial phase offset for each channel divider is programmable through the Qx initial phase bit fields: Register 0x141, Bits[5:0], Register 0x147, Bits[5:0], Register 0x14B, Bits[5:0], Register 0x241, Bits[5:0], Register 0x245, Bits[5:0], and Register 0x110, Bits[5:0] for Q0, Q1, Q2, Q3, Q4, and Q_{ZD}, respectively. The bit fields each have a programming range of 0 to 63 in units of half cycles of the input clock period. For Output Group 0, if the M0 output clock is 625 MHz, the LSB of this bit field corresponds to 800 ps of phase delay and an initial phase offset value of 23 delays the first edge of the Q0 divider output by 18.4 ns relative to an initial phase offset value of 0. To guarantee the initial phase offset of the Qx channel divider, a synchronization command must be executed on Qx after the corresponding Qx initial phase bit field is programmed by the user. Refer to the Synchronization section for additional information regarding this process.

Each channel divider can be independently powered down using the respective power-down bits. These bits are the Q0 PD (Register 0x140, Bit 6), Q1 PD (Register 0x146, Bit 6), Q2 PD (Register 0x14A, Bit 6), Q3 PD (Register 0x240, Bit 6), and Q4 PD (Register 0x244, Bit 6) bits in the serial register. When the channel divider power-down bit is set to Logic 1, the respective channel divider powers down, whereas Logic 0 powers up the channel divider for normal operation.

Input Sources

The Q0 and Q_{ZD} channel dividers are driven solely by the M0 VCO divider output clock. The Q1 and Q2 channel dividers can be driven by the output clock from either VCO divider, M0 or M1. The user must select which VCO divider is driving the Q1 and Q2 channel dividers using the Qx source bits (Register 0x147, Bit 6 for the Q1 source and Register 0x14B, Bit 6 for the Q2 source). Programming either Qx source bit to Logic 0 selects the M0 output clock as the input clock for the channel divider, whereas Logic 1 selects the M1 output clock as the channel divider input clock.

The Q3 channel divider can be driven by the output clock from the M0 VCO divider or the output of PLL1, f_{VCO1}. The user must select which input is driving the Q3 channel divider using the Q3 source bit (Register 0x241, Bit 6). Programming this bit to Logic 0 selects the PLL1 output as the Q3 input, whereas a Logic 1 selects the M0 output as the Q3 input.

The Q4 channel divider is driven solely by the output of PLL1, f_{VCO1}.

Synchronization

Each channel divider has a sync input that allows the divider to be placed into a known phase, determined by its initial phase bit field. When the sync input is Logic 1, the divider is held in reset, which establishes the initial phase of the divider. When the sync input is logic low, the divider is in normal operation. Coordinating the Logic 1 to Logic 0 transition of the sync input of multiple channel dividers to occur simultaneously results in a deterministic initial phase alignment between the outputs of said dividers. Provided the set of synchronized dividers share a common input clock, the initial phase alignment is repeated at a rate equal to the GCD between all channel divider outputs.

As an example, assume the Q0 output is 50 MHz and the Q1 output is 100 MHz. The outputs have a GCD equal to 50 MHz; therefore, the initial phase relationship between the Q0 and Q1 channel divider outputs repeats every 20 ns (for example, at a 50 MHz rate).

Consider another example: assume that the Q0 output is 50 MHz, the Q1 output is 100 MHz, and the Q2 output is 125 MHz. The outputs have a GCD equal to 25 MHz; therefore, the initial phase relationship between the Q0, Q1, and Q2 channel divider outputs repeats every 40 ns (for example, at a 25 MHz rate).

Four synchronization domains exist to facilitate the synchronization of multiple channel dividers. A single synchronization domain is a grouping of channel dividers in which the sync inputs of each channel divider are tied to a common control bit. The channel dividers are grouped based on their selected input source, and the four domains are as follows:

- M0 sync domain. This domain includes all channel dividers that are configured to use the M0 VCO divider as the input clock source.
- M1 sync domain. This domain includes all channel dividers that are configured to use the M1 VCO divider as the input clock source.
- PLL0 sync domain. This domain includes consists of the aggregate of the M0 and M1 sync domains.
- PLL1 sync domain. This domain includes includes all channel dividers that are configured to use the PLL1 output as the input clock source

Each sync domain has an associated manual sync bit—Register 0x120, Bit 2, Register 0x120, Bit 6, Register 0x100, Bit 2, and Register 0x200, Bit 2 for the M0, M1, PLL0, and PLL1 sync domains, respectively. Each manual sync bit allows user control of the divider sync inputs, but there are also automatically generated signals that are logically OR'ed with the manual sync bits of the individual sync domains. The actions that generate these automatically generated sync signals are described as follows, for the sync domains they affect:

- M0 sync domain. Deassertion of the M0 reset bit (Register 0x120, Bit 0) and deassertion of the M0 power-down bit (Register 0x120, Bit 1).
- M1 sync domain. Deassertion of the M1 reset bit (Register 0x120, Bit 4) and deassertion of the M1 power-down bit (Register 0x120, Bit 5).
- PLL0 sync domain. Completion of the first VCO0 calibration routine issued after the deassertion of any chip level reset or deassertion of the PLL0 reset bit (Register 0x100, Bit 0). Note that this automatic sync affects both the M0 and M1 sync domains.
- PLL1 sync domain. Deassertion of the PLL1 reset bit (Register 0x200, Bit 0).

To manually synchronize a sync domain, the user must program the associated manual sync bit to a Logic 1 followed by a Logic 0. The following example shows the required sequence for the PLL0 synchronization domain:

13. Set the PLL0 sync bit. Write Register 0x100, Bit 2 = 1.
14. Issue an I/O update. Write Register 0x00F = 0x01.
15. Clear the PLL0 sync bit. Write Register 0x100, Bit 2 = 0.
16. Issue an I/O update. Write Register 0x00F = 0x01.

Note that the M0 and M1 sync domains (and therefore the PLL0 sync domain) have mask sync bits (see the Register 0x122 description in Table 48). Setting a channel divider mask sync bit for a particular sync domain precludes said sync domain from affecting the operation of that channel divider. For example, if the Q1, Q2, and Q3 source bits are all programmed to Logic 0, the M0 sync domain includes the Q0, Q1, Q2, and Q_{ZD} channel dividers, the M1 sync domain does not include channel dividers, and the PLL1 sync domain includes the Q3 and Q4 channel dividers. Programming the M0 mask sync Q2 (Register 0x122, Bit 2) to Logic 1 results in the Q2 channel divider being unaffected by a M0 or PLL0 sync command. Programming the M1 mask sync Q2 (Register 0x122, Bit 6) to Logic 1 has no functional impact because Q2 is not a part of the M1 sync domain in this configuration.

Output Driver Sources

The output drivers in Output Group 0, Output Group 1, and Output Group 2 (see Table 29) are driven by the outputs of their respective channel divider. For example, OUT4 and OUT5 in Output Group 1 are driven by the output of the Q1 channel divider.

Output Group 3 or Output Group 4 can be driven by the output of their respective channel divider or by the PLL1 active input reference. The user must select which source is driving the outputs in Output Group 3 and Output Group 4. For Output Group 3, this is accomplished by programming the OUT89 source bit (Register 0x241, Bit 7). Programming this bit to Logic 0 selects the Q3 output as the input for the OUT8/OUT9 output drivers, whereas a Logic 1 selects the PLL1 active input reference as the input to the output drivers. Note that, if the PLL1 active input reference is selected as the source to an output group and the PLL1 active input reference is configured for a XTAL, the PLL1 active input reference loss of reference signal gates the output drivers of the output group.

The input clock source for OUT10 is selected via the OUT10 source bit (Register 0x245, Bit 6). Programming this bit to Logic 0 selects the output of the Q4 divider as the clock source for OUT10, whereas a Logic 1 selects the PLL1 active input reference as the OUT10 clock source.

Note that, if none of the 3-channel output drivers, OUT8, OUT9, or OUT10, use the PLL1 output as their input, then the PLL1 power-down signal is automatically asserted, and PLL1 is powered down.

Output Power-Down

The eight output drivers, OUT0 through OUT7, have independent power-down control via the corresponding OUTx PD bits in the serial register. For example, the OUT0 output driver is powered down via the OUT0 PD bit (Register 0x142, Bit 2). When the corresponding OUTx PD bit is set to Logic 1, OUTx is powered down; otherwise, it is powered on and functionally operational.

The three output drivers, OUT8, OUT9, and OUT10 have independent power-down control via the corresponding OUTx enable bits. For example, the OUT8 output driver is powered down via the OUT8 enable bit (Register 0x242, Bit 0). When the corresponding driver enable bit is set to Logic 0, the OUTx output driver is powered down. Likewise, OUTx is powered up when the corresponding OUTx PD bit is set to Logic 1.

Output Driver Format

The OUT0 through OUT7 output channels support HSTL, LVDS, and 1.8 V CMOS outputs. The user has independent control of the operating mode of each of the eight output channels via the OUTx driver format bits in the serial register (for example, Register 0x142, Bits[1:0] for OUT0). Table 49 contains a detailed description of the OUTx driver format bit fields for OUT0 through OUT7. The differential resistive load termination is removed for 1.8 V CMOS outputs. When an OUT0 through OUT7 driver is configured as 1.8 V CMOS, the positive and negative pins are in a complimentary phase relationship (for example, 180° offset).

Use HSTL format and ac couple the output signal for an LVPECL-compatible output.

The OUT8, OUT9, and OUT10 output channels also support HSTL, LVDS, and 1.8 V CMOS outputs as well as HCSL and full swing CMOS outputs. The user has independent control of the operating mode of OUT8, OUT9, and OUT10 through the OUTx driver format bits (Register 0x242, Bits[6:4], Register 0x243, Bits[6:4], and Register 0x246, Bits[6:4]). Table 51 contains a detailed description of the OUTx driver format bit fields for OUT8, OUT9, and OUT10.

When OUT8, OUT9, or OUT10 are operating in the CMOS output format, the user must select the output swing level via the OUTx CMOS enable full swing bits (Register 0x242, Bit 7, Register 0x243, Bit 7, and Register 0x246, Bit 7). For example, OUT8 is controlled via the OUT8 CMOS enable full swing bit (Register 0x242, Bit 7). When the OUTx CMOS enable full swing bit is set to Logic 0, the CMOS ouput of the corresponding driver has a 1.8 V swing. When the OUTx CMOS enable full swing bit is set to Logic 1, the CMOS swing is determined by the voltage applied to VDD_OUTx. Only set the OUTx CMOS enable full swing bits to Logic 1 if the associated output format is configured as CMOS.

When OUT8, OUT9, or OUT10 is operating in the CMOS output format, the user must also select the polarity of the output driver via the OUTx CMOS polarity bits (Register 0x242, Bits[3:2], Register 0x243, Bits[3:2], and Register 0x246, Bits[3:2]). For example, the polarity of OUT8 is controlled via the OUT8 CMOS polarity bits (Register 0x242, Bits[3:2]). Table 51 contains a detailed description of the OUTx CMOS polarity bit fields for OUT8, OUT9, and OUT10.

Additionally, when the output format for OUT8, OUT9, or OUT10 is configured for either LVDS or full swing CMOS, the driver strength of the output is determined by the OUTx drive strength bits (Register 0x242, Bit 1, Register 0x243, Bit 1, and Register 0x246, Bit 1 for OUT8, OUT9, and OUT10, respectively).

When operating in the LVDS output format (OUTx driver format bit = 010), programming this bit to Logic 0 results in an output drive strength of 3.5 mA, whereas a Logic 1 produces a drive strength of 4.5 mA.

When operating in the full swing CMOS output format, programming this bit to Logic 0 results in nominal output drive strength, whereas a Logic 1 results in low output drive strength that can be used to minimize coupling effects. The drive strength bit only applies to the full swing CMOS format. The 1.8 V swing CMOS output drivers only operate in a low drive strength mode.

PPRx PINS

The AD9576 makes use of four PPRx pins to configure the device. Internal circuitry scans the PPRx pins for the presence of resistor terminations and configures the device accordingly. A PPRx pin scan occurs automatically as part of the power-on reset sequence (see the Power-On Reset (POR) section) or following the assertion of the $\overline{\text{RESET}}$ pin.

Each PPRx pin controls a specific function or functional block within the device (see Table 30). The power-on configuration of a functional block depends on the scanned state of the corresponding PPRx pin. The scan of a PPRx pin identifies one of eight possible states based on an external pull-up or pull-down resistor (maximum 10% tolerance) per Table 31.

Table 30. PPRx Pin Function Assignments

Mnemonic	Pin No.	Function Assignment
PPR0	24	Input receiver configurations, PLL1 source, and PLL input doubler states
PPR1	26	OUT10 configuration
PPR2, PPR3	32, 56	PLL0 frequency translation and OUT0 to OUT9 configuration

Device programming consists of connecting the appropriate value programming resistors to the PPRx pins and terminating the resistors to V_{DD_x} or GND (per Table 31). For example, Figure 27 shows how to program PPR0 to State 3.

Table 31. PPRx State

PPRx State	Resistance	Terminus
0	820 Ω	GND
1	1.8 kΩ	GND
2	3.9 kΩ	GND
3	8.2 kΩ	GND
4	820 Ω	V_{DD}
5	1.8 kΩ	V_{DD}
6	3.9 kΩ	V_{DD}
7	8.2 kΩ	V_{DD}

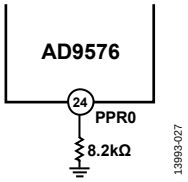


Figure 27. PPRx Programming Resistor Example

For details regarding the device configuration based on the scanned PPRx states, refer to the description of each PPRx pin in the following sections.

PPR0—Reference Clock Input Configuration

The PPR0 pin controls the configuration of the reference clock inputs (REF0, REF1, REF2) and the select line of the PLL1 reference input mux. Table 32 associates each PPR0 state with a particular reference input configuration and PLL1 source combination.

PPR1—OUT10 Configuration

The PPR1 pin controls the frequency, driver format, and source of OUT10, which requires the PLL1 reference input, and therefore REF2, if used, to be 25 MHz. Note that, if REF0/REF1 is configured to a frequency other than 25 MHz, the PLL1 source must be configured as REF2. Table 33 associates each PPR1 state with a particular OUT10 configuration.

PPR2 and PPR3—REF0/REF1 Frequency and OUT0 to OUT9 Configuration

The PPR2 and PPR3 pins control the configuration of the REF0 and REF1 input frequency, PLL0, OUT0 to OUT9 driver format and frequency, and the OUT8 to OUT9 source. Table 34 associates each combination of PPR2 and PPR3 states with a particular predefined frequency translation.

Table 32. PPR0—Input Receiver Formats and PLL1 Source

PPR0 State	REF0/REF1 Input Configuration	REF2 Input Configuration	PLL1 Source	PLL0 Doubler	PLL1 Doubler
0	XTAL	2.5 V/3.3 V CMOS	PLL0 active reference	Enabled	Disabled
1	2.5 V/3.3 V CMOS	2.5 V/3.3 V CMOS	PLL0 active reference	Enabled	Disabled
2	2.5 V/3.3 V CMOS	2.5 V/3.3 V CMOS	PLL0 active reference	Disabled	Disabled
3	Differential/1.8 V LVCMOS	2.5 V/3.3 V CMOS	PLL0 active reference	Disabled	Disabled
4	XTAL	XTAL	REF2	Enabled	Disabled
5	2.5 V/3.3 V CMOS	2.5 V/3.3 V CMOS	REF2	Enabled	Disabled
6	Differential/1.8 V LVCMOS	XTAL	REF2	Enabled	Disabled
7	Differential/1.8 V LVCMOS	2.5 V/3.3 V CMOS	REF2	Enabled	Disabled

Table 33. PPR1—OUT10 Configuration

PPR1 State	OUT10 Frequency (MHz)	OUT10 Format	OUT10 Source
0	25	2.5 V/3.3 V CMOS	PLL1 reference
1	33.3 (100/3)	2.5 V/3.3 V CMOS	PLL1 output
2	50	2.5 V/3.3 V CMOS	PLL1 output
3	66.67 (200/3)	2.5 V/3.3 V CMOS	PLL1 output
4	100	LVDS	PLL1 output
5	133.3 (400/3)	LVDS	PLL1 output
6	200	LVDS	PLL1 output
7	400	LVDS	PLL1 output

Table 34. PPR2 and PPR3—REF0/REF1 Frequency and OUT0 to OUT9 Configuration[1]

		REF0/REF1	OUT0 to OUT3		OUT4 to OUT5		OUT6 to OUT7		OUT8 to OUT9		
PPR2 State	PPR3 State	Frequency (MHz)	Frequency (MHz)	Format	Frequency (MHz)	Format	Frequency (MHz)	Format	Frequency (MHz)	Format	Source
0	0	25	Disabled	N/A	Disabled	N/A	Disabled	N/A	Disabled	N/A	N/A
0	1	25	156.25	HSTL	156.25	HSTL	156.25	HSTL	156.25	HSTL	PLL0
0	2	25	156.25	LVDS	156.25	LVDS	156.25	LVDS	156.25	LVDS	PLL0
0	3	25	156.25	HSTL	156.25	HSTL	100	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
0	4	25	156.25	LVDS	156.25	LVDS	100	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
0	5	25	156.25	HSTL	125	HSTL	100	HSTL	50	2.5 V/3.3 V CMOS	PLL1
0	6	25	156.25	HSTL	125	HSTL	100	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
0	7	25	156.25	LVDS	125	LVDS	100	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
1	0	25	156.25	LVDS	125	LVDS	25	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
1	1	25	156.25	HSTL	125	HSTL	25	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
1	2	25	156.25	HSTL	100	HSTL	50	HSTL	125	HSTL	PLL0
1	3	25	156.25	LVDS	100	LVDS	50	HSTL	125	HSTL	PLL0
1	4	25	156.25	LVDS	100	LVDS	100	LVDS	25	2.5 V/3.3 V CMOS	PLL1 source
1	5	25	156.25	HSTL	100	HSTL	25	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
1	6	25	156.25	LVDS	100	LVDS	25	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
1	7	25	156.25	HSTL	100	HSTL	125	HSTL	312.5	HSTL	PLL0
2	0	25	156.25	LVDS	100	LVDS	125	LVDS	312.5	LVDS	PLL0
2	1	25	156.25	HSTL	312.5	HSTL	125	HSTL	25	HSTL	PLL1 source
2	2	25	156.25	LVDS	312.5	LVDS	125	LVDS	25	LVDS	PLL1 source
2	3	25	312.5	HSTL	100	HSTL	100	HSTL	156.25	HSTL	PLL0
2	4	25	312.5	LVDS	100	LVDS	100	LVDS	156.25	LVDS	PLL0
2	5	25	312.5	HSTL	100	HSTL	125	HSTL	156.25	HSTL	PLL0
2	6	25	312.5	LVDS	100	LVDS	125	LVDS	156.25	LVDS	PLL0
2	7	25	312.5	HSTL	100	HSTL	156.25	HSTL	156.25	HSTL	PLL0
3	0	25	312.5	LVDS	100	LVDS	156.25	LVDS	156.25	LVDS	PLL0
3	1	25	625	HSTL	100	LVDS	100	LVDS	156.25	HSTL	PLL0
3	2	25	100	HSTL	312.5	HSTL	156.25	HSTL	125	HSTL	PLL0
3	3	25	100	LVDS	312.5	LVDS	156.25	LVDS	125	LVDS	PLL0
3	4	25	100	HSTL	312.5	HSTL	156.25	HSTL	25	HSTL	PLL1 source
3	5	25	100	LVDS	312.5	LVDS	156.25	LVDS	25	LVDS	PLL1 source
3	6	25	100	HSTL	100	HSTL	100	HSTL	100	HCSL	PLL0
3	7	25	100	LVDS	100	LVDS	100	LVDS	100	HCSL	PLL0
4	0	25	125	HSTL	125	HSTL	125	HSTL	125	HSTL	PLL0
4	1	25	125	LVDS	125	LVDS	125	LVDS	125	LVDS	PLL0
4	2	25	125	HSTL	100	HSTL	100	HSTL	100/3	HSTL	PLL1
4	3	25	125	LVDS	100	LVDS	100	LVDS	100/3	LVDS	PLL1
4	4	25	125	HSTL	100	HSTL	25	HSTL	25	HSTL	PLL1 source
4	5	25	125	LVDS	100	LVDS	25	LVDS	25	LVDS	PLL1 source
4	6	25	25	LVDS	25	LVDS	125	LVDS	100	HCSL	PLL0
4	7	25	100	LVDS	100	LVDS	125	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
5	0	25	100	HSTL	100	HSTL	125	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source

PPR2 State	PPR3 State	REF0/REF1	OUT0 to OUT3		OUT4 to OUT5		OUT6 to OUT7		OUT8 to OUT9		
		Frequency (MHz)	Frequency (MHz)	Format	Frequency (MHz)	Format	Frequency (MHz)	Format	Frequency (MHz)	Format	Source
5	1	25	156.25	HSTL	50	HSTL	125	HSTL	25	2.5 V/3.3 V CMOS	PLL1 source
5	2	25	156.25	LVDS	50	LVDS	125	LVDS	25	2.5 V/3.3 V CMOS	PLL1 source
5	3	25	100	HSTL	100	HSTL	100	HSTL	100	HCSL	PLL1
5	4	25	100	LVDS	100	LVDS	100	LVDS	100	HCSL	PLL1
5	5	25	25	HSTL	25	HSTL	25	HSTL	400	LVDS	PLL1
5	6	25	156.25	HSTL	50	HSTL	125	HSTL	400	HCSL	PLL1
5	7	25	156.25	LVDS	50	LVDS	125	LVDS	400	HCSL	PLL1
6[2]	0[2]	25	70.656	HSTL	70.656	HSTL	70.656	HSTL	25	HSTL	PLL1 source
6[2]	1[2]	25	24.576	HSTL	24.576	HSTL	24.576	HSTL	100	HCSL	PLL1
6[2]	2[2]	25	24.576	LVDS	24.576	LVDS	24.576	LVDS	100	HCSL	PLL1
6[2]	3[2]	25	312.5 × (33/32)	HSTL	156.25 × (33/32)	HSTL	156.25 × (33/32)	HSTL	100	HCSL	PLL1
6[2]	4[2]	25	312.5 × (33/32)	LVDS	156.25 × (33/32)	LVDS	156.25 × (33/32)	LVDS	100	HCSL	PLL1
6[2]	5[2]	25	148.5	HSTL	148.5	HSTL	148.5	HSTL	100	HCSL	PLL1
6[2]	6[2]	25	148.5	LVDS	148.5	LVDS	148.5	LVDS	100	HCSL	PLL1
6[3]	7[3]	19.44	625 × (33/32)	HSTL	156.25 × (33/32)	HSTL	156.25 × (33/32)	HSTL	100	HCSL	PLL1
7[3]	0[3]	19.44	625 × (33/32)	LVDS	156.25 × (33/32)	LVDS	156.25 × (33/32)	LVDS	100	HCSL	PLL1
7[3]	1[3]	19.44	156.25	HSTL	125	HSTL	50	HSTL	100	LVDS	PLL1
7[3]	2[3]	19.44	156.25	LVDS	125	LVDS	50	LVDS	100	LVDS	PLL1
7[3]	3[3]	30.72	156.25	HSTL	50	HSTL	125	HSTL	25	2.5 V/3.3 V CMOS	PLL0
7[3]	4[3]	30.72	156.25	LVDS	50	LVDS	125	LVDS	25	2.5 V/3.3 V CMOS	PLL0
7[3]	5[3]	30.72	156.25	HSTL	125	HSTL	50	HSTL	100	HCSL	PLL1
7[3]	6[3]	30.72	156.25	LVDS	125	LVDS	50	LVDS	100	HCSL	PLL1
7	7	Reserved									

[1] N/A means not applicable.
[2] Frequency translation requires the PLL0 input doubler to be enabled. Only valid if PPR0 = 0, 1, 4, 5, 6, or 7.
[3] PLL1 input must be 25 MHz. Only valid if PPR0 = 4, 5, 6, or 7.

POWER-ON RESET (POR)

Applying power to the AD9576 causes an internal power-on reset (POR) event. A POR event allows the device to initialize to a known state at power-up by initiating a scan of the PPRx pins (see the PPRx Pins section).

In general, the AD9576 follows an orderly power-on sequence beginning with the POR circuit detecting a valid 2.5 V or 3.3 V supply. This activates the internal LDO regulators. Detection of valid LDO voltages by the POR circuit triggers a PPRx scan sequence, which results in the configuration of the internal registers. With a reference signal applied to the input of each PLL, the VCO0 calibration sequence initiates, while PLL1 immediately begins locking to the reference. Assuming a valid input reference signal, the PLLs eventually locks to the reference signal(s), as indicated by assertion of the LD_0 pin and the LD_1 pin. These lock signals enable the prescale dividers at the output of each VCO, which starts the output drivers toggling (that is, those output drivers enabled per the PPRx settings).

SERIAL CONTROL PORT

The AD9576 serial control port is a flexible, synchronous serial communications port that provides a convenient interface to many industry-standard microcontrollers and microprocessors. The AD9576 serial control port is compatible with I²C and SPI. The serial control port allows read/write access to the AD9576 register map.

The AD9576 uses the Analog Devices unified SPI protocol (see the Analog Devices Serial Control Interface Standard) implementation, but does not support a 4-wire protocol with dedicated input and output data pins. Rather, only a 3-wire mode with a single, bidirectional data pin is supported. The SPI port configuration is programmable via Register 0x000. This register is a part of the SPI control logic rather than in the register map and is distinct from the I²C Register 0x000.

Although the AD9576 supports both the SPI and I²C serial port protocols, only one is active following power-up (as determined by the SP0 and SP1 pins during the start-up sequence). The only way to change the serial port protocol is to reset (or power cycle) the device.

SPI/I²C PORT SELECTION

Because the AD9576 supports both SPI and I²C protocols, the active serial port protocol depends on the logic state of the SP0 and SP1 pins at reset or power-on. See Table 35 for the serial port configuration decode.

Table 35. SPI/I²C Serial Port Setup

SP1	SP0	SPI/I²C Address
Floating	Floating	SPI with PPRx load
0	Floating	I²C, 0111001 (0x39)
1	Floating	I²C, 0111010 (0x3A)
Floating	0	I²C, 0111011 (0x3B)
0	0	I²C, 0111100 (0x3C)
1	0	I²C, 0111101 (0x3D)
Floating	1	I²C, 0111110 (0x3E)
0	1	I²C, 0111111 (0x3F)
1	1	SPI

SPI SERIAL PORT OPERATION

Pin Descriptions

The SCLK (serial clock) pin serves as the serial shift clock. This pin is an input. SCLK synchronizes serial control port read and write operations. The rising edge SCLK registers write data bits, and the falling edge registers read data bits. The SCLK pin supports a maximum clock rate of 50 MHz.

The SPI port supports only a 3-wire (bidirectional) hardware configuration. This 3-wire mode uses the SDIO (serial data input/output) pin for transferring data in both directions. Both MSB first and LSB first data formats are supported and are software programmable.

The $\overline{CS}$ (chip select) pin is an active low control that gates read and write operations. Assertion (active low) of the $\overline{CS}$ pin initiates a write or read operation to the AD9576 SPI port. Any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented based on the setting of the address ascension bit (Register 0x000). $\overline{CS}$ must be deasserted at the end of the last byte transferred, thereby ending the stream mode. When $\overline{CS}$ is high, the SDIO pin goes into a high impedance state.

Implementation Specific Details

The following product specific items are defined in the unified SPI protocol:

- Analog Devices unified SPI protocol revision: 1.0
- Chip type: 0x5
- Product ID: 0x014F
- Physical layer: 3-wire supported and 2.5 V and 3.3 V operation supported
- Optional single-byte instruction mode: not supported
- Data link: not used
- Control: not used

Communication Cycle—Instruction Plus Data

The unified SPI protocol consists of a two part communication cycle. The first part is a 16-bit instruction word that is coincident with the first 16 SCLK rising edges and a payload. The instruction word provides the AD9576 serial control port with information regarding the payload. The instruction word includes the R/$\overline{W}$ bit that indicates the direction of the payload transfer (that is, a read or write operation). The instruction word also indicates the starting register address of the first payload byte.

Write

If the instruction word indicates a write operation, the payload is written into the serial control port buffer of the AD9576. Data bits are registered on the rising edge of SCLK. Generally, it does not matter what data is written to blank registers; however, it is customary to use 0s. Note that the user must verify that all reserved registers within a specific range have a default value of 0x00; however, Analog Devices makes every effort to avoid having reserved registers with nonzero default values.

Most of the serial port registers are buffered. Therefore, data written into buffered registers does not take effect immediately. An additional operation is needed to transfer buffered serial control port contents to the registers that actually control the device. This transfer is accomplished with an I/O update operation, which is performed by writing a Logic 1 to Register 0x00F, Bit 0 (this bit is an autoclearing bit). The user can change as many register bits as desired before executing an I/O update. The I/O update operation transfers the buffer register contents to their active register counterparts.

Read

If the instruction word indicates a read operation, the next N × 8 SCLK cycles clock out the data starting from the address specified in the instruction word. N is the number of data bytes read. The read back data is driven to the pin on the falling edge and must be latched on the rising edge of SCLK. Blank registers are not skipped over during read back.

A read back operation takes data from either the serial control port buffer registers or the active registers, as determined by Register 0x001, Bit 5.

SPI Instruction Word (16 Bits)

The MSB of the 16-bit instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next 15 bits are the register address (A14 to A0), which indicates the starting register address of the read/write operation (see Table 37).

SPI MSB/LSB First Transfers

The AD9576 instruction word and payload can be MSB first or LSB first. The default for the AD9576 is MSB first. The LSB first mode can be set by writing a 1 to Register 0x0000, Bit 6 and Bit 1. Immediately after the LSB first bit(s) is set, subsequent serial control port operations are LSB first.

Address Ascension

If the address ascension bits (Register 0x0000, Bit 5 and Bit 2) are zero, the serial control port register address decrements from the specified starting address toward Address 0x0000.

If the address ascension bits (Register 0x0000, Bit 5 and Bit 2) are one, the serial control port register address increments from the starting address toward Address 0x7FFF. Reserved addresses are not skipped during multi-byte input/output operations; therefore, write the default value to a reserved register and 0s to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 36. Streaming Mode (No Addresses Skipped)

Address Ascension	Stop Sequence
Increment	0x0000 … 0x7FFF
Decrement	0x7FFF … 0x0000

Table 37. Serial Control Port, 16-Bit Instruction Word

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 38. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and the rising edge of SCLK
t_{DH}	Hold time between data and the rising edge of SCLK
t_{SCLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of the communication cycle)
t_C	Setup time between the SCLK rising edge and $\overline{CS}$ rising edge (end of the communication cycle)
t_{HIGH}	Minimum period that SCLK should be in a logic high state
t_{LOW}	Minimum period that SCLK should be in a logic low state
t_{DV}	SCLK to valid SDIO (see Figure 36)

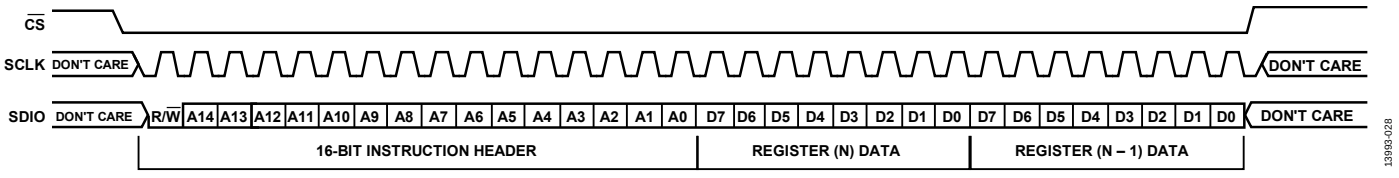


Figure 28. Serial Control Port Write—MSB First, Address Decrement, Two Bytes of Data

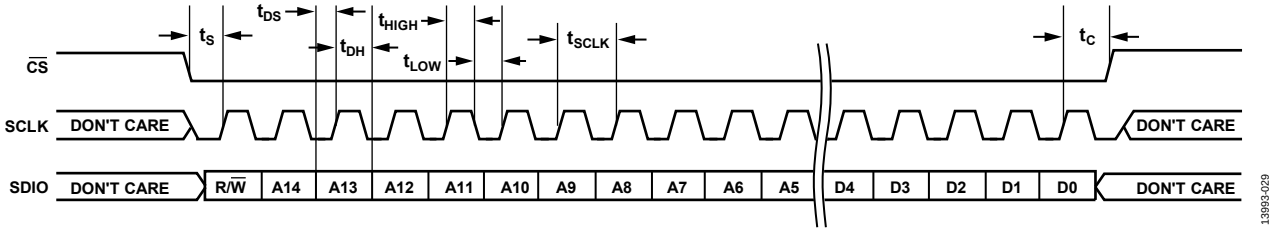


Figure 29. Timing Diagram for Serial Control Port Write—MSB First

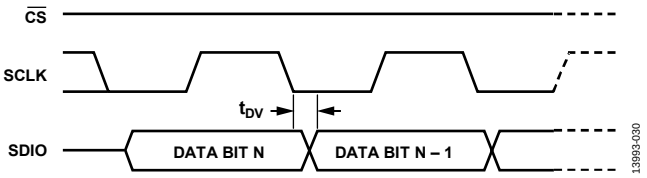


Figure 30. Timing Diagram for Serial Control Port Register Read—MSB First

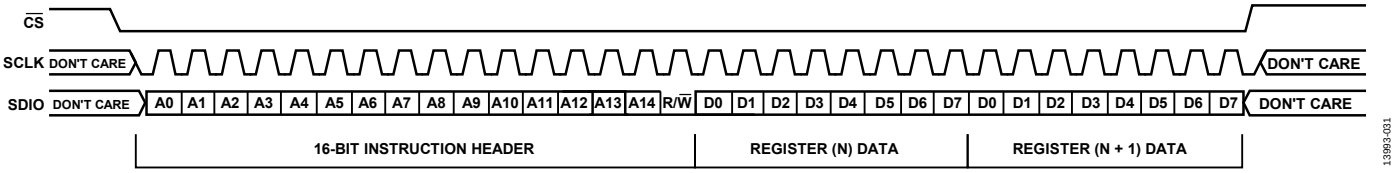


Figure 31. Serial Control Port Write—LSB First, Address Increment, Two Bytes of Data

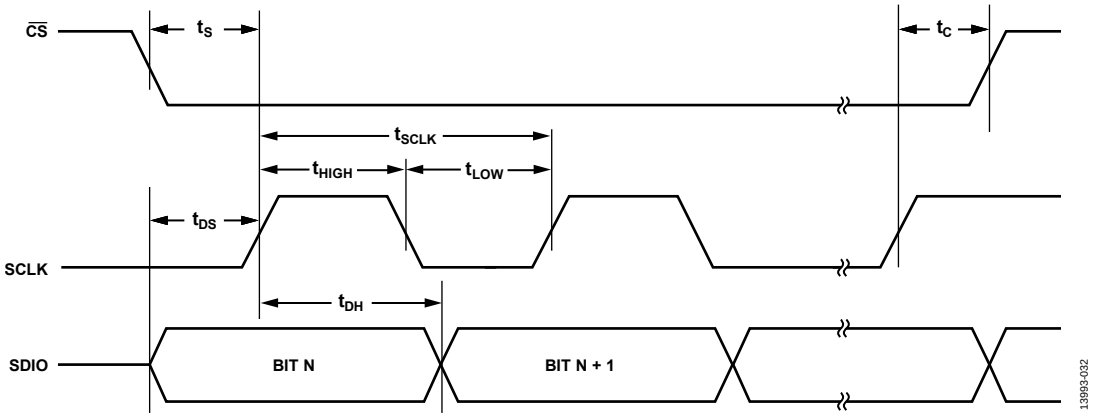


Figure 32. Timing Diagram for Serial Control Port—Write

I²C SERIAL PORT OPERATION

The I²C interface is popular because it requires only two pins and easily supports multiple devices on the same bus. Its main disadvantage is programming speed, which is 400 kbps maximum. The AD9576 I²C port design uses the I²C fast mode; however, it supports both the 100 kHz standard mode and 400 kHz fast mode.

The AD9576 does not strictly adhere to every requirement in the original I²C specification. In particular, specifications such as slew rate limiting and glitch filtering are not implemented. Therefore, the AD9576 is I²C-compatible, but may not be fully I²C compliant.

The AD9576 I²C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I²C bus system, the AD9576 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by the AD9576. The AD9576 uses direct 16-bit memory addressing instead of more common 8-bit memory addressing.

The AD9576 allows up to seven unique slave devices to occupy the I²C bus. These are accessed via a 7-bit slave address transmitted as part of an I²C packet. Only the device with a matching slave address responds to subsequent I²C commands. Table 35 lists the supported device slave addresses.

I²C Bus Characteristics

A summary of the various I²C abbreviations appears in Table 39.

Table 39. I²C Bus Abbreviation Definitions

Abbreviation	Definition
S	Start
Sr	Repeated start
P	Stop
A	Acknowledge
$\overline{A}$	No acknowledge
$\overline{W}$	Write
R	Read

The transfer of data is shown in Figure 33. One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low.

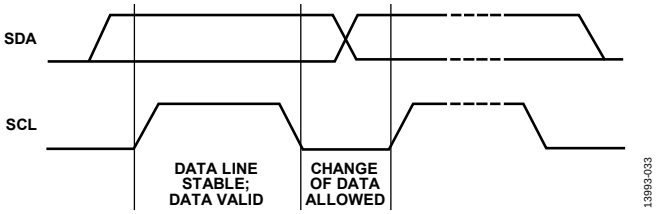


Figure 33. Valid Bit Transfer

Start/stop functionality is shown in Figure 33. The start condition is characterized by a high to low transition on the SDA line while SCL is high. The master always generates the start condition to initialize a data transfer. The stop condition is characterized by a low to high transition on the SDA line while SCL is high. The master always generates the stop condition to terminate a data transfer. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit; bytes are sent MSB first.

The acknowledge bit (A) is the ninth bit attached to any 8-bit data byte. An acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has been received. It is done by pulling the SDA line low during the ninth clock pulse after each 8-bit data byte.

The no acknowledge bit ($\overline{A}$) is the ninth bit attached to any 8-bit data byte. A no acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has not been received. It is done by leaving the SDA line high during the ninth clock pulse after each 8-bit data byte. After issuing a nonacknowledge bit, the AD9576 I²C state machine goes into an idle state.

Data Transfer Process

The master initiates data transfer by asserting a start condition, which indicates that a data stream follows. All I²C slave devices connected to the serial bus respond to the start condition.

The master then sends an 8-bit address byte over the SDA line, consisting of a 7-bit slave address (MSB first) plus an R/$\overline{W}$ bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write and 1 = read).

The peripheral whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master (transmitter) writes to the slave device (receiver). If the R/$\overline{W}$ bit is 1, the master (receiver) reads from the slave device (transmitter).

The format for these commands is described in the Data Transfer Format section.

Data is then sent over the serial bus in the format of nine clock pulses, one data byte (eight bits) from either master (write mode) or slave (read mode) followed by an acknowledge bit from the receiving device. The number of bytes that can be transmitted per transfer is unrestricted. In write mode, the first two data bytes immediately after the slave address byte are the internal memory (control registers) address bytes, with the high address byte first. This addressing scheme gives a memory address of up to $2^{16} - 1 = 65{,}535$. The data bytes after these two memory address bytes are register data written to or read from the control registers. In read mode, the data bytes after the slave address byte are register data written to or read from the control registers.

When all the data bytes are read or written, stop conditions are established. In write mode, the master (transmitter) asserts a stop condition to end data transfer during the clock pulse following the acknowledge bit for the last data byte from the slave device (receiver). In read mode, the master device (receiver) receives the last data byte from the slave device (transmitter) but does not pull SDA low during the ninth clock pulse. This is known as a nonacknowledge bit. By receiving the non-acknowledge bit, the slave device knows that the data transfer is finished and enters idle mode. The master then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition.

A start condition can be used in place of a stop condition. Furthermore, a start or stop condition can occur at any time, and partially transferred bytes are discarded.

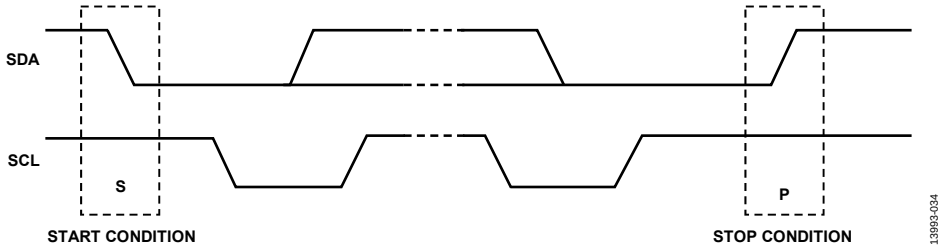


Figure 34. Start and Stop Conditions

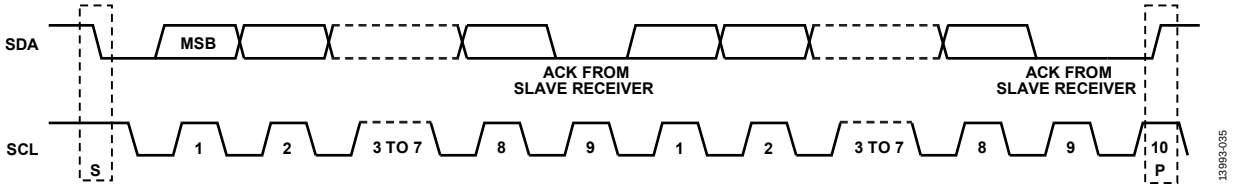


Figure 35. Acknowledge Bit

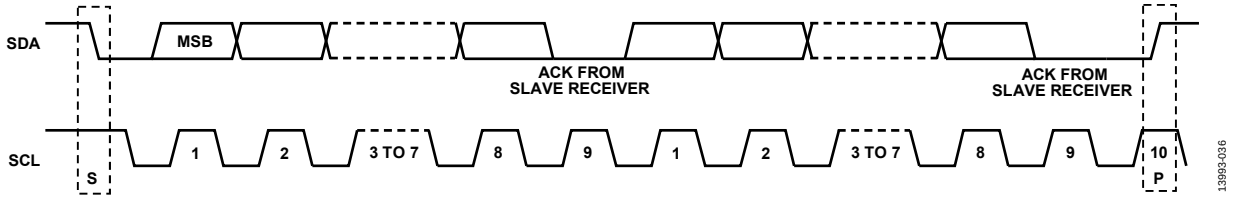


Figure 36. Data Transfer Process (Master Write Mode, 2-Byte Transfer)

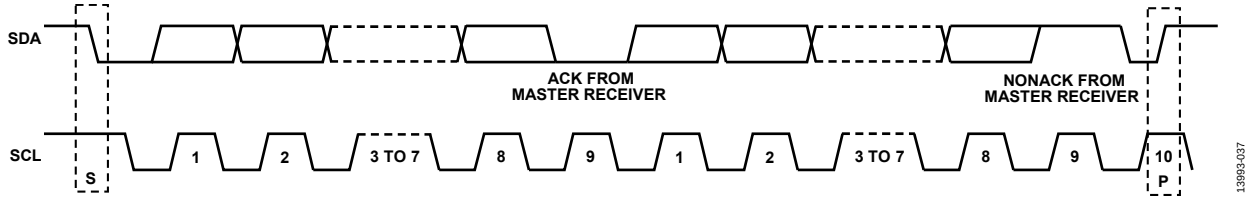


Figure 37. Data Transfer Process (Master Read Mode, 2-Byte Transfer), First Acknowledge From Slave

Data Transfer Format

The write byte format is used to write a register address to the RAM starting from the specified RAM address.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	A	P

The send byte format is used to set up the register address for subsequent reads.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	P

The receive byte format is used to read the data byte(s) from RAM starting from the current address.

S	Slave address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

The read byte format is the combined format of the send byte and the receive byte.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	Sr	Slave address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

I²C Serial Port Timing

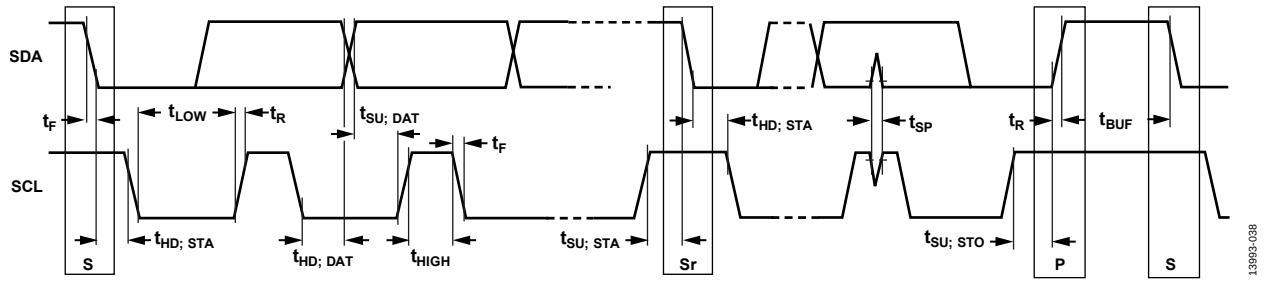


Figure 38. I²C Serial Port Timing

Table 40. I²C Timing Definitions

Parameter	Description
f_{SCL}	Serial clock
t_{BUF}	Bus free time between stop and start conditions
$t_{HD;\ STA}$	Repeated hold time start condition
$t_{SU;\ STA}$	Repeated start condition setup time
$t_{SU;\ STO}$	Stop condition setup time
$t_{HD;\ DAT}$	Data hold time
$t_{SU;\ DAT}$	Data setup time
t_{LOW}	SCL clock low period
t_{HIGH}	SCL clock high period
t_R	Minimum/maximum receive SCL and SDA rise time
t_F	Minimum/maximum receive SCL and SDA fall time
t_{SP}	Pulse width of voltage spikes that must be suppressed by the input filter

CONTROL REGISTER MAP

Table 41. Register Summary

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default (Hex)	R/W
Serial Port Configuration Registers											
0x000	SPI Configuration A	Soft reset	LSB first	Address ascension	Reserved		Address ascension	LSB first	Soft reset	0x00	R/W
0x001	SPI Configuration B	Single instruction	Reserved	Read buffer registers	Reserved		Reset sans register map	Reserved		0x00	R/W
0x003	Chip type	Reserved				Chip type				0x05	R
0x004	Product ID1	Serial ID[3:0]				Reserved				0x4F	R
0x005	Product ID2	Serial ID[11:4]								0x01	R
0x006	Revision	Device version				Device revision				0x11	R
0x00B	SPI version	SPI version								0x00	R
0x00C	Vendor ID	Vendor ID[7:0]								0x56	R
0x00D		Vendor ID[15:8]								0x04	R
0x00F	I/O update	Reserved							I/O update	0x00	R/W
Status Indicator Registers											
0x020	PLL status	Reserved					PLL0 calibration in progress	PLL1 lock detect	PLL0 lock detect	0x00	R
0x021	Reference	Reserved		Reference status		Active reference	REF2 LOR	REF1 LOR	REF0 LOR	0x00	R
Chip Mode Register											
0x040	Mode selection	Reserved						Chip power-down	PLL1 reference select	0x02	R/W
Reference Input Configuration Registers											
0x080	Reference inputs	Reserved	REF1 power-down	REF1 format		Reserved	REF0 power-down	REF0 format		0x00	R/W
0x081		Reserved					REF2 power-down	REF2 format		0x00	R/W
Reference Switchover Registers											
0x082	Reference switchover	Reserved				Disable smooth switchover	Enable XTAL redundancy switchover	Enable soft reference select	Soft reference select	0x00	R/W
0x083	Reference monitor control	Enable reference monitor	Reserved	Monitored frequency	Reference monitor 8 kHz operation	Reference monitor clock frequency		Error window		0x00	R/W
PLL0 Configuration Registers											
0x100	PLL0 controls	Reserved				PLL0 calibration	PLL0 sync	PLL0 power-down	PLL0 reset	0x00	R/W
0x101	PLL0 configuration	Reserved				PLL0 doubler enable	PLL0 loop mode		N0 SDM power-down	0x01	R/W
0x102	PLL0 charge pump current	PLL0 charge pump current								0x8D	R/W
0x103	PLL0 loop filter	PLL0 RPOLE2 loop filter		PLL0 R_{ZERO} loop filter			PLL0 CPOLE1 loop filter			0xE8	R/W
0x104		Reserved							PLL0 loop filter bypass	0x00	R/W
0x105	PLL0 input divider	Reserved		R0 divider ratio						0x01	R/W
0x107	PLL0 fractional feedback divider (integer)	N0 divider integer value								0x64	R/W

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default (Hex)	R/W
0x108	PLL0 fractional feedback divider (fractional)	N0 divider fractional value								0x00	R/W
0x109		N0 divider fractional value								0x00	R/W
0x10A		N0 divider fractional value								0x00	R/W
0x10B	PLL0 fractional feedback divider (modulus)	N0 divider modulus value								0x00	R/W
0x10C		N0 divider modulus value								0x00	R/W
0x10D		N0 divider modulus value								0x00	R/W
0x10E	PLL0 cascaded feedback divider	N0A Divider Ratio								0x00	R/W
0x10F		Reserved				N0A Divider Ratio[11:8]				0x00	R/W
0x110	PLL0 zero delay feedback divider	Reserved		Q_{ZD} divider ratio						0x00	R/W
0x111		Reserved		Q_{ZD} initial phase						0x00	R/W
PLL0 VCO Dividers Registers											
0x120	VCO dividers control	Reserved	M1 sync	M1 power-down	M1 reset	Reserved	M0 sync	M0 power-down	M0 reset	0x20	R/W
0x121	VCO dividers ratios	M1 divider ratio				M0 divider ratio				0x44	R/W
0x122	VCO dividers sync mask	Reserved	M1 mask sync Q2	M1 mask sync Q1	M0 mask sync Q_{ZD}	M0 mask sync Q3	M0 mask sync Q2	M0 mask sync Q1	M0 mask sync Q0	0x00	R/W
PLL0 Distribution Registers											
0x140	Q0 divider	Reserved	Q0 power-down	Q0 divider ratio						0x03	R/W
0x141		Reserved		Q0 initial phase						0x00	R/W
0x142	Channel 0 driver configuration	Reserved					OUT0 power-down	OUT0 driver format		0x00	R/W
0x143	Channel 1 driver configuration	Reserved					OUT1 power-down	OUT1 driver format		0x00	R/W
0x144	Channel 2 driver configuration	Reserved					OUT2 power-down	OUT2 driver format		0x00	R/W
0x145	Channel 3 driver configuration	Reserved					OUT3 power-down	OUT3 driver format		0x00	R/W
0x146	Q1 divider	Reserved	Q1 power-down	Q1 divide ratio						0x03	R/W
0x147		Reserved	Q1 source	Q1 initial phase						0x00	R/W
0x148	Channel 4 driver configuration	Reserved					OUT4 power-down	OUT4 driver format		0x00	R/W
0x149	Channel 5 driver configuration	Reserved					OUT5 power-down	OUT5 driver format		0x00	R/W
0x14A	Q2 Divider	Reserved	Q2 power-down	Q2 divide ratio						0x03	R/W
0x14B		Reserved	Q2 source	Q2 initial phase						0x00	R/W
0x14C	Channel 6 driver configuration	Reserved					OUT6 power-down	OUT6 driver format		0x00	R/W
0x14D	Channel 7 driver configuration	Reserved					OUT7 power-down	OUT7 driver format		0x00	R/W

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default (Hex)	R/W
PLL1 Configuration Registers											
0x200	PLL1 controls	Reserved					PLL1 sync	PLL1 power-down	PLL1 reset	0x00	R/W
0x201	PLL1 feedback divider	N1 divider ratio								0x10	R/W
0x202	PLL1 input dividers	Reserved				R1 divider ratio			PLL1 doubler enable	0x01	R/W
PLL1 Distribution Registers											
0x240	Q3 divider	Reserved	Q3 power-down	Q3 divider ratio						0x83	R/W
0x241		OUT89 source	Q3 source	Q3 initial phase						0x00	R/W
0x242	Channel 8 driver configuration	OUT8 CMOS enable full swing	OUT8 driver format			OUT8 CMOS polarity		OUT8 drive strength	OUT8 enable	0xC1	R/W
0x243	Channel 9 driver configuration	OUT9 CMOS enable full swing	OUT9 driver format			OUT9 CMOS polarity		OUT9 drive strength	OUT9 enable	0xC1	R/W
0x244	Q4 divider	Reserved	Q4 power-down	Q4 divider ratio						0x83	R/W
0x245		Reserved	OUT10 source	Q4 initial phase						0x80	R/W
0x246	Channel 10 driver configuration	OUT10 CMOS enable full swing	OUT10 driver format			OUT10 CMOS polarity		OUT10 drive strength	OUT10 enable	0xC1	R/W

CONTROL REGISTER DESCRIPTIONS

SERIAL PORT CONFIGURATION REGISTERS (REGISTER 0x000 TO REGISTER 0x00F)

Table 42. Serial Port Configuration Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x000	7	Soft reset		Mirror of Bit 0.	0x0	R/W
	6	LSB first		Mirror of Bit 1.	0x0	R/W
	5	Address ascension		Mirror of Bit 2.	0x0	R/W
	[4:3]	Reserved		Reserved.	0x0	R
	2	Address ascension		This bit determines how the register address pointer is automatically changed in a multibyte transfer.	0x0	R/W
			0	Decrement.		
			1	Increment.		
	1	LSB first		This bit determines the bit order for data readback. This bit has no effect in I^2C mode.	0x0	R/W
			0	Serial data stream starts with the LSB.		
			1	Serial data stream starts with the MSB.		
	0	Soft reset		This bit issues a chip level reset. This bit is autoclearing.	0x0	R/W
0x001	7	Single instruction		This bit disables streaming operation. For SPI transfers, this bit forces each data byte to be preceded by a new instruction.	0x0	R/W
	6	Reserved		Reserved.	0x0	R/W
	5	Read buffer registers		This bit specifies the data source for serial port read commands.	0x0	R/W
	[4:3]	Reserved		Reserved.	0x0	R
	2	Reset sans register map		This bit issues a chip level reset, but does not reset register map values.	0x0	R/W
			0	Normal operation.		
			1	Chip held in reset.		
	[1:0]	Reserved		Reserved.	0x0	R
0x003	[7:4]	Reserved		Reserved.	0x0	R
	[3:0]	Chip type		These bits are the unique identifier for the type of device.	0x5	R
0x004	[7:4]	Serial ID[3:0]		These bits are a unique identifier, when combined with chip type, for an individual device supporting the Analog Devices serial control interface standard.	0x4	R
	[3:0]	Reserved		Reserved.	0xF	R
0x005	[7:0]	Serial ID[11:4]		These bits are a unique identifier, when combined with chip type, for an individual device supporting the Analog Devices serial control interface standard.	0x1	R
0x006	[7:4]	Device version		These bits indicate the silicon variant of the device	0x1	R
	[3:0]	Device revision		These bits indicate the silicon revision of the device.	0x1	R
0x00B	[7:0]	SPI version		These bits indicate the version of the analog devices serial control interface standard implemented on the device.	0x0	R
0x00C	[7:0]	Vendor ID[7:0]		These bits are the unique vendor ID and are reflective of the Analog Devices allocated USB vendor ID.	0x56	R
0x00D	[7:0]	Vendor ID[15:8]		These bits are the unique vendor ID and are reflective of the Analog Devices allocated USB vendor ID.	0x4	R
0x00F	[7:1]	Reserved		Reserved.	0x0	R
	0	I/O update		This bit initiates a transfer of the buffered registers to the active registers. This is an autoclearing bit.	0x0	R/W

STATUS INDICATOR REGISTERS (REGISTER 0x020 TO REGISTER 0x021)

Table 43. Status Indicator Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x020	[7:3]	Reserved		Reserved.	0x0	R
	2	PLL0 calibration in progress		This bit indicates the status of the PLL0 VCO calibration.	0x0	R
			0	PLL normal operation.		
			1	VCO calibration active.		
	1	PLL1 lock detect		PLL1 lock detect status.	0x0	R
			0	Unlocked.		
			1	Locked.		
	0	PLL0 lock detect		PLL0 lock detect status.	0x0	R
			0	Unlocked.		
			1	Locked.		
0x021	[7:6]	Reserved		Reserved.	0x0	R
	[5:4]	Reference status		PLL0 active reference frequency indicator. If the reference monitor is Inactive, this bit field indicates the relationship between the requested reference input and the currently active reference.	0x0	R
			00	Agreement.		
			11	Disagreement.		
				If the reference monitor is active, the following settings apply:		
			00	Valid.		
			01	Slow.		
			10	Fast.		
			11	Indeterminate fault.		
	3	Active reference		PLL0 active reference indicator.	0x0	R
			0	REF0.		
			1	REF1.		
	2	REF2 LOR		Reference status indicator.	0x0	R
			0	Reference present.		
			1	Loss of reference.		
	1	REF1 LOR		Reference status indicator.	0x0	R
			0	Reference present.		
			1	Loss of reference.		
	0	REF0 LOR		Reference status indicator.	0x0	R
			1	Loss of reference.		
			0	Reference present.		

CHIP MODE REGISTER (REGISTER 0x040)

Table 44. Chip Mode Register

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x040	[7:2]	Reserved		Reserved.	0x0	R
	1	Chip power-down		Chip level power-down control.	0x1	R/W
			0	Enabled.		
			1	Powered down.		
	0	PLL1 reference select		This bit determines the PLL1 reference input source.	0x0	R/W
			0	PLL0 active reference.		
			1	REF2.		

REFERENCE INPUT CONFIGURATION REGISTERS (REGISTER 0x080 TO REGISTER 0x081)

Table 45. Reference Input Configuration Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x080	7	Reserved		Reserved.	0x0	R
	6	REF1 power-down		Input receiver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[5:4]	REF1 format		Input receiver format.	0x0	R/W
			00	CMOS (V_{DD_x} swing).		
			01	AC-coupled differential.		
			10	XTAL.		
			11	Reserved.		
	3	Reserved		Reserved.	0x0	R
	2	REF0 power-down		Input receiver power-down control.	0x0	R/W
			1	Powered down.		
			0	Normal operation.		
	[1:0]	REF0 format		Input receiver format.	0x0	R/W
			00	CMOS (V_{DD_x} swing).		
			01	AC-coupled differential.		
			10	XTAL.		
			11	Reserved.		
0x081	[7:3]	Reserved		Reserved.	0x0	R
	2	REF2 power-down		Input receiver power-down control.	0x0	R/W
			1	Powered down.		
			0	Normal operation.		
	[1:0]	REF2 format		Input receiver format.	0x0	R/W
			00	CMOS (V_{DD_x} swing).		
			01	AC-coupled differential.		
			10	XTAL.		
			11	Reserved.		

REFERENCE SWITCHOVER REGISTERS (REGISTER 0x082 TO REGISTER 0x083)

Table 46. Reference Switchover Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x082	[7:4]	Reserved		Reserved.	0x0	R
	3	Disable smooth switchover		This bit sets the reference switchover mode.	0x0	R/W
			0	Bounded phase transient.		
			1	Immediate.		
	2	Enable XTAL redundancy switchover		This bit requires the reference monitor to be enabled and both REF0 and REF1 to be configured as XTAL inputs.	0x0	R/W
	1	Enable soft reference select		This bit establishes the control source of the PLL0 reference input mux select line. Not applicable when XTAL redundancy switchover is enabled.	0x0	R/W
			0	REF_SEL pin (Pin 3).		
			1	Soft reference select (Register 0x082, Bit 0).		
	0	Soft reference select		This bit controls the PLL0 reference input mux select line. Applicable only when the enable soft reference select = 1.	0x0	R/W
			0	REF0 select.		
			1	REF1 select.		
0x083	7	Enable reference monitor		The REF2 input clock serves as the reference monitor frequency reference.	0x0	R/W
	6	Reserved		Reserved.	0x0	R
	5	Monitored frequency		This bit determines the frequency being monitored by the reference monitor.	0x0	R/W
			0	REF0 and REF1 input frequency is 25 MHz.		
			1	REF0 and REF1 input frequency is 19.44 MHz.		
	4	Reference monitor 8 kHz operation		This bit configures the reference monitor for an 8 kHz frequency reference and overrides the reference monitor clock frequency bit field (Register 0x083, Bits[3:2]).	0x0	R/W
	[3:2]	Reference monitor clock frequency		These bits designate the reference monitor frequency reference carrier.	0x0	R/W
			00	10 MHz.		
			01	19.44 MHz.		
			10	25 MHz.		
			11	38.88 MHz.		
	[1:0]	Error window		These bits set the frequency tolerance for a reference monitor decision.	0x0	R/W
			00	±10 ppm.		
			01	±25 ppm.		
			10	±50 ppm.		
			11	±100 ppm.		

PLL0 CONFIGURATION REGISTERS (REGISTER 0x100 TO REGISTER 0x111)

Table 47. PLL0 Configuration Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x100	[7:4]	Reserved		Reserved.	0x0	R
	3	PLL0 calibration		This bit issues a manual VCO calibration on a low to high transition.	0x0	R/W
	2	PLL0 sync		This bit issues a distribution sync command to the dividers driven by PLL0.	0x0	R/W
			0	Normal operation.		
			1	Dividers held in sync.		
	1	PLL0 power-down		PLL0 power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	0	PLL0 reset		PLL0 reset control.	0x0	R/W
			0	Normal operation.		
			1	Reset.		
0x101	[7:4]	Reserved		Reserved.	0x0	R
	3	PLL0 doubler enable		This bit selects the PLL0 input divider path used.	0x0	R/W
			0	R0 divider output.		
			1	×2.		
	[2:1]	PLL0 loop mode		These bits select the PLL0 feedback path.	0x0	R/W
			00	Loop Mode 0 (single feedback divider).		
			01	Loop Mode 1 (cascaded feedback dividers).		
			10	Loop Mode 2 (fixed delay divider).		
			11	Reserved.		
	0	N0 SDM power-down		N0 SDM power-down control	0x1	R/W
			0	Normal operation.		
			1	Powered down.		
0x102	[7:0]	PLL0 charge pump current		These bits control the magnitude of the PLL0 charge pump current.	0x8D	R/W
				Total current (μA) = 4 × the bit field value.		
0x103	[7:6]	PLL0 RPOLE2 loop filter		Internal loop filter Pole 2 resistor setting.	0x3	R/W
			00	2000 Ω.		
			01	666 Ω.		
			10	400 Ω.		
			11	285 Ω.		
	[5:3]	PLL0 R_{ZERO} loop filter		Internal loop filter zero resistor setting.	0x5	R/W
			000	1500 Ω.		
			001	1875 Ω.		
			010	2250 Ω.		
			011	2650 Ω.		
			100	3000 Ω.		
			101	3375 Ω.		
			110	3750 Ω.		
			111	4125 Ω.		
	[2:0]	PLL0 CPOLE1 loop filter		Internal loop filter Pole 1 capacitor setting.	0x0	R/W
			000	2 pF.		
			001	8 pF.		
			010	42 pF.		
			011	48 pF.		
			100	82 pF.		
			101	88 pF.		
			110	122 pF.		
			111	128 pF.		

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x104	[7:1]	Reserved		Reserved.	0x0	R
	0	PLL0 loop filter bypass		This bit bypasses the internal loop filter.	0x0	R/W
0x105	[7:6]	Reserved		Reserved.	0x0	R
	[5:0]	R0 divider ratio		PLL0 reference input divide ratio.	0x1	R/W
			0	Reserved.		
			1 to 63	Divide ratio = bit field value.		
0x107	[7:0]	N0 divider integer value		These bits set the operating divide ratio. Divide ratio = bit field value.	0x64	R/W
			0 to 11	Invalid.		
			12 to 14	Valid if the SDM is disabled.		
			15 to 252	Valid.		
			253 to 255	Valid if the SDM is disabled.		
0x108	[7:0]	N0 divider fractional value		These bits set the SDM fractional value, Bits[7:0].	0x0	R/W
0x109	[7:0]			These bits set the SDM fractional value, Bits[15:8].	0x0	R/W
0x10A	[7:0]			These bits set the SDM fractional value, Bits[23:16].	0x0	R/W
0x10B	[7:0]	N0 divider modulus value		These bits set the SDM modulus value, Bits[7:0]. These bits must be greater than fractional value.	0x0	R/W
0x10C	[7:0]			These bits set the SDM modulus value, Bits[15:8]. These bits must be greater than fractional value.	0x0	R/W
0x10D	[7:0]			These bits set the SDM modulus value, Bits[23:16]. These bits must be greater than fractional value.	0x0	R/W
0x10E	[7:0]	N0A Divider Ratio[7:0]		These bits set the operating divide ratio. Divide ratio = bit field value.	0x0	R/W
			0 to 3	Invalid.		
			4 to 4095	Valid.		
0x10F	[7:4]	Reserved		Reserved.	0x0	R
	[3:0]	N0A Divider Ratio[11:8]		These bits set the operating divide ratio. Divide ratio = bit field value.	0x0	R/W
			0 to 3	Invalid.		
			4 to 4095	Valid.		
0x110	[7:6]	Reserved		Reserved.	0x0	R
	[5:0]	Q_{ZD} divider ratio		PLL0 fixed delay feedback divider ratio.	0x0	R/W
				Divide ratio = bit field value + 1.		
0x111	[7:6]	Reserved		Reserved.	0x0	R
	[5:0]	Q_{ZD} initial phase		PLL0 fixed delay feedback divider static phase offset.	0x0	R/W
				Phase offset in units of half cycles of the input clock.		

PLL0 VCO DIVIDERS REGISTERS (REGISTER 0x120 TO REGISTER 0x122)

Table 48. PLL0 VCO Dividers Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x120	7	Reserved		Reserved.	0x0	R
	6	M1 sync		This bit issues a distribution sync command to the dividers driven by M1.	0x0	R/W
			0	Normal operation.		
			1	Dividers held in reset.		
	5	M1 power-down		Divider power-down control.	0x1	R/W
			0	Normal operation.		
			1	Powered down.		
	4	M1 reset		Divider reset control	0x0	R/W
			0	Normal operation.		
			1	Divider held in reset.		
	3	Reserved		Reserved.	0x0	R
	2	M0 sync		This bit issues a distribution sync command to the dividers driven by M0.	0x0	R/W
			0	Normal operation.		
			1	Dividers held in reset.		
	1	M0 power-down		Divider power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	0	M0 reset		Divider reset control	0x0	R/W
			0	Normal operation.		
			1	Divider held in reset.		
0x121	[7:4]	M1 divider ratio		Sets operating divide ratio.	0x4	R/W
			0 to 1	Powered down.		
			2 to 11	Divide = bit field value.		
			12 to 15	Powered down.		
	[3:0]	M0 divide ratio		These bits set the operating divide ratio.	0x4	R/W
			0 to 1	Powered down.		
			2 to 11	Divide = bit field value.		
			12 to 15	Powered down.		
0x122	7	Reserved		Reserved.	0x0	R
	6	M1 mask sync Q2		This bit sets the Divider Q2 ignore and M1 sync signal flag.	0x0	R/W
	5	M1 mask sync Q1		This bit sets the Divider Q1 ignore and M1 sync signal flag.	0x0	R/W
	4	M0 mask sync Q_{ZD}		This bit sets the Divider Q_{ZD} ignore and M0 sync signal flag.	0x0	R/W
	3	M0 mask sync Q3		This bit sets the Divider Q3 ignore and M0 sync signal flag.	0x0	R/W
	2	M0 mask sync Q2		This bit sets the Divider Q2 ignore and M0 sync signal flag.	0x0	R/W
	1	M0 mask sync Q1		This bit sets the Divider Q1 ignore and M0 sync signal flag.	0x0	R/W
	0	M0 mask sync Q0		This bit sets the Divider Q0 ignore and M0 sync signal flag.	0x0	R/W

PLL0 DISTRIBUTION REGISTERS (REGISTER 0x140 TO REGISTER 0x14D)

Table 49. PLL0 Distribution Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x140	7	Reserved		Reserved.	0x0	R
	6	Q0 power-down		Divider power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[5:0]	Q0 divider ratio		These bits set the operating divide ratio. Divide ratio = bit field value + 1.	0x3	R/W
0x141	[7:6]	Reserved		Reserved.	0x0	R
	[5:0]	Q0 initial phase		These bits set the divider static phase offset. The phase offset is in units of half cycles of the input clock.	0x0	R/W
0x142	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT0 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT0 driver format		These bits select the driver format of OUT0.	0x0	R/W
			00	LVDS, 3.5 mA.		
			01	LVDS, 4.2 mA.		
			10	HSTL, 8 mA.		
			11	1.8 V CMOS.		
0x143	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT1 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT1 driver format		These bits select the driver format of OUT1.	0x0	R/W
			00	LVDS, 3.5 mA.		
			01	LVDS, 4.2 mA.		
			10	HSTL, 8 mA.		
			11	1.8 V CMOS.		
0x144	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT2 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT2 driver format		These bits select the driver format of OUT2.	0x0	R/W
			00	LVDS, 3.5 mA.		
			01	LVDS, 4.2 mA.		
			10	HSTL, 8 mA.		
			11	1.8 V CMOS.		
0x145	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT3 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT3 driver format		These bits select the driver format of OUT3.	0x0	R/W
			00	LVDS 3.5 mA.		
			01	LVDS 4.2 mA.		
			10	HSTL 8 mA.		
			11	1.8 V CMOS.		
0x146	7	Reserved		Reserved.	0x0	R
	6	Q1 power-down		Divider power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[5:0]	Q1 divide ratio		These bits set the operating divide ratio. Divide ratio = bit field value + 1.	0x3	R/W

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x147	7	Reserved		Reserved.	0x0	R
	6	Q1 source		This bit selects the divider input clock.	0x0	R/W
			0	M0 output.		
			1	M1 output.		
	[5:0]	Q1 initial phase		These bits set the divider static phase offset. The phase offset is in units of half cycles of the input clock.	0x0	R/W
0x148	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT4 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT4 driver format		These bits select the driver format of OUT4.	0x0	R/W
			00	LVDS, 3.5 mA.		
			01	LVDS, 4.2 mA.		
			10	HSTL, 8 mA.		
			11	1.8 V CMOS.		
0x149	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT5 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT5 driver format		These bits select the driver format of OUT5.	0x0	R/W
			00	LVDS, 3.5 mA.		
			01	LVDS, 4.2 mA.		
			10	HSTL, 8 mA.		
			11	1.8 V CMOS.		
0x14A	7	Reserved		Reserved.	0x0	R
	6	Q2 power-down		Divider power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[5:0]	Q2 divide ratio		These bits set the operating divide ratio. Divide ratio = bit field value + 1.	0x3	R/W
0x14B	7	Reserved		Reserved.	0x0	R
	6	Q2 source		This bit selects the divider input clock.	0x0	R/W
			0	M0 output.		
			1	M1 output.		
	[5:0]	Q2 initial phase		These bits set the divider static phase offset. The phase offset is in units of half cycles of the input clock.	0x0	R/W
0x14C	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT6 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT6 driver format		These bits select the driver format of OUT6.	0x0	R/W
			00	LVDS, 3.5 mA.		
			01	LVDS, 4.2 mA.		
			10	HSTL, 8 mA.		
			11	1.8 V CMOS.		
0x14D	[7:3]	Reserved		Reserved.	0x0	R
	2	OUT7 power-down		Driver power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[1:0]	OUT7 driver format		These bits select the driver format of OUT7.	0x0	R/W
			00	LVDS, 3.5 mA.		
			01	LVDS, 4.2 mA.		
			10	HSTL, 8 mA.		
			11	1.8 V CMOS.		

PLL1 CONFIGURATION REGISTERS (REGISTER 0x200 TO REGISTER 0x202)

Table 50. PLL1 Configuration Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x200	[7:3]	Reserved		Reserved.	0x0	R
	2	PLL1 sync		Issues a distribution sync command to dividers driven by PLL1.	0x0	R/W
			0	Normal operation.		
			1	Dividers held in sync.		
	1	PLL1 power-down		PLL power-down control.	0x0	R/W
			0	Normal operation.		
			1	Power down.		
	0	PLL1 reset		PLL reset control.	0x0	R/W
			0	Normal operation.		
			1	PLL1 held in reset.		
0x201	[7:0]	N1 divider ratio		These bits set the operating divide ratio. Divide value = bit field value.	0x10	R/W
			0 to 3	Invalid values.		
			4 to 255	Valid values.		
0x202	[7:4]	Reserved		Reserved.	0x0	R
	[3:1]	R1 divider ratio		PLL1 reference input divider.	0x0	R/W
			0	Power down.		
			1	÷1.		
			10	÷1.5.		
			11	÷2.		
			100	÷3.		
			101	÷4.		
			110	÷6.		
			111	÷8.		
	0	PLL1 doubler enable		This bit selects the PLL1 input divider path used.	0x1	R/W
			0	R1 divider output.		
			1	×2.		

PLL1 DISTRIBUTION REGISTERS (REGISTER 0x240 TO REGISTER 0x246)

Table 51. PLL1 Distribution Registers

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x240	7	Reserved		Reserved. Always configure this bit to the default value.	0x1	R/W
	6	Q3 power-down		Divider power-down control.	0x0	R/W
			0	Normal operation.		
			1	Powered down.		
	[5:0]	Q3 divider ratio		These bits set the operating divide ratio. Divide ratio = bit field value + 1.	0x3	R/W
0x241	7	OUT89 source		This bit selects the OUT8 and OUT9 input clock.	0x0	R/W
			0	Q3 divider output.		
			1	PLL1 active reference.		
	6	OUT10 source		This bit selects the divider input clock.	0x0	R/W
			0	PLL1 output.		
			1	M0 output.		
	[5:0]	Q3 initial phase		These bits select the divider static phase offset. The phase offset is in units of half cycles of the input clock.	0x0	R/W

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x242	7	OUT8 CMOS enable full swing		This bit determines the full swing of the OUT8 CMOS driver. Set this bit only if the associated output format is configured as CMOS.	0x1	R/W
			0	1.8 V swing.		
			1	Full swing.		
	[6:4]	OUT8 driver format		These bits select the driver format of OUT8.	0x4	R/W
			000	Tristate.		
			001	HSTL.		
			010	LVDS.		
			011	HCSL.		
			100	CMOS (both outputs active).		
			101	CMOS (positive output only).		
			110	CMOS (negative output only).		
			111	Reserved.		
	[3:2]	OUT8 CMOS polarity		These bits set the polarity of the full swing CMOS output driver.	0x0	R/W
			00	Noninverted, inverted.		
			01	Inverted, inverted.		
			10	Noninverted, noninverted.		
			11	Inverted, noninverted.		
	1	OUT8 drive strength		This bit selects the drive strength of the OUT8 driver and is only applicable when the output format is configured as LVDS or full swing CMOS.	0x0	R/W
			0	CMOS—nominal drive; LVDS—3.5 mA.		
			1	CMOS—low drive; LVDS—4.5 mA.		
	0	OUT8 enable		Output driver enable control.	0x1	R/W
			0	Power down.		
			1	Enable.		
0x243	7	OUT9 CMOS enable full swing		This bit determines the swing of the OUT9 CMOS driver. Set this bit only if the associated output format is configured as CMOS.	0x1	R/W
			0	1.8 V swing.		
			1	Full swing.		
	[6:4]	OUT9 driver format		These bits select the driver format of OUT9.	0x4	R/W
			000	Tristate.		
			001	HSTL.		
			010	LVDS.		
			011	HCSL.		
			100	CMOS (both outputs active).		
			101	CMOS (positive output only).		
			110	CMOS (negative output only).		
			111	Reserved.		
	[3:2]	OUT9 CMOS polarity		These bits set the polarity of the full swing CMOS output driver.	0x0	R/W
			00	Noninverted, inverted.		
			01	Inverted, inverted.		
			10	Noninverted, noninverted.		
			11	Inverted, noninverted.		
	1	OUT9 drive strength		This bit selects the drive strength of the OUT9 driver and is only applicable when the output format is configured as LVDS or full swing CMOS.	0x0	R/W
			0	CMOS—nominal drive; LVDS—3.5 mA.		
			1	CMOS—low drive; LVDS—4.5 mA.		
	0	OUT9 enable		Output driver enable control.	0x1	R/W
			0	Power down.		
			1	Enable.		

Address	Bits	Bit Name	Settings	Description	Reset	Access
0x244	7	Reserved		Reserved. Always configure this bit to the default value.	0x1	R/W
	6	Q4 power-down		Divider power-down control.	0x0	R/W
			0	Normal operation (default). The Q4 divider works normally.		
			1	Powered down. The Q0 divider is powered down.		
	[5:0]	Q4 divider ratio		These bits set the operating divide ratio. Divide ratio = bit field value + 1.	0x3	R/W
0x245	7	Reserved		Reserved. Always configure this bit to the default value.	0x1	R/W
	6	Q4 source		This bit selects the OUT10 input clock source.	0x0	R/W
			1	PLL1 selected reference input.		
			0	Divider, Q4, output.		
	[5:0]	Q4 initial phase		These bits set the divider static phase offset. The phase offset in units of half cycles of the input clock.	0x0	R/W
0x246	7	OUT10 CMOS enable full swing		This bit determines the full swing of the OUT10 CMOS driver. Only set this bit if the associated output format is configured as CMOS.	0x1	R/W
			0	1.8 V swing.		
			1	Full swing.		
	[6:4]	OUT10 driver format		These bits select the driver format of OUT10.	0x4	R/W
			000	Tristate.		
			001	HSTL.		
			010	LVDS.		
			011	HCSL.		
			100	CMOS (both outputs active).		
			101	CMOS (positive output only).		
			110	CMOS (negative output only).		
			111	Reserved.		
	[3:2]	OUT10 CMOS polarity		These bits set the polarity of the full swing CMOS output driver.	0x0	R/W
			00	Noninverted, inverted.		
			01	Inverted, inverted.		
			10	Noninverted, noninverted.		
			11	Inverted, noninverted.		
	1	OUT10 drive strength		This bit selects the drive strength of the OUT10 driver and is only applicable when the output format is configured as LVDS or full swing CMOS.	0x0	R/W
			0	CMOS—nominal drive; LVDS—3.5 mA.		
			1	CMOS—low drive; LVDS—4.5 mA.		
	0	OUT10 enable		Output driver enable control.	0x1	R/W
			0	Power down.		
			1	Enable.		

APPLICATIONS INFORMATION

INTERFACING TO CMOS CLOCK OUTPUTS

Apply the following general guidelines when using the single-ended 1.8 V or 3.3 V CMOS clock output drivers.

Design point to point nets such that a driver has only one receiver on the net, if possible. This allows simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver.

The value of the series termination depends on the board design and timing requirements (typically 10 Ω to 100 Ω). CMOS outputs are limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 6 inches are recommended to preserve signal rise/fall times and signal integrity.

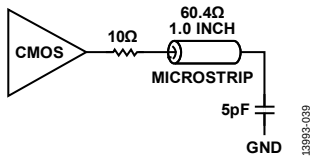


Figure 39. Series Termination of CMOS Output

Termination at the far end of the PCB trace is a second option. The CMOS outputs of the AD9576 do not supply enough current to provide a full voltage swing with a low impedance resistive, far end termination, as shown in Figure 40. Ensure that the impedance of the far end termination network matches the PCB trace impedance and provides the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

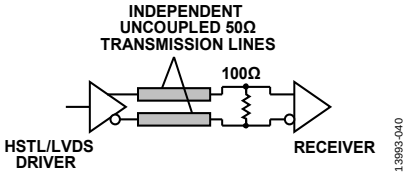


Figure 40. LVDS or HSTL Output Termination

INTERFACING TO LVDS AND HSTL CLOCK OUTPUTS

LVDS and HSTL both employ a differential output driver. The recommended termination circuit for LVDS and HSTL drivers appears in Figure 41.

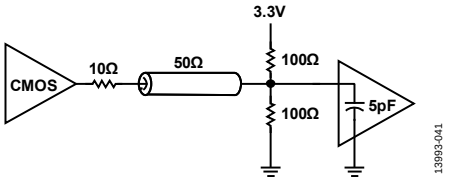


Figure 41. CMOS Output with Far End Termination

See the AN-586 Application Note for more information about LVDS.

INTERFACING TO HCSL CLOCK OUTPUTS

HCSL uses a differential open-drain architecture. The open-drain architecture necessitates the use of an external termination resistor. Figure 42 shows the typical method for interfacing to HCSL drivers.

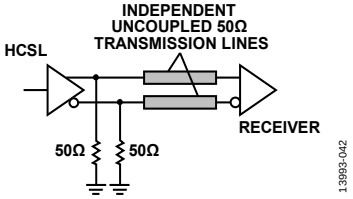


Figure 42. HCSL Output Termination

In some cases, the fast switching capability of HCSL drivers results in overshoot and ringing. The alternative HCSL interface shown in Figure 43 can mitigate this problem via a small series resistor, typically in the 10 Ω to 30 Ω range.

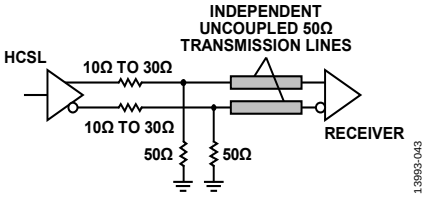


Figure 43. Alternate HCSL Output Termination

POWER SUPPLY

The AD9576 requires a power supply of 2.5 V ± 5% or 3.3 V ± 10%. The Specifications section gives the performance expected from the AD9576 with the power supply voltage within this range. The absolute maximum range of −0.3 V to +3.6 V, with respect to GND, must never be exceeded on the VDD_x pins.

Follow good engineering practice in the layout of power supply traces and the ground plane of the PCB. Bypass the power supply on the PCB with adequate capacitance (>10 µF). Bypass the AD9576 with adequate capacitors (0.1 µF) at all power pins as close as possible to the device.

In addition to these bypass capacitors, the AD9576 evaluation board uses six ferrite beads between the 2.5 V (or 3.3 V) source and Pin 29, Pin 35, Pin 41, Pin 46, Pin 52, and Pin 57. Although these ferrite beads may not be needed for every application, the use of these ferrite beads is strongly recommended. At a minimum, include a place for the ferrite beads (as close to the bypass capacitors as possible) and populate the board with 0402, 0 Ω resistors. By doing so, there is a place for the ferrite beads, if needed. Ferrite beads with low (<0.7 Ω) dc resistance and approximately 600 Ω impedance at 100 MHz are suitable for use with Pin 29, Pin 35, Pin 41, and Pin 46, while ferrite beads with approximately 75 Ω impedance at 100 MHz are suitable for use with Pin 52 and Pin 57.

The layout of the AD9576 evaluation board is a good example of how to route power supply traces and where to place bypass capacitors and ferrite beads.

The exposed metal pad on the AD9576 package is an electrical connection, as well as a thermal enhancement. For the device to function properly, the pad must be properly attached to ground (GND). The PCB acts as a heat sink for the AD9576; therefore, this GND connection provides a good thermal path to a larger heat dissipation area, such as a ground plane on the PCB.

POWER AND GROUNDING CONSIDERATIONS AND POWER SUPPLY REJECTION

Many applications seek high speed and performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the PCB is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as for power supply bypassing and grounding to ensure optimum performance.

OUTLINE DIMENSIONS

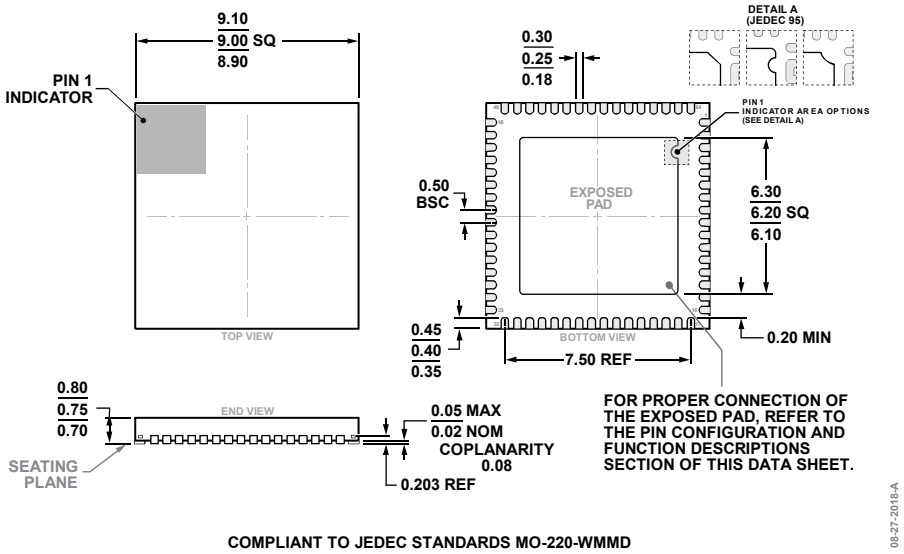


Figure 44. 64-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 9 mm and 0.75 mm Package Height
(CP-64-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9576BCPZ	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
AD9576BCPZ-REEL7	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
AD9576/PCBZ		Evaluation Board	

[1]Z = RoHS-Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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