One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Register Map Reference Manual for the AD9542

INTRODUCTION

This reference manual contains the complete register map and details for the AD9542, used in conjunction with the AD9542 data sheet.

The AD9542 has five differential outputs, and the user can reconfigure each differential output as two single-ended outputs.

The pin names for each differential output follows the naming convention OUTxyP/N, where x is 0 for DPLL Channel 0 and 1 for DPLL Channel 1. In this naming convention, y refers to the output number and can be 0, 1, or 2 for DPLL Channel 0, and either 0 or 1 for DPLL Channel 1.

Each output has a distribution divider that follows the naming convention of Qxy for positive outputs and Qxyy for negative (or complementary) outputs. Distribution Divider Qxy connects to Output Driver OUTxyP, and Distribution Divider Qxyy connects to OUTxyN. For example, Distribution Divider Q0AA connects to the output driver connected to the OUT0AN pin, and Distribution Divider Q1B connects to the output driver connected to the OUT1BP pin.

Note that throughout this reference manual, multifunction pins, such as SDO/M5, are referred to by a single function of the pin, for example, M5, when only that function is relevant.

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT
WARNING AND LEGAL TERMS AND CONDITIONS.

TABLE OF CONTENTS

Introduction 1
Revision History 2
Registers 3
Serial Port Registers—Register 0x0000 to Register 0x0023 3
Mx Pin Registers—Register 0x0100 to Register 0x010B 5
Mx Pin Function Registers—Register 0x0102 to Register 0x0108 10
IRQ Map Common Mask Registers—Register 0x10C to Register 0x110 13
IRQ Map DPLL0 Mask Registers—Register 0x0111 to Register 0x0115 15
IRQ Map DPLL1 Mask Registers—Register 0x116 to Register 0x11A 17
System Clock (SYSCLK) Registers—Register 0x0200 to Register 0x0209 18
SYSCLK Compensation Registers—Register 0x0280 to Register 0x029C 20
Reference General A Register—Register 0x0300 24
Reference General B Register—Register 0x0304 25
Reference Input A (REFA) Registers—Register 0x0400 to Register 0x0414 26
Reference Input AA (REFAA) Registers—Register 0x0420 to Register 0x0434 28
Reference Input B (REFB) Registers—Register 0x0440 to Register 0x0454 30
Reference Input BB (REFBB) Registers—Register 0x0460 to Register 0x0474 32
Source Profile 0 A Registers—Register 0x0800 to Register 0x0811 34
Loop Filter Coefficients 0 Registers—Register 0x0C00 to Register 0x0C0B 36
Loop Filter Coefficients 1 Registers—Register 0x0C0C to Register 0x0C17 36
DPLL Channel 0 Registers—Register 0x1000 to Register 0x102A 37
Distribution General 0 Registers—Register 0x10D2 to Register 0x10DC 43
APLL Channel 0 Registers—Register 0x1080 to Register 0x1083 47
Distribution Divider Q0A Registers—Register 0x1100 to Register 0x1108 48
DPLL Translation Profile 0.0 Registers—Register 0x1200 to Register 0x1217 50
DPLL Channel 1 Registers—Register 0x1400 to Register 0x142A 54
Distribution General 1 Registers—Register 0x14D2 to Register 0x14DC 60
APLL Channel 1 Registers—Register 0x1480 to Register 0x1483 64
Distribution Divider Q1A Registers—Register 0x1500 to Register 0x1508 65
DPLL Translation Profile 1.0 Registers—Register 0x1600 to Register 0x1617 67
Operational Controls General Registers—Register 0x2000 to Register 0x2005 71
IRQ Map Common Clear Registers—Register 0x2006 to Register 0x200A 74
IRQ Map DPLL0 Clear Registers—Register 0x200B to Register 0x200F 75
Operational Control Channel 0 Registers—Register 0x2100 to Register 0x2107 77
Operational Control Channel 1 Registers—Register 0x2200 to Register 0x2207 82
Temperature Sensor Registers—Register 0x2900 to Register 0x2906 87
EEPROM Registers—Register 0x2E00 to Register 0x2E1E .. 88
Status Readback Registers—Register 0x3000 to Register 0x300A 90
IRQ Map Common Read Registers—Register 0x300B to Register 0x300F 94
IRQ Map DPLL0 Read Registers—Register 0x3010 to Register 0x3014 96
IRQ Map DPLL1 Read Registers—Register 0x3015 to Register 0x3019 97
Status Readback PLL0 Registers—Register 0x3100 to Register 0x310E 99
Status Readback PLL1 Registers—Register 0x3200 to Register 0x320E 102

REVISION HISTORY

9/2017—Revision 0: Initial Version

REGISTERS

SERIAL PORT REGISTERS—REGISTER 0x0000 TO REGISTER 0x0023

Table 1. Serial Port Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0000	Configuration	Soft reset	LSB first (SPI only)	Address ascension (SPI only)	SDO active (SPI only)		Address ascension (SPI only)	LSB first (SPI only)	Soft reset	0x00	0x00
0x0001		Reserved		Read buffer register	Reserved		Reset sans register map	Reserved		0x00	R/W
0x0004	Part ID	Part ID [7:0]								0x20	R
0x0005		Part ID [15:8]								0x01	R
0x000B	SPI version	SPI version								0x00	R
0x000C	Vendor ID	Vendor ID [7:0]								0x56	R
0x000D		Vendor ID [15:8]								0x04	R
0x000F	IO_UPDATE	Reserved						Address loop IO_UPDATE	IO_UPDATE	0x00	R/W
0x0010	Loop length	Address loop length								0x00	R/W
0x0020	Scratch pad	User scratchpad [7:0]								0x00	R/W
0x0021		User scratchpad [15:8]								0x00	R/W
0x0022		User scratchpad [23:16]								0x00	R/W
0x0023		User scratchpad [31:24]								0x00	R/W

Table 2. Serial Port Registers Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0000	Configuration	7	Soft reset		Soft reset. This bit must be set identically to the other soft reset bit in this register.	0x0	R/W
		6	LSB first (SPI only)		Serial peripheral interface (SPI) least significant bit (LSB) first. This bit must be set identically to the other LSB first (SPI only) bit in this register.	0x0	R/W
				0	Most significant bit (MSB) first.		
				1	LSB first.		
		5	Address ascension (SPI only)		SPI address ascension. This bit must be set identically to the other address ascension bit in this register.	0x0	R/W
				0	Address descension mode.		
				1	Address ascension mode.		
		4	SDO active (SPI only)		Enable SPI 4-wire mode. This bit must be set identically to the other serial data output (SDO) active bit in this register.	0x0	R/W
				0	3-wire SPI mode.		
				1	4-wire SPI mode (SDO pin active)		
		3	SDO active (SPI only)		Enable SPI 4-wire mode. This bit enables the SPI port SDO pin. This bit has no effect in I^2C mode.	0x0	R/W
				0	3-wire SPI mode.		
				1	4-wire SPI mode (SDO pin active).		
		2	Address ascension (SPI only)		SPI address ascension. This bit controls whether the register address is automatically incremented during a multibyte transfer. This bit has no effect in I^2C mode.	0x0	R/W
				0	Address descension mode. The address pointer is automatically decremented. For multibyte bit fields, the most significant byte is read first.		
				1	Address ascension mode. The address pointer is automatically incremented. For multibyte bit fields, the least significant byte is read first.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	LSB first (SPI only)		SPI LSB first. This bit sets the bit order for the SPI port. Setting this bit to 1 selects SPI LSB first mode, and setting it to 0 selects MSB first mode. This bit has no effect in I²C mode.	0x0	R/W
				0	MSB first.		
				1	LSB first.		
		0	Soft reset		Soft reset. Invokes an EEPROM download or pin program ROM download if EEPROM is enabled.	0x0	R/W
0x0001		[7:6]	Reserved		Reserved.	0x0	R
		5	Read buffer register		Read buffer register. For buffered registers, this bit controls whether the value read from the serial port is from the actual active registers or the buffered copy.	0x0	R/W
				0	Reads the register values that are currently active (default).		
				1	Reads buffered values that take effect the next time the user writes 1b to the IO_UPDATE bit.		
		[4:3]	Reserved		Reserved.	0x0	R
		2	Reset sans register map		Reset sans register map. This autoclearing bit resets the device while maintaining the current settings.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R
0x0004	Part ID	[7:0]	Part ID [7:0]		Part ID. This read only bit field identifies this device as a member of the AD9542/AD9545 family.	0x21	R
0x0005		[7:0]	Part ID [15:8]			0x01	R
0x000B	SPI version	[7:0]	SPI version		Version of Analog Devices, Inc., unified SPI protocol.	0x0	R
0x000C	Vendor ID	[7:0]	Vendor ID [7:0]		Analog Devices unified SPI vendor ID.	0x56	R
				0x0456	Analog Devices.		
				0x0000	Other vendor.		
0x000D		[7:0]	Vendor ID [15:8]		Analog Devices unified SPI vendor ID.	0x4	R
				0x0456	Analog Devices.		
				0x0000	Other vendor.		
0x000F	IO_UPDATE	[7:2]	Reserved		Reserved.	0x0	R
		1	Address loop IO_UPDATE		When this bit is 1, an IO_UPDATE command is automatically issued each time the address field loops. This is useful when polling a range of registers, and an IO_UPDATE command must be issued after each cycle.	0x0	R/W
		0	IO_UPDATE		Input/output update. Setting this autoclearing bit to Logic 1 transfers values from the buffered to the active register space, and this action is called an IO_UPDATE command in this reference manual. Unless a register is identified as a live register, the user must perform this command for the value written to a buffered register to take effect and for a read only buffered register to read back its most current value.	0x0	WC
0x0010	Loop length	[7:0]	Address loop length		Address loop length. The number of consecutive addresses that are written or read in each cycle in an address loop.	0x0	R/W
0x0020	Scratch pad	[7:0]	User scratchpad [7:0]		User scratchpad. This register has no effect on device operation. It is available for device debugging or register setting revision control.	0x0	R/W
0x0021		[7:0]	User scratchpad [15:8]			0x0	R/W
0x0022		[7:0]	User scratchpad [23:16]			0x0	R/W
0x0023		[7:0]	User scratchpad [31:24]			0x0	R/W

Mx PIN REGISTERS—REGISTER 0x0100 TO REGISTER 0x010B

The M0 through M6 pins are individually configurable as either status or control pins using the registers in this section. Bit 7 of Register 0x0102 through Register 0x0108 determine whether M0 through M6 are an input (control) pin or an output (status) pin.

Table 3. Mx Pin Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0100	Mx pin mode	M3 driver/receiver		M2 driver/receiver		M1 driver/receiver		M0 driver/receiver		0x00	R/W
0x0101	Mx pin mode	Reserved		M6 driver/receiver		M5 driver/receiver		M4 driver/receiver		0x00	R/W
0x0102	M0	M0 output enable	M0 control/status function							0x00	R/W
0x0103	M1	M1 output enable	M1 control/status function							0x00	R/W
0x0104	M2	M2 output enable	M2 control/status function							0x00	R/W
0x0105	M3	M3 output enable	M3 control/status function							0x00	R/W
0x0106	M4	M4 output enable	M4 control/status function							0x00	R/W
0x0107	M5	M5 output enable	M5 control/status function							0x00	R/W
0x0108	M6	M6 output enable	M6 control/status function							0x00	R/W
0x0109	Pin drive strength	SPI configuration	M6 configuration	M5 configuration	M4 configuration	M3 configuration	M2 configuration	M1 configuration	M0 configuration	0x00	R/W
0x010A	Watchdog timer	Watchdog timer (ms) [7:0]								0x00	R/W
0x010B	Watchdog timer	Watchdog timer (ms) [15:8]								0x00	R/W

Table 4. Mx Pin Register Description

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0100	Mx pin mode	[7:6]	M3 driver		M3 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high complementary metal-oxide semiconductor (CMOS).	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain positive metal-oxide semiconductor (PMOS) (requires an external pull-down resistor).		
				11	Open-drain negative metal-oxide semiconductor (NMOS) (requires an external pull-up resistor).		
		[7:6]	M3 receiver		M3 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined; at least one must be high for the assigned control input to be considered true.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				11	OR inverted mode. This mode allows two or more Mx pins to be combined; at least one must be low for the assigned control input to be considered true.		
		[5:4]	M2 driver		M2 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[5:4]	M2 receiver		M2 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined; at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined; at least one must be low for the assigned control input to be considered true.		
		[3:2]	M1 driver		M1 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[3:2]	M1 receiver		M1 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined; at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined; at least one must be low for the assigned control input to be considered true.		
		[1:0]	M0 driver		M0 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[1:0]	M0 receiver		M0 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined; at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined; at least one must be low for the assigned control input to be considered true.		
0x0101	Mx pin mode	[7:6]	Reserved		Reserved.	0x0	R
		[5:4]	M6 driver		M6 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[5:4]	M6 receiver		M6 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined; at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined; at least one must be low for the assigned control input to be considered true.		
		[3:2]	M5 driver		M5 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[3:2]	M5 receiver		M5 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be low for the assigned input function to be considered true.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				10	OR true mode. This mode allows two or more Mx pins to be combined; at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined; at least one must be low for the assigned control input to be considered true.		
		[1:0]	M4 driver		M4 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[1:0]	M4 receiver		M4 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined; all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined; at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined; at least one must be low for the assigned control input to be considered true.		
0x0102	M0	7	M0 output enable		M0 output/$\overline{\text{input}}$ enable. The M0 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M0 control function		M0 pin function input. These bits determine the control function of the M0 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0103	M1	7	M1 output enable		M1 output/$\overline{\text{input}}$ enable. The M1 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M1 control function		M1 pin function input. These bits determine the control function of the M1 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0104	M2	7	M2 output enable		M2 output/$\overline{\text{input}}$ enable. The M2 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M2 control function		M2 pin function input. These bits determine the control function of the M2 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0105	M3	7	M3 output enable		M3 output/input enable. The M3 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M3 control function		M3 pin function input. These bits determine the control function of the M3 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0106	M4	7	M4 output enable		M4 output/input enable. The M4 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M4 control function		M4 pin function input. These bits determine the control function of the M4 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0107	M5	7	M5 output enable		M5 output/input enable. The M5 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M5 control function		M5 pin function input. These bits determine the control function of the M5 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0108	M6	7	M6 output enable		M6 output/input enable. The M6 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M6 control function		M6 pin function input. These bits determine the control function of the M6 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0109	Pin drive strength	7	SPI configuration		SPI drive strength.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		6	M6 configuration		M6 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		5	M5 configuration		M5 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		4	M4 configuration		M4 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		3	M3 configuration		M3 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		2	M2 configuration		M2 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		1	M1 configuration		M1 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		0	M0 configuration		M0 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x010A	Watchdog timer	[7:0]	Watchdog timer (ms) [7:0]		Watchdog timer. The watchdog timer stops when this register is written and restarts the next time the user writes 1b to the IO_UPDATE bit. Writing all zeros to this register disables the function. The units are in milliseconds.	0x0	R/W
0x010B		[7:0]	Watchdog timer (ms) [15:8]			0x0	R/W

Mx PIN FUNCTION REGISTERS—REGISTER 0x0102 TO REGISTER 0x0108

Table 5. Mx Pin Control Function Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0102 to 0x0108	Mx	Mx output enable	Mx control/status function							0x00	R/W

Table 6. Mx Pin Control Function Register Details

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0102 to 0x0108	Mx	7	Mx output enable		Mx output/$\overline{\text{input}}$. The M0 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	Mx control function		Mx pin function input. These bits determine the control function of the Mx pin. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
				0x00	No function. No destination proxy.		
				0x01	IO_UPDATE. Destination proxy is Register 0x000F, Bit 0.		
				0x02	Full power-down. Destination proxy is Register 0x2000, Bit 0.		
				0x03	Clear watchdog timer. Destination proxy is Register 0x2005, Bit 7.		
				0x04	Sync all distribution dividers. Destination proxy is Register 0x2000, Bit 3.		
				0x10	Clear all interrupt requests (IRQs). Destination proxy is Register 0x2005, Bit 0		
				0x11	Clear common IRQs. Destination proxy is Register 0x2005, Bit 1.		
				0x12	Clear PLL0 IRQs. Destination proxy is Register 0x2005, Bit 2.		
				0x13	Clear PLL1 IRQs. Destination proxy is Register 0x2005, Bit 3.		
				0x20	Force REFA invalid. Destination proxy is Register 0x2003, Bit 0.		
				0x21	Force REFAA invalid. Destination proxy is Register 0x2003, Bit 1.		
				0x22	Force REFB invalid. Destination proxy is Register 0x2003, Bit 2.		
				0x23	Force REFBB invalid. Destination proxy is Register 0x2003, Bit 3.		
				0x28	Force REFA validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 0.		
				0x29	Force REFAA validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 1.		
				0x2A	Force REFB validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 2.		
				0x2B	Force REFBB validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 3.		
				0x40	Power-down Channel 0. Destination proxy is Register 0x2100, Bit 0.		
				0x41	DPLL0 force freerun mode. Destination proxy is Register 0x2105, Bit 0.		
				0x42	DPLL0 force holdover mode. Destination proxy is Register 0x2105, Bit 1.		
				0x43	DPLL0 clear tuning word history. Destination proxy is Register 0x2107, Bit 1.		
				0x44	DPLL0 synchronize dividers. Destination proxy is Register 0x2101, Bit 3.		
				0x45	DPLL0 translation profile select, Bit 0. Destination proxy is Register 0x2105, Bit 4.		
				0x46	DPLL0 translation profile select, Bit 1. Destination proxy is Register 0x2105, Bit 5.		
				0x47	DPLL0 translation profile select, Bit 2. Destination proxy is Register 0x2105, Bit 6.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0x50	Mute OUT0A. Destination proxy is Register 0x2102, Bit 2.		
				0x51	Mute OUT0AA. Destination proxy is Register 0x2102, Bit 3.		
				0x52	Reset OUT0A/OUT0AA. Destination proxy is Register 0x2102, Bit 5.		
				0x53	Mute OUT0B. Destination proxy is Register 0x2103, Bit 2.		
				0x54	Mute OUT0BB. Destination proxy is Register 0x2103, Bit 3.		
				0x55	Reset OUT0B/OUT0BB. Destination proxy is Register 0x2103, Bit 5.		
				0x56	Mute OUT0C. Destination proxy is Register 0x2104, Bit 2.		
				0x57	Mute OUT0CC. Destination proxy is Register 0x2104, Bit 3.		
				0x58	Reset OUT0C/OUT0CC. Destination proxy is Register 0x2104, Bit 5.		
				0x59	Mute all Channel 0 drivers. Destination proxy is Register 0x2101, Bit 1.		
				0x5A	Reset all Channel 0 drivers. Destination proxy is Register 0x2101, Bit 2.		
				0x5B	Channel 0 JESD204B N-shot request. Destination proxy is Register 0x2101, Bit 0.		
				0x60	Power-down Channel 1. Destination proxy is Register 0x2200, Bit 0.		
				0x61	DPLL1 force freerun mode. Destination proxy is Register 0x2205, Bit 0.		
				0x62	DPLL1 force holdover mode. Destination proxy is Register 0x2205, Bit 1.		
				0x63	DPLL1 clear tuning word history. Destination proxy is Register 0x2207, Bit 1.		
				0x64	DPLL1 synchronize dividers. Destination proxy is Register 0x2201, Bit 3.		
				0x65	DPLL1 translation profile select, Bit 0. Destination proxy is Register 0x2205, Bit 4.		
				0x66	DPLL1 translation profile select, Bit 1. Destination proxy is Register 0x2205, Bit 5.		
				0x67	DPLL1 translation profile select, Bit 2. Destination proxy is Register 0x2205, Bit 6.		
				0x70	Mute OUT1A. Destination proxy is Register 0x2202, Bit 2.		
				0x71	Mute OUT1AA. Destination proxy is Register 0x2202, Bit 3.		
				0x72	Reset OUT1A/OUT1AA. Destination proxy is Register 0x2202, Bit 5.		
				0x73	Mute OUT1B. Destination proxy is Register 0x2203, Bit 2.		
				0x74	Mute OUT1BB. Destination proxy is Register 0x2203, Bit 3.		
				0x75	Reset OUT1B/OUT1BB. Destination proxy is Register 0x2203, Bit 5.		
				0x76	Mute all Channel 1 drivers. Destination proxy is Register 0x2201, Bit 1.		
				0x77	Reset all Channel 1 drivers. Destination proxy is Register 0x2201, Bit 2.		
				0x78	Channel 1 JESD204B N-shot request. Destination proxy is Register 0x2201, Bit 0.		

Table 7. Mx Pin Status Register Details

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0102 to 0x0108	Mx	7	Mx output enable		Mx output. The Mx pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	Mx status function		Mx pin status output. These bits determine the status function of the Mx pins. Note that the Mx pin always reads the live status of the selected function, and an IO_UPDATE command is never needed to reflect the latest status. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
				0x00	Static Logic 0. No source proxy.		
				0x01	Static Logic 1. No source proxy.		
				0x02	System clock divided by 96. No Source proxy.		
				0x03	Watchdog timer timeout. The duration of this strobe equals (96/(one system clock period)) when timer expires. No source proxy.		
				0x04	System clock phase-locked loop (PLL) calibration in progress. Source proxy is Register 0x3001, Bit 2.		
				0x05	System clock PLL lock detect. Source proxy is Register 0x3001, Bit 0.		
				0x06	System clock PLL stable. Source proxy is Register 0x3001, Bit 1.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0x07	All PLLs locked. Source proxy is the logical AND of the following bits in Register 0x3001: Bit 5, Bit 4, and Bit 1.		
				0x08	Channel 0 PLLs locked. Source proxy is Register 0x3001, Bit 4.		
				0x09	Channel 1 PLLs locked. Source proxy is Register 0x3001, Bit 5.		
				0x0A	EEPROM upload (write to EEPROM) in progress. Source proxy is Register 0x3000, Bit 0.		
				0x0B	EEPROM download (read from EEPROM) in progress. Source proxy is Register 0x3000, Bit 1.		
				0x0C	EEPROM general fault detected. Source proxy is Register 0x3000, Bit 2.		
				0x0D	Temperature sensor limit alarm. Source proxy is Register 0x3002, Bit 0.		
				0x10	All IRQs. (IRQ common) OR (IRQ PLL0) OR (IRQ PLL1). No source proxy.		
				0x11	Common IRQ. This activates general IRQs not related to one channel or the other (for example, EEPROM fault or temperature sensor alarm). No source proxy.		
				0x12	Channel 0 IRQ. No source proxy.		
				0x13	Channel 1 IRQ. No source proxy.		
				0x1C	REFA R divider resynchronized. Source proxy is Register 0x3000D, Bit 3 (as IRQ).		
				0x1D	REFAA R divider resynchronized. Source proxy is Register 0x3000D, Bit 7 (as IRQ).		
				0x1E	REFB R divider resynchronized. Source proxy is Register 0x3000E, Bit 3 (as IRQ).		
				0x1F	REFBB R divider resynchronized. Source proxy is Register 0x3000E, Bit 7 (as IRQ).		
				0x20	REFA fault. Source proxy is Register 0x3005, Bit 3.		
				0x21	REFAA fault. Source proxy is Register 0x3006, Bit 3.		
				0x22	REFB fault. Source proxy is Register 0x3007, Bit 3.		
				0x23	REFBB fault. Source proxy is Register 0x3008, Bit 3.		
				0x24	REFA valid. Source proxy is Register 0x3005, Bit 4.		
				0x25	REFAA valid. Source proxy is Register 0x3006, Bit 4.		
				0x26	REFB valid. Source proxy is Register 0x3007, Bit 4.		
				0x27	REFBB valid. Source proxy is Register 0x3008, Bit 4.		
				0x28	REFA active. No source proxy.		
				0x29	REFAA active. No source proxy.		
				0x2A	REFB active. No source proxy.		
				0x2B	REFBB active. No source proxy.		
				0x30	DPLL0 phase lock. Source proxy is Register 0x3100, Bit 1.		
				0x31	DPLL0 frequency lock. Source proxy is Register 0x3100, Bit 2.		
				0x32	APLL0 lock. Source proxy is Register 0x3100, Bit 3.		
				0x33	APLL0 calibration busy. Source proxy is Register 0x3100, Bit 4.		
				0x34	DPLL0 actively tracking a reference input. Source proxy is Register 0x3101, Bit 3.		
				0x35	DPLL0 in freerun mode. Source proxy is Register 0x3101, Bit 0.		
				0x36	DPLL0 in holdover mode. Source proxy is Register 0x3101, Bit 1.		
				0x37	DPLL0 reference switch. Source proxy is Register 0x3101, Bit 2.		
				0x38	DPLL0 holdover history available. Source proxy is Register 0x3102, Bit 0.		
				0x39	DPLL0 holdover history update. Source proxy is Register 0x3011, Bit 2.		
				0x3A	DPLL0 frequency clamp is active. Source proxy is Register 0x3102, Bit 1.		
				0x3B	DPLL0 phase slew limiter is active. Source proxy is Register 0x3102, Bit 2.		
				0x3C	Channel 0 output distribution sync event. Source proxy is Register 0x3014, Bit 4.		
				0x3E	DPLL0 phase step detect. Source proxy is Register 0x3011, Bit 0.		
				0x3F	DPLL0 fast acquisition (FACQ) active. Source proxy is Register 0x3102, Bit 4.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0x40	DPLL0 fast acquisition complete. Source proxy is Register 0x3102, Bit 5.		
				0x41	DPLL0 N-divider resync. Source proxy is Register 0x3012, Bit 4.		
				0x42	Channel 0 distribution phase slew in progress. Source proxy is the logical OR of Register 0x310D, Bit 0 through Bit 5.		
				0x43	Channel 0 distribution phase control error. Source proxy is the logical OR of Register 0x310E, Bit 0 through Bit 5.		
				0x50	DPLL1 phase lock. Source proxy is Register 0x3200, Bit 1.		
				0x51	DPLL1 frequency lock. Source proxy is Register 0x3200, Bit 2.		
				0x52	APLL1 lock. Source proxy is Register 0x3200, Bit 3.		
				0x53	APLL1 calibration busy. Source proxy is Register 0x3200, Bit 4.		
				0x54	DPLL1 actively tracking a reference input. Source proxy is Register 0x3201, Bit 3.		
				0x55	DPLL1 in freerun mode. Source proxy is Register 0x3201, Bit 0.		
				0x56	DPLL1 in holdover mode. Source proxy is Register 0x3201, Bit 1.		
				0x57	DPLL1 reference switch. Source proxy is Register 0x3201, Bit 2.		
				0x58	DPLL1 holdover history available. Source proxy is Register 0x3202, Bit 0.		
				0x59	DPLL1 holdover history update. Source proxy is Register 0x3016, Bit 2.		
				0x5A	DPLL1 frequency clamp is active. Source proxy is Register 0x3202, Bit 1.		
				0x5B	DPLL1 phase slew limiter is active. Source proxy is Register 0x3202, Bit 2.		
				0x5C	Channel 1 output distribution sync event. Source proxy is Register 0x3019, Bit 4.		
				0x5E	DPLL1 phase step detect. Source proxy is Register 0x3016, Bit 0.		
				0x5F	DPLL1 fast acquisition active. Source proxy is Register 0x3202, Bit 4.		
				0x60	DPLL1 fast acquisition complete. Source proxy is Register 0x3202, Bit 5.		
				0x61	DPLL1 N-divider resync. Source proxy is Register 0x3017, Bit 4 (as IRQ).		
				0x62	Channel 1 distribution phase slew in progress. Source proxy is the logical OR of Register 0x320D, Bit 3 through Bit 0.		
				0x63	Channel 1 distribution phase control error. Source proxy is the logical OR of Register 0x320E, Bit 3 through Bit 0.		
				0x74	Auxiliary digital phase-locked loop (DPLL) locked. Source proxy is Register 0x3002, Bit 1.		
				0x75	Auxiliary DPLL reference faulted. Source proxy is Register 0x3002, Bit 2.		

IRQ MAP COMMON MASK REGISTERS—REGISTER 0x10C TO REGISTER 0x110

An IRQ may activate immediately after enabling it. Therefore, clear any IRQs immediately after enabling them.

Table 8. IRQ Map Common Mask Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x010C	System clock (SYSCLK)	SYSCLK unlocked	SYSCLK stabilized	SYSCLK locked	SYSCLK calibration deactivated	SYSCLK calibration activated	Watchdog timeout occurred	EEPROM faulted	EEPROM completed	0x00	R/W
0x010D	Auxiliary DPLL	Reserved		Skew limit exceeded	Temperature warning occurred	Auxiliary DPLL unfaulted	Auxiliary DPLL faulted	Auxiliary DPLL unlocked	Auxiliary DPLL locked	0x00	R/W
0x010E	REFA	REFAA R divider resynced	REFAA validated	REFAA unfaulted	REFAA faulted	REFA R divider resynced	REFA validated	REFA unfaulted	REFA faulted	0x00	R/W
0x010F	REFB	REFBB R divider resynced	REFBB validated	REFBB unfaulted	REFBB faulted	REFB R divider resynced	REFB validated	REFB unfaulted	REFB faulted	0x00	R/W

Table 9. IRQ Map Common Mask Registers Details

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x010C	System clock (SYSCLK)	7	SYSCLK unlocked		System clock unlocked. Set this bit to Logic 1 to enable the SYSCLK unlocked IRQ. This IRQ alerts the user when a system clock PLL unlock event occurs.	0x0	R/W
		6	SYSCLK stabilized		System clock stabilized. Set this bit to Logic 1 to enable the SYSCLK stabilized IRQ. This IRQ alerts the user that the system clock PLL is stable.	0x0	R/W
		5	SYSCLK locked		System clock locked. Set this bit to Logic 1 to enable the SYSCLK locked IRQ. This IRQ alerts the user when a system clock PLL unlock event occurs.	0x0	R/W
		4	SYSCLK calibration deactivated		System clock calibration deactivated. Set this bit to Logic 1 to enable the SYSCLK calibration inactive IRQ. This IRQ alerts the user when the system clock calibration is either not running or completes.	0x0	R/W
		3	SYSCLK calibration activated		System clock calibration activated. Set this bit to Logic 1 to enable the SYSCLK calibration started IRQ. This IRQ alerts the user that the system clock calibration is in progress.	0x0	R/W
		2	Watchdog timeout occurred		Watchdog timeout occurred. Set this bit to Logic 1 to enable the watchdog timer timeout IRQ.	0x0	R/W
		1	EEPROM faulted		EEPROM faulted. Set this bit to Logic 1 to enable the EEPROM faulted IRQ.	0x0	R/W
		0	EEPROM completed		EEPROM operation completed. Set this bit to Logic 1 to enable the EEPROM operation completed IRQ.	0x0	R/W
0x10D	Auxiliary DPLL	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew limit exceeded		Skew limit exceeded. Set this bit to Logic 1 to enable the reference input skew measurement limit exceeded IRQ.	0x0	R/W
		4	Temperature warning occurred		Temperature range warning. Set to Logic 1 to enable the temperature warning IRQ. This IRQ alerts the user when the temperature sensor is out of range. This IRQ activates, if enabled, and the temperature limits are configured before the system clock locks.	0x0	R/W
		3	Auxiliary DPLL unfaulted		Closed-loop SYSCLK compensation DPLL unfaulted. Set this bit to Logic 1 to enable the auxiliary DPLL unfaulted IRQ.	0x0	R/W
		2	Auxiliary DPLL faulted		Closed-loop SYSCLK compensation DPLL faulted. Set this bit to Logic 1 to enable the auxiliary DPLL faulted IRQ.	0x0	R/W
		1	Auxiliary DPLL unlocked		Closed-loop SYSCLK compensation DPLL unlocked. Set this bit to Logic 1 to enable the auxiliary DPLL unlocked IRQ.	0x0	R/W
		0	Auxiliary DPLL locked		Closed-loop SYSCLK compensation DPLL locked. Set this bit to Logic 1 to enable the auxiliary DPLL locked IRQ.	0x0	R/W
0x010E	REFA	7	REFAA R divider resynced		REFAA R divider resynced. Set this bit to Logic 1 to enable the REFAA R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		6	REFAA validated		REFAA validated. Set this bit to Logic 1 to enable the REFAA validated IRQ.	0x0	R/W
		5	REFAA unfaulted		REFAA unfaulted. Set this bit to Logic 1 to enable the REFAA unfaulted IRQ.	0x0	R/W
		4	REFAA faulted		REFAA faulted. Set this bit to Logic 1 to enable the REFAA faulted IRQ.	0x0	R/W
		3	REFA R divider resynced		REFA R divider resynced. Set this bit to Logic 1 to enable the REFA R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		2	REFA validated		REFA validated. Set this bit to Logic 1 to enable the REFA validated IRQ.	0x0	R/W
		1	REFA unfaulted		REFA unfaulted. Set this bit to Logic 1 to enable the REFA unfaulted IRQ.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	REFA faulted		REFA faulted. Set to Logic 1 to enable the REFA faulted IRQ.	0x0	R/W
0x010F	REFB	7	REFBB R divider resynced		REFBB R divider resynced. Set this bit to Logic 1 to enable the REFBB R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		6	REFBB validated		REFBB validated. Set this bit to Logic 1 to enable the REFBB validated IRQ.	0x0	R/W
		5	REFBB unfaulted		REFBB unfaulted. Set this bit to Logic 1 to enable the REFBB unfaulted IRQ.	0x0	R/W
		4	REFBB faulted		REFBB faulted. Set this bit to Logic 1 to enable the REFBB faulted IRQ.	0x0	R/W
		3	REFB R divider resynced		REFB R divider resynced. Set this bit to Logic 1 to enable the REFB R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		2	REFB validated		REFB validated. Set this bit to Logic 1 to enable the REFB validated IRQ.	0x0	R/W
		1	REFB unfaulted		REFB unfaulted. Set this bit to Logic 1 to enable the REFB unfaulted IRQ.	0x0	R/W
		0	REFB faulted		REFB faulted. Set this bit to Logic 1 to enable the REFB faulted IRQ.	0x0	R/W

IRQ MAP DPLL0 MASK REGISTERS—REGISTER 0x0111 TO REGISTER 0x0115

An IRQ may activate immediately after enabling it. Therefore, clear any IRQs immediately after enabling them.

Table 10. IRQ Map DPLL0 Mask Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0111	Lock	DPLL0 frequency clamp deactivated	DPLL0 frequency clamp activated	DPLL0 phase slew limiter deactivated	DPLL0 phase slew limiter activated	DPLL0 frequency unlocked	DPLL0 frequency locked	DPLL0 phase unlocked	DPLL0 phase locked	0x00	R/W
0x0112	State	DPLL0 reference switched	DPLL0 freerun entered	DPLL0 holdover entered	DPLL0 hitless entered	DPLL0 hitless exited	DPLL0 history updated	Reserved	DPLL0 phase step detected	0x00	R/W
0x0113	Fast acquisition	Reserved			DPLL0 N-divider resynced	DPLL0 fast acquisition completed	DPLL0 fast acquisition started	Reserved		0x00	R/W
0x0114	Active profile	Reserved		DPLL0 Profile 5 activated	DPLL0 Profile 4 activated	DPLL0 Profile 3 activated	DPLL0 Profile 2 activated	DPLL0 Profile 1 activated	DPLL0 Profile 0 activated	0x00	R/W
0x0115	APLL	Reserved			DPLL0 distribution synced	APLL0 unlocked	APLL0 locked	APLL0 calibration completed	APLL0 calibration started	0x00	R/W

Table 11. IRQ Map DPLL0 Mask Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0111	Lock	7	DPLL0 frequency clamp deactivated		Frequency clamp deactivated. Set this bit to Logic 1 to enable the IRQ for DPLL0 frequency clamp inactive.	0x0	R/W
		6	DPLL0 frequency clamp activated		Frequency clamp activated. Set this bit to Logic 1 to enable the IRQ for DPLL0 frequency clamp active.	0x0	R/W
		5	DPLL0 phase slew limiter deactivated		Phase slew limiter deactivated. Set this bit to Logic 1 to enable the IRQ for DPLL0 phase slew limiter deactivated.	0x0	R/W
		4	DPLL0 phase slew limiter activated		Phase slew limiter activated. Set this bit to Logic 1 to enable the IRQ for DPLL0 phase slew limiter activated.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	DPLL0 frequency unlocked		Frequency unlocked. Set this bit to Logic 1 to enable the IRQ for DPLL0 frequency unlock detect (lock to unlock transition).	0x0	R/W
		2	DPLL0 frequency locked		Frequency locked. Set this bit to Logic 1 to enable the IRQ for DPLL0 frequency lock detect (unlock to lock transition).	0x0	R/W
		1	DPLL0 phase unlocked		Phase unlocked. Set this bit to Logic 1 to enable the IRQ for DPLL0 phase unlock detect (lock to unlock transition).	0x0	R/W
		0	DPLL0 phase locked		Phase locked. Set this bit to Logic 1 to enable the IRQ for DPLL0 phase lock detect (unlock to lock transition).	0x0	R/W
0x0112	State	7	DPLL0 reference switched		Reference switched. Set this bit to Logic 1 to enable the IRQ for DPLL0 reference input switched.	0x0	R/W
		6	DPLL0 freerun entered		Freerun mode entered. Set this bit to Logic 1 to enable the IRQ for DPLL0 freerun mode entered.	0x0	R/W
		5	DPLL0 holdover entered		Holdover mode entered. Set this bit to Logic 1 to enable the IRQ for DPLL0 holdover mode entered.	0x0	R/W
		4	DPLL0 hitless entered		Hitless mode entered. Set this bit to Logic 1 to enable the IRQ for DPLL0 hitless mode entered.	0x0	R/W
		3	DPLL0 hitless exited		Hitless mode exited. Set this bit to Logic 1 to enable the IRQ for DPLL0 hitless mode exited.	0x0	R/W
		2	DPLL0 history updated		Holdover history updated. Set this bit to Logic 1 to enable the IRQ for DPLL0 tuning word holdover history updated.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DPLL0 phase step detected		Phase step detected. Set this bit to Logic 1 to enable the IRQ for DPLL0 reference input phase step detected.	0x0	R/W
0x0113	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 N-divider resynced		N-divider resynchronized. Set this bit to Logic 1 to enable the IRQ for DPLL0 N-divider resynced.	0x0	R/W
		3	DPLL0 fast acquisition completed		Fast acquisition complete. Set this bit to Logic 1 to enable the IRQ for DPLL0 fast acquisition complete.	0x0	R/W
		2	DPLL0 fast acquisition started		Fast acquisition started. Set this bit to Logic 1 to enable the IRQ for DPLL0 fast acquisition started.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R/W
0x0114	Active profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 Profile 5 activated		Profile 5 active. Set this bit to Logic 1 to enable the IRQ for DPLL0 Profile 5 activated.	0x0	R/W
		4	DPLL0 Profile 4 activated		Profile 4 active. Set this bit to Logic 1 to enable the IRQ for DPLL0 Profile 4 activated.	0x0	R/W
		3	DPLL0 Profile 3 activated		Profile 3 active. Set this bit to Logic 1 to enable the IRQ for DPLL0 Profile 3 activated.	0x0	R/W
		2	DPLL0 Profile 2 activated		Profile 2 active. Set this bit to Logic 1 to enable the IRQ for DPLL0 Profile 2 activated.	0x0	R/W
		1	DPLL0 Profile 1 activated		Profile 1 active. Set this bit to Logic 1 to enable the IRQ for DPLL0 Profile 1 activated.	0x0	R/W
		0	DPLL0 Profile 0 activated		Profile 0 active. Set this bit to Logic 1 to enable the IRQ for DPLL0 Profile 0 activated.	0x0	R/W
0x0115	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 distribution synced		Clock distribution synced. Set this bit to Logic 1 to enable the IRQ for DPLL0 clock distribution synced.	0x0	R/W
		3	APLL0 unlocked		Unlock detect. Set this bit to Logic 1 to enable the IRQ for APLL0 unlock detect (lock to unlock transition).	0x0	R/W
		2	APLL0 locked		Lock detect. Set this bit to Logic 1 to enable the IRQ for APLL0 lock detect (unlock to lock transition).	0x0	R/W
		1	APLL0 calibration completed		Calibration complete. Set this bit to Logic 1 to enable the IRQ for APLL0 calibration complete.	0x0	R/W
		0	APLL0 calibration started		Calibration start. Set this bit to Logic 1 to enable the IRQ for APLL0 calibration start.	0x0	R/W

IRQ MAP DPLL1 MASK REGISTERS—REGISTER 0x116 TO REGISTER 0x11A

An IRQ may activate immediately after enabling it. Therefore, clear any IRQs immediately after enabling them.

Table 12. IRQ Map DPLL1 Mask Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0116	Lock	DPLL1 frequency clamp deactivated	DPLL1 frequency clamp activated	DPLL1 phase slew limiter deac-tivated	DPLL1 phase slew limiter activated	DPLL1 frequency unlocked	DPLL1 frequency locked	DPLL1 phase unlocked	DPLL1 phase locked	0x00	R/W
0x0117	State	DPLL1 reference switched	DPLL1 freerun entered	DPLL1 holdover entered	DPLL1 hitless entered	DPLL1 hitless exited	DPLL1 history updated	Reserved	DPLL1 phase step detected	0x00	R/W
0x0118	Fast acquisition	Reserved			DPLL1 N-divider resynced	DPLL1 fast acquisition completed	DPLL1 fast acquisition started	Reserved		0x00	R/W
0x0119	Active profile	Reserved		DPLL1 Profile 5 activated	DPLL1 Profile 4 activated	DPLL1 Profile 3 activated	DPLL1 Profile 2 activated	DPLL1 Profile 1 activated	DPLL1 Profile 0 activated	0x00	R/W
0x011A	APLL	Reserved			DPLL1 distribution synced	APLL1 unlocked	APLL1 locked	APLL1 calibration completed	APLL1 calibration started	0x00	R/W

Table 13. IRQ_MAP_DPLL_1_MASK Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0116	Lock	7	DPLL1 frequency clamp deactivated		Frequency clamp deactivated. Set this bit to Logic 1 to enable the IRQ for DPLL1 frequency clamp inactive.	0x0	R/W
		6	DPLL1 frequency clamp activated		Frequency clamp activated. Set this bit to Logic 1 to enable the IRQ for DPLL1 frequency clamp active.	0x0	R/W
		5	DPLL1 phase slew limiter deactivated		Phase slew limiter deactivated. Set this bit to Logic 1 to enable the IRQ for DPLL1 phase slew limiter deactivated.	0x0	R/W
		4	DPLL1 phase slew limiter activated		Phase slew limiter activated. Set this bit to Logic 1 to enable the IRQ for DPLL1 phase slew limiter activated.	0x0	R/W
		3	DPLL1 frequency unlocked		Frequency unlocked. Set this bit to Logic 1 to enable the IRQ for DPLL1 frequency unlock detect (lock to unlock transition).	0x0	R/W
		2	DPLL1 frequency locked		Frequency locked. Set this bit to Logic 1 to enable the IRQ for DPLL1 frequency lock detect (unlock to lock transition).	0x0	R/W
		1	DPLL1 phase unlocked		Phase unlocked. Set this bit to Logic 1 to enable the IRQ for DPLL1 phase unlock detect (lock to unlock transition).	0x0	R/W
		0	DPLL1 phase locked		Phase locked. Set this bit to Logic 1 to enable the IRQ for DPLL1 phase lock detect (unlock to lock transition).	0x0	R/W
0x0117	State	7	DPLL1 reference switched		Reference switched. Set this bit to Logic 1 to enable the IRQ for DPLL1 reference input switched.	0x0	R/W
		6	DPLL1 freerun entered		Freerun mode entered. Set this bit to Logic 1 to enable the IRQ for DPLL1 freerun mode entered.	0x0	R/W
		5	DPLL1 holdover entered		Holdover mode entered. Set this bit to Logic 1 to enable the IRQ for DPLL1 holdover mode entered.	0x0	R/W
		4	DPLL1 hitless entered		Hitless mode entered. Set this bit to Logic 1 to enable the IRQ for DPLL1 hitless mode entered.	0x0	R/W
		3	DPLL1 hitless exited		Hitless mode exited. Set this bit to Logic 1 to enable the IRQ for DPLL1 hitless mode exited.	0x0	R/W
		2	DPLL1 history updated		Holdover history updated. Set this bit to Logic 1 to enable the IRQ for DPLL1 tuning word holdover history updated.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DPLL1 phase step detected		Phase step detected. Set this bit to Logic 1 to enable the IRQ for DPLL1 reference input phase step detected.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0118	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 N-divider resynced		N-divider resynchronized. Set this bit to Logic 1 to enable the IRQ for DPLL1 N-divider resynced.	0x0	R/W
		3	DPLL1 fast acquisition completed		Fast acquisition complete. Set to Logic 1 to enable the IRQ for DPLL1 fast acquisition complete.	0x0	R/W
		2	DPLL1 fast acquisition started		Fast acquisition started. Set to Logic 1 to enable the IRQ for DPLL1 fast acquisition started.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R/W
0x0119	Active profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 Profile 5 activated		Profile 5 active. Set this bit to Logic 1 to enable the IRQ for DPLL1 Profile 5 activated.	0x0	R/W
		4	DPLL1 Profile 4 activated		Profile 4 active. Set this bit to Logic 1 to enable the IRQ for DPLL1 Profile 4 activated.	0x0	R/W
		3	DPLL1 Profile 3 activated		Profile 3 active. Set this bit to Logic 1 to enable the IRQ for DPLL1 Profile 3 activated.	0x0	R/W
		2	DPLL1 Profile 2 activated		Profile 2 active. Set this bit to Logic 1 to enable the IRQ for DPLL1 Profile 2 activated.	0x0	R/W
		1	DPLL1 Profile 1 activated		Profile 1 active. Set this bit to Logic 1 to enable the IRQ for DPLL1 Profile 1 activated.	0x0	R/W
		0	DPLL1 Profile 0 activated		Profile 0 active. Set this bit to Logic 1 to enable the IRQ for DPLL1 Profile 0 activated.	0x0	R/W
0x011A	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 distribution synced		Clock distribution synced. Set to Logic 1 to enable the IRQ for DPLL1 clock distribution synced.	0x0	R/W
		3	APLL1 unlocked		Unlock detect. Set to Logic 1 to enable the IRQ for APLL1 unlock detect (lock to unlock transition).	0x0	R/W
		2	APLL1 locked		Lock detect. Set to Logic 1 to enable the IRQ for APLL1 lock detect (unlock to lock transition).	0x0	R/W
		1	APLL1 calibration completed		Calibration complete. Set to Logic 1 to enable the IRQ for APLL1 calibration complete.	0x0	R/W
		0	APLL1 calibration started		Calibration start. Set to Logic 1 to enable the IRQ for APLL1 calibration start.	0x0	R/W

SYSTEM CLOCK (SYSCLK) REGISTERS—REGISTER 0x0200 TO REGISTER 0x0209

Table 14. System Clock Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0200	Feedback divider ratio	Feedback divider ratio								0x00	R/W
0x0201	Input	Reserved				Enable maintaining amplifier	SYSCLK input divider ratio		Enable SYSCLK doubler	0x00	R/W
0x0202	Reference frequency	SYSCLK reference frequency [7:0]								0x00	R/W
0x0203		SYSCLK reference frequency [15:8]								0x00	R/W
0x0204		SYSCLK reference frequency [23:16]								0x00	R/W
0x0205		SYSCLK reference frequency [31:24]								0x00	R/W
0x0206		SYSCLK reference frequency [39:32]								0x00	R/W
0x0207	Stability timer	System clock stability period [7:0]								0x00	R/W
0x0208		System clock stability period [15:8]								0x00	R/W
0x0209		Reserved				System clock stability period [19:16]				0x00	R/W

Table 15. System Clock Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0200	Feedback divider ratio	[7:0]	Feedback divider ratio		SYSCLK PLL feedback divide ratio. This bit field is the SYSCLK PLL multiplication ratio.	0x0	R/W
0x0201	Input	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable maintaining amplifier		Enable SYSCLK maintaining amplifier. Logic 0: crystal maintaining amplifier disabled. Use this setting when not using a crystal as the system clock input. Logic 1: crystal maintaining amplifier enabled. Use this setting when using a crystal as the system clock input.	0x0	R/W
		[2:1]	SYSCLK input divider ratio		SYSCLK prescaler ratio. This bit field controls the system clock input divider.	0x0	R/W
				0	Prescaler bypassed.		
				1	Divide by 2. System clock input frequency is divided by 2.		
				2	Divide by 4. System clock input frequency is divided by 4.		
				3	Divide by 8. System clock input frequency is divided by 2.		
		0	Enable SYSCLK doubler		Enable SYSCLK doubler. The system clock doubler decreases the noise contribution of the system clock PLL. However, refer to the AD9542 data sheet for the input doubler duty cycle requirements to use the doubler. Logic 0: system clock doubler disabled. Logic 1: system clock doubler enabled.	0x0	R/W
0x0202	Reference frequency	[7:0]	SYSCLK reference frequency [7:0]		SYSCLK reference frequency. This 40-bit unsigned integer bit field contains the system clock reference frequency in units of millihertz. For example, the bit field setting for a 49.152 MHz crystal is 49,152,000,000 decimal (0x0B71B00000).	0x0	R/W
0x0203		[7:0]	SYSCLK reference frequency [15:8]			0x0	R/W
0x0204		[7:0]	SYSCLK reference frequency [23:16]			0x0	R/W
0x0205		[7:0]	SYSCLK reference frequency [31:24]			0x0	R/W
0x0206		[7:0]	SYSCLK reference frequency [39:32]			0x0	R/W
0x0207	Stability timer	[7:0]	System clock stability period [7:0]		SYSCLK stability period. This 20-bit unsigned integer bit field is the amount of time that the system clock PLL must be locked before the SYSCLK stable bit is Logic 1. This time is in units of milliseconds. For example, for a system clock stability period of 50 ms, the value in this bit field is 50 decimal (0x32).	0x0	R/W
0x0208		[7:0]	System clock stability period [15:8]			0x0	R/W
0x0209		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	System clock stability period [19:16]		SYSCLK stability period. This 20-bit unsigned integer bit field is the amount of time that the system clock PLL must be locked before the SYSCLK stable bit is Logic 1. This time is in units of milliseconds. For example, for a system clock stability period of 50 ms, the value in this bit field is 50 decimal (0x32).	0x0	R/W

SYSCLK COMPENSATION REGISTERS—REGISTER 0x0280 TO REGISTER 0x029C

Table 16. SYSCLK Compensation Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0280	Auxiliary DPLL and reference time to digital converter (TDC) compensation source	Reserved		Compensate auxiliary DPLL via DPLLx	Compensate auxiliary DPLL via coefficients	Reserved	Compensate TDCs via auxiliary DPLL	Compensate TDCs via DPLLx	Compensate TDCs via coefficients	0x00	R/W
0x0282	DPLL compensation source	Reserved	Compensate DPLL1 via auxiliary DPLL	Compensate DPLL1 via DPLLx	Compensate DPLL1 via coefficients	Reserved	Compensate DPLL0 via auxiliary DPLL	Compensate DPLL0 via DPLLx	Compensate DPLL0 via coefficients	0x00	R/W
0x0283	Rate change limit	Reserved					Slew rate limit			0x00	R/W
0x0284	Closed-loop source	Reserved						Auxiliary DPLL source		0x00	R/W
0x0285	Auxiliary DPLL bandwidth	Auxiliary DPLL bandwidth [7:0]								0x00	R/W
0x0286		Auxiliary DPLL bandwidth [15:8]								0x00	R/W
0x0287	Error source	Reserved							DPLL channel error source	0x00	R/W
0x0288	Open-loop cutoff	Reserved					Coefficient output filter cutoff			0x00	R/W
0x0289	SYSCLK compensation polynomial	Constant compensation value [7:0]								0x00	R/W
0x028A		Constant compensation value [15:8]								0x00	R/W
0x028B		Constant compensation value [23:16]								0x00	R/W
0x028C		Constant compensation value [31:24]								0x00	R/W
0x028D		Constant compensation value [39:32]								0x00	R/W
0x028E		T^1 significand [7:0]								0x00	R/W
0x028F		T^1 significand [15:8]								0x00	R/W
0x0290		T^1 exponent								0x00	R/W
0x0291		T^2 significand [7:0]								0x00	R/W
0x0292		T^2 significand [15:8]								0x00	R/W
0x0293		T^2 exponent								0x00	R/W
0x0294		T^3 significand [7:0]								0x00	R/W
0x0295		T^3 significand [15:8]								0x00	R/W
0x0296		T^3 exponent								0x00	R/W
0x0297		T^4 significand [7:0]								0x00	R/W
0x0298		T^4 significand [15:8]								0x00	R/W
0x0299		T^4 exponent								0x00	R/W
0x029A		T^5 significand [7:0]								0x00	R/W
0x029B		T^5 significand [15:8]								0x00	R/W
0x029C		T^5 exponent								0x00	R/W

Table 17. SYSCLK Compensation Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0280	Auxiliary DPLL and reference TDC compensation source	[7:6]	Reserved		Reserved.	0x0	R
		5	Compensate auxiliary DPLL via DPLLx		Use DPLLx as the source to compensate the auxiliary DPLL. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to the auxiliary DPLL. DPLL0 is chosen if the channel error source bit is Logic 0, and DPLL1 is chosen if this bit is Logic 1. This mode is useful if one of the DPLLs is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		4	Compensate auxiliary DPLL via coefficients		Use temperature compensation polynomial for the auxiliary DPLL. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for the auxiliary DPLL. This mode is useful if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/ W
		3	Reserved		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	Compensate TDCs via auxiliary DPLL		Use the auxiliary DPLL as the source to compensate TDCs. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to the time to digital converters, including both the reference TDCs. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source. This bit must be set for the auxiliary DPLL frequency corrections to go to the DPLL reference input frequency monitoring logic.	0x0	R/W
		1	Compensate TDCs via DPLLx		Use DPLLx as the source to compensate TDCs. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to the time to digital converters, including the reference TDCs. DPLL0 is chosen if the channel error source bit is Logic 0, and DPLL1 is chosen if this bit is Logic 1. This mode is useful if one of the DPLLs is locked to a reference input with a frequency considered more accurate than the system clock source, and this bit must be set for the frequency corrections to go to the DPLL reference input frequency monitoring logic.	0x0	R/W
		0	Compensate TDCs via coefficients		Use temperature compensation polynomial for TDCs. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for TDCs, including the reference TDCs. This mode is useful if applying a known frequency vs. temperature characteristic to the TDCs that can be fit to a fifth-order polynomial, and this bit must be set for the frequency corrections to go to the DPLL reference input frequency monitoring logic.	0x0	R/W
0x0282	DPLL compensation source	7	Reserved		Reserved.	0x0	R
		6	Compensate DPLL1 via auxiliary DPLL		Use auxiliary DPLL as the source to compensate DPLL1. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to DPLL1. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		5	Compensate DPLL1 via DPLLx		Use DPLLx as the source to compensate DPLL1. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to DPLL1. The channel error source bit must be set to Logic 0 so that DPLL0 is chosen to compensate DPLL1. This mode is useful if DPLL0 is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		4	Compensate DPLL1 via coefficients		Use temperature compensation polynomial for DPLL1. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for DPLL0. This mode is useful if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	Compensate DPLL0 via auxiliary DPLL		Use auxiliary DPLL as the source to compensate DPLL0. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to DPLL0. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		1	Compensate DPLL0 via DPLLx		Use DPLLx as the source to compensate DPLL0. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to DPLL0. The channel error source bit must be set to Logic 1 so that DPLL1 is chosen to compensate DPLL0. This mode is useful if DPLL1 is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Compensate DPLL0 via coefficients		Use temperature compensation polynomial for DPLL0. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for DPLL0. This mode is useful if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/W
0x0283	Rate change limit	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Slew rate limit		Error compensation rate change limiting. This 3-bit bit field controls the system clock compensation rate change limiting. It prevents the system clock compensation block from introducing system clock frequency changes that can cause system instabilities.	0x0	R/W
				000	None.		
				001	0.715 ppm/sec.		
				010	1.43 ppm/sec.		
				011	2.86 ppm/sec.		
				100	5.72 ppm/sec.		
				101	11.44 ppm/sec.		
				110	22.88 ppm/sec.		
				111	45.76 ppm/sec.		
0x0284	Closed-loop source	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Auxiliary DPLL source		Auxiliary DPLL closed-loop source. This 2-bit bit field selects the source of the auxiliary DPLL when using auxiliary DPLL compensation. For example, if the clock input connected to REFA is considered to have the best frequency accuracy in the system, select REFA in this bit field.	0x0	R/W
				0	REFA.		
				1	REFAA.		
				2	REFB.		
				3	REFBB.		
0x0285	Auxiliary DPLL bandwidth	[7:0]	Auxiliary DPLL bandwidth [7:0]		Auxiliary DPLL bandwidth. This 16-bit bit field is the loop bandwidth of the auxiliary DPLL that tracks the system clock frequency error and provides a correction to the AD9542 digital logic. It is in units of 0.1 Hz (1 dHz). For example, to set a loop bandwidth of 247.6 Hz, enter 2476 decimal (0x09AC) into this bit field.	0x0	R/W
0x0286		[7:0]	Auxiliary DPLL bandwidth [15:8]			0x0	R/W
0x0287	Error source	[7:1]	Reserved		Reserved.	0x0	R
		0	DPLL channel error source		Compensation error source for DPLL Channel x. This bit allows the user to select which DPLL to use as the reference for correcting the system clock frequency error while using DPLL channel compensation.	0x0	R/W
				0	DPLL0. Selects DPLL0 as the source of system clock compensation error signal.		
				1	DPLL1. Selects DPLL1 as the source of system clock compensation error signal.		
0x0288	Open-loop cutoff	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Coefficient output filter cutoff		Open-loop compensation filter cutoff frequency. This 3-bit bit field controls the open-loop compensation low-pass filter cutoff frequency.	0x0	R/W
				000	400 Hz (maximum).		
				001	200 Hz.		
				010	100 Hz.		
				011	50 Hz.		
				100	25 Hz.		
				101	12 Hz.		
				110	6 Hz.		
				111	3 Hz (minimum).		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0289	SYSCLK compensation polynomial	[7:0]	Constant compensation value [7:0]		Constant compensation value. This 40-bit bit field is the T^0 temperature compensation coefficient used in the open-loop direct compensation method. This bit field applies a fixed correction to the oscillator frequency and is useful for compensating for oscillator aging. Contact Analog Devices for more information.	0x0	R/W
0x028A		[7:0]	Constant compensation value [15:8]			0x0	R/W
0x028B		[7:0]	Constant compensation value [23:16]			0x0	R/W
0x028C		[7:0]	Constant compensation value [31:24]			0x0	R/W
0x028D		[7:0]	Constant compensation value [39:32]			0x0	R/W
0x028E		[7:0]	T^1 significand [7:0]		T^1 coefficient significand. This bit field is the significand portion of the T^1 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x028F		[7:0]	T^1 significand [15:8]			0x0	R/W
0x0290		[7:0]	T^1 exponent		T^1 coefficient exponent. This bit field is the exponent portion of the T^1 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x0291		[7:0]	T^2 significand [7:0]		T^2 coefficient significand. This bit field is the significand portion of the T^2 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x0292		[7:0]	T^2 significand [15:8]			0x0	R/W
0x0293		[7:0]	T^2 exponent		T^2 coefficient exponent. This bit field is the exponent portion of the T^2 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x0294		[7:0]	T^3 significand [7:0]		T^3 coefficient significand. This bit field is the significand portion of the T^3 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x0295		[7:0]	T^3 significand [15:8]			0x0	R/W
0x0296		[7:0]	T^3 exponent		T^3 coefficient exponent. This bit field is the exponent portion of the T^3 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x0297		[7:0]	T^4 significand [7:0]		T^4 coefficient significand. This bit field is the significand portion of the T^4 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x0298		[7:0]	T^4 significand [15:8]			0x0	R/W
0x0299		[7:0]	T^4 exponent		T^4 coefficient exponent. This bit field is the exponent portion of the T^4 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x029A		[7:0]	T^5 significand [7:0]		T^5 coefficient significand. This bit field is the significand portion of the T^5 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W
0x029B		[7:0]	T^5 significand [15:8]			0x0	R/W
0x029C	SYSCLK compensation polynomial	[7:0]	T^5 exponent		T^5 coefficient exponent. This bit field is the exponent portion of the T^5 temperature compensation coefficient used in the open-loop direct compensation method. Contact Analog Devices for more information.	0x0	R/W

REFERENCE GENERAL A REGISTER—REGISTER 0x0300

Table 18. Reference General A Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0300	Receiver settings	REFAA single-ended mode		REFA single-ended mode		REFA differential mode		Reserved	REFA input mode	0x00	R/W

Table 19. Reference General A Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0300	Receiver settings	[7:6]	REFAA single-ended mode		REFAA single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V, CMOS, single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		
		[5:4]	REFA single-ended mode		REFA single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V CMOS single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		
		[3:2]	REFA differential mode		REFA differential mode.	0x0	R/W
				0	Self biased ac-coupled. Use this mode for ac-coupled differential clocks. The self generated dc bias voltage is approximately 0.6 V, and the minimum input frequency depends on the size of the decoupling capacitors.		
				1	DC-coupled differential mode. Use this mode for dc-coupled differential clocks with common-mode voltages of approximately 0.6 V. There is no internally generated dc bias voltage in this mode. See the AD9542 data sheet for the actual limits.		
				10	DC-coupled low voltage differential signaling (LVDS) mode. Use this mode for dc-coupled LVDS clocks <450 MHz. The expected dc bias level is approximately 1.2 V. See the AD9542 data sheet for the actual limits, and in cases of a discrepancy, use the specification in the data sheet.		
		1	Reserved		Reserved.	0x0	R
		0	REFA input mode		REFA input mode.	0x0	R/W
				0	The REFA and REFAA input pins are single-ended inputs.		
				1	The REFA and REFAA input pins form a differential pair.		

REFERENCE GENERAL B REGISTER—REGISTER 0x0304

Table 20. Reference General B Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0304	Receiver settings	REFBB single-ended mode		REFB single-ended mode		REFB differential mode		Reserved	REFB input mode	0x00	R/W

Table 21. Reference General B Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0304	Receiver settings	[7:6]	REFBB single-ended mode		REFBB single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V, CMOS, single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		
		[5:4]	REFB single-ended mode		REFB single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V CMOS single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		
		[3:2]	REFB differential mode		REFB differential mode.	0x0	R/W
				0	Self biased, ac-coupled. Use this mode for ac-coupled differential clocks. The self generated dc bias voltage is approximately 0.6 V, and the minimum input frequency depends on the size of the decoupling capacitors.		
				1	DC-coupled differential mode. Use this mode for dc-coupled differential clocks with common-mode voltages of approximately 0.6 V. There is no internally generated dc bias voltage in this mode. See the AD9542 data sheet for the actual limits.		
				10	DC-coupled LVDS mode. Use this mode for dc-coupled LVDS clocks <450 MHz. The expected dc bias level is approximately 1.2 V. See the AD9542 data sheet for the actual limits, and in cases of a discrepancy, use the specification in the data sheet.		
		1	Reserved		Reserved.	0x0	R
		0	REFB input mode		REFB input mode.	0x0	R/W
				0	The REFB and REFBB input pins are single-ended inputs.		
				1	The REFB and REFBB input pins form a differential pair.		

REFERENCE INPUT A (REFA) REGISTERS—REGISTER 0x0400 TO REGISTER 0x0414

Table 22. Reference Input A Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0400	R divider	REFA R divide ratio [7:0]								0x00	R/W
0x0401		REFA R divide ratio [15:8]								0x00	R/W
0x0402		REFA R divide ratio [23:16]								0x00	R/W
0x0403		Reserved		REFA R divide ratio [29:24]						0x00	R/W
0x0404	Input period	REFA nominal period [7:0]								0x00	R/W
0x0405		REFA nominal period [15:8]								0x00	R/W
0x0406		REFA nominal period [23:16]								0x00	R/W
0x0407		REFA nominal period [31:24]								0x00	R/W
0x0408		REFA nominal period [39:32]								0x00	R/W
0x0409		REFA nominal period [47:40]								0x00	R/W
0x040A		Reserved							REFA nominal period [48]	0x00	R/W
0x040B		Reserved								0x00	R/W
0x040C	Offset limit	REFA offset limit [7:0]								0xA0	R/W
0x040D		REFA offset limit [15:8]								0x86	R/W
0x040E		REFA offset limit [23:16]								0x01	R/W
0x040F	Monitor hysteresis	Reserved					REFA monitor hysteresis			0x03	R/W
0x0410	Validation timer	REFA validation timer [7:0]								0x0A	R/W
0x0411		REFA validation timer [15:8]								0x00	R/W
0x0412		Reserved				REFA validation timer [19:16]				0x00	R/W
0x0413	Jitter tolerance	REFA jitter tolerance [7:0]								0x00	R/W
0x0414		REFA jitter tolerance [15:8]								0x00	R/W

Table 23. Reference Input A Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0400	R divider	[7:0]	REFA R divide ratio [7:0]		REFA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0401		[7:0]	REFA R divide ratio [15:8]		REFA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0402		[7:0]	REFA R divide ratio [23:16]		REFA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0403		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFA R divide ratio [29:24]		REFA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0404	Input period	[7:0]	REFA nominal period [7:0]		REFA nominal period. This bit field is called T_{REF} in the evaluation software and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0405		[7:0]	REFA nominal period [15:8]			0x0	R/W
0x0406		[7:0]	REFA nominal period [23:16]			0x0	R/W
0x0407		[7:0]	REFA nominal period [31:24]			0x0	R/W
0x0408		[7:0]	REFA nominal period [39:32]			0x0	R/W
0x0409		[7:0]	REFA nominal period [47:40]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x040A		[7:1]	Reserved		Reserved.	0x0	R
		0	REFA nominal period [48]		REFA nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x040B	Reserved	[7:0]	Reserved		Reserved.	0x0	R
0x040C	Offset limit	[7:0]	REFA offset limit [7:0]		REFA offset limit. This bit field is called ΔT_{REF} in the evaluation software. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x040D		[7:0]	REFA offset limit [15:8]			0x86	R/W
0x040E		[7:0]	REFA offset limit [23:16]			0x1	R/W
0x040F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFA monitor hysteresis		REFA monitor hysteresis. This bit field is called T_{HYS} in the evaluation software and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of ΔT_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of ΔT_{REF}.		
				2	6.25% of ΔT_{REF}.		
				3	12.5% of ΔT_{REF}.		
				4	25% of ΔT_{REF}.		
				5	50% of ΔT_{REF}.		
				6	75% of ΔT_{REF}.		
				7	87.5% of ΔT_{REF}.		
0x0410	Validation timer	[7:0]	REFA validation timer [7:0]		REFA validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x0411		[7:0]	REFA validation timer [15:8]			0x0	R/W
0x0412		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFA validation timer [19:16]		REFA validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0x0	R/W
0x0413	Jitter tolerance	[7:0]	REFA jitter tolerance [7:0]		REFA jitter tolerance. This bit field is called T_{TOL} in the evaluation software, and determines the maximum amount of rms jitter before the excess jitter status bit is activated. This 16-bit value is in units of nanoseconds, and setting this bit to zero disables this feature.	0x0	R/W
0x0414		[7:0]	REFA jitter tolerance [15:8]			0x0	R/W

REFERENCE INPUT AA (REFAA) REGISTERS—REGISTER 0x0420 TO REGISTER 0x0434

Table 24. Reference Input AA Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0420	R divider	REFAA R divide ratio [7:0]								0x00	R/W
0x0421		REFAA R divide ratio [15:8]								0x00	R/W
0x0422		REFAA R divide ratio [23:16]								0x00	R/W
0x0423		Reserved		REFAA R divide ratio [29:24]						0x00	R/W
0x0424	Input period	REFAA nominal period [7:0]								0x00	R/W
0x0425		REFAA nominal period [15:8]								0x00	R/W
0x0426		REFAA nominal period [23:16]								0x00	R/W
0x0427		REFAA nominal period [31:24]								0x00	R/W
0x0428		REFAA nominal period [39:32]								0x00	R/W
0x0429		REFAA nominal period [47:40]								0x00	R/W
0x042A		Reserved							REFAA nominal period [48]	0x00	R/W
0x042B	Reserved	Reserved								0x00	R/W
0x042C	Offset limit	REFAA offset limit [7:0]								0xA0	R/W
0x042D		REFAA offset limit [15:8]								0x86	R/W
0x042E		REFAA offset limit [23:16]								0x01	R/W
0x042F	Monitor hysteresis	Reserved					REFAA monitor hysteresis			0x03	R/W
0x0430	Validation timer	REFAA validation timer [7:0]								0x0A	R/W
0x0431		REFAA validation timer [15:8]								0x00	R/W
0x0432		Reserved				REFAA validation timer [19:16]				0x00	R/W
0x0433	Jitter tolerance	REFAA jitter tolerance [7:0]								0x00	R/W
0x0434		REFAA jitter tolerance [15:8]								0x00	R/W

Table 25. Reference Input AA Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0420	R divider	[7:0]	REFAA R divide ratio [7:0]		REFAA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0421		[7:0]	REFAA R divide ratio [15:8]			0x0	R/W
0x0422		[7:0]	REFAA R divide ratio [23:16]			0x0	R/W
0x0423		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFAA R divide ratio [29:24]		REFAA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0424	Input period	[7:0]	REFAA nominal period [7:0]		REFAA nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0425		[7:0]	REFAA nominal period [15:8]			0x0	R/W
0x0426		[7:0]	REFAA nominal period [23:16]			0x0	R/W
0x0427		[7:0]	REFAA nominal period [31:24]			0x0	R/W
0x0428		[7:0]	REFAA nominal period [39:32]			0x0	R/W
0x0429		[7:0]	REFAA nominal period [47:40]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x042A		[7:1]	Reserved		Reserved.	0x0	R
		0	REFAA nominal period [48]		REFAA nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x042B	Reserved	[7:0]	Reserved		Reserved.	0x0	R
0x042C	Offset limit	[7:0]	REFAA offset limit [7:0]		REFAA offset limit. This bit field is called ΔT_{REF} in the evaluation software. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x042D		[7:0]	REFAA offset limit [15:8]			0x86	R/W
0x042E		[7:0]	REFAA offset limit [23:16]			0x1	R/W
0x042F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFAA monitor hysteresis		REFAA monitor hysteresis. This bit field is called T_{HYS} in the evaluation software and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of ΔT_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of ΔT_{REF}.		
				2	6.25% of ΔT_{REF}.		
				3	12.5% of ΔT_{REF}.		
				4	25% of ΔT_{REF}.		
				5	50% of ΔT_{REF}.		
				6	75% of ΔT_{REF}.		
				7	87.5% of ΔT_{REF}.		
0x0430	Validation timer	[7:0]	REFAA validation timer [7:0]		REFAA validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x0431		[7:0]	REFAA validation timer [15:8]			0x0	R/W
0x0432		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFAA validation timer [19:16]		REFAA validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0x0	R/W
0x0433	Jitter tolerance	[7:0]	REFAA jitter tolerance [7:0]			0x0	R/W
0x0434		[7:0]	REFAA jitter tolerance [15:8]			0x0	R/W

REFERENCE INPUT B (REFB) REGISTERS—REGISTER 0x0440 TO REGISTER 0x0454

Table 26. Reference Input B Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0440	R divider	REFB R divide ratio [7:0]								0x00	R/W
0x0441		REFB R divide ratio [15:8]								0x00	R/W
0x0442		REFB R divide ratio [23:16]								0x00	R/W
0x0443		Reserved		REFB R divide ratio [29:24]						0x00	R/W
0x0444	Input period	REFB nominal period [7:0]								0x00	R/W
0x0445		REFB nominal period [15:8]								0x00	R/W
0x0446		REFB nominal period [23:16]								0x00	R/W
0x0447		REFB nominal period [31:24]								0x00	R/W
0x0448		REFB nominal period [39:32]								0x00	R/W
0x0449		REFB nominal period [47:40]								0x00	R/W
0x044A		Reserved							REFB nominal period [48]	0x00	R/W
0x044B	Reserved	Reserved								0x00	R/W
0x044C	Offset limit	REFB offset limit [7:0]								0xA0	R/W
0x044D		REFB offset limit [15:8]								0x86	R/W
0x044E		REFB offset limit [23:16]								0x01	R/W
0x044F	Monitor hysteresis	Reserved					REFB monitor hysteresis			0x03	R/W
0x0450	Validation timer	REFB validation timer [7:0]								0x0A	R/W
0x0451		REFB validation timer [15:8]								0x00	R/W
0x0452		Reserved				REFB validation timer [19:16]				0x00	R/W
0x0453	Jitter tolerance	REFB jitter tolerance [7:0]								0x00	R/W
0x0454		REFB jitter tolerance [15:8]								0x00	R/W

Table 27. Reference Input B Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0440	R divider	[7:0]	REFB R divide ratio [7:0]		REFB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0441		[7:0]	REFB R divide ratio [15:8]			0x0	R/W
0x0442		[7:0]	REFB R divide ratio [23:16]			0x0	R/W
0x0443		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFB R divide ratio [29:24]		REFB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0444	Input period	[7:0]	REFB nominal period [7:0]		REFB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0445		[7:0]	REFB nominal period [15:8]			0x0	R/W
0x0446		[7:0]	REFB nominal period [23:16]			0x0	R/W
0x0447		[7:0]	REFB nominal period [31:24]			0x0	R/W
0x0448		[7:0]	REFB nominal period [39:32]			0x0	R/W
0x0449		[7:0]	REFB nominal period [47:40]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x044A		[7:1]	Reserved		Reserved.	0x0	R
		0	REFB nominal period [48]		REFB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x044B	Reserved	[7:0]	Reserved		Reserved.	0x0	R
0x044C	Offset limit	[7:0]	REFB offset limit [7:0]		REFB offset limit. This bit field is called ΔT_{REF} in the evaluation software. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x044D		[7:0]	REFB offset limit [15:8]			0x86	R/W
0x044E		[7:0]	REFB offset limit [23:16]			0x1	R/W
0x044F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFB monitor hysteresis		REFB monitor hysteresis. This bit field is called T_{HYS} in the evaluation software and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of ΔT_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of ΔT_{REF}.		
				2	6.25% of ΔT_{REF}.		
				3	12.5% of ΔT_{REF}.		
				4	25% of ΔT_{REF}.		
				5	50% of ΔT_{REF}.		
				6	75% of ΔT_{REF}.		
				7	87.5% of ΔT_{REF}.		
0x0450	Validation timer	[7:0]	REFB validation timer [7:0]		REFB validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x0451		[7:0]	REFB validation timer [15:8]			0x0	R/W
0x0452		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFB validation timer [19:16]		REFB validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0x0	R/W
0x0453	Jitter tolerance	[7:0]	REFB jitter tolerance [7:0]		REFB jitter tolerance. This bit field is called T_{TOL} in the evaluation software, and determines the maximum amount of rms jitter before the excess jitter status bit is activated. This 16-bit value is in units of nanoseconds, and setting this bit to zero disables this feature.	0x0	R/W
0x0454		[7:0]	REFB jitter tolerance [15:8]			0x0	R/W

REFERENCE INPUT BB (REFBB) REGISTERS—REGISTER 0x0460 TO REGISTER 0x0474

Table 28. Reference Input BB Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0460	R divider	REFBB R divide ratio [7:0]								0x00	R/W
0x0461		REFBB R divide ratio [15:8]								0x00	R/W
0x0462		REFBB R divide ratio [23:16]								0x00	R/W
0x0463		Reserved		REFBB R divide ratio [29:24]						0x00	R/W
0x0464	Input period	REFBB nominal period [7:0]								0x00	R/W
0x0465		REFBB nominal period [15:8]								0x00	R/W
0x0466		REFBB nominal period [23:16]								0x00	R/W
0x0467		REFBB nominal period [31:24]								0x00	R/W
0x0468		REFBB nominal period [39:32]								0x00	R/W
0x0469		REFBB nominal period [47:40]								0x00	R/W
0x046A		Reserved							REFBB nominal period [48]	0x00	R/W
0x046B	Reserved	Reserved								0x00	R/W
0x046C	Offset limit	REFBB offset limit [7:0]								0xA0	R/W
0x046D		REFBB offset limit [15:8]								0x86	R/W
0x046E		REFBB offset limit [23:16]								0x01	R/W
0x046F	Monitor hysteresis	Reserved					REFBB monitor hysteresis			0x03	R/W
0x0470	Validation timer	REFBB validation timer [7:0]								0x0A	R/W
0x0471		REFBB validation timer [15:8]								0x00	R/W
0x0472		Reserved				REFBB validation timer [19:16]				0x00	R/W
0x0473	Jitter tolerance	REFBB jitter tolerance [7:0]								0x00	R/W
0x0474		REFBB jitter tolerance [15:8]								0x00	R/W

Table 29. Reference Input BB Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0460	R divider	[7:0]	REFBB R divide ratio [7:0]		REFBB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0461		[7:0]	REFBB R divide ratio [15:8]			0x0	R/W
0x0462		[7:0]	REFBB R divide ratio [23:16]			0x0	R/W
0x0463		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFBB R divide ratio [29:24]		REFBB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0464	Input period	[7:0]	REFBB nominal period [7:0]		REFBB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0465		[7:0]	REFBB nominal period [15:8]			0x0	R/W
0x0466		[7:0]	REFBB nominal period [23:16]			0x0	R/W
0x0467		[7:0]	REFBB nominal period [31:24]			0x0	R/W
0x0468		[7:0]	REFBB nominal period [39:32]			0x0	R/W
0x0469		[7:0]	REFBB nominal period [47:40]			0x0	R/W
0x046A	Input period	[7:1]	Reserved		Reserved.	0x0	R
		0	REFBB nominal period [48]		REFBB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x046B	Reserved	[7:0]	Reserved		Reserved.	0x0	R
0x046C	Offset limit	[7:0]	REFBB offset limit [7:0]		REFBB offset limit. This bit field is called ΔT_{REF} in the evaluation software. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x046D		[7:0]	REFBB offset limit [15:8]			0x86	R/W
0x046E		[7:0]	REFBB offset limit [23:16]			0x1	R/W
0x046F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFBB monitor hysteresis		REFBB monitor hysteresis. This bit field is called T_{HYS} in the evaluation software and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of ΔT_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of ΔT_{REF}.		
				2	6.25% of ΔT_{REF}.		
				3	12.5% of ΔT_{REF}.		
				4	25% of ΔT_{REF}.		
				5	50% of ΔT_{REF}.		
				6	75% of ΔT_{REF}.		
				7	87.5% of ΔT_{REF}.		
0x470	Validation timer	[7:0]	REFBB validation timer [7:0]		REFBB validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x471		[7:0]	REFBB validation timer [15:8]			0x0	R/W
0x472		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFBB validation timer [19:16]		REFBB validation timer. This bit field is called T_{VALID} in the evaluation software and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0x0	R/W
0x0473	Jitter tolerance	[7:0]	REFBB jitter tolerance [7:0]		REFBB jitter tolerance. This bit field is called T_{TOL} in the evaluation software and determines the maximum amount of rms jitter before the excess jitter status bit is activated. This 16-bit value is in units of nanoseconds, and setting this bit to zero disables this feature.	0x0	R/W
0x0474		[7:0]	REFBB jitter tolerance [15:8]			0x0	R/W

SOURCE PROFILE 0 A REGISTERS—REGISTER 0x0800 TO REGISTER 0x0811

Table 30. Source Profile 0 A Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0800	Phase lock threshold	Profile 0 phase lock threshold [7:0]								0xBC	R/W
0x0801		Profile 0 phase lock threshold [15:8]								0x02	R/W
0x0802		Profile 0 phase lock threshold [23:16]								0x00	R/W
0x0803	Phase lock fill rate	Profile 0 phase lock fill rate								0x0A	R/W
0x0804	Phase lock drain rate	Profile 0 phase lock drain rate								0x0A	R/W
0x0805	Frequency lock threshold	Profile 0 frequency lock threshold [7:0]								0xBC	R/W
0x0806		Profile 0 frequency lock threshold [15:8]								0x02	R/W
0x0807		Profile 0 frequency lock threshold [23:16]								0x00	R/W
0x0808	Frequency lock fill rate	Profile 0 frequency lock fill rate								0x0A	R/W
0x0809	Frequency lock drain rate	Profile 0 frequency lock drain rate								0x0A	R/W
0x080A	Phase step threshold	Profile 0 phase step threshold [7:0]								0x00	R/W
0x080B		Profile 0 phase step threshold [15:8]								0x00	R/W
0x080C		Profile 0 phase step threshold [23:16]								0x00	R/W
0x080D		Profile 0 phase step threshold [31:24]								0x00	R/W
0x080E	Phase skew	Profile 0 phase skew [7:0]								0x00	R/W
0x080F		Profile 0 phase skew [15:8]								0x00	R/W
0x0810		Profile 0 phase skew [23:16]								0x00	R/W
0x0811	Phase refinement	Profile 0 phase skew refinement steps								0x00	R/W

Table 31. Source Profile 1 AA Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x0820 to 0x0831	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 32. Source Profile 2 B Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x0840 to 0x0851	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 33. Source Profile 3 BB Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x0860 to 0x0871	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 34. Source Profile 4 NCO 0 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x0880 to 0x0891	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 35. Source Profile 5 NCO 1 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x08A0 to 0x08B1	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 36. Source Profile 6 DPLL0 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x08C0 to 0x08D1	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 37. Source Profile 7 DPLL1 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x08E0 to 0x08F1	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 38. Source Profile 0 A Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0800	Phase lock threshold	[7:0]	Profile 0 phase lock threshold [7:0]		Profile 0 phase lock threshold. Phase lock detector threshold (in picoseconds).	0xBC	R/W
0x0801		[7:0]	Profile 0 phase lock threshold [15:8]			0x2	R/W
0x0802		[7:0]	Profile 0 phase lock threshold [23:16]			0x0	R/W
0x0803	Phase lock fill rate	[7:0]	Profile 0 phase lock fill rate		Profile 0 phase lock fill rate. Phase lock detector fill rate per phase frequency detector (PFD) cycle.	0xA	R/W
0x0804	Phase lock drain rate	[7:0]	Profile 0 phase lock drain rate		Profile 0 phase lock drain rate. Phase lock detector lock drain rate per PFD cycle.	0xA	R/W
0x0805	Frequency lock threshold	[7:0]	Profile 0 frequency lock threshold [7:0]		Profile 0 frequency lock threshold. Frequency lock detector threshold (in picoseconds).	0xBC	R/W
0x0806		[7:0]	Profile 0 frequency lock threshold [15:8]			0x2	R/W
0x0807		[7:0]	Profile 0 frequency lock threshold [23:16]			0x0	R/W
0x0808	Frequency lock fill rate	[7:0]	Profile 0 frequency lock fill rate		Profile 0 frequency lock fill rate. Frequency lock detector fill rate per PFD cycle.	0xA	R/W
0x0809	Frequency lock drain rate	[7:0]	Profile 0 frequency lock drain rate		Profile 0 frequency lock drain rate. Frequency lock detector drain rate per PFD cycle.	0xA	R/W
0x080A	Phase step threshold	[7:0]	Profile 0 phase step threshold [7:0]		Profile 0 phase step detector threshold. This 32-bit bit field is the threshold (in picoseconds) at which the DPLL declares that an input reference phase step occurred. The value of this register must always be set so that the detector only activates during a reference switching event and never during normal PLL operation (when the DPLL is not switching). A value of zero indicates that the feature is disabled.	0x0	R/W
0x080B		[7:0]	Profile 0 phase step threshold [15:8]			0x0	R/W
0x080C		[7:0]	Profile 0 phase step threshold [23:16]			0x0	R/W
0x080D		[7:0]	Profile 0 phase step threshold [31:24]			0x0	R/W
0x080E	Phase skew	[7:0]	Profile 0 phase skew [7:0]		Profile 0 phase skew. Closed-loop phase skew adjustment in picoseconds.	0x0	R/W
0x080F		[7:0]	Profile 0 phase skew [15:8]			0x0	R/W
0x0810		[7:0]	Profile 0 phase skew [23:16]			0x0	R/W
0x0811	Phase refinement	[7:0]	Profile 0 Phase skew refinement steps		Profile 0 phase skew refinement steps. This 8-bit bit field contains the number of the PFD cycles averaged during a phase build out acquisition.	0x0	R/W

LOOP FILTER COEFFICIENTS 0 REGISTERS—REGISTER 0x0C00 TO REGISTER 0x0C0B

Table 39. Loop Filter Coefficients 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0C00	Base Loop Filter 0	Alpha Significand 0 [7:0]								0xC2	R/W
0x0C01		Alpha Significand 0 [15:8]								0xF0	R/W
0x0C02		Alpha Exponent 0								0xB3	R/W
0x0C03		Beta Significand 0 [7:0]								0x55	R/W
0x0C04		Beta Significand 0 [15:8]								0xC9	R/W
0x0C05		Beta Exponent 0								0xFB	R/W
0x0C06		Gamma Significand 0 [7:0]								0x5C	R/W
0x0C07		Gamma Significand 0 [15:8]								0xF6	R/W
0x0C08		Gamma Exponent 0								0xCA	R/W
0x0C09		Delta Significand 0 [7:0]								0x11	R/W
0x0C0A		Delta Significand 0 [15:8]								0xDF	R/W
0x0C0B		Delta Exponent 0								0xCC	R/W

Table 40. Loop Filter Coefficients 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0C00	Base Loop Filter 0	[7:0]	Alpha Significand 0 [7:0]		Alpha Significand 0.	0xC2	R/W
0x0C01		[7:0]	Alpha Significand 0 [15:8]		Alpha Significand 0.	0xF0	R/W
0x0C02		[7:0]	Alpha Exponent 0		Alpha Exponent 0.	0xB3	R/W
0x0C03		[7:0]	Beta Significand 0 [7:0]		Beta Significand 0.	0x55	R/W
0x0C04		[7:0]	Beta Significand 0 [15:8]		Beta Significand 0.	0xC9	R/W
0x0C05		[7:0]	Beta Exponent 0		Beta Exponent 0.	0xFB	R/W
0x0C06		[7:0]	Gamma Significand 0 [7:0]		Gamma Significand 0.	0x5C	R/W
0x0C07		[7:0]	Gamma Significand 0 [15:8]		Gamma Significand 0.	0xF6	R/W
0x0C08		[7:0]	Gamma Exponent 0		Gamma Exponent 0.	0xCA	R/W
0x0C09		[7:0]	Delta Significand 0 [7:0]		Delta Significand 0.	0x11	R/W
0x0C0A		[7:0]	Delta Significand 0 [15:8]		Delta Significand 0.	0xDF	R/W
0x0C0B		[7:0]	Delta Exponent 0		Delta Exponent 0.	0xCC	R/W

LOOP FILTER COEFFICIENTS 1 REGISTERS—REGISTER 0x0C0C TO REGISTER 0x0C17

Table 41. Loop Filter Coefficients 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0C0C	Base Loop Filter 1	Alpha Significand 1 [7:0]								0xA9	R/W
0x0C0D		Alpha Significand 1 [15:8]								0xA0	R/W
0x0C0E		Alpha Exponent 1								0xB7	R/W
0x0C0F		Beta Significand 1 [7:0]								0xCD	R/W
0x0C10		Beta Significand 1 [15:8]								0xDB	R/W
0x0C11		Beta Exponent 1								0xF3	R/W
0x0C12		Gamma Significand 1 [7:0]								0x79	R/W
0x0C13		Gamma Significand 1 [15:8]								0xD4	R/W
0x0C14		Gamma Exponent 1								0xCE	R/W
0x0C15		Delta Significand 1 [7:0]								0x4D	R/W
0x0C16		Delta Significand 1 [15:8]								0xA7	R/W
0x0C17		Delta Exponent 1								0xCF	R/W

Table 42. Loop Filter Coefficients 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0C0C	Base Loop Filter 1	[7:0]	Alpha Significand 1 [7:0]		Alpha Significand 1.	0xA9	R/W
0x0C0D		[7:0]	Alpha Significand 1 [15:8]		Alpha Significand 1.	0xA0	R/W
0x0C0E		[7:0]	Alpha Exponent 1		Alpha Exponent 1.	0xB7	R/W
0x0C0F		[7:0]	Beta Significand 1 [7:0]		Beta Significand 1.	0xCD	R/W
0x0C10		[7:0]	Beta Significand 1 [15:8]		Beta Significand 1.	0xDB	R/W
0x0C11		[7:0]	Beta Exponent 1		Beta Exponent 1.	0xF3	R/W
0x0C12		[7:0]	Gamma Significand 1 [7:0]		Gamma Significand 1.	0x79	R/W
0x0C13		[7:0]	Gamma Significand 1 [15:8]		Gamma Significand 1.	0xD4	R/W
0x0C14		[7:0]	Gamma Exponent 1		Gamma Exponent 1.	0xCE	R/W
0x0C15		[7:0]	Delta Significand 1 [7:0]		Delta Significand 1.	0x4D	R/W
0x0C16		[7:0]	Delta Significand 1 [15:8]		Delta Significand 1.	0xA7	R/W
0x0C17		[7:0]	Delta Exponent 1		Delta Exponent 1.	0xCF	R/W

DPLL CHANNEL 0 REGISTERS—REGISTER 0x1000 TO REGISTER 0x102A

Table 43. DPLL Channel 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1000	Freerun tuning word	DPLL0 freerun tuning word [7:0]								0x00	R/W
0x1001		DPLL0 freerun tuning word [15:8]								0x00	R/W
0x1002		DPLL0 freerun tuning word [23:16]								0x00	R/W
0x1003		DPLL0 freerun tuning word [31:24]								0x00	R/W
0x1004		DPLL0 freerun tuning word [39:32]								0x00	R/W
0x1005		Reserved		DPLL0 freerun tuning word [45:40]						0x00	R/W
0x1006	Tuning word clamp	DPLL0 freerun tuning word offset clamp [7:0]								0xFF	R/W
0x1007		DPLL0 freerun tuning word offset clamp [15:8]								0xFF	R/W
0x1008		DPLL0 freerun tuning word offset clamp [23:16]								0xFF	R/W
0x1009	NCO gain	Reserved				DPLL0 NCO gain filter bandwidth				0x00	R/W
0x100A	History accumulation timer	DPLL0 history accumulation timer [7:0]								0x0A	R/W
0x100B		DPLL0 history accumulation timer [15:8]								0x00	R/W
0x100C		DPLL0 history accumulation timer [23:16]								0x00	R/W
0x100D		Reserved				DPLL0 history accumulation timer [27:24]				0x00	R/W
0x100E		Reserved		DPLL0 delay history until not slew limiting	DPLL0 delay history frequency lock	DPLL0 delay history phase lock	DPLL0 quick start history	DPLL0 single sample history	DPLL0 persistent history	0x38	R/W
0x100F		Reserved					DPLL0 pause history while phase slew limiting	DPLL0 pause history frequency unlock	DPLL0 pause history phase unlock	0x00	R/W
0x1010	History accumulator hold off	DPLL0 history hold off time								0x00	R/W
0x1011	Phase slew limit	DPLL0 phase slew limit rate [7:0]								0x00	R/W
0x1012		DPLL0 phase slew limit rate [15:8]								0x00	R/W
0x1013		DPLL0 phase slew limit rate [23:16]								0x00	R/W
0x1014		DPLL0 phase slew limit rate [31:24]								0x06	R/W
0x1015	Phase offset	DPLL0 phase offset [7:0]								0x00	R/W
0x1016		DPLL0 phase offset [15:8]								0x00	R/W
0x1017		DPLL0 phase offset [23:16]								0x00	R/W
0x1018		DPLL0 phase offset [31:24]								0x00	R/W
0x1019		DPLL0 phase offset [39:32]								0x00	R/W

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x101A	Phase temperature compensation polynomial	DPLL0 phase temperature compensation C_1 significand [7:0]								0x00	R/W
0x101B		DPLL0 phase temperature compensation C_1 significand [15:8]								0x00	R/W
0x101C		DPLL0 phase temperature compensation C_1 exponent								0x00	R/W
0x101D		DPLL0 phase temperature compensation C_2 significand [7:0]								0x00	R/W
0x101E		DPLL0 phase temperature compensation C_2 significand [15:8]								0x00	R/W
0x101F		DPLL0 phase temperature compensation C_2 exponent								0x00	R/W
0x1020		DPLL0 phase temperature compensation C_3 significand [7:0]								0x00	R/W
0x1021		DPLL0 phase temperature compensation C_3 significand [15:8]								0x00	R/W
0x1022		DPLL0 phase temperature compensation C_3 exponent								0x00	R/W
0x1023		DPLL0 phase temperature compensation C_4 significand [7:0]								0x00	R/W
0x1024		DPLL0 phase temperature compensation C_4 significand [15:8]								0x00	R/W
0x1025		DPLL0 phase temperature compensation C_4 exponent								0x00	R/W
0x1026		DPLL0 phase temperature compensation C_5 significand [7:0]								0x00	R/W
0x1027		DPLL0 phase temperature compensation C_5 significand [15:8]								0x00	R/W
0x1028		DPLL0 phase temperature compensation C_5 exponent								0x00	R/W
0x1029	Phase adjust filter bandwidth	Reserved					DPLL0 phase temperature compensation filter bandwidth			0x00	R/W
0x102A	Inactive profile	Reserved					DPLL0 inactive profile index			0x00	R/W

Table 44. DPLL Channel 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1000	Freerun tuning word	[7:0]	DPLL0 freerun tuning word [7:0]		DPLL0 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL0 while it is in freerun mode.	0x0	R/W
0x1001		[7:0]	DPLL0 freerun tuning word [15:8]			0x0	R/W
0x1002		[7:0]	DPLL0 freerun tuning word [23:16]			0x0	R/W
0x1003		[7:0]	DPLL0 freerun tuning word [31:24]			0x0	R/W
0x1004		[7:0]	DPLL0 freerun tuning word [39:32]			0x0	R/W
0x1005		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 freerun tuning word [45:40]		DPLL0 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL0 while it is in freerun mode.	0x0	R/W
0x1006	Tuning word clamp	[7:0]	DPLL0 freerun tuning word offset clamp [7:0]		DPLL0 freerun tuning word offset clamp. This 24-bit bit field sets the DPLL0 tuning word offset clamp, f_{CLAMP}. The formula is f_{CLAMP} = DPLL0 freerun tuning word offset clamp × ($f_S/2^{36}$), where f_S is the system clock frequency.	0xFF	R/W
0x1007		[7:0]	DPLL0 freerun tuning word offset clamp [15:8]			0xFF	R/W
0x1008		[7:0]	DPLL0 freerun tuning word offset clamp [23:16]			0xFF	R/W
0x1009	NCO gain	[7:4]	Reserved		Reserved.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:0]	DPLL0 NCO gain filter bandwidth		DPLL0 NCO gain freerun tuning word filter bandwidth. This 4-bit bit field controls the low-pass filter, −3 dB cutoff frequency of the DPLL0 NCO.	0x0	R/W
				0x0	250 kHz (maximum).		
				0x1	120 kHz.		
				0x2	62 kHz.		
				0x3	31 kHz.		
				0x4	16 kHz.		
				0x5	7.8 kHz.		
				0x6	3.9 kHz.		
				0x7	1.9 kHz.		
				0x8	970 Hz.		
				0x9	490 Hz.		
				0xa	240 Hz.		
				0xb	120 Hz.		
				0xc	61 Hz.		
				0xd	30 Hz.		
				0xe	15 Hz.		
				0xf	7.6 Hz (minimum).		
0x100A	History accumulation timer	[7:0]	DPLL0 history accumulation timer [7:0]		DPLL0 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the evaluation software. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and the behavior is undefined for a timer value of 0x0000.	0xA	R/W
0x100B		[7:0]	DPLL0 history accumulation timer [15:8]			0x0	R/W
0x100C		[7:0]	DPLL0 history accumulation timer [23:16]			0x0	R/W
0x100D		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL0 history accumulation timer [27:24]		DPLL0 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the evaluation software. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and the behavior is undefined for a timer value of 0x0000.	0x0	R/W
0x100E		[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 delay history until not phase slew limiting		DPLL0 delay history until not phase slew limiting. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL0 phase slew limiter is inactive. At that point, the tuning word averaging is further delayed by the value in the DPLL0 history hold off time. This bit ensures that the holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase slew limiter.	0x1	R/W
		4	DPLL0 delay history frequency lock		DPLL0 delay history until frequency lock. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL0 is frequency locked. At that point, the tuning word averaging is further delayed by the value in the DPLL0 history hold off time. This bit ensures that the holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the frequency lock detector.	0x1	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	DPLL0 delay history phase lock		DPLL0 delay history until phase lock. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL0 is phase locked. At this point, the tuning word averaging is further delayed by the value in the DPLL0 history hold off time. This bit ensures that holdover history averaging begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase lock detector.	0x1	R/W
		2	DPLL0 quick start history		DPLL0 quick start history. Setting this bit to Logic 1 allows the DPLL0 tuning word history to be available in 1/4 of the time specified in the DPLL0 history accumulation timer. This bit ensures that there is sufficient holdover history in cases where the DPLL is locked to a reference for a short period.	0x0	R/W
		1	DPLL0 single sample history		DPLL0 single sample history. Setting this bit to Logic 1 allows DPLL0 to use the most recent tuning word for holdover in the event that the tuning word history is not available. This bit can be used in conjunction with the quick start history bit in this register. This bit ensures that there is a minimal holdover history available in cases where the DPLL is locked to a reference for a short period.	0x0	R/W
		0	DPLL0 persistent history		DPLL0 persistent history. Setting this bit to Logic 1 prevents the DPLL0 tuning word history from being reset if there is an interruption in the tuning word averaging. This bit ensures that there is sufficient holdover history when the DPLL is locked to a reference for a short period. When this bit is Logic 0, and the DPLL exits holdover and reacquires a reference input, the history accumulation resets.	0x0	R/W
0x100F		[7:3]	Reserved		Reserved.	0x0	R
		2	DPLL0 pause history while phase slew limiting		DPLL0 pause history while phase slew limiting. Setting this bit to Logic 1 pauses the tuning word history averaging when DPLL0 is phase slewing. The tuning word history is reset when the DPLL regains phase lock if the persistent history bit is Logic 0. This bit ensures that tuning word history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase slewing.	0x0	R/W
		1	DPLL0 pause history frequency unlock		DPLL0 pause history while frequency unlock. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when DPLL0 is frequency unlocked. The holdover history is reset when the DPLL regains frequency lock if the persistent history bit is Logic 0. This bit ensures that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of frequency lock status.	0x0	R/W
		0	DPLL0 pause history phase unlock		DPLL0 pause history while phase unlock. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when the DPLL0 phase slew limiter is active. The holdover history is reset when the DPLL is no longer phase slew limited if the persistent history bit is Logic 0. This bit ensures that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase lock status.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1010	History accumulation hold off	[7:0]	DPLL0 history hold off time		DPLL0 history hold off time. This 8-bit bit field is the amount of time (in milliseconds) that the DPLL tuning word history accumulation is delayed. Hold off is disabled if this bit field is 0x00.	0x0	R/W
0x1011	Phase slew limit	[7:0]	DPLL0 phase slew limit rate [7:0]		DPLL0 phase slew limit rate. This 32-bit bit field is the DPLL0 phase slew limit rate (in picoseconds per second) and is referred to as t_{OFST} in the evaluation software.	0x0	R/W
0x1012		[7:0]	DPLL0 phase slew limit rate [15:8]			0x0	R/W
0x1013		[7:0]	DPLL0 phase slew limit rate [23:16]			0x0	R/W
0x1014		[7:0]	DPLL0 phase slew limit rate [31:24]			0x6	R/W
0x1015	Phase offset	[7:0]	DPLL0 phase offset [7:0]		DPLL0 closed-loop phase offset. This signed 40-bit bit field is the DPLL0 closed-loop phase offset (in picoseconds) and is referred to as t_{OFST} in the evaluation software.	0x0	R/W
0x1016		[7:0]	DPLL0 phase offset [15:8]			0x0	R/W
0x1017		[7:0]	DPLL0 phase offset [23:16]			0x0	R/W
0x1018		[7:0]	DPLL0 phase offset [31:24]			0x0	R/W
0x1019		[7:0]	DPLL0 phase offset [39:32]			0x0	R/W
0x101A	Phase temperature compensation polynomial	[7:0]	DPLL0 phase temperature compensation C_1 significand [7:0]		DPLL0 temperature compensation C_1 significand. This 16-bit bit field is the significand for the C_1 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x101B		[7:0]	DPLL0 phase temperature compensation C_1 significand [15:8]			0x0	R/W
0x101C		[7:0]	DPLL0 phase temperature compensation C_1 exponent		DPLL0 temperature compensation C_1 exponent. This 8-bit bit field is the exponent for the C_1 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x101D		[7:0]	DPLL0 phase temperature compensation C_2 significand [7:0]		DPLL0 temperature compensation C_2 significand. This 16-bit bit field is the significand for the C_2 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x101E		[7:0]	DPLL0 phase temperature compensation C_2 significand [15:8]			0x0	R/W
0x101F		[7:0]	DPLL0 phase temperature compensation C_2 exponent		DPLL0 temperature compensation C_2 exponent. This 8-bit bit field is the exponent for the C_2 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1020		[7:0]	DPLL0 phase temperature compensation C_3 significand [7:0]		DPLL0 temperature compensation C_3 significand. This 16-bit bit field is the significand for the C_3 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1021		[7:0]	DPLL0 phase temperature compensation C_3 significand [15:8]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1022		[7:0]	DPLL0 phase temperature compensation C_3 exponent		DPLL0 temperature compensation C_3 exponent. This 8-bit bit field is the exponent for the C_3 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1023		[7:0]	DPLL0 phase temperature compensation C_4 significand [7:0]		DPLL0 temperature compensation C_4 significand. This 16-bit bit field is the significand for the C_4 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1024		[7:0]	DPLL0 phase temperature compensation C_4 significand [15:8]			0x0	R/W
0x1025		[7:0]	DPLL0 phase temperature compensation C_4 exponent		DPLL0 temperature compensation C_4 exponent. This 8-bit bit field is the exponent for the C_4 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1026		[7:0]	DPLL0 phase temperature compensation C_5 significand [7:0]		DPLL0 temperature compensation C_5 significand. This 16-bit bit field is the significand for the C_5 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1027		[7:0]	DPLL0 phase temperature compensation C_5 significand [15:8]			0x0	R/W
0x1028		[7:0]	DPLL0 phase temperature compensation C_5 exponent		DPLL0 temperature compensation C_5 exponent. This 8-bit bit field is the exponent for the C_5 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1029	Phase adjust filter bandwidth	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL0 phase temperature compensation filter bandwidth		DPLL0 temperature compensation low-pass filter bandwidth. This 3-bit bit field controls the low-pass filter −3 dB cutoff frequency of the DPLL0 delay compensation block.	0x0	R/W
				0x0	240 Hz (maximum).		
				0x1	120 Hz.		
				0x2	60 Hz.		
				0x3	30 Hz.		
				0x4	15 Hz.		
				0x5	7.6 Hz.		
				0x6	3.8 Hz.		
				0x7	1.9 Hz (minimum).		
0x102A	Inactive profile	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL0 inactive profile index		DPLL0 inactive profile index. The inactive profile index is used while DPLL0 is in holdover to retain the exact DPLL configuration, including the desired input/output phase relationship.	0x0	R/W

DISTRIBUTION GENERAL 0 REGISTERS—REGISTER 0x10D2 TO REGISTER 0x10DC

Table 45. Distribution General 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x10D2	N-shot gaps	N-shot gap								0x00	R/W
0x10D3	N-shot request	Reserved	N-shot request mode	N-shot						0x00	R/W
0x10D4	N-shot enable	Enable Q0BB PRBS	Enable Q0BB N-shot	Enable Q0B PRBS	Enable Q0B N-shot	Enable Q0AA PRBS	Enable Q0AA N-shot	Enable Q0A PRBS	Enable Q0A N-shot	0x00	R/W
0x10D5	N-shot settings	Reserved				Enable Q0CC PRBS	Enable Q0CC N-shot	Enable Q0C PRBS	Enable Q0C N-shot	0x00	R/W
0x10D6	N-shot retime	Reserved							Enable N-shot retime	0x00	R/W
0x10D7	Driver A configuration	Reserved		Bypass mute retiming Channel A	OUT0A driver mode		OUT0A driver current		Enable OUT0A HCSL	0x01	R/W
0x10D8	Driver B configuration	Reserved		Bypass mute retiming Channel B	OUT0B driver mode		OUT0B driver current		Enable OUT0B HCSL	0x01	R/W
0x10D9	Driver C configuration	Reserved		Bypass mute retiming Channel C	OUT0C driver mode		OUT0C driver current		Enable OUT0C HCSL	0x01	R/W
0x10DA	Secondary clock path	Reserved				Enable SYSCLK Q0C	Enable SYSCLK Q0B	Enable SYSCLK Q0A	Enable SYSCLK sync mask	0x00	R/W
0x10DB	Sync control	Reserved					Enable DPLL0 reference sync	Autosync mode		0x00	R/W
0x10DC	Automute control	Mask OUT0CC autounmute	Mask OUT0C autounmute	Mask OUT0BB autounmute	Mask OUT0B autounmute	Mask OUT0AA autounmute	Mask OUT0A autounmute	DPLL0 autounmute mode		0x00	R/W

Table 46. Distribution General 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10D2	N-shot gaps	[7:0]	N-shot gap		N-shot gap. This unsigned, 8-bit bit field contains the length (measured in Q divider output cycles) of the gap in a JESD204B N-shot pattern generation.	0x0	R/W
0x10D3	N-shot request	7	Reserved		Reserved.	0x0	R
		6	N-shot request mode		Channel 0 N-shot request mode. Logic 0: the N-shot generators operate in burst mode, and the rising edge of the trigger signal initiates the burst. Logic 1: the N-shot generators operate in period gapped mode. In this mode, N-shot bursts occur as long as the trigger is in a Logic 1 state; for this reason, it is referred to as a level sensitive trigger mode.	0x0	R/W
		[5:0]	N-shot		Number of clock pulses in an N-shot burst. This unsigned, 6-bit bit field contains the number of clock cycles in an N-shot burst.	0x0	R/W
0x10D4	N-shot enable	7	Enable Q0BB PRBS		Q0BB JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at divider output rate.	0x0	R/W
		6	Enable Q0BB N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
		5	Enable Q0B PRBS		Q0B JESD204B PRBS enable. Setting this bit to Logic 1 enables pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	Enable Q0B N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
		3	Enable Q0AA PRBS		Q0AA JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		2	Enable Q0AA N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
		1	Enable Q0A PRBS		Q0A JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		0	Enable Q0A N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
0x10D5	N-shot settings	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable Q0CC PRBS		Q0CC JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		2	Enable Q0CC N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
		1	Enable Q0C PRBS		Q0C JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		0	Enable Q0C N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
0x10D6	N-shot retime	[7:1]	Reserved		Reserved.	0x0	R
		0	Enable N-shot retime		Enable N-shot retiming. Logic 0: Mx pins or registers (user selectable) provide the JESD204B N-shot retiming source. Logic 1: the N short retiming block provides the JESD204B N-shot retiming source.	0x0	R/W
0x10D7	Driver A configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel A		Removes retiming from Channel A mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function, and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT0A driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q0A determines the divide ratio.		
				1	Dual-, single-ended output driven by Divider Q0A. Divider Q0A determines the divide ratio.		
				10	Dual-, single-ended output driven by separate Q dividers. Both Divider Q0A and Divider Q0AA are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT0A driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Enable OUT0A HCSL		Selects current source (HCSL) or current sink (CML) mode. Logic 0: CML mode. An external pull-up resistor is required. Logic 1: HCSL mode. An external pull-down resistor is required.	0x0	R/W
0x10D8	Driver B configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel B		Removes retiming from Channel B mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT0B driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q0B determines the divide ratio.		
				1	Dual-, single-ended output driven by Divider Q0A. Divider Q0B determines the divide ratio.		
				10	Dual-, single-ended output driven by separate Q dividers. Both Divider Q0B and Divider Q0BB are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT0B driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT0B HCSL		Selects HCSL or CML mode. Logic 0: CML mode. An external pull-up resistor is required. Logic 1: HCSL mode. An external pull-down resistor is required.	0x0	R/W
0x10D9	Driver C configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel C		Removes retiming from Channel C mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function, and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT0C driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q0C determines the divide ratio.		
				1	Dual-, single-ended output driven by Divider Q0A. Divider Q0C determines the divide ratio.		
				10	Dual-, single-ended output driven by separate Q dividers. Both Divider Q0C and Divider Q0CC are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT0C driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT0C HCSL		Selects HCSL or CML mode. Logic 0: CML mode. An external pull-up resistor is required. Logic 1: HCSL mode. An external pull-down resistor is required.	0x0	R/W
0x10DA	Secondary clock path	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable SYSCLK Q0C		Enable SYSCLK to Divider Q0C. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q0C.	0x0	R/W
		2	Enable SYSCLK Q0B		Enable SYSCLK to Divider Q0B. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q0B.	0x0	R/W
		1	Enable SYSCLK Q0A		Enable SYSCLK to Divider Q0A. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q0A.	0x0	R/W
		0	Enable SYSCLK sync mask		Enable SYSCLK sync mask. Setting this bit to Logic 1 ensures no sync events occur on outputs that are assigned to outputting the SYSCLK. The purpose of this feature is to ensure no runt pulses or stalled clocks occur when a SYSCLK output clocks a microprocessor. Set this bit to Logic 1 only when the SYSCLK is fully configured and stable, because runt pulses can occur while configuring the SYSCLK.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10DB	Sync control	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable DPLL0 reference sync		DPLL0 reference sync enable. Setting this bit to Logic 1 enables automatic reference synchronization on DPLL0.	0x0	R/W
		[1:0]	Autosync mode		Autosync mode. This bit field controls when the clock distribution block receives a synchronization event. The output drivers do not toggle until there is a synchronization event.	0x0	R/W
				0	Manual sync. Automatic output synchronization disabled. In this mode, the user must issue a clock distribution synchronization command manually.		
				1	Immediate. Output synchronization occurs immediately after APLL lock.		
				10	DPLL phase lock. Output synchronization occurs when the DPLL phase locks.		
				11	DPLL frequency lock. Output synchronization occurs when the DPLL frequency locks.		
0x10DC	Automute control	7	Mask OUT0CC autounmute		Mask OUT0CC autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		6	Mask OUT0C autounmute		Mask OUT0C autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		5	Mask OUT0BB autounmute		Mask OUT0BB autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		4	Mask OUT0B autounmute		Mask OUT0B autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		3	Mask OUT0AA autounmute		Mask OUT0AA autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		2	Mask OUT0A autounmute		Mask OUT0A autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		[1:0]	DPLL0 autounmute mode		DPLL0 autounmute mode. This bit field controls the point at which the output drivers start to toggle during acquisition while DPLL0 is in hitless mode.	0x0	R/W
				0	Disabled. Automatic unmuting is disabled and the output driver starts toggling immediately.		
				1	Hitless acquisition. Automatic driver unmuting occurs upon activation of a hitless profile.		
				10	Phase lock detect (hitless mode only). Automatic driver unmuting occurs when phase lock is detected and the DPLL is in hitless mode.		
				11	Frequency lock detect (hitless mode only). Automatic driver unmuting occurs when frequency lock is detected and the DPLL is in hitless mode.		

APLL CHANNEL 0 REGISTERS—REGISTER 0x1080 TO REGISTER 0x1083

Table 47. APLL Channel 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1080	Charge pump current	Enable APLL0 manual charge pump current	APLL0 manual charge pump current							0x94	R/W
0x1081	M0 divider	APLL0 M0 feedback divider								0x00	R/W
0x1082	Loop filter control	APLL0 loop filter zero resistor (R1)			APLL0 loop filter pole capacitor (C2)			APLL0 loop filter second pole resistor (R3)		0xE0	R/W
0x1083	DC offset current	Reserved				APLL0 dc offset current direction	APLL0 dc offset current value		Enable APLL0 dc offset current	0x03	R/W

Table 48. APLL Channel 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1080	Charge pump current	7	Enable APLL0 manual charge pump current		Enables manual control of the APLL0 charge pump current.	0x0	R/W
				0	Disables manual charge pump current control. Disables manual control of the APLL0 charge pump current.		
				1	Enables manual charge pump current control. Enables manual control of the APLL0 charge pump current.		
		[6:0]	APLL0 manual charge pump current		APLL0 manual charge pump current (LSB = 3.5 µA). The user must set the enable APLL0 manual charge pump current control bit in this register for this setting to be enabled.	0x0	R/W
				0000001b	1 × LSB.		
				0000010b	2 × LSB.		
				…	…		
				1111111b	127 × LSB.		
0x1081	M0 divider	[7:0]	APLL0 M0 feedback divider		APLL multiplication ratio. APLL0 M0 feedback divider ratio. Allowable values are 14 to 255.	0x0	R/W
0x1082	Loop filter control	[7:5]	APLL0 loop filter zero resistor (R1)		Loop Filter R1. APLL0 Loop Filter R1 (zero resistor) value.	0x0	R/W
				000	0 Ω (short).		
				001	250 Ω.		
				010	500 Ω.		
				011	750 Ω.		
				100	1.00 kΩ.		
				101	1.25 kΩ.		
				110	1.50 kΩ.		
				111	1.75 kΩ.		
		[4:2]	APLL0 loop filter pole capacitor (C2)		Loop Filter C2. APLL0 Loop Filter C2 (pole capacitor) value.	0x0	R/W
				000	8 pF.		
				001	24 pF.		
				010	40 pF.		
				011	56 pF.		
				100	72 pF.		
				101	88 pF.		
				110	104 pF.		
				111	120 pF.		
		[1:0]	APLL0 loop filter second pole resistor (R3)		Loop Filter R3. APLL0 Loop Filter R3 (second pole resistor) value.	0x0	R/W
				00	200 Ω.		
				01	250 Ω.		
				10	333 Ω.		
				11	500 Ω.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1083	DC offset current	[7:4]	Reserved		Reserved.	0x0	R
		3	APLL0 dc offset current direction		DC offset current direction. This bit sets the direction of the APLL0 dc offset current.	0x0	R/W
				0	Up. The dc offset current offset is positive.		
				1	Down. The dc offset current offset is negative.		
		[2:1]	APLL0 dc offset current value		DC offset current. Magnitude of the APLL0 charge pump dc offset current value.	0x0	R/W
				00	50% offset current. Offset current is 50% of the programmed APLL0 charge pump current (default).		
				01	25% offset current. Offset current is 25% of the programmed APLL0 charge pump current.		
				10	12.5% offset current. Offset current is 12.5% of the programmed APLL0 charge pump current.		
				11	6.25% offset current. Offset current is 6.25% of the programmed APLL0 charge pump current.		
		0	Enable APLL0 dc offset current		DC offset current enable. Setting this bit enables the APLL0 dc offset current.	0x0	R/W

DISTRIBUTION DIVIDER Q0A REGISTERS—REGISTER 0x1100 TO REGISTER 0x1108

Table 49. Distribution Divider Q0A Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1100	Divide ratio	Q0A divide ratio [7:0]								0x00	R/W
0x1101		Q0A divide ratio [15:8]								0x00	R/W
0x1102		Q0A divide ratio [23:16]								0x00	R/W
0x1103		Q0A divide ratio [31:24]								0x00	R/W
0x1104	Phase offset	Q0A phase [7:0]								0x00	R/W
0x1105		Q0A phase [15:8]								0x00	R/W
0x1106		Q0A phase [23:16]								0x00	R/W
0x1107		Q0A phase [31:24]								0x00	R/W
0x1108	Phase slew configuration	Reserved	Q0A Phase [32]	Enable Q0A half divide	Enable Q0A pulse width control	Q0A phase slew mode	Maximum phase slew step			0x07	R/W

Table 50. Distribution Divider Q0AA Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1109 to 0x1111	These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 51. Distribution Divider Q0B Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1112 to 0x111A	These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 52. Distribution Divider Q0BB Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x111B to 0x1123	These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 53. Distribution Divider Q0C Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1124 to 0x112C	These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 54. Distribution Divider Q0CC Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x112D to 0x1135	These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 55. Distribution Divider Q0A Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1100	Divide ratio	[7:0]	Q0A divide ratio [7:0]		Q0A divide ratio. This 32-bit bit field is the divide ratio for the Q0A divider. The default value of 0x00000000 equals a divide ratio of 1, resulting in an output frequency that exceeds the maximum frequency for the AD9542.	0x0	R/W
0x1101		[7:0]	Q0A divide ratio [15:8]			0x0	R/W
0x1102		[7:0]	Q0A divide ratio [23:16]			0x0	R/W
0x1103		[7:0]	Q0A divide ratio [31:24]			0x0	R/W
0x1104	Phase offset	[7:0]	Q0A phase [7:0]		Q0A phase control. This bit field controls the Q0A phase in two ways: the bit field sets the initial phase offset after divider sync (reset); and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q0A distribution input clock half cycles.	0x0	R/W
0x1105		[7:0]	Q0A phase [15:8]			0x0	R/W
0x1106		[7:0]	Q0A phase [23:16]			0x0	R/W
0x1107		[7:0]	Q0A phase [31:24]			0x0	R/W
0x1108	Phase slew configuration	7	Reserved		Reserved.	0x0	R
		6	Q0A phase [32]		Q0A phase control. This bit field controls the Q0A phase in two ways: the bit field sets the initial phase offset after divider sync (reset); and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q0A distribution input clock half cycles.	0x0	R/W
		5	Enable Q0A half divide		Enable Q0A half divide. Setting this bit to Logic 1 adds 0.5 to the divide ratio programmed into the corresponding 32-bit Q0A divide ratio bit field.	0x0	R/W
		4	Enable Q0A pulse width control		Enable pulse width control mode. This bit controls whether the Q0A phase bit field adjusts the phase offset or the pulse width.	0x0	R/W
				0	The Q0A phase bit field controls the phase offset.		
				1	The Q0A phase bit field controls the pulse width.		
		3	Q0A phase slew mode		Q0A phase slew mode.	0x0	R/W
				0	Lag only (always slows down frequency). The phase controller slews the phase in the direction that always reduces the output frequency.		
				1	Lead or lag (quickest is automatically calculated). The phase controller slews the phase in the direction requiring the fewest steps. This means the output frequency can increase or decrease during a stepwise phase adjustment sequence.		
		[2:0]	Maximum phase slew step		Maximum phase slew step. This 3-bit bit field controls the maximum allowable phase step while adjusting the phase in the Q0A divider. Each step occurs every output clock cycle.	0x0	R/W
				0	One input clock half cycle. The phase slew step size is half of the Q divider input period.		
				1	Two input clock half cycles. The maximum phase slew step size equals the Q divider input period.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				10	11°. The maximum phase slew step size equals 1/32 (~11.25°) of the output clock period.		
				11	23°. The maximum phase slew step size equals 1/16 (~22.5°) of the output clock period.		
				100	45°. The maximum phase slew step size equals 1/8 (~45°) of the output clock period.		
				101	90°. The maximum phase slew step size equals 1/4 (~90°) of the output clock period.		
				110	180°. The maximum phase slew step size equals half (~180°) of the output clock period.		
				111	Maximum. The maximum phase slew step size equals the output clock period.		

DPLL TRANSLATION PROFILE 0.0 REGISTERS—REGISTER 0x1200 TO REGISTER 0x1217

Table 56. DPLL Translation Profile 0.0 Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1200	Priority and enable	Reserved		Profile 0.0 selection priority					Enable Profile 0.0	0x00	R/W
0x1201	Source	Reserved			Profile 0.0 reference source selection					0x00	R/W
0x1202	Zero delay feedback path	Reserved			External/internal zero delay feedback path					0x00	R/W
0x1203	Feedback mode	Profile 0.0 loop filter base	Reserved					Enable Profile 0.0 external zero delay	Enable Profile 0.0 hitless	0x00	R/W
0x1204	Loop bandwidth	Profile 0.0 loop bandwidth [7:0]								0x00	R/W
0x1205		Profile 0.0 loop bandwidth [15:8]								0x00	R/W
0x1206		Profile 0.0 loop bandwidth [23:16]								0x00	R/W
0x1207		Profile 0.0 loop bandwidth [31:24]								0x00	R/W
0x1208	Hitless feedback divider	Profile 0.0 hitless N-divider [7:0]								0xA0	R/W
0x1209		Profile 0.0 hitless N-divider [15:8]								0x0F	R/W
0x120A		Profile 0.0 hitless N-divider [23:16]								0x00	R/W
0x120B		Profile 0.0 hitless N-divider [31:24]								0x00	R/W
0x120C	Buildout feedback divider	Profile 0.0 buildout N-divider [7:0]								0xA0	R/W
0x120D		Profile 0.0 buildout N-divider [15:8]								0x0F	R/W
0x120E		Profile 0.0 buildout N-divider [23:16]								0x00	R/W
0x120F		Profile 0.0 buildout N-divider [31:24]								0x00	R/W
0x1210	Buildout feedback fraction	Profile 0.0 buildout fraction [7:0]								0x00	R/W
0x1211		Profile 0.0 buildout fraction [15:8]								0x00	R/W
0x1212		Profile 0.0 buildout fraction [23:16]								0x00	R/W
0x1213	Buildout feedback modulus	Profile 0.0 buildout modulus [7:0]								0x00	R/W
0x1214		Profile 0.0 buildout modulus [15:8]								0x00	R/W
0x1215		Profile 0.0 buildout modulus [23:16]								0x00	R/W
0x1216	Fast lock	Reserved				Profile 0.0 fast acquisition excess bandwidth				0x00	R/W
0x1217		Reserved	Profile 0.0 fast acquisition timeout			Reserved	Profile 0.0 fast acquisition lock settle time			0x00	R/W

Table 57. DPLL Translation Profile 0.1 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1220 to 0x1237	These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 58. DPLL Translation Profile 0.2 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1240 to 0x1257	These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 59. DPLL Translation Profile 0.3 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1260 to 0x1277	These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 60. DPLL Translation Profile 0. 4 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1280 to 0x1297	These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 61. DPLL Translation Profile 0.5 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x12A0 to 0x12B7	These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.								R/W

Table 62. DPLL Translation Profile 0.0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1200	Priority and enable	[7:6]	Reserved		Reserved.	0x0	R
		[5:1]	Profile 0.0 selection priority		Profile 0 (Profile 0.0) selection priority. This 5-bit bit field contains the priority of the translation profile. This 5-bit bit field allows the user to assign different priorities to different reference inputs. 0x00 is the highest priority, and 0x1F is the lowest priority. The choice of priority level for a given translation profile is important. If the priority difference between the active profile and a valid, but inactive, higher priority profile is >7, the DPLL state machine always switches to the higher priority profile, called revertive reference switching. Therefore, if revertive switching is desired, ensure that the higher priority profile has a priority that is at least 8 greater than a lower priority profile. If the difference between the priorities of the active profile and a valid, but inactive, higher priority profile is 0 to 7, the DPLL state machine remains on the lower priority profile, called nonrevertive reference switching.	0x0	R/W
		0	Enable Profile 0.0		Enable DPLL0 Profile 0.0. Setting this bit to Logic 1 enables DPLL0 Profile 0. If this bit is Logic 0, DPLL0 never uses this profile.	0x0	R/W
0x1201	Source	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Profile 0.0 reference source selection		Profile 0.0 reference source selection. This 5-bit bit field contains the input source of the translation profile.	0x0	R/W
				0	REFA.		
				1	REFAA.		
				2	REFB.		
				3	REFBB.		
				5	Feedback from DPLL1.		
0x1202	Zero delay feedback path	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	External zero delay feed-back path		Profile 0.0 external zero delay feedback path. This 5-bit bit field configures the Profile 0.0 feedback path in hitless external zero delay mode.	0x0	R/W
				0	REFA. Select this mode if REFA is single-ended or in differential mode.		
				1	REFAA.		
				2	REFB. Select this mode if REFB is single-ended or in differential mode.		
				3	REFBB.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:0]	Internal zero delay feedback path		Profile 0.0 internal zero delay feedback path. This 5-bit bit field configures the Profile 0.0 feedback path in hitless internal zero delay mode.	0x0	R/W
				0	OUT0AP. Select this mode if OUT0A is single-ended or in differential mode.		
				1	OUT0AN.		
				2	OUT0BP. Select this mode if OUT0B is single-ended or in differential mode.		
				3	OUT0BN.		
				4	OUT0CP. Select this mode if OUT0C is single-ended or in differential mode.		
				5	OUT0CN.		
0x1203	Feedback mode	7	Profile 0.0 loop filter base		Profile 0.0 loop filter base coefficients. This bit controls the set of loop filter coefficients used for DPLL0 Profile 0.	0x0	R/W
				0	Nominal phase margin (~70°).		
				1	High phase margin (~88.5°). Use this setting for applications that require no more than 0.1 dB of peaking in the DPLL closed-loop transfer function.		
		[6:2]	Reserved		Reserved.	0x0	R/W
		1	Enable Profile 0.0 external zero delay		Enable DPLL0 Profile 0 external zero delay mode. Setting this bit to Logic 1 enables the DPLL0 Profile 0 external zero delay path for hitless mode.	0x0	R/W
		0	Enable Profile 0.0 hitless		Enable Profile 0.0 hitless operation.	0x0	R/W
				0	Selects the default phase buildout mode for DPLL0 Profile 0.		
				1	Enables hitless mode for DPLL0 Profile 0. Enable this bit for zero delay operation.		
0x1204	Loop bandwidth	[7:0]	Profile 0.0 loop bandwidth [7:0]		DPLL0 Profile 0 loop bandwidth. This 32-bit bit field is the DPLL loop bandwidth scaling factor. The default unit for this bit field is microhertz (10^{-6} Hz).	0x0	R/W
0x1205		[7:0]	Profile 0.0 loop bandwidth [15:8]			0x0	R/W
0x1206		[7:0]	Profile 0.0 loop bandwidth [23:16]			0x0	R/W
0x1207		[7:0]	Profile 0.0 loop bandwidth [31:24]			0x0	R/W
0x1208	Hitless feedback divider	[7:0]	Profile 0.0 hitless N-divider [7:0]		Profile 0.0 feedback divider in hitless mode. This 32-bit bit field is the DPLL0 feedback divide ratio while DPLL0 is in hitless mode. The feedback divide ratio is the value stored in this bit field plus one.	0xA0	R/W
0x1209		[7:0]	Profile 0.0 hitless N-divider [15:8]			0xF	R/W
0x120A		[7:0]	Profile 0.0 hitless N-divider [23:16]			0x0	R/W
0x120B		[7:0]	Profile 0.0 hitless N-divider [31:24]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x120C	Buildout feedback divider	[7:0]	Profile 0.0 buildout N-divider [7:0]		DPLL0 Profile 0 buildout N-divide ratio. This 32-bit bit field is the integer portion of the DPLL feedback divide ratio while DPLL0 is in phase buildout mode. It is also referred to as the N-divider in the evaluation software.	0xA0	R/W
0x120D		[7:0]	Profile 0.0 buildout N-divider [15:8]			0xF	R/W
0x120E		[7:0]	Profile 0.0 buildout N-divider [23:16]			0x0	R/W
0x120F		[7:0]	Profile 0.0 buildout N-divider [31:24]			0x0	R/W
0x1210	Buildout feedback fraction	[7:0]	Profile 0.0 buildout fraction [7:0]		DPLL0 Profile 0 feedback divider fraction in buildout mode. This 24-bit bit field is the numerator of the DPLL fractional feedback divider while DPLL0 is in phase buildout mode. It is also referred to as FRAC in the evaluation software.	0x0	R/W
0x1211		[7:0]	Profile 0.0 buildout fraction [15:8]			0x0	R/W
0x1212		[7:0]	Profile 0.0 buildout fraction [23:16]			0x0	R/W
0x1213	Buildout feedback modulus	[7:0]	Profile 0.0 buildout modulus [7:0]		DPLL0 Profile 0 feedback divider modulus in buildout mode. This 24-bit bit field is the denominator of the DPLL fractional feedback divider while DPLL0 is in phase buildout mode. It is also referred to as MOD in the evaluation software.	0x0	R/W
0x1214		[7:0]	Profile 0.0 buildout modulus [15:8]			0x0	R/W
0x1215		[7:0]	Profile 0.0 buildout modulus [23:16]			0x0	R/W
0x1216	Fast lock	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Profile 0.0 fast acquisition excess bandwidth		DPLL0 Profile 0 fast acquisition excess bandwidth. This 4-bit bit field controls the DPLL0 loop bandwidth scaling factor (relative to the programmed DPLL loop bandwidth) while in fast acquisition mode. The DPLL automatically reduces the loop bandwidth by successive factors of 2 while the loop is acquiring. Setting this bit field to 0000b disables the feature.	0x0	R/W
				0000	Feature disabled.		
				0001	2×. The initial loop bandwidth is 2× the programmed value.		
				0010	4×. The initial loop bandwidth is 4× the programmed value.		
				0011	8×. The initial loop bandwidth is 8× the programmed value.		
				0100	16×. The initial loop bandwidth is 16× the programmed value.		
				0101	32×. The initial loop bandwidth is 32× the programmed value.		
				0110	64×. The initial loop bandwidth is 64× the programmed value.		
				0111	128×. The initial loop bandwidth is 128× the programmed value.		
				1000	256×. The initial loop bandwidth is 256× the programmed value.		
				1001	512×. The initial loop bandwidth is 512× the programmed value.		
				1010	1024×. The initial loop bandwidth is 1024× the programmed value.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1217	Fast lock	7	Reserved		Reserved.	0x0	R
		[6:4]	Profile 0.0 fast acquisition timeout		DPLL0 Profile 0 fast acquisition timeout. This 3-bit bit field controls the maximum amount of time that DPLL0 waits to achieve phase lock (without chatter) before reducing the loop bandwidth by a factor of 2 while in fast acquisition mode. This feature prevents the fast acquisition algorithm from stalling in the event that lock is not achieved during the fast acquisition process.	0x0	R/W
				0	1 ms.		
				1	10 ms.		
				10	50 ms.		
				11	100 ms.		
				100	500 ms.		
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Profile 0.0 fast acquisition lock settle time		DPLL0 Profile 0 fast acquisition lock settle time. This 3-bit bit field controls how long DPLL0 must wait after achieving phase lock (without chatter) before reducing the loop bandwidth by a factor of 2 while in fast acquisition mode. If the lock detector chatters, this timer is reset.	0x0	R/W
				0	1 ms.		
				1	10 ms.		
				10	50 ms.		
				11	100 ms.		
				100	500 ms.		
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		

DPLL CHANNEL 1 REGISTERS—REGISTER 0x1400 TO REGISTER 0x142A

Table 63. DPLL Channel 1 Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1400	Freerun tuning word	DPLL1 freerun tuning word [7:0]								0x00	R/W
0x1401		DPLL1 freerun tuning word [15:8]								0x00	R/W
0x1402		DPLL1 freerun tuning word [23:16]								0x00	R/W
0x1403		DPLL1 freerun tuning word [31:24]								0x00	R/W
0x1404		DPLL1 freerun tuning word [39:32]								0x00	R/W
0x1405		Reserved		DPLL1 freerun tuning word [45:40]						0x00	R/W
0x1406	Tuning word clamp	DPLL1 freerun tuning word offset clamp [7:0]								0xFF	R/W
0x1407		DPLL1 freerun tuning word offset clamp [15:8]								0xFF	R/W
0x1408		DPLL1 freerun tuning word offset clamp [23:16]								0xFF	R/W
0x1409	NCO gain	Reserved				DPLL1 NCO gain filter bandwidth				0x00	R/W
0x140A	History accumulation timer	DPLL1 history accumulation timer [7:0]								0x0A	R/W
0x140B		DPLL1 history accumulation timer [15:8]								0x00	R/W
0x140C		DPLL1 history accumulation timer [23:16]								0x00	R/W
0x140D		Reserved				DPLL1 history accumulation timer [27:24]				0x00	R/W
0x140E		Reserved		DPLL1 delay history while not phase slew limiting	DPLL1 delay history frequency lock	DPLL1 delay history phase lock	DPLL1 quick start history	DPLL1 single sample history	DPLL1 persistent history	0x38	R/W
0x140F		Reserved					DPLL1 pause history while phase slew limiting	DPLL1 pause history frequency unlock	DPLL1 pause history phase unlock	0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1410	History accumulation hold off	DPLL1 history hold off time								0x00	R/W
0x1411	Phase slew limit	DPLL1 phase slew limit rate [7:0]								0x00	R/W
0x1412		DPLL1 phase slew limit rate [15:8]								0x00	R/W
0x1413		DPLL1 phase slew limit rate [23:16]								0x00	R/W
0x1414		DPLL1 phase slew limit rate [31:24]								0x06	R/W
0x1415	Phase offset	DPLL1 phase offset [7:0]								0x00	R/W
0x1416		DPLL1 phase offset [15:8]								0x00	R/W
0x1417		DPLL1 phase offset [23:16]								0x00	R/W
0x1418		DPLL1 phase offset [31:24]								0x00	R/W
0x1419		DPLL1 phase offset [39:32]								0x00	R/W
0x141A	Phase temperature compensation polynomial	DPLL1 phase temperature compensation C_1 significand [7:0]								0x00	R/W
0x141B		DPLL1 phase temperature compensation C_1 significand [15:8]								0x00	R/W
0x141C		DPLL1 phase temperature compensation C_1 exponent								0x00	R/W
0x141D		DPLL1 phase temperature compensation C_2 significand [7:0]								0x00	R/W
0x141E		DPLL1 phase temperature compensation C_2 significand [15:8]								0x00	R/W
0x141F		DPLL1 phase temperature compensation C_2 exponent								0x00	R/W
0x1420		DPLL1 phase temperature compensation C_3 significand [7:0]								0x00	R/W
0x1421		DPLL1 phase temperature compensation C_3 significand [15:8]								0x00	R/W
0x1422		DPLL1 phase temperature compensation C_3 exponent								0x00	R/W
0x1423		DPLL1 phase temperature compensation C_4 significand [7:0]								0x00	R/W
0x1424		DPLL1 phase temperature compensation C_4 significand [15:8]								0x00	R/W
0x1425		DPLL1 phase temperature compensation C_4 exponent								0x00	R/W
0x1426		DPLL1 phase temperature compensation C_5 significand [7:0]								0x00	R/W
0x1427		DPLL1 phase temperature compensation C_5 significand [15:8]								0x00	R/W
0x1428		DPLL1 phase temperature compensation C_5 exponent								0x00	R/W
0x1429	Phase adjust filter bandwidth	Reserved					DPLL1 phase temperature compensation filter bandwidth			0x00	R/W
0x142A	Inactive profile	Reserved					DPLL1 inactive profile index			0x00	R/W

Table 64. DPLL Channel 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1400	Freerun tuning word	[7:0]	DPLL1 freerun tuning word [7:0]		DPLL1 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL1 while it is in freerun mode.	0x0	R/W
0x1401		[7:0]	DPLL1 freerun tuning word [15:8]			0x0	R/W
0x1402		[7:0]	DPLL1 freerun tuning word [23:16]			0x0	R/W
0x1403		[7:0]	DPLL1 freerun tuning word [31:24]			0x0	R/W
0x1404		[7:0]	DPLL1 freerun tuning word [39:32]			0x0	R/W
0x1405		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL1 freerun tuning word [45:40]		DPLL1 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL1 while it is in freerun mode.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1406	Tuning word clamp	[7:0]	DPLL1 freerun tuning word offset clamp [7:0]		DPLL1 freerun tuning word offset clamp. This 24-bit bit field sets the DPLL1 tuning word offset clamp, f_{CLAMP}. The formula is f_{CLAMP} = DPLL1 freerun tuning word offset clamp × ($f_S/2^{36}$), where f_S is the system clock frequency.	0xFF	R/W
0x1407		[7:0]	DPLL1 freerun tuning word offset clamp [15:8]			0xFF	R/W
0x1408		[7:0]	DPLL1 freerun tuning word offset clamp [23:16]			0xFF	R/W
0x1409	NCO gain	[7:4]	Reserved		Reserved.	0x0	R/W
		[3:0]	DPLL1 NCO gain filter bandwidth		DPLL1 NCO gain freerun tuning word filter bandwidth. This 4-bit bit field controls the low-pass filter −3 dB cutoff frequency of the DPLL1 NCO.	0x0	R/W
				0x0	250 kHz (maximum).		
				0x1	120 kHz.		
				0x2	62 kHz.		
				0x3	31 kHz.		
				0x4	16 kHz.		
				0x5	7.8 kHz.		
				0x6	3.9 kHz.		
				0x7	1.9 kHz.		
				0x8	970 Hz.		
				0x9	490 Hz.		
				0xA	240 Hz.		
				0xB	120 Hz.		
				0xC	61 Hz.		
				0xD	30 Hz.		
				0xE	15 Hz.		
				0xF	7.6 Hz (minimum).		
0x140A	History accumulation timer	[7:0]	DPLL1 history accumulation timer [7:0]		DPLL1 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the evaluation software. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and behavior is undefined for a timer value of 0x0000.	0xA	R/W
0x140B		[7:0]	DPLL1 history accumulation timer [15:8]			0x0	R/W
0x140C		[7:0]	DPLL1 history accumulation timer [23:16]			0x0	R/W
0x140D		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 history accumulation timer [27:24]		DPLL1 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the evaluation software. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and behavior is undefined for a timer value of 0x0000.	0x0	R/W
0x140E		[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 delay history while not phase slew limiting		DPLL1 delay history while not phase slew limiting. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL1 phase slew limiter is inactive. At that point, the tuning word averaging is further delayed by the value in the DPLL1 history hold off time. This bit ensures that holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase slew limiter.	0x1	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	DPLL1 delay history frequency lock		DPLL1 delay history until frequency lock. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL1 is frequency locked. At that point, the tuning word averaging is further delayed by the value in the DPLL1 history hold off time. This bit is intended to ensure that holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the frequency lock detector.	0x1	R/W
		3	DPLL1 delay history phase lock		DPLL1 delay history until phase lock. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL1 is phase locked. At that point, the tuning word averaging is further delayed by the value in the DPLL1 history hold off time. This bit is intended to ensure that holdover history averaging begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase lock detector.	0x1	R/W
		2	DPLL1 quick start history		DPLL1 quick start history. Setting this bit to Logic 1 allows the DPLL1 tuning word history to be available in 1/4 of the time specified in the DPLL1 history accumulation timer. This bit is intended to ensure that there is sufficient holdover history when the DPLL has been locked to a reference for a short period.	0x0	R/W
		1	DPLL1 single sample history		DPLL1 single sample history. Setting this bit to Logic 1 allows DPLL1 to use the most recent tuning word for holdover in the event that the tuning word history is not available. This bit can be used in conjunction with the DPLL1 quick start history bit in this register. This bit is intended to ensure that there is a minimal holdover history available when the DPLL has been locked to a reference for a short period.	0x0	R/W
		0	DPLL1 persistent history		DPLL1 persistent history. Setting this bit to Logic 1 allows the DPLL1 tuning word history to not be reset if there is an interruption in the tuning word averaging. This bit is intended to ensure that there is sufficient holdover history when the DPLL has been locked to a reference for a short period. When this bit is Logic 0, and the DPLL exits holdover and reacquires a reference input, the history accumulation resets.	0x0	R/W
0x140F		[7:3]	Reserved		Reserved.	0x0	R
		2	DPLL1 pause history while phase slew limiting		DPLL1 pause history while phase slew limiting. Setting this bit to Logic 1 pauses the tuning word history averaging when DPLL1 is phase slewing. The tuning word history is reset when the DPLL regains phase lock if the persistent history bit is Logic 0. This bit is intended to ensure that tuning word history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase slewing.	0x0	R/W
		1	DPLL1 pause history frequency unlock		DPLL1 pause history while frequency unlock. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when DPLL1 is frequency unlocked. The holdover history is reset when the DPLL regains frequency lock if the persistent history bit is Logic 0. This bit is intended to ensure that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of frequency lock status.	0x0	R/W
		0	DPLL1 pause history phase unlock		DPLL1 pause history while phase unlock. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when DPLL1 phase slew limiter is active. The holdover history is reset when the DPLL is no longer phase slew limited if the DPLL1 persistent history bit is Logic 0. This bit is intended to ensure that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase lock status.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1410	History accumulation hold off	[7:0]	DPLL1 history hold off time		DPLL1 history hold off time. This 8-bit bit field is the amount of time (in milliseconds) that the DPLL tuning word history accumulation is delayed. Hold off is disabled if this bit field is 0x00.	0x0	R/W
0x1411	Phase slew limit	[7:0]	DPLL1 phase slew limit rate [7:0]		DPLL1 phase slew limit rate. This 32-bit bit field is the DPLL1 phase slew limit rate (in picoseconds/second). It is referred to as t_{OFST} in the evaluation software.	0x0	R/W
0x1412		[7:0]	DPLL1 phase slew limit rate [15:8]			0x0	R/W
0x1413		[7:0]	DPLL1 phase slew limit rate [23:16]			0x0	R/W
0x1414		[7:0]	DPLL1 phase slew limit rate [31:24]			0x6	R/W
0x1415	Phase offset	[7:0]	DPLL1 phase offset [7:0]		DPLL1 closed-loop phase offset. This signed, 40-bit bit field is the DPLL1 closed-loop phase offset (in picoseconds). It is referred to as t_{OFST} in the evaluation software	0x0	R/W
0x1416		[7:0]	DPLL1 phase offset [15:8]			0x0	R/W
0x1417		[7:0]	DPLL1 phase offset [23:16]			0x0	R/W
0x1418		[7:0]	DPLL1 phase offset [31:24]			0x0	R/W
0x1419		[7:0]	DPLL1 phase offset [39:32]			0x0	R/W
0x141A	Phase temperature compensation polynomial	[7:0]	DPLL1 phase temperature compensation C_1 significand [7:0]		DPLL1 temperature compensation C_1 significand. This 16-bit bit field is the significand for the C_1 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x141B		[7:0]	DPLL1 phase temperature compensation C_1 significand [15:8]			0x0	R/W
0x141C		[7:0]	DPLL1 phase temperature compensation C_1 exponent		DPLL1 temperature compensation C_1 exponent. This 8-bit bit field is the exponent for the C_1 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x141D		[7:0]	DPLL1 phase temperature compensation C_2 significand [7:0]		DPLL1 temperature compensation C_2 significand. This 16-bit bit field is the significand for the C_2 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x141E		[7:0]	DPLL1 phase temperature compensation C_2 significand [15:8]			0x0	R/W
0x141F		[7:0]	DPLL1 phase temperature compensation C_2 exponent		DPLL1 temperature compensation C_2 exponent. This 8-bit bit field is the exponent for the C_2 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1420		[7:0]	DPLL1 phase temperature compensation C_3 significand [7:0]		DPLL1 temperature compensation C_3 significand. This 16-bit bit field is the significand for the C_3 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1421		[7:0]	DPLL1 phase temperature compensation C_3 significand [15:8]			0x0	R/W
0x1422		[7:0]	DPLL1 phase temperature compensation C_3 exponent		DPLL1 temperature compensation C_3 exponent. This 8-bit bit field is the exponent for the C_3 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1423		[7:0]	DPLL1 phase temperature compensation C_4 significand [7:0]		DPLL1 temperature compensation C_4 significand. This 16-bit bit field is the significand for the C_4 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1424		[7:0]	DPLL1 phase temperature compensation C_4 significand [15:8]			0x0	R/W
0x1425		[7:0]	DPLL1 phase temperature compensation C_4 exponent		DPLL1 temperature compensation C_4 exponent. This 8-bit bit field is the exponent for the C_4 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1426		[7:0]	DPLL1 phase temperature compensation C_5 significand [7:0]		DPLL1 temperature compensation C_5 significand. This 16-bit bit field is the significand for the C_5 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1427		[7:0]	DPLL1 phase temperature compensation C_5 significand [15:8]			0x0	R/W
0x1428		[7:0]	DPLL1 phase temperature compensation C_5 exponent		DPLL1 temperature compensation C_5 exponent. This 8-bit bit field is the exponent for the C_5 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1429	Phase adjust filter bandwidth	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL1 phase temperature compensation filter bandwidth		DPLL1 temperature compensation low-pass filter bandwidth. This 3-bit bit field controls the low-pass filter −3 dB cutoff frequency of the DPLL1 delay compensation block.	0x0	R/W
				0x0	240 Hz (maximum).		
				0x1	120 Hz.		
				0x2	60 Hz.		
				0x3	30 Hz.		
				0x4	15 Hz.		
				0x5	7.6 Hz.		
				0x6	3.8 Hz.		
				0x7	1.9 Hz (minimum).		
0x142A	Inactive profile	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL1 inactive profile index		DPLL1 inactive profile index. The inactive profile index is used while DPLL1 is in holdover to retain the exact DPLL configuration, including the desired input/output phase relationship.	0x0	R/W

DISTRIBUTION GENERAL 1 REGISTERS—REGISTER 0x14D2 TO REGISTER 0x14DC

Table 65. Distribution General 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x14D2	N-shot gaps	N-shot gap								0x00	R/W
0x14D3	N-shot request	Reserved	N-shot request mode	N-shot						0x00	R/W
0x14D4	N-shot enable	Enable Q1BB PRBS	Enable Q1BB N-shot	Enable Q1B PRBS	Enable Q1B N-shot	Enable Q1AA PRBS	Enable Q1AA N-shot	Enable Q1A PRBS	Enable Q1A N-shot	0x00	R/W
0x14D6	N-shot retime	Reserved							Enable N-shot retime	0x00	R/W
0x14D7	Driver A configuration	Reserved		Bypass mute retiming Channel A	OUT1A driver mode		OUT1A driver current		Enable OUT1A HCSL	0x01	R/W
0x14D8	Driver B configuration	Reserved		Bypass mute retiming Channel B	OUT1B driver mode		OUT1B driver current		Enable OUT1B HCSL	0x01	R/W
0x14DA	Secondary clock path	Reserved					Enable SYSCLK Q1B	Enable SYSCLK Q1A	Enable SYSCLK sync mask	0x00	R/W
0x14DB	Sync control	Reserved					Enable DPLL1 reference sync	Autosync mode		0x00	R/W
0x14DC	Automute control	Mask OUT1CC autounmute	Mask OUT1C autounmute	Mask OUT1BB autounmute	Mask OUT1B autounmute	Mask OUT1AA autounmute	Mask OUT1A autounmute	DPLL1 autounmute mode		0x00	R/W

Table 66. Distribution General 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x14D2	N-shot gaps	[7:0]	N-shot gap		N-shot gap. This unsigned, 8-bit bit field contains the length (measured in Q divider output cycles) of the gap in a JESD204B N-shot pattern generation.	0x0	R/W
0x14D3	N-shot request	7	Reserved		Reserved.	0x0	R
		6	N-shot request mode		Channel 0 N-shot request mode. Logic 0: the N-shot generators operate in burst mode, and the rising edge of the trigger signal initiates the burst. Logic 1: the N-shot generators operate in period gapped mode. In this mode, N-shot bursts occur as long as the trigger is in a Logic 1 state; for this reason, it is referred to as a level sensitive trigger mode.	0x0	R/W
		[5:0]	N-shot		Number of clock pulses in an N-shot burst. This unsigned, 6-bit bit field contains the number of clock cycles in an N-shot burst.	0x0	R/W
0x14D4	N-shot enable	7	Enable Q1BB PRBS		Q1BB JESD204B PRBS Enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at divider output rate.	0x0	R/W
		6	Enable Q1BB N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
		5	Enable Q1B PRBS		Q1B JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	Enable Q1B N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
		3	Enable Q1AA PRBS		Q1AA JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		2	Enable Q1AA N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
		1	Enable Q1A PRBS		Q1A JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		0	Enable Q1A N-shot		N-shot enable. Logic 0: JESD204B N-shot mode disabled. Logic 1: JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.	0x0	R/W
0x14D6	N-shot retime	[7:1]	Reserved		Reserved.	0x0	R
		0	Enable N-shot retime		Enable N-shot retiming. Logic 0: Mx pins or registers (user selectable) provide the JESD204B N-shot retiming source. Logic 1: the N short retiming block provides the JESD204B N-shot retiming source.	0x0	R/W
0x14D7	Driver A configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel A		Removes retiming from Channel A mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function, and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT1A driver mode	0 1 10	Selects single-ended or differential output mode. Differential output. Divider Q0A determines the divide ratio. Dual-, single-ended output driven by Divider Q0A. Divider Q0A determines the divide ratio. Dual-, single-ended output driven by separate Q dividers. Both Divider Q0A and Divider Q0AA are enabled, although it is recommended that they have the same divide ratio.	0x0	R/W
		[2:1]	OUT1A driver current	0 1 10	Output driver current. This current setting applies to both the normal and complementary output pins. 7.5 mA. 12.5 mA. 15 mA.	0x0	R/W
		0	Enable OUT1A HCSL		Selects HCSL or CML mode. Logic 0: CML mode. An external pull-up resistor is required. Logic 1: HCSL mode. An external pull-down resistor is required.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x14D8	Driver B configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel B		Removes retiming from Channel B mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT1B driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q1B determines the divide ratio.		
				1	Dual-, single-ended output driven by Divider Q1A. Divider Q1B determines the divide ratio.		
				10	Dual-, single-ended output driven by separate Q dividers. Both Divider Q1B and Divider Q1BB are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT1B driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT1B HCSL		Selects HCSL or CML mode. Logic 0: CML mode. An external pull-up resistor is required. Logic 1: HCSL mode. An external pull-down resistor is required.	0x0	R/W
0x14DA	Secondary clock path	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable SYSCLK Q1B		Enable SYSCLK to Divider Q1B. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q1B.	0x0	R/W
		1	Enable SYSCLK Q1A		Enable SYSCLK to Divider Q1A. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q1A.	0x0	R/W
		0	Enable SYSCLK sync mask		Enable SYSCLK sync mask. Setting this bit to Logic 1 ensures that no sync events occur on outputs that are assigned to outputting the SYSCLK. This purpose of this feature is to ensure that no runt pulses or stalled clocks occur when a SYSCLK output clocks a microprocessor. Set this bit to Logic 1 only when the SYSCLK is fully configured and stable, because runt pulses can occur while configuring the SYSCLK.	0x0	R/W
0x14DB	Sync control	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable DPLL1 reference sync		DPLL1 reference sync enable. Setting this bit to Logic 1 enables automatic reference synchronization on DPLL0.	0x0	R/W
		[1:0]	Autosync mode		Autosync mode. This bit field controls when the clock distribution block receives a synchronization event. The output drivers do not toggle until there is a synchronization event.	0x0	R/W
				0	Manual sync. Automatic output synchronization disabled. In this mode, the user must issue a clock distribution synchronization command manually.		
				1	Immediate. Output synchronization occurs immediately after APLL lock.		
				10	DPLL phase lock. Output synchronization occurs when the DPLL phase locks.		
				11	DPLL frequency lock. Output synchronization occurs when the DPLL frequency locks.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x14DC	Automute control	7	Mask OUT1CC autounmute		Mask OUT1CC autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		6	Mask OUT1C autounmute		Mask OUT1C autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		5	Mask OUT1BB autounmute		Mask OUT1BB autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		4	Mask OUT1B autounmute		Mask OUT1B autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		3	Mask OUT1AA autounmute		Mask OUT1AA autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		2	Mask OUT1A autounmute		Mask OUT1A autounmute. Logic 0: normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode. Logic 1: the automatic unmuting conditions are ignored and the driver is unmuted immediately.	0x0	R/W
		[1:0]	DPLL1 autounmute mode		DPLL1 autounmute mode. This bit field controls the point at which the output drivers start to toggle during acquisition while DPLL1 is in hitless mode.	0x0	R/W
				0	Disabled. Automatic unmuting is disabled and the output driver starts toggling immediately.		
				1	Hitless acquisition. Automatic driver unmuting occurs upon activation of a hitless profile.		
				10	Phase lock detect (PLD) (hitless mode only). Automatic driver unmuting occurs when phase lock is detected and the DPLL is in hitless mode.		
				11	Frequency lock detect (FLD) (hitless mode only). Automatic driver unmuting occurs when frequency lock is detected and the DPLL is in hitless mode.		

APLL CHANNEL 1 REGISTERS—REGISTER 0x1480 TO REGISTER 0x1483

Table 67. APLL Channel 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1480	Charge pump current	Enable APLL1 manual charge pump current	APLL1 manual charge pump current							0x90	R/W
0x1481	M1 divider	APLL1 M1 feedback divider								0x00	R/W
0x1482	Loop filter control	APLL1 loop filter zero resistor (R1)			APLL1 loop filter pole capacitor (C2)			APLL1 loop filter second pole resistor (R3)		0xE0	R/W
0x1483	DC offset current	Reserved				APLL1 dc offset current direction	APLL1 dc offset current value		Enable APLL1 dc offset current	0x03	R/W

Table 68. APLL Channel 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1480	Charge pump current	7	Enable APLL1 manual charge pump current		Enables manual control of the APLL1 charge pump current.	0x0	R/W
				0	Disable manual charge pump current control. Disables manual control of the APLL1 charge pump current.		
				1	Enable manual charge pump current control. Enables manual control of the APLL1 charge pump current.		
		[6:0]	APLL1 manual charge pump current		APLL1 manual charge pump current. LSB = 3.5 µA. The user must set the enable manual charge pump current control bit in this register for this setting to be enabled.	0x0	R/W
				0000001b	1 × LSB.		
				0000010b	2 × LSB.		
				1111111b	127 × LSB.		
0x1481	M1 divider	[7:0]	APLL1 M1 feedback divider		APLL1 multiplication ratio. APLL1 M1 feedback divide ratio. Allowable values are 14 to 255.	0x0	R/W
0x1482	Loop filter control	[7:5]	APLL1 loop filter zero resistor (R1)		Loop Filter R1. APLL1 Loop Filter R1 (zero resistor) value.	0x0	R/W
				000	0 Ω (short).		
				001	250 Ω.		
				010	500 Ω.		
				011	750 Ω.		
				100	1.00 kΩ.		
				101	1.25 kΩ.		
				110	1.50 kΩ.		
				111	1.75 kΩ.		
		[4:2]	APLL1 loop filter pole capacitor (C2)		Loop Filter C2. APLL1 Loop Filter C2 (pole capacitor) value.	0x0	R/W
				000	8 pF.		
				001	24 pF.		
				010	40 pF.		
				011	56 pF.		
				100	72 pF.		
				101	88 pF.		
				110	104 pF.		
				111	120 pF.		
		[1:0]	APLL1 loop filter second pole resistor (R3)		Loop Filter R3. APLL1 Loop Filter R3 (second pole resistor) value.	0x0	R/W
				00	200 Ω.		
				01	250 Ω.		
				10	333 Ω.		
				11	500 Ω.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1483	DC offset current	[7:4]	Reserved		Reserved.	0x0	R
		3	APLL1 dc offset current direction		DC offset current direction. This bit sets the direction of the APLL1 dc offset current.	0x0	R/W
				0	Up. DC offset current offset is positive.		
				1	Down. DC offset current offset is negative.		
		[2:1]	APLL1 dc offset current value		DC offset current. Magnitude of the APLL1 charge pump dc offset current value.	0x0	R/W
				00	50% offset current. Offset current is 50% of the programmed APLL1 charge pump current (default).		
				01	25% offset current. Offset current is 25% of the programmed APLL1 charge pump current.		
				10	12.5% offset current. Offset current is 12.5% of the programmed APLL1 charge pump current.		
				11	6.25% offset current. Offset current is 6.25% of the programmed APLL1 charge pump current.		
		0	Enable APLL1 dc offset current		DC offset current enable. Setting this bit enables the APLL1 dc offset current.	0x0	R/W

DISTRIBUTION DIVIDER Q1A REGISTERS—REGISTER 0x1500 TO REGISTER 0x1508

Table 69. Distribution Divider Q1A Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1500	Divider ratio	Q1A divider ratio [7:0]								0x00	R/W
0x1501		Q1A divider ratio [15:8]								0x00	R/W
0x1502		Q1A divider ratio [23:16]								0x00	R/W
0x1503		Q1A divider ratio [31:24]								0x00	R/W
0x1504	Phase offset	Q1A phase [7:0]								0x00	R/W
0x1505		Q1A phase [15:8]								0x00	R/W
0x1506		Q1A phase [23:16]								0x00	R/W
0x1507		Q1A phase [31:24]								0x00	R/W
0x1508	Phase slew configuration	Reserved	Q1A phase [32]	Enable Q1A half divide	Enable Q1A pulse width control	Q1A phase slew mode	Maximum phase slew step			0x07	R/W

Table 70. Distribution Divider Q1AA Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1509 to 0x1511	These registers mimic the Distribution Divider Q1A registers (Register 0x1500 through Register 0x1508), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 71. Distribution Divider Q1B Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x1512 to 0x151A	These registers mimic the Distribution Divider Q1A registers (Register 0x1500 through Register 0x1508), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 72. Distribution Divider Q1BB Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RW
0x151B to 0x1523	These registers mimic the Distribution Divider Q1A registers (Register 0x1500 through Register 0x1508), but the register addresses are offset by 0x0009. All default values are identical.								R/W

Table 73. Distribution Divider Q1A Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1500	Divider ratio	[7:0]	Q1A divider ratio [7:0]		Q1A divide ratio. This 32-bit bit field is the divide ratio for the Q1A divider. The default value of 0x00000000 equals a divide ratio of 1, which is invalid because it results in an output frequency that exceeds the maximum for the AD9542.	0x0	R/W
0x1501		[7:0]	Q1A divider ratio [15:8]			0x0	R/W
0x1502		[7:0]	Q1A divider ratio [23:16]			0x0	R/W
0x1503		[7:0]	Q1A divider ratio [31:24]			0x0	R/W
0x1504	Phase offset	[7:0]	Q1A phase [7:0]		Q1A phase control. This bit field controls the Q1A phase in two ways: the bit field sets the initial phase offset after divider sync (reset) and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q1A distribution input clock half cycles.	0x0	R/W
0x1505		[7:0]	Q1A phase [15:8]			0x0	R/W
0x1506		[7:0]	Q1A phase [23:16]			0x0	R/W
0x1507		[7:0]	Q1A phase [31:24]			0x0	R/W
0x1508	Phase slew configuration	7	Reserved		Reserved.	0x0	R
		6	Q1A phase [32]		Q1A phase control. This bit field controls the Q1A phase in two ways: the bit field sets the initial phase offset after a divider sync (reset); and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q1A distribution input clock half cycles.	0x0	R/W
		5	Enable Q1A half divide		Enable Q1A half divide. Setting this bit to Logic 1 adds 0.5 to the divide ratio programmed into the corresponding 32-bit Q1A divide ratio bit field.	0x0	R/W
		4	Enable Q1A pulse width control		Enable pulse width control mode. This bit controls whether the Q1A phase bit field adjusts the phase offset or the pulse width.	0x0	R/W
				0	The Q1A phase bit field controls the phase offset.		
				1	The Q1A phase bit field controls the pulse width.		
		3	Q1A phase slew mode		Q1A phase slew mode.	0x0	R/W
				0	Lag only (always slows down frequency). The phase controller slews the phase in the direction that always reduces the output frequency.		
				1	Lead or lag—quickest is automatically calculated. The phase controller slews the phase in the direction requiring the fewest steps, which means that the output frequency can increase or decrease during a stepwise phase adjustment sequence.		
		[2:0]	Maximum phase slew step		Maximum phase slew step.	0x0	R/W
				0	Maximum phase slew step. This 3-bit bit field controls the maximum allowable phase step while adjusting the phase in the Q1A divider. Each step occurs every output clock cycle.		
				1	One input clock half cycle. The phase slew step size is half of the Q divider input period.		
				10	Two input clock half cycles. The maximum phase slew step size equals the Q divider input period.		
				11	1°. The maximum phase slew step size equals 1/32 (~11.25°) of the output clock period.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				100	23°. The maximum phase slew step size equals 1/16 (~22.5°) of the output clock period.		
				101	45°. The maximum phase slew step size equals 1/8 (~45°) of the output clock period.		
				110	90°. The maximum phase slew step size equals 1/4 (~90°) of the output clock period.		
				111	180°. The maximum phase slew step size equals half (~180°) of the output clock period.		

DPLL TRANSLATION PROFILE 1.0 REGISTERS—REGISTER 0x1600 TO REGISTER 0x1617

Table 74. DPLL Translation Profile 1.0 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1600	Priority and enable	Reserved		Profile 1.0 selection priority					Enable Profile 1.0	0x00	R/W
0x1601	Source	Reserved			Profile 1.0 reference source selection					0x00	R/W
0x1602	Zero delay feedback path	Reserved			External/internal zero delay feedback path					0x00	R/W
0x1603	Feedback mode	Profile 1.0 loop filter base	Reserved					Enable Profile 1.0 external zero delay	Enable Profile 1.0 hitless	0x00	R/W
0x1604	Loop bandwidth	Profile 1.0 loop bandwidth [7:0]								0x00	R/W
0x1605		Profile 1.0 loop bandwidth [15:8]								0x00	R/W
0x1606		Profile 1.0 loop bandwidth [23:16]								0x00	R/W
0x1607		Profile 1.0 loop bandwidth [31:24]								0x00	R/W
0x1608	Hitless feedback divider	Profile 1.0 hitless N-divider [7:0]								0xA0	R/W
0x1609		Profile 1.0 hitless N-divider [15:8]								0x0F	R/W
0x160A		Profile 1.0 hitless N-divider [23:16]								0x00	R/W
0x160B		Profile 1.0 hitless N-divider [31:24]								0x00	R/W
0x160C	Buildout feedback divider	Profile 1.0 buildout N-divider [7:0]								0xA0	R/W
0x160D		Profile 1.0 buildout N-divider [15:8]								0x0F	R/W
0x160E		Profile 1.0 buildout N-divider [23:16]								0x00	R/W
0x160F		Profile 1.0 buildout N-divider [31:24]								0x00	R/W
0x1610	Buildout feedback fraction	Profile 1.0 buildout fraction [7:0]								0x00	R/W
0x1611		Profile 1.0 buildout fraction [15:8]								0x00	R/W
0x1612		Profile 1.0 buildout fraction [23:16]								0x00	R/W
0x1613	Buildout feedback modulus	Profile 1.0 buildout modulus [7:0]								0x00	R/W
0x1614		Profile 1.0 buildout modulus [15:8]								0x00	R/W
0x1615		Profile 1.0 buildout modulus [23:16]								0x00	R/W
0x1616	Fast lock	Reserved				Profile 1.0 fast acquisition excess bandwidth				0x00	R/W
0x1617		Reserved	Profile 1.0 fast acquisition timeout			Reserved	Profile 1.0 fast acquisition lock settle time			0x00	R/W

Table 75. DPLL Translation Profile 1.1 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1620 to 0x1637	These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 76. DPLL Translation Profile 1.2 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1640 to 0x1657	These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 77. DPLL Translation Profile 1.3 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1660 to 0x1677	These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 78. DPLL Translation Profile 1.4 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1680 to 0x1697	These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 79. DPLL Translation Profile 1.5 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x16A0 to 0x16B7	These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 80. DPLL Translation Profile 1.0 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1600	Priority and enable	[7:6]	Reserved		Reserved.	0x0	R
		[5:1]	Profile 1.0 selection priority		Profile 1.0 selection priority. This 5-bit bit field contains the priority of the translation profile. This 5-bit bit field allows the user to assign different priorities to different reference inputs. 0x00 is the highest priority, and 0x1F is the lowest priority. The choice of priority level for a given translation profile is important. If the priority difference between the active profile and a valid, but inactive, higher priority profile is >7, the DPLL state machine always switches to the higher priority profile, called revertive reference switching. Therefore, if revertive switching is desired, ensure the higher priority profile has a priority that is at least 8 greater than a lower priority profile. If the difference between the priorities of the active profile and a valid, but inactive, higher priority profile is 0 to 7, the DPLL state machine remains on the lower priority profile, called nonrevertive reference switching.	0x0	R/W
		0	Enable Profile 1.0		Enable DPLL1 Profile 0 (Profile 1.0). Setting this bit to Logic 1 enables DPLL1 Profile 0. If this bit is Logic 0, DPLL1 never uses this profile.	0x0	R/W
0x1601	Source	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Profile 1.0 reference source selection		Profile 1.0 reference source selection. This 5-bit bit field contains the input source of the translation profile.	0x0	R/W
				0	REFA.		
				1	REFAA.		
				2	REFB.		
				3	REFBB.		
				4	Feedback from DPLL1.		
0x1602	Zero delay feedback path	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	External zero delay feedback path		Profile 1.0 external zero delay feedback path. This 5-bit bit field configures the Profile1.0 feedback path in hitless external zero delay mode. Setting the Enable Profile 1.0 external zero delay bit to Logic 1 enables external zero delay mode for Prolife 1.0.	0x0	R/W
				0	REFA. Select this mode if REFA is single-ended or in differential mode.		
				1	REFAA.		
				2	REFB. Select this mode if REFB is single-ended or in differential mode.		
				3	REFBB.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:0]	Internal zero delay feedback path		Profile 1.0 internal zero delay feedback path. This 5-bit bit field configures the Profile 1.0 feedback path in hitless internal zero delay mode. Setting the enable Profile 1.0 internal zero delay bit to Logic 1 enables internal zero delay mode for Prolife 1.0.	0x0	R/W
				0	OUT1AP. Select this mode if OUT1A is single-ended or in differential mode.		
				1	OUT1AN.		
				2	OUT1BP. Select this mode if OUT1B is single-ended or in differential mode.		
				3	OUT1BN.		
0x1603	Feedback mode	7	Profile 1.0 loop filter base		Profile 1.0 loop filter base coefficients. This bit controls which set of loop filter coefficients is used for DPLL1 Profile 0.	0x0	R/W
				0	Nominal phase margin (~70°).		
				1	High phase margin (~88.5°). Use this setting for applications that require no more than 0.1 dB of peaking in the DPLL closed-loop transfer function.		
		[6:2]	Reserved		Reserved.	0x0	R/W
		1	Enable Profile 1.0 external zero delay		Enable DPLL1 Profile 0 external zero delay mode. Setting this bit to Logic 1 enables the DPLL1 Profile 0 external zero delay path for hitless mode.	0x0	R/W
		0	Enable Profile 1.0 hitless		Enable Profile 1.0 hitless operation.	0x0	R/W
				0	Selects the default phase buildout mode for the DPLL1 Profile 0		
				1	Enables hitless mode for DPLL1 Profile 0. This bit must also be enabled for zero delay operation.		
0x1604	Loop band-width	[7:0]	Profile 1.0 loop bandwidth [7:0]		DPLL1 Profile 0 loop bandwidth. This 32-bit bit field is the DPLL loop bandwidth scaling factor. The default units for this bit field are microseconds (10^{-6} sec).	0x0	R/W
0x1605		[7:0]	Profile 1.0 loop bandwidth [15:8]			0x0	R/W
0x1606		[7:0]	Profile 1.0 loop bandwidth [23:16]			0x0	R/W
0x1607		[7:0]	Profile 1.0 loop bandwidth [31:24]			0x0	R/W
0x1608	Hitless feedback divider	[7:0]	Profile 1.0 hitless N-divider [7:0]		Profile 1.0 feedback divider in hitless mode. This 32-bit bit field is the DPLL1 feedback divide ratio while DPLL1 is in hitless mode. The feedback divide ratio is the value stored in this bit field plus one.	0xA0	R/W
0x1609		[7:0]	Profile 1.0 hitless N-divider [15:8]			0xF	R/W
0x160A		[7:0]	Profile 1.0 hitless N-divider [23:16]			0x0	R/W
0x160B		[7:0]	Profile 1.0 hitless N-divider [31:24]			0x0	R/W
0x160C	Buildout feedback divider	[7:0]	Profile 1.0 buildout N-divider [7:0]		DPLL1 Profile 0 buildout N-divide ratio. This 32-bit bit field is the integer portion of the DPLL feedback divide ratio while DPLL1 is in phase buildout mode. It is also referred to as the N-divider in the data sheet.	0xA0	R/W
0x160D		[7:0]	Profile 1.0 buildout N-divider [15:8]			0xF	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x160E		[7:0]	Profile 1.0 buildout N-divider [23:16]			0x0	R/W
0x160F		[7:0]	Profile 1.0 buildout N-divider [31:24]			0x0	R/W
0x1610	Buildout feedback fraction	[7:0]	Profile 1.0 buildout fraction [7:0]		DPLL1 Profile 0 feedback divider fraction in buildout mode. This 24-bit bit field is the numerator of the DPLL fractional feedback divider while DPLL1 is in phase buildout mode. It is also referred to as FRAC in the evaluation software.	0x0	R/W
0x1611		[7:0]	Profile 1.0 buildout fraction [15:8]			0x0	R/W
0x1612		[7:0]	Profile 1.0 buildout fraction [23:16]			0x0	R/W
0x1613	Buildout feedback modulus	[7:0]	Profile 1.0 buildout modulus [7:0]		DPLL1 Profile 0 feedback divider modulus in buildout mode. This 24-bit bit field is the denominator of the DPLL fractional feedback divider while DPLL1 is in phase buildout mode. It is also referred to as MOD in the evaluation software.	0x0	R/W
0x1614		[7:0]	Profile 1.0 buildout modulus [15:8]			0x0	R/W
0x1615		[7:0]	Profile 1.0 buildout modulus [23:16]			0x0	R/W
0x1616	Fast lock	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Profile 1.0 fast acquisition excess bandwidth		DPLL1 Profile 0 fast acquisition excess bandwidth. This 4-bit bit field controls the DPLL1 loop bandwidth scaling factor (relative to the programmed DPLL loop bandwidth) while in fast acquisition mode. The DPLL automatically reduces its loop bandwidth by successive factors of 2 while the loop is acquiring. Setting this bit field to 0000b disables the feature.	0x0	R/W
				0000	Feature disabled.		
				0001	2×. The initial loop bandwidth is 2× the programmed value.		
				0010	4×. The initial loop bandwidth is 4× the programmed value.		
				0011	8×. The initial loop bandwidth is 8× the programmed value.		
				0100	16×. The initial loop bandwidth is 16× the programmed value.		
				0101	32×. The initial loop bandwidth is 32× the programmed value.		
				0110	64×. The initial loop bandwidth is 64× the programmed value.		
				0111	128×. The initial loop bandwidth is 128× the programmed value.		
				1000	256×. The initial loop bandwidth is 256× the programmed value.		
				1001	512×. The initial loop bandwidth is 512× the programmed value.		
				1010	1024×. The initial loop bandwidth is 1024× the programmed value.		
0x1617	Fast lock	7	Reserved		Reserved.	0x0	R
		[6:4]	Profile 1.0 fast acquisition timeout		DPLL1 Profile 0 fast acquisition timeout. This 3-bit bit field controls the maximum amount of time that DPLL1 waits to achieve phase lock (without chatter) before reducing the loop bandwidth by a factor of 2 while in fast acquisition mode. This feature prevents the fast acquisition algorithm from stalling in the event that lock is not achieved during the fast acquisition process.	0x0	R/W
				0	1 ms.		
				1	10 ms.		
				10	50 ms.		
				11	100 ms.		
				100	500 ms.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Profile 1.0 fast acquisition lock settle time		DPLL1 Profile 0 fast acquisition lock settle time. This 3-bit bit field controls how long DPLL1 must wait after achieving phase lock (without chatter) before reducing the loop bandwidth by a factor of 2 while in fast acquisition mode. If the lock detector chatters, this timer is reset.	0x0	R/W
				000	1 ms.		
				001	10 ms.		
				010	50 ms.		
				011	100 ms.		
				100	500 ms.		
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		

OPERATIONAL CONTROLS GENERAL REGISTERS—REGISTER 0x2000 TO REGISTER 0x2005

Table 81. Operational Controls General Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2000	Global	Reserved				Sync all	Calibrate SYSCLK	Calibrate all	Power down all	0x00	R/W
0x2001	Power-down reference	Reserved				Power-down REFBB	Power-down REFB	Power-down REFAA	Power-down REFA	0x00	R/W
0x2002	Timeout reference	Reserved				Timeout Reference Monitor BB	Timeout Reference Monitor B	Timeout Reference Monitor AA	Timeout Reference Monitor A	0x00	R/W
0x2003	Fault reference	Reserved				Fault REFBB	Fault REFB	Fault REFAA	Fault REFA	0x00	R/W
0x2004	Bypass reference monitor	Reserved				Bypass Reference Monitor BB	Bypass Reference Monitor B	Bypass Reference Monitor AA	Bypass Reference Monitor A	0x00	R/W
0x2005	Clear IRQ	Clear watchdog timer	Reserved			IRQ clear PLL1	IRQ clear PLL0	IRQ clear common	IRQ clear all	0x00	R/W

Table 82. Operational Controls General Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2000	Global	[7:4]	Reserved		Reserved.	0x0	R/W
		3	Sync all		Synchronize all distribution dividers. The proper sequence for synchronizing the output dividers manually is to set this bit to Logic 1, write 0x01 to the IO_UPDATE register, set this bit to Logic 0, and write 0x01 to the IO_UPDATE register a second time. Logic 0: normal operation. Logic 1: hold all distribution dividers in reset with the divider outputs static.	0x0	R/W
		2	Calibrate SYSCLK		Calibrate system clock PLL. Setting this bit to Logic 1 calibrates the system clock PLL. Because calibration occurs on the Logic 0 to Logic 1 transition, it is recommended to clear this bit after setting it. The system clock PLL must be calibrated during initial programming of the AD9542. Because the calibration signal is a logical OR of this bit and the calibrate all bit, this calibration bit is ineffective if the calibrate all bit is Logic 1 at the time this bit is set to Logic 1.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	Calibrate all		Calibrate all PLLs. Setting this bit to Logic 1 calibrates all PLLs, including the system clock PLL. Because calibration occurs on the Logic 0 to Logic 1 transition, it is recommended to clear this bit after setting it; this recommendation applies to all calibration bits on the AD9542. The system clock PLL and both APLLs must be calibrated during initial programming of the AD9542 for both PLL0 and PLL1 to function normally.	0x0	R/W
		0	Power down all		Power down entire chip. Setting this bit to Logic 1 puts the entire chip into a lower power mode. The serial port is still active in this state.	0x0	R/W
0x2001	Power-down reference	[7:4]	Reserved		Reserved.	0x0	R/W
		3	Power-down REFBB		Power-down REFBB. Setting this bit to Logic 1 powers down the REFBB input receiver.	0x0	R/W
		2	Power-down REFB		Power-down REFB. Setting this bit to Logic 1 powers down the REFB input receiver.	0x0	R/W
		1	Power-down REFAA		Power-down REFAA. Setting this bit to Logic 1 powers down the REFAA input receiver.	0x0	R/W
		0	Power-down REFA		Power-down REFA. Setting this bit to Logic 1 powers down the REFA input receiver.	0x0	R/W
0x2002	Timeout reference	[7:4]	Reserved		Reserved.	0x0	R/W
		3	Timeout Reference Monitor BB		Timeout REFBB validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE command) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following conditions force a valid REFBB setting. Set the bypass Reference Monitor BB bit to Logic 1. Set the Fault REFBB bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.	0x0	R/W
		2	Timeout Reference Monitor B		Timeout REFB validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following settings force REFB valid: Set the bypass Reference Monitor B bit to Logic 1. Set the Fault REFB bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.		
		1	Timeout Reference Monitor AA		Timeout REFAA validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following settings force REFAA valid: Set the Bypass Reference Monitor AA bit to Logic 1. Set the Fault REFAA bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Timeout Reference Monitor A		Timeout REFA validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following settings force REFA valid: Set the Bypass Reference Monitor A bit to Logic 1. Set the Fault REFA bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.	0x0	R/W
0x2003	Fault reference	[7:4]	Reserved		Reserved.	0x0	R
		3	Fault REFBB		Force REFBB invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFBB is not available as long as this bit is Logic 1.	0x0	R/W
		2	Fault REFB		Force REFB invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFB is not available as long as this bit is Logic 1.	0x0	R/W
		1	Fault REFAA		Force REFAA invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFAA is not available as long as this bit is Logic 1.	0x0	R/W
		0	Fault REFA		Force REFA invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFA is not available as long as this bit is Logic 1.	0x0	R/W
0x2004	Bypass reference monitor	[7:4]	Reserved		Reserved.	0x0	R
		3	Bypass Reference Monitor BB		Bypass REFBB frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declares the reference unfaulted. See the description for the Timeout Reference Monitor BB bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
		2	Bypass Reference Monitor B		Bypass REFB frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declare that reference unfaulted. See the description for the Timeout Reference Monitor B bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
		1	Bypass Reference Monitor AA		Bypass REFAA frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declare that reference unfaulted. See the description for the Timeout Reference Monitor AA bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
		0	Bypass Reference Monitor A		Bypass REFA frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declare that reference unfaulted. See the description for the Timeout Reference Monitor A bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
0x2005	Clear IRQ	7	Clear watchdog		Clear watchdog timer. Setting this write only bit to Logic 1 immediately clears the watchdog timer.	0x0	R
		[6:4]	Reserved		Reserved.	0x0	R/W
		3	IRQ clear PLL1		Clear all PLL1 IRQ. Setting this write only bit to Logic 1 clears all PLL1 IRQs. This bit always reads back as Logic 0.	0x0	R/W
		2	IRQ clear PLL0		Clear all PLL0 IRQ. Setting this write only bit to Logic 1 clears all PLL0 IRQs. This bit always reads back as Logic 0.	0x0	R/W
		1	IRQ clear common		Clear common IRQ. Setting this write only bit to Logic 1 clears all PLL1 IRQs. This bit always reads back as Logic 0.	0x0	R/W
		0	IRQ clear all		Clear all IRQs. Setting this write only bit to Logic 1 clears all PLL1 IRQs. This bit always reads back as Logic 0.	0x0	R/W

IRQ MAP COMMON CLEAR REGISTERS—REGISTER 0x2006 TO REGISTER 0x200A

Table 83. IRQ Map Common Clear Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2006	System clock (SYSCLK)	SYSCLK unlocked	SYSCLK stabilized	SYSCLK locked	SYSCLK calibration deactivated	SYSCLK calibration activated	Watchdog timeout occurred	EEPROM faulted	EEPROM completed	0x00	R/W
0x2007	Auxiliary DPLL	Reserved		Skew limit exceeded	Temperature warning occurred	Auxiliary DPLL unfaulted	Auxiliary DPLL faulted	Auxiliary DPLL unlocked	Auxiliary DPLL locked	0x00	R/W
0x2008	REFA	REFAA R divider resynced	REFAA validated	REFAA unfaulted	REFAA faulted	REFA R divider resynced	REFA validated	REFA unfaulted	REFA faulted	0x00	R/W
0x2009	REFB	REFBB R divider resynced	REFBB validated	REFBB unfaulted	REFBB faulted	REFB R divider resynced	REFB validated	REFB unfaulted	REFB faulted	0x00	R/W

Table 84. IRQ Map Common Clear Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2006	System clock (SYSCLK)	7	SYSCLK unlocked		System clock unlocked. Set this bit to Logic 1 to clear the SYSCLK unlocked IRQ.	0x0	R/W
		6	SYSCLK stabilized		System clock stabilized. Set this bit to Logic 1 to clear the SYSCLK stabilized IRQ.	0x0	R/W
		5	SYSCLK locked		System clock locked. Set this bit to Logic 1 to clear the SYSCLK locked IRQ.	0x0	R/W
		4	SYSCLK calibration deactivated		System clock calibration ended. Set this bit to Logic 1 to clear the SYSCLK calibration ended IRQ.	0x0	R/W
		3	SYSCLK calibration activated		System clock calibration started. Set this bit to Logic 1 to clear the SYSCLK calibration started IRQ.	0x0	R/W
		2	Watchdog timeout occurred		Watchdog timeout occurred. Set this bit to Logic 1 to clear the watchdog timer timeout IRQ.	0x0	R/W
		1	EEPROM faulted		EEPROM faulted. Set this bit to Logic 1 to clear the EEPROM faulted IRQ.	0x0	R/W
		0	EEPROM completed		EEPROM operation completed. Set this bit to Logic 1 to clear the EEPROM operation completed IRQ.	0x0	R/W
0x2007	Auxiliary DPLL	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew limit exceeded		Skew limit exceeded. Set this bit to Logic 1 to clear the reference input skew measurement limit exceeded IRQ.	0x0	R/W
		4	Temperature warning occurred		Temperature range warning. Set to Logic 1 to clear the temperature warning IRQ.	0x0	R/W
		3	Auxiliary DPLL unfaulted		Closed-loop SYSCLK compensation DPLL unfaulted. Set this bit to Logic 1 to clear the auxiliary DPLL unfaulted IRQ.	0x0	R/W
		2	Auxiliary DPLL faulted		Closed-loop SYSCLK compensation DPLL faulted. Set this bit to Logic 1 to clear the auxiliary DPLL faulted IRQ.	0x0	R/W
		1	Auxiliary DPLL unlocked		Closed-loop SYSCLK compensation DPLL unlocked. Set this bit to Logic 1 to clear the auxiliary DPLL unlocked IRQ.	0x0	R/W
		0	Auxiliary DPLL locked		Closed-loop SYSCLK compensation DPLL locked. Set this bit to Logic 1 to clear the auxiliary DPLL locked IRQ.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2008	REFA	7	REFAA R divider resynced		REFAA R divider resynced. Set this bit to Logic 1 to clear the REFAA R divider resynced IRQ.	0x0	R/W
		6	REFAA validated		REFAA validated. Set this bit to Logic 1 to clear the REFAA validated IRQ.	0x0	R/W
		5	REFAA unfaulted		REFAA unfaulted. Set this bit to Logic 1 to clear the REFAA unfaulted IRQ.	0x0	R/W
		4	REFAA faulted		REFAA faulted. Set this bit to Logic 1 to clear the REFAA faulted IRQ.	0x0	R/W
		3	REFA R divider resynced		REFA R divider resynced. Set this bit to Logic 1 to clear the REFA R divider resynced IRQ.	0x0	R/W
		2	REFA validated		REFA validated. Set this bit to Logic 1 to clear the REFA validated IRQ.	0x0	R/W
		1	REFA unfaulted		REFA unfaulted. Set this bit to Logic 1 to clear the REFA unfaulted IRQ.	0x0	R/W
		0	REFA faulted		REFA faulted. Set this bit to Logic 1 to clear the REFA faulted IRQ.	0x0	R/W
0x2009	REFB	7	REFBB R divider resynced		REFBB R divider resynced. Set this bit to Logic 1 to clear the REFBB R divider resynced IRQ.	0x0	R/W
		6	REFBB validated		REFBB validated. Set this bit to Logic 1 to clear the REFBB validated IRQ.	0x0	R/W
		5	REFBB unfaulted		REFBB unfaulted. Set this bit to Logic 1 to clear the REFBB unfaulted IRQ.	0x0	R/W
		4	REFBB faulted		REFBB faulted. Set this bit to Logic 1 to clear the REFBB faulted IRQ.	0x0	R/W
		3	REFB R divider resynced		REFB R divider resynced. Set this bit to Logic 1 to clear the REFB R divider resynced IRQ.	0x0	R/W
		2	REFB validated		REFB validated. Set this bit to Logic 1 to clear the REFB validated IRQ.	0x0	R/W
		1	REFB unfaulted		REFB unfaulted. Set to this bit to Logic 1 to clear the REFB unfaulted IRQ.	0x0	R/W
		0	REFB faulted		REFB faulted. Set this bit to Logic 1 to clear the REFB faulted IRQ.	0x0	R/W

IRQ MAP DPLL0 CLEAR REGISTERS—REGISTER 0x200B TO REGISTER 0x200F

Table 85. IRQ Map DPLL0 Clear Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x200B	Lock	DPLL0 frequency clamp deactivated	DPLL0 frequency clamp activated	DPLL0 phase slew limiter deactivated	DPLL0 phase slew limiter activated	DPLL0 frequency unlocked	DPLL0 frequency locked	DPLL0 phase unlocked	DPLL0 phase locked	0x00	R/W
0x200C	State	DPLL0 reference switched	DPLL0 freerun entered	DPLL0 holdover entered	DPLL0 hitless entered	DPLL0 hitless exited	DPLL0 history updated	Reserved	DPLL0 phase step detected	0x00	R/W
0x200D	Fast acquisition	Reserved			DPLL0 N-divider resynced	DPLL0 fast acquisition completed	DPLL0 fast acquisition started	Reserved		0x00	R/W
0x200E	Active profile	Reserved		DPLL0 Profile 5 activated	DPLL0 Profile 4 activated	DPLL0 Profile 3 activated	DPLL0 Profile 2 activated	DPLL0 Profile 1 activated	DPLL0 Profile 0 activated	0x00	R/W
0x200F	APLL	Reserved			DPLL0 distribution synced	APLL0 unlocked	APLL0 locked	APLL0 calibration completed	APLL0 calibration start	0x00	R/W

Table 86. IRQ Map DPLL1 Clear Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2010 to 0x2014	These registers mimic the IRQ Map DPLL0 clear registers (Register 0x200B through Register 0x200F), but the register addresses are offset by 0x0005. All default values are identical.								0x00	R/W

Table 87. IRQ Map DPLL0 Clear Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x200B	Lock	7	DPLL0 frequency clamp deactivated		Frequency clamp deactivated. Set this bit to Logic 1 to clear the IRQ for DPLL0 frequency clamp deactivated.	0x0	R/W
		6	DPLL0 frequency clamp activated		Frequency clamp activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 frequency clamp activated.	0x0	R/W
		5	DPLL0 phase slew limiter deactivated		Phase slew limiter deactivated. Set this bit to Logic 1 to clear the IRQ for DPLL0 phase slew limiter deactivated.	0x0	R/W
		4	DPLL0 phase slew limiter activated		Phase slew limiter activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 phase slew limiter activated.	0x0	R/W
		3	DPLL0 frequency unlocked		Frequency unlocked. Set this bit to Logic 1 to clear the IRQ for DPLL0 FLD (lock to unlock transition).	0x0	R/W
		2	DPLL0 frequency locked		Frequency locked. Set this bit to Logic 1 to clear the IRQ for DPLL0 frequency unlock detected (unlock to lock transition).	0x0	R/W
		1	DPLL0 phase unlocked		Phase unlocked. Set this bit to Logic 1 to clear the IRQ for DPLL0 PLD (lock to unlock transition).	0x0	R/W
		0	DPLL0 phase locked		Phase locked. Set this bit to Logic 1 to clear the IRQ for DPLL0 phase unlock detected (unlock to lock transition).	0x0	R/W
0x200C	State	7	DPLL0 reference switched		Reference switched. Set this bit to Logic 1 to clear the IRQ for DPLL0 reference input switched.	0x0	R/W
		6	DPLL0 freerun entered		Freerun mode entered. Set this bit to Logic 1 to clear the IRQ for DPLL0 freerun mode entered.	0x0	R/W
		5	DPLL0 holdover entered		Holdover mode entered. Set this bit to Logic 1 to clear the IRQ for DPLL0 holdover mode entered.	0x0	R/W
		4	DPLL0 hitless entered		Hitless mode entered. Set this bit to Logic 1 to clear the IRQ for DPLL0 hitless mode entered.	0x0	R/W
		3	DPLL0 hitless exited		Hitless mode exited. Set this bit to Logic 1 to clear the IRQ for DPLL0 hitless mode exited.	0x0	R/W
		2	DPLL0 history updated		Holdover history updated. Set this bit to Logic 1 to clear the IRQ for DPLL0 tuning word holdover history updated.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DPLL0 phase step detected		Phase step detected. Set to Logic 1 to clear the IRQ for DPLL0 reference input phase step detected.	0x0	R/W
0x200D	Fast acquisi-tion	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 N-divider resynced		N-divider resynchronized. Set this bit to Logic 1 to clear the IRQ for DPLL0 N-divider resynced.	0x0	R/W
		3	DPLL0 fast acquisition completed		Fast acquisition completed. Set this bit to Logic 1 to clear the IRQ for DPLL0 fast acquisition complete.	0x0	R/W
		2	DPLL0 fast acquisition started		Fast acquisition started. Set this bit to Logic 1 to clear the IRQ for DPLL0 fast acquisition started.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R/W
0x200E	Active profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 Profile 5 activated		Profile 5 activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 Profile 5 activated.	0x0	R/W
		4	DPLL0 Profile 4 activated		Profile 4 activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 Profile 4 activated.	0x0	R/W
		3	DPLL0 Profile 3 activated		Profile 3 activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 Profile 3 activated.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	DPLL0 Profile 2 activated		Profile 2 activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 Profile 2 activated.	0x0	R/W
		1	DPLL0 Profile 1 activated		Profile 1 activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 Profile 1 activated.	0x0	R/W
		0	DPLL0 Profile 0 activated		Profile 0 activated. Set this bit to Logic 1 to clear the IRQ for DPLL0 Profile 0 activated.	0x0	R/W
0x200F	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 distribution synced		Clock distribution synced. Set this bit to Logic 1 to clear the IRQ for DPLL0 clock distribution synced.	0x0	R/W
		3	APLL0 unlocked		Unlock detected. Set this bit to Logic 1 to clear the IRQ for APLL0 unlock detected (lock to unlock transition).	0x0	R/W
		2	APLL0 locked		Lock Detected. Set this bit to Logic 1 to clear the IRQ for APLL0 lock detected (unlock to lock transition).	0x0	R/W
		1	APLL0 calibration completed		Calibration completed. Set this bit to Logic 1 to clear the IRQ for APLL0 calibration complete.	0x0	R/W
		0	APLL0 calibration start		Calibration start. Set this bit to Logic 1 to clear the IRQ for APLL0 calibration start.	0x0	R/W

OPERATIONAL CONTROL CHANNEL 0 REGISTERS—REGISTER 0x2100 TO REGISTER 0x2107

Table 88. Operational Control Channel 0 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2100	Power down and calibration	Reserved						Calibrate APLL0	Power down Channel 0	0x00	R/W
0x2101	All Channel 0 control	Reserved				Sync all Channel 0 drivers	Reset all Channel 0 drivers	Mute all Channel 0 drivers	N-shot request Channel 0	0x00	R/W
0x2102	Divider Q0A	Reserved		Reset OUT0A/OUT0AA	Power down OUT0A/OUT0AA	Mute OUT0AA	Mute OUT0A	Reset Q0AA	Reset Q0A	0x00	R/W
0x2103	Divider Q0B	Reserved		Reset OUT0B/ OUT0BB	Power down OUT0B/OUT0BB	Mute OUT0BB	Mute OUT0B	Reset Q0BB	Reset Q0B	0x00	R/W
0x2104	Divider Q0C	Reserved		Reset OUT0C/ OUT0CC	Power down OUT0C/OUT0CC	Mute OUT0CC	Mute OUT0C	Reset Q0CC	Reset Q0C	0x00	R/W
0x2105	DPLL0 mode	Enable step detect reference fault	DPLL0 assign translation profile			DPLL0 translation profile select mode		DPLL0 force holdover	DPLL0 force freerun	0x00	R/W
0x2106	DPLL0 fast acquisition mode	Reserved				Enable DPLL0 fast acquisition no output	Enable DPLL0 fast acquisition first	Enable DPLL0 fast acquisition from holdover	Enable DPLL0 fast acquisition from freerun	0x00	R/W
0x2107	Clear state	Reserved			Channel 0 automute clear	Clear DPLL0 fast acquisition done	Reserved	DPLL0 clear history	Channel 0 autosync one shot	0x00	R/W

Table 89. Operational Control Channel 0 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2100	Power down and calibration	[7:2]	Reserved		Reserved.	0x0	R
		1	Calibrate APLL0		APLL0 voltage controlled oscillator (VCO) calibration. Setting this bit from Logic 0 to Logic 1 performs the APLL VCO calibration the next time the user writes 1b to the IO_UPDATE bit. VCO calibration must be done during initial configuration and any time the nominal APLL VCO frequency changes. VCO calibration must be performed after the APLL dividers are configured and the desired APLL input frequency is present. This bit field is not self clearing, and it is recommended that the user write a Logic 0 to this bit field after performing the VCO calibration.	0x0	R/W
		0	Power down Channel 0		Power down Channel 0. Setting this bit to Logic 1 powers all blocks in Channel 0. All Channel 0 outputs are tristated.	0x0	R/W
0x2101	All Channel 0 control	[7:4]	Reserved		Reserved.	0x0	R
		3	Sync all Channel 0 drivers		Synchronize all Channel 0 drivers. If making the output driver static without resetting the corresponding Q divider, use the mute all Channel 0 drivers bit in this register instead. The power down OUT0x/OUT0xx bits in Register 0x2102, Register 0x2103, and Register 0x2104 tristate the corresponding output driver.	0x0	R/W
				0	Normal operation.		
				1	All Channel 0 output drivers are held in a static state and the corresponding Q dividers are held in reset. In the sync state, differential drivers are held in a muted state. Releasing from Logic 1 to Logic 0 initializes all outputs synchronously.		
		2	Reset all Channel 0 drivers		Reset all Channel 0 drivers. The reset function is identical to the mute all Channel 0 drivers bit in this register, except the mute function delays muting an output driver to avoid a runt pulse, whereas the reset function mutes the output driver immediately. Both the reset and mute functions contain logic to prevent runt pulses while unmuting an output driver.	0x0	R/W
		1	Mute all Channel 0 drivers		Mute all Channel 0 drivers. The Channel 0 drivers are not tristated while muted. In contrast, the power down OUT0x/OUT0xx bit tristates the output driver.	0x0	R/W
				0	Channel 0 drivers are unmuted. The output drivers contain logic to prevent runt pulses while transitioning from a mute to unmute state.		
				1	Channel 0 drivers are muted. In the muted state, differential drivers are held in a state in which the positive leg of the differential driver is static low, while the complementary output is static high.		
		0	N-shot request Channel 0		Channel 0 JESD204B N-shot request. In most cases, return this bit to zero to avoid unwanted retriggering of the N-shot generators.	0x0	R/W
				0	Normal operation (JESD204B N-shot not requested).		
				1	Channel 0 JESD204B N-shot request. This bit is in a buffered register, meaning an IO_UPDATE command must follow this register write.		
0x2102	Divider Q0A	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT0A/OUT0AA		Reset OUT0A and OUT0AA drivers. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT0A/OUT0AA are OUT0AP/OUT0AN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT0A/AA is put immediately into reset and driven static low/high. In differential mode, OUT0AA is static high.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	Power down OUT0A/OUT0AA		Power down OUT0A/OUT0AA.	0x0	R/W
				0	Normal operation.		
				1	OUT0A/OUT0AA are powered down and tristated. OUT0A/OUT0AA correspond to Pin OUT0AP and Pin OUT0AN, respectively.		
		3	Mute OUT0AA		Mute OUT0AA. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0AA is OUT0AN.	0x0	R/W
				0	Normal operation. OUT0AA is unmuted.		
				1	OUT0AA is muted and driven static low. Use power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT0A is in differential mode.		
		2	Mute OUT0A		Mute OUT0A. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0A is OUT0AP.	0x0	R/W
				0	Normal operation. OUT0A is unmuted.		
				1	OUT0A is muted and driven static low. In differential mode, OUT0AA is static high.		
		1	Reset Q0AA		Reset Divider Q0AA. Setting this bit to Logic 1 immediately puts the Q0AA divider into reset.	0x0	R/W
		0	Reset Q0A		Reset Divider Q0A. Setting this bit to Logic 1 immediately puts the Q0A divider into reset.	0x0	R/W
0x2103	Divider Q0B	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT0B/OUT0BB		Reset OUT0B and OUT0BB drivers. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT0B/OUT0BB are OUT0BP/OUT0BN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT0B/OUT0BB is put immediately into reset and driven static low/high. In differential mode, OUT0BB is static high.		
		4	Power down OUT0B/OUT0BB		Power down OUT0B/OUT0BB.	0x0	R/W
				0	Normal operation.		
				1	OUT0B/OUT0BB are powered down and tristated. OUT0B/OUT0BB correspond to Pin OUT0BP and Pin OUT0BN, respectively.		
		3	Mute OUT0BB		Mute OUT0BB. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0BB is OUT0BN.	0x0	R/W
				0	Normal operation. OUT0BB is unmuted.		
				1	OUT0BB is muted and driven static low. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT0B is in differential mode.		
		2	Mute OUT0B		Mute OUT0B. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0B is OUT0BP.	0x0	R/W
				0	Normal operation. OUT0B is unmuted.		
				1	OUT0B is muted and driven static low. In differential mode, OUT0BB is static high.		
		1	Reset Q0BB		Reset Divider Q0BB. Setting this bit to Logic 1 immediately puts the Q0BB divider into reset.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Reset Q0B		Reset Divider Q0B. Setting this bit to Logic 1 immediately puts the Q0B divider into reset.	0x0	R/W
0x2104	Divider Q0C	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT0C/OUT0CC		Reset OUT0C and CC Drivers. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT0C/OUT0CC are OUT0CP/OUT0CCN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT0C/OUT0CC is put immediately into reset and driven static low/high. In differential mode, OUT0CC is static high.		
		4	Power down OUT0C/ OUT0CC		Power down OUT0C/OUT0CC.	0x0	R/W
				0	Normal operation.		
				1	OUT0C/OUT0CC are powered down and tristated. OUT0C/OUT0CC correspond to Pin OUT0CP and Pin OUT0CN, respectively.		
		3	Mute OUT0CC		Mute OUT0CC. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0CC is OUT0CN.	0x0	R/W
				0	Normal operation. OUT0CC is unmuted.		
				1	OUT0CC is muted and driven static low. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT0C is in differential mode.		
		2	Mute OUT0C		Mute OUT0C. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0C is OUT0CP.	0x0	R/W
				0	Logic 0: normal operation. OUT0C is unmuted.		
				1	Logic 1: OUT0C is muted and driven static low. In differential mode, OUT0CC is static high.		
		1	Reset Q0CC		Reset Divider Q0CC. Setting this bit to Logic 1 immediately puts the Q0CC divider into reset.	0x0	R/W
		0	Reset Q0C		Reset Divider Q0C. Setting this bit to Logic 1 immediately puts the Q0C divider into reset.	0x0	R/W
0x2105	DPLL0 mode	7	Enable step detect reference fault		Enable step detect reference fault.	0x0	R/W
				0	Logic 0: in the event that the phase step detector activates, DPLL0 ignores the clock edge that activated the step detector and initiates a new reference acquisition.		
				1	Logic 1: similar to Logic 0, but the input reference monitor is reset. In this case, validate the input reference prior to DPLL00 beginning a new reference input acquisition.		
		[6:4]	DPLL0 assign translation profile		DPLL0 manual translation profile assign. This 3-bit bit field controls which DPLL0 translation profile is selected when DPLL0 is in manual mode. Manual mode is selected in the DPLL0 profile selection mode bit field.	0x0	R/W
				000	DPLL Translation Profile 0.0.		
				001	DPLL Translation Profile 0.1.		
				010	DPLL Translation Profile 0.2.		
				011	DPLL Translation Profile 0.3.		
				100	DPLL Translation Profile 0.4.		
				101	DPLL Translation Profile 0.5.		
				110, 111	Do not use.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:2]	DPLL0 translation profile select mode		DPLL0 translation profile selection mode. This 2-bit bit field controls how DPLL0 selects which translation profile to use.	0x0	R/W
				0	Fully automatic, based on priority-based selection. In this fully automatic mode, the DPLL state machine chooses the highest priority translation profile. If the DPLL is unable to find a profile per the selection process, it reverts to either holdover mode (if there is sufficient tuning word history) or freerun mode. In the case of a tie, the lowest numbered profile is chosen.		
				1	Manual profile selection with fallback to autoprofile selection. In this mode, the user chooses the profile to use. The DPLL uses the selected profile until it becomes invalid. At that time, the DPLL reverts to normal, priority-based profile selection.		
				2	Manual profile selection with fallback to holdover mode. In this mode, the user chooses the profile to use. The DPLL uses this profile until it becomes invalid. At that time, the DPLL reverts to holdover mode.		
				3	The user controls all operation.		
		1	DPLL0 force holdover		Force DPLL0 into holdover mode.	0x0	R/W
				0	Logic 0: normal operation.		
				1	DPLL0 is forced into holdover mode. In this mode, DPLL0 does not lock to any input references and behaves like a frequency synthesizer. If the DPLL0 history available bit is Logic 0, there is insufficient tuning word history, and DPLL0 uses its freerun tuning word instead of its accumulated tuning word history.		
		0	DPLL0 force freerun		Force DPLL0 into freerun mode.	0x0	R/W
				0	Normal operation.		
				1	DPLL0 is forced into freerun mode. In this mode, DPLL0 does not lock to any input references and behaves like a frequency synthesizer.		
0x2106	DPLL0 fast acquisition mode	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable DPLL0 fast acquisition no output		Enable DPLL0 fast acquisition if no outputs.	0x0	R/W
				0	Normal operation. A fast acquisition event on DPLL0 is permitted to occur regardless of whether or not the Channel 0 outputs receive a sync signal or not. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is enabled only if the none of the DPLL0 outputs receive a sync signal. The purpose of this bit is to ensure that none of the outputs are toggling during a fast acquisition sequence.		
		2	Enable DPLL0 fast acquisition first		Enable DPLL0 fast acquisition only during first acquisition.	0x0	R/W
				0	DPLL0 fast acquisition mode is not dependent the status of the DPLL0 fast acquisition done bit. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is not enabled if the DPLL0 fast acquisition done bit is Logic 1. The purpose of this bit is to execute a fast acquisition sequence only once.		
		1	Enable DPLL0 fast acquisition from holdover		Enable DPLL0 fast acquisition from holdover mode.	0x0	R/W
				0	DPLL0 fast acquisition mode is not enabled when exiting holdover mode. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is enabled when exiting holdover mode.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Enable DPLL0 fast acquisition from freerun		Enable DPLL0 fast acquisition from freerun mode.	0x0	R/W
				0	DPLL0 fast acquisition mode is not enabled when exiting freerun mode. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is enabled when exiting freerun mode.		
0x2107	Clear state	[7:5]	Reserved		Reserved.	0x0	R
		4	Channel 0 automute clear		Clear automute state. Setting this bit to Logic 1 allows the user to manually clear the automatic muting of Channel 0. This reinitializes the muting of outputs until the currently programmed condition in the DPLL0 autounmute mode bit field is satisfied.	0x0	R/W
		3	Clear DPLL0 fast acquisition done		Clear the DPLL0 fast acquisition done bit. Setting this autoclearing bit to Logic 1 clears the DPLL0 fast acquisition done bit.	0x0	R/W
		2	Reserved		Reserved.	0x0	R/W
		1	DPLL0 clear history		Clear DPLL0 tuning word history. Setting this bit to Logic 1 sets the DPLL0 history available bit to Logic 0 and clears the internal tuning word history values for DPLL0. However, the DPLL0 tuning work history bit field remains intact until the processor calculates a new average and sets the DPLL0 history available bit to Logic 1, indicating a new average is available.	0x0	R/W
		0	Channel 0 clear autosync one shot		Channel 0 clear autosync one-shot. This autoclearing bit reactivates the autosync state machine for Channel 0. When used in conjunction with Register 0x10DB, Bits[1:0], autosync mode = 01 binary, it is a convenient way to sync or resync the outputs.	0x0	R/W
				0	Normal operation. A clock distribution autosync event only occurs once per channel when an autosync condition is met. The autosync mode bit field controls when this happens. For example, the output synchronizes on DPLL frequency lock.		
				1	Clock distribution autosync is reactivated, and an output resync occurs when the next autosync event occurs. If the autosync mode bit field is set to 01b, setting this bit to Logic 1 triggers an immediate sync event provided that APLL0 is locked.		

OPERATIONAL CONTROL CHANNEL 1 REGISTERS—REGISTER 0x2200 TO REGISTER 0x2207

Table 90. Operational Control Channel 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2200	Power down and calibration	Reserved						Calibrate APLL1	Power down Channel 1	0x00	R/W
0x2201	All Channel 1 control	Reserved				Sync all Channel 1 drivers	Reset all Channel 1 drivers	Mute all Channel 1 drivers	N-shot request Channel 1	0x00	R/W
0x2202	Divider Q1A	Reserved		Reset OUT1A/ OUT1AA	Power down OUT1A/OUT1AA	Mute OUT1AA	Mute OUT1A	Reset Q1AA	Reset Q1A	0x00	R/W
0x2203	Divider Q1B	Reserved		Reset OUT1B/OUT1BB	Power down OUT1B/OUT1BB	Mute OUT1BB	Mute OUT1B	Reset Q1BB	Reset Q1B	0x00	R/W
0x2204	Reserved	Reserved								0x00	R/W
0x2205	DPLL1 mode	Enable step detect reference fault	DPLL1 assign translation profile			DPLL1 translation profile select mode		DPLL1 force holdover	DPLL1 force freerun	0x00	R/W

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2206	DPLL1 fast acquisition mode	Reserved				Enable DPLL1 fast acquisition no output	Enable DPLL1 fast acquisition first	Enable DPLL1 fast acquisition from holdover	Enable DPLL1 fast acquisition from freerun	0x00	R/W
0x2207	Clear state	Reserved			Channel 1 automute clear	Clear DPLL1 fast acquisition done	Reserved	DPLL1 clear history	Channel 1 autosync one shot	0x00	R/W

Table 91. Operational Control Channel 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2200	Power down and calibration	[7:2]	Reserved		Reserved.	0x0	R
		1	Calibrate APLL1		APLL1 VCO calibration. Setting this bit from Logic 0 to Logic 1 performs the APLL VCO calibration the next time the user writes 1b to the IO_UPDATE bit. VCO calibration must be done during initial configuration and any time the nominal APLL VCO frequency changes. Perform VCO calibration after the APLL dividers are configured and the desired APLL input frequency is present. This bit field is not self clearing, and it is recommended that the user write a Logic 0 to this bit field after performing the VCO calibration.	0x0	R/W
		0	Power down Channel 1		Power down Channel 1. Setting this bit to Logic 1 powers all blocks in Channel 1. All Channel 1 outputs are tristated.	0x0	R/W
0x2201	All Channel 1 control	[7:4]	Reserved		Reserved.	0x0	R
		3	Sync all Channel 1 drivers		Synchronize all Channel 1 drivers. If making the output driver static without resetting the corresponding Q divider, use the mute all Channel 1 drivers bit in this register instead. The power down OUT1x/OUT1xx bits in Register 0x2202 and Register 0x2203 tristate the corresponding output driver.	0x0	R/W
				0	Normal operation.		
				1	All Channel 1 output drivers are held in a static state at the corresponding Q dividers (held in reset). In the sync state, differential drivers are held in a muted state. Releasing from Logic 1 to Logic 0 initializes all outputs synchronously.		
		2	Reset all Channel 1 drivers		Reset all Channel 1 drivers. The reset function is identical to the mute all Channel 1 drivers bit in this register, except the mute function delays muting an output driver to avoid a runt pulse, whereas the reset function mutes the output driver immediately. Both the reset and mute functions contain logic to prevent runt pulses while unmuting an output driver.	0x0	R/W
		1	Mute all Channel 1 drivers		Mute all Channel 1 drivers. Use the power down OUT0x/OUT0xx bit to tristate the output driver.	0x0	R/W
				0	Channel 1 drivers are unmuted. The output drivers contain logic to prevent runt pulses while transitioning from a mute to unmute state.		
				1	Channel 1 drivers are muted. In the muted state, differential drivers are held in a state in which the positive leg of the differential driver is static low, while the complementary output is static high.		
		0	N-shot request Channel 1		Channel 1 JESD204B N-shot request. In most cases, return this bit to zero to avoid unwanted retriggering of the N-shot generators.	0x0	R/W
				0	Normal operation (JESD204B N-shot not requested).		
				1	Channel 1 JESD204B N-Shot request. This bit is in a buffered register, meaning that an IO_UPDATE command must follow this register write.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2202	Divider Q1A	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT1A/OUT1AA		Reset OUT1A and OUT1AA drivers. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT1A/OUT1AA are OUT1AP/OUT1AN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT1A/OUT1AA is put immediately into reset and driven static low/high. In differential mode, OUT1AA is static high.		
		4	Power down OUT1A/OUT1AA		Power down OUT1A/OUT1AA.	0x0	R/W
				0	Normal operation.		
				1	OUT1A/OUT1AA are powered down and tristated. OUT1A/OUT1AA correspond to Pin OUT1AP and Pin OUT1AN, respectively.		
		3	Mute OUT1AA		Mute OUT1AA. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1AA is OUT1AN.	0x0	R/W
				0	Normal operation. OUT1AA is unmuted.		
				1	OUT1AA is muted and driven static low. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT1A is in differential mode.		
		2	Mute OUT1A		Mute OUT1A. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1A is OUT1AP.	0x0	R/W
				0	Normal operation. OUT1A is unmuted.		
				1	OUT1A is muted and driven static low. In differential mode, OUT1AA is static high.		
		1	Reset Q1AA		Reset Divider Q1AA. Setting this bit to Logic 1 immediately puts the Q1AA divider into reset.	0x0	R/W
		0	Reset Q1A		Reset Divider Q1A. Setting this bit to Logic 1 immediately puts the Q1A divider into reset.	0x0	R/W
0x2203	Divider Q1B	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT1B/OUT1BB		Reset OUT1B and OUT1BB drivers. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT1B/OUT1BB are OUT1BP/OUT1BN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT1B/OUT1BB is put immediately into reset and driven static low/high. In differential mode, OUT1BB is static high.		
		4	Power down OUT1B/OUT1BB		Power down OUT1B/OUT1BB.	0x0	R/W
				0	Normal operation.		
				1	OUT1B/OUT1BB are powered down and tristated. OUT1B/OUT1BB correspond to Pin OUT1BP and Pin OUT1BN, respectively.		
		3	Mute OUT1BB		Mute OUT1BB. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1BB is OUT1BN	0x0	R/W
				0	Normal operation. OUT1BB is unmuted.		
				1	OUT1BB is muted and driven static low. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT1B is in differential mode.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	Mute OUT1B		Mute OUT1B. Use the power down OUT0x/OUT0xx bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1B is OUT1BP.	0x0	R/W
				0	Normal operation. OUT1B is unmuted.		
				1	OUT0B is muted and driven static low. In differential mode, OUT1BB is static high.		
		1	Reset Q1BB		Reset Divider Q1BB. Setting this bit to Logic 1 immediately puts the Q1BB divider into reset.	0x0	R/W
		0	Reset Q1B		Reset Divider Q1B. Setting this bit to Logic 1 immediately puts the Q1B divider into reset.	0x0	R/W
0x2205	DPLL1 mode	7	Enable step detect reference fault		Enable step detect reference fault.	0x0	R/W
				0	In the event that the phase step detector activates, DPLL1 ignores the clock edge that activates the step detector and initiates a new reference acquisition.		
				1	Similar to Logic 0, but the input reference monitor is reset. In this case, the input reference must be validated prior to DPLL1 beginning a new reference input acquisition.		
		[6:4]	DPLL1 assign translation profile		DPLL1 manual translation profile assign. This 3-bit bit field controls which DPLL1 translation profile is selected when DPLL1 is in manual mode. Manual mode is selected in the DPLL1 profile selection mode bit field.	0x0	R/W
				000	DPLL Translation Profile 1.0.		
				001	DPLL Translation Profile 1.1.		
				010	DPLL Translation Profile 1.2.		
				011	DPLL Translation Profile 1.3.		
				100	DPLL Translation Profile 1.4.		
				101	DPLL Translation Profile 1.5.		
				110, 111	Do not use.		
		[3:2]	DPLL1 translation profile select mode		DPLL1 translation profile selection mode. This 2-bit bit field controls how DPLL1 selects which translation profile to use.	0x0	R/W
				0	Fully automatic, based on priority-based selection. In this fully automatic mode, the DPLL state machine chooses the highest priority translation profile. If the DPLL is unable to find a profile per the selection process, it reverts to either holdover (if there is sufficient tuning word history) or freerun mode. In the case of a tie, the lowest numbered profile is chosen.		
				1	Manual profile selection with fallback to autoprofile selection. In this mode, the user chooses the profile to use. The DPLL uses the selected profile until it becomes invalid. At that time, the DPLL reverts to normal, priority-based profile selection.		
				2	Manual profile selection with fallback to holdover mode. In this mode, the user chooses the profile to use. The DPLL uses this profile until it becomes invalid. At that time, the DPLL reverts to holdover mode.		
				3	The user controls all operation.		
		1	DPLL1 force holdover		Force DPLL1 into holdover mode.	0x0	R/W
				0	Normal operation.		
				1	DPLL1 is forced into holdover mode. In this mode, DPLL1 does not lock to any input references and behaves like a frequency synthesizer. If the DPLL1 history available bit is Logic 0, there is insufficient tuning word history, and DPLL1 uses its freerun tuning word instead of its accumulated tuning word history.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	DPLL1 force freerun		Force DPLL1 into freerun mode.	0x0	R/W
				0	Normal operation.		
				1	DPLL1 is forced into freerun mode. In this mode, DPLL1 does not lock to any input references and behaves like a frequency synthesizer.		
0x2206	DPLL1 fast acquisition mode	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable DPLL1 fast acquisition if no output		Enable DPLL1 fast acquisition if no outputs.	0x0	R/W
				0	Normal operation. A fast acquisition event on DPLL1 is permitted to occur regardless of whether or not the Channel 1 outputs receive a sync signal or not. When all four FACQ bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is enabled only if none of the DPLL1 outputs receive a sync signal. The purpose of this bit is to ensure that none of the outputs are toggling during a fast acquisition sequence.		
		2	Enable DPLL1 fast acquisition first		Enable DPLL1 fast acquisition only during first acquisition.	0x0	R/W
				0	DPLL1 fast acquisition mode is not dependent the status of the DPLL1 fast acquisition done bit. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is not enabled if the DPLL1 FACQ done bit is Logic 1. The purpose of this bit is to execute a fast acquisition sequence only once.		
		1	Enable DPLL1 fast acquisition from holdover		Enable DPLL1 fast acquisition from holdover mode.	0x0	R/W
				0	DPLL1 fast acquisition mode is not enabled when exiting holdover mode. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is enabled when exiting holdover mode.		
		0	Enable DPLL1 fast acquisition from freerun		Enable DPLL1 fast acquisition from freerun mode.	0x0	R/W
				0	DPLL1 fast acquisition mode is not enabled when exiting freerun mode. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is enabled when exiting freerun mode.		
0x2207	Clear state	[7:5]	Reserved		Reserved.	0x0	R
		4	Channel 1 automute clear		Clear automute state. Setting this bit to Logic 1 allows the user to manually clear the automatic muting of Channel 1, which reinitializes the muting of outputs until the currently programmed condition in the DPLL1 autounmute mode bit field is satisfied.	0x0	R/W
		3	Clear DPLL1 fast acquisition done		Clear the DPLL1 fast acquisition done bit. Setting this autoclearing bit to Logic 1 clears the DPLL1 FACQ done bit.	0x0	R/W
		2	Reserved		Reserved.	0x0	R/W
		1	DPLL1 clear history		Clear DPLL1 tuning word history. Setting this bit to Logic 1 sets the DPLL1 history available bit to Logic 0 and clears the internal tuning word history values for DPLL1. However, the DPLL1 tuning work history bit field remains intact until the processor calculates a new average and sets the DPLL1 history available bit to Logic 1, indicating that a new average is available.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Channel 1 clear autosync one-shot		Channel 1 clear autosync one shot. This autoclearing bit reactivates the autosync state machine for Channel 1. When used in conjunction with Register 0x10DB, Bits[1:0], autosync mode = 01 binary, it is a convenient way to sync (or resync) the outputs.	0x0	R/W
				0	Normal operation. A clock distribution autosync event only occurs once per channel when an autosync condition is met. The autosync mode bit field controls when this happens. For example, output sync on DPLL frequency lock.		
				1	Clock distribution autosync is reactivated, and an output resync occurs when the next autosync event occurs. If the autosync mode bit field is set to 01b, setting this bit to Logic 1 triggers an immediate sync event provided that APLL1 is locked.		

TEMPERATURE SENSOR REGISTERS—REGISTER 0x2900 TO REGISTER 0x2906

Table 92. Temperature Sensor Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2900	External temperature	External temperature [7:0]								0x00	R/W
0x2901		External temperature [15:8]								0x00	R/W
0x2902	Temperature source	Reserved					Select DPLL1 delay temperature compensation source	Select DPLL0 delay temperature compensation source	Select SYSCLK temperature compensation source	0x00	R/W
0x2903	Low temperature alarm	Low temperature threshold [7:0]								0x00	R/W
0x2904		Low temperature threshold [15:8]								0x00	R/W
0x2905	High temperature alarm	High temperature threshold [7:0]								0x00	R/W
0x2906		High temperature threshold [15:8]								0x00	R/W

Table 93. Temperature Sensor Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2900	External temperature	[7:0]	External temperature [7:0]		External temperature. The user inputs the temperature of a remote temperature sensor in this signed, 16-bit bit field. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The value in this bit field is computed by multiplying the temperature (in degrees Celsius) by 128. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required after writing for the newly programmed value to take effect.	0x0	R/W
0x2901		[7:0]	External temperature [15:8]		For example, to enter a temperature of −15.6°C, T = −15.6 × 128 = −1997 (decimal) = 0xF833. To enter a temperature of 35.1°C, T = 35.1 × 128 = 4493 (decimal) = 0x118D.	0x0	R/W
0x2902	Temperature source	[7:3]	Reserved		Reserved.	0x0	R
		2	Select DPLL1 delay temperature compensation source		DPLL1 delay compensation source. This bit allows the user to choose which temperature reading to use when compensating the temperature variation of the DPLL1 static phase offset.	0x0	R/W
				0	Use the internal temperature sensor.		
				1	Use the external temperature bit field.		
		1	Select DPLL0 delay temperature compensation source		DPLL0 delay compensation source. This bit allows the user to choose which temperature reading to use when compensating the temperature variation of the DPLL0 static phase offset.	0x0	R/W
				0	Use the internal temperature sensor.		
				1	Use the external temperature bit field.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Select SYSCLK temperature compensation source		SYSCLK temperature compensation source. This bit allows the user to choose which temperature reading to use when compensating the system clock frequency temperature variation.	0x0	R/W
				0	Use the internal temperature sensor.		
				1	Use the external temperature bit field.		
0x2903	Low temperature alarm	[7:0]	Low temperature threshold [7:0]		Low temperature threshold. This signed, 16-bit bit field contains the lower threshold of the internal temperature of the device before the temperature alarm is activated. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The value in this bit field is computed by multiplying the desired temperature setting (in degrees Celsius) by 128. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required after writing for the newly programmed value to take effect. The temperature sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, to enter a temperature of −15.6°C, T = −15.6 × 128 = −1997 (decimal) = 0xF833. To enter a temperature of 35.1°C, T = 35.1 × 128 = 4493 (decimal) = 0x118D.	0x0	R/W
0x2904		[7:0]	Low temperature threshold [15:8]			0x0	R/W
0x2905	High temperature alarm	[7:0]	High temperature threshold [7:0]		High temperature threshold. This signed, 16-bit bit field contains the upper threshold of the internal temperature of the device before the temperature alarm is activated. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The value in this bit field is computed by multiplying the desired temperature setting (in degrees Celsius) by 128. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required after writing for the newly programmed value to take effect. The temperature sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, to enter a temperature of −15.6°C, T = −15.6 × 128 = −1997 (decimal) = 0xF833. To enter a temperature of 35.1°C, T = 35.1 × 128 = 4493 (decimal) = 0x118D.	0x0	R/W
0x2906		[7:0]	High temperature threshold [15:8]			0x0	R/W

EEPROM REGISTERS—REGISTER 0x2E00 TO REGISTER 0x2E1E

Table 94. EEPROM Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2E00	EEPROM options	Reserved					Verify EEPROM CRC	EEPROM fast mode	EEPROM write enable	0x00	R/W
0x2E01	EEPROM condition	Reserved				EEPROM load condition				0x00	R/W
0x2E02	EEPROM save	Reserved							EEPROM save	0x00	R/W
0x2E03	EEPROM load	Reserved							EEPROM load	0x00	R/W
0x2E10 to 0x2E1E	EEPROM sequence	EEPROM sequence								0xFF	R/W

Table 95. EEPROM Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2E00	EEPROM options	[7:3]	Reserved		Reserved.	0x0	R
		2	Verify EEPROM CRC		Verify EEPROM cyclic redundancy check (CRC). Setting this autoclearing bit to Logic 1 immediately starts a register loading from the EEPROM into the device to verify the EEPROM contents, and requires the same amount of time as a load from EEPROM operation. The key difference between this command and load from EEPROM is that the current AD9542 register settings are not overwritten using this command. An IO_UPDATE command is not required.	0x0	R/W
		1	EEPROM fast mode		EEPROM I^2C fast mode. Logic 0: 100 kHz I^2C mode. Logic 1: fast I^2C (400 kHz) mode. These clock rates are the maximum internally generated SCL frequencies. The nominal frequency of the internally generated I^2C SCL clock is typically 30% slower than these values.	0x0	R/W
		0	EEPROM write enable		EEPROM write enable. This bit must be set to Logic 1 before performing a save to EEPROM operation. This bit is not autoclearing, and is in a live register. Live registers do not require an IO_UPDATE command to take effect. Logic 0: writing to EEPROM disabled. Logic 1: writing to EEPROM enabled.	0x0	R/W
0x2E01	EEPROM condition	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	EEPROM load condition		EEPROM condition map. This 4-bit bit field contains the EEPROM condition map, which allows conditional processing of EEPROM commands. Conditional processing allows users to store multiple configurations in the AD9542 EEPROM and select them at EEPROM loading time. Conditional processing is disabled by setting this bit field to 0x0 during an EEPROM write; this is called condition zero, and EEPROM instructions that are stored with condition zero are executed unconditionally during a load from EEPROM operation. Refer to the AD9542 data sheet for details on conditional EEPROM instructions.	0x0	R/W
0x2E02	EEPROM save	[7:1]	Reserved		Reserved.	0x0	R
		0	EEPROM save		Save to EEPROM. Setting this autoclearing bit to Logic 1 immediately starts a register save to the EEPROM from the AD9542. The user must write a Logic 1 to the EEPROM write enable bit in this register prior to writing a Logic 1 to this bit. This bit is in a live register and an IO_UPDATE command is not required after writing this bit.	0x0	R/W
0x2E03	EEPROM load	[7:1]	Reserved		Reserved.	0x0	R
		0	EEPROM load		Load from EEPROM. Setting this autoclearing bit to Logic 1 immediately starts a register loading from the EEPROM into the device. An IO_UPDATE command is not required.	0x0	R/W
0x2E10 to 0x2E1E	EEPROM sequence	[7:0]	EEPROM sequence		EEPROM storage sequence. This group of 15 registers contain the EEPROM storage sequence instructions for the AD9542 EEPROM controller. These instructions include operational codes (such as input/output update or APLL calibration), as well as the sequence of AD9542 register values that are to be stored in the EEPROM. Refer to the AD9542 data sheet for the list operational controls and programming sequence details.	0xFF	R/W

STATUS READBACK REGISTERS—REGISTER 0x3000 TO REGISTER 0x300A

Table 96. Status Readback Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3000	EEPROM status	Reserved				EEPROM CRC error	EEPROM fault	EEPROM load in progress	EEPROM save in progress	0x0X	R
0x3001	SYSCLK and PLL status	Reserved		PLL1 locked	PLL0 locked	Reserved	SYSCLK calibration busy	SYSCLK stable	SYSCLK locked	0xXX	R
0x3002	Miscellaneous status	Reserved					Auxiliary DPLL reference fault	Auxiliary DPLL lock detect	Temperature alarm	0xXX	R
0x3003	Temperature readback	Internal temperature [7:0]								0xXX	R
0x3004	Temperature readback	Internal temperature [15:8]								0xXX	R
0x3005	REFA status	Reserved		REFA LOS	REFA valid	REFA fault	REFA excess jitter	REFA fast	REFA slow	0xXX	R
0x3006	REFAA status	Reserved		REFAA LOS	REFAA valid	REFAA fault	REFAA excess jitter	REFAA fast	REFAA slow	0xXX	R
0x3007	REFB status	Reserved		REFB LOS	REFB valid	REFB fault	REFB excess jitter	REFB fast	REFB slow	0xXX	R
0x3008	REFBB status	Reserved		REFBB LOS	REFBB valid	REFBB fault	REFBB excess jitter	REFBB fast	REFBB slow	0xXX	R
0x3009	DPLL0 active profile	Reserved		DPLL0 Profile 5 active	DPLL0 Profile 4 active	DPLL0 Profile 3 active	DPLL0 Profile 2 active	DPLL0 Profile 1 active	DPLL0 Profile 0 active	0xXX	R
0x300A	DPLL1 active profile	Reserved		DPLL1 Profile 5 active	DPLL1 Profile 4 active	DPLL1 Profile 3 active	DPLL1 Profile 2 active	DPLL1 Profile 1 active	DPLL1 Profile 0 active	0xXX	R

Table 97. Status Readback Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3000	EEPROM status	[7:4]	Reserved		Reserved.	0x0	R
		3	EEPROM CRC error		EEPROM CRC error detected. A Logic 1 indicates a CRC error occurred during an EEPROM operation. This bit is in a live register, meaning an IO_UPDATE command is not needed while polling this register. If an EEPROM fault is detected, this bit remains Logic 1 until the next EEPROM operation.	0x0	R
		2	EEPROM fault		EEPROM general fault detected. A Logic 1 indicates that a general EEPROM error occurred during an EEPROM operation. This bit is in a live register, meaning an IO_UPDATE command is not needed while polling this register. If an EEPROM fault is detected, this bit remains Logic 1 until the next EEPROM operation.	0x0	R
		1	EEPROM load in progress		EEPROM load in progress. A Logic 1 indicates that a load from EEPROM operation is in progress. This bit is in a live register, meaning an IO_UPDATE command is not needed while polling this register.	0x0	R
		0	EEPROM save in progress		EEPROM save in progress. A Logic 1 indicates that a save to EEPROM operation is in progress. This bit is in a live register, meaning that an IO_UPDATE command is not needed while polling this register.	0x0	R
0x3001	SYSCLK and PLL status	[7:6]	Reserved		Reserved.	0x0	R
		5	PLL1 locked		DPLL1 and APLL1 locked. A Logic 1 indicates that both Channel 1 PLLs (DPLL1 and APLL0) are locked. This bit is the logical AND of system clock lock detect, APLL1 lock detect, DPLL1 frequency, and DPLL1 PLD. This bit is in a live register, meaning that an IO_UPDATE command is not needed prior to reading.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	PLL0 locked		DPLL0 and APLL0 locked. A Logic 1 indicates that both Channel 0 PLLs (DPLL0 and APLL0) are locked. This bit is the logical AND of system clock lock detect, APLL0 lock detect, DPLL0 frequency, and DPLL0 PLD. This bit is in a live register, meaning that an IO_UPDATE command is not needed prior to reading.	Prog	RP
		3	Reserved		Reserved.	0x0	R
		2	SYSCLK calibration busy		System clock calibration in progress. A Logic 1 indicates that the system clock VCO is calibrating. This status bit is in a live register, meaning that an IO_UPDATE command is not required prior to reading.	Prog	RP
		1	SYSCLK stable		System clock stable. A Logic 1 indicates that the system clock PLL is stable, meaning that the system clock PLL has been locked for at least as long as the value programmed into the system clock stability timer bit field. This status bit is in a live register, meaning that an IO_UPDATE command is not required prior to reading.	Prog	RP
		0	SYSCLK locked		System clock PLL locked. A Logic 1 indicates that the system clock PLL is locked. This status bit is in a live register, meaning that an IO_UPDATE command is not required prior to reading.	Prog	RP
0x3002	Miscel-laneous status	[7:3]	Reserved		Reserved.	Prog	R
		2	Auxiliary DPLL reference fault		Auxiliary DPLL reference fault. This bit indicates an out of range reference fault of the auxiliary DPLL. Logic 0: auxiliary DPLL reference fault is not detected. Logic 1: auxiliary DPLL reference fault is detected.	Prog	RP
		1	Auxiliary DPLL lock detect		Auxiliary DPLL lock detect. This bit indicates the status of the auxiliary DPLL, which calculates an offset to compensate for any frequency error in the system clock PLL. Logic 0: auxiliary DPLL is not locked. Logic 1: auxiliary DPLL is locked.	Prog	RP
		0	Temperature alarm		Temperature alarm. A Logic 1 indicates that the temperature sensor detected a temperature that is outside of the range programmed into the high temperature threshold and low temperature threshold. This status bit is a buffered register, meaning that an IO_UPDATE command is required prior to reading to read back the latest value.	Prog	RP
0x3003	Temperature readback	[7:0]	Internal temperature [7:0]		Internal temperature. This signed, 16-bit bit field contains the internal temperature of the device. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The temperature reading is computed by multiplying the value in this bit field by 2^{-7} and is in degrees Celsius. The sensor samples at approximately 6.1 kHz. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required prior to reading to read back the latest value. The sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, if the internal temperature reads 0xF833 (−1997 decimal), T = −1997 × 2^{-7}°C = −15.6°C.	Prog	RP
0x3004	Temperature readback	[7:0]	Internal temperature [15:8]		Internal temperature. This signed, 16-bit bit field contains the internal temperature of the device. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The temperature reading is computed by multiplying the value in this bit field by 2^{-7} and is in degrees Celsius. The sensor samples at approximately 6.1 kHz. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required prior to reading to read back the latest value. The sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, if the internal temperature reads 0xF833 (−1997 decimal), T = −1997 × 2^{-7}°C = −15.6°C.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3005	REFA status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFA LOS		REFA loss of signal (LOS). A Logic 1 indicates a REFA LOS. This bit is in a buffered register, meaning the user must issue an IO_UPDATE command prior to reading to read back the latest value. The value of this bit can change dynamically; instead of monitoring this bit, monitor the REFA fault bit in this register, which remains high whenever REFA is faulted (due to any type of fault).	0x0	R
		4	REFA valid		REFA frequency valid. A Logic 1 indicates that the period of the REFA clock is within the range allowed by the REFA nominal period and the REFA offset limit settings for at least as long as the REFA validation timer setting. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFA fault		REFA fault. A Logic 1 indicates that the REFA clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFA LOS, REFA fast, REFA slow, and REFA excess jitter bits. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFA excess jitter		Excess jitter detected on REFA. A Logic 1 indicates that the jitter of the REFA clock is higher than allowed by its profile settings as specified in the REFA jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		1	REFA fast		REFA frequency is above upper limit. A Logic 1 indicates that the frequency of the REFA clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading. If the REFA clock is missing, the REFA fast and REFA slow bits in this register can both be Logic 1.	0x0	R
		0	REFA slow		REFA frequency is below lower limit. A Logic 1 indicates that the frequency of the REFA clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFA clock is missing, the REFA fast and REFA slow bits in this register can both be Logic 1.	0x0	R
0x3006	REFAA status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFAA LOS		REFAA LOS. A Logic 1 indicates a REFAA LOS. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command prior to reading to read back the latest value. The value of this bit can change dynamically; instead of monitoring this bit, monitor the REFAA fault bit in this register, which remains high whenever REFAA is faulted (due to any type of fault).	0x0	R
		4	REFAA valid		REFAA frequency valid. A Logic 1 indicates that the period of the REFAA clock is within the range allowed by the REFAA nominal period and REFAA offset limit settings for at least as long as the REFAA validation timer setting. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFAA fault		REFAA fault. A Logic 1 indicates that the REFAA clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFAA LOS, REFAA fast, REFAA slow, and REFAA excess jitter bits. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFAA excess jitter		Excess jitter detected on REFAA. A Logic 1 indicates that the jitter of the REFAA clock is higher than allowed by its profile settings as specified in the REFAA jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		1	REFAA fast		REFAA frequency is above upper limit. A Logic 1 indicates that the frequency of the REFAA clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFAA clock is missing, the REFAA fast and REFAA slow bits in this register can both be Logic 1.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	REFAA slow		REFAA frequency is below lower limit. A Logic 1 indicates the frequency of the REFAA clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFAA clock is missing, the REFAA fast and REFAA slow bits in this register can both be Logic 1.	0x0	R
0x3007	REFB status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFB LOS		REFB LOS. A Logic 1 indicates a REFB LOS. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command prior to reading to read back the latest value. The value of this bit can change dynamically, so instead of monitoring this bit, monitor the REFB fault bit in this register, which remains high whenever REFB is faulted (due to any type of fault).	0x0	R
		4	REFB valid		REFB frequency valid. A Logic 1 indicates that the period of the REFB clock is within the range allowed by the REFB nominal period and REFB offset limit settings for at least as long as the REFB validation timer setting. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFB fault		REFB fault. A Logic 1 indicates that the REFB clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFB LOS, REFB fast, REFB slow, and REFB excess jitter bits. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFB excess jitter		Excess jitter detected on REFB. A Logic 1 indicates that the jitter of the REFB clock is higher than allowed by its profile settings as specified in the REFB jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		1	REFB fast		REFB frequency is above upper limit. A Logic 1 indicates that the frequency of the REFB clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFB clock is missing, the REFB fast and REFB slow bits in this register can both be Logic 1.	0x0	R
		0	REFB slow		REFB frequency is below lower limit. A Logic 1 indicates the frequency of the REFB clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFB clock is missing, the REFB fast and REFB slow bits in this register can both be Logic 1.	0x0	R
0x3008	REFBB status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFBB LOS		REFBB LOS. A Logic 1 indicates a REFBB LOS. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command prior to reading to read back the latest value. The value of this bit can change dynamically, so instead of monitoring this bit, monitor the REFB fault bit in this register, which remains high whenever REFBB is faulted (due to any type of fault).	0x0	R
		4	REFBB valid		REFBB frequency valid. A Logic 1 indicates that the period of the REFBB clock is within the range allowed by the REFBB nominal period and REFBB offset limit settings for at least as long as the REFBB validation timer setting. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFBB fault		REFBB fault. A Logic 1 indicates that the REFBB clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFBB LOS, REFBB fast, REFBB slow, and REFBB excess jitter bits. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFBB excess jitter		Excess jitter detected on REFBB. A Logic 1 indicates that the jitter of the REFBB clock is higher than allowed by its profile settings as specified in the REFBB jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	REFBB fast		REFBB frequency is above upper limit. A Logic 1 indicates that the frequency of the REFBB clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFBB clock is missing, the REFBB fast and REFBB slow bits in this register can both be Logic 1.	0x0	R
		0	REFBB slow		REFBB frequency is below lower limit. A Logic 1 indicates the frequency of the REFBB clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFBB clock is missing, the REFBB fast and REFBB slow bits in this register can both be Logic 1.	0x0	R
0x3009	DPLL0 active profile	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 Profile x active		Active translation profile for DPLL0.	0x0	R
				000000	DPLL0 does not have an active translation profile.		
				000001	DPLL0 Translation Profile 0.0 is active.		
				000010	DPLL0 Translation Profile 0.1 is active.		
				000100	DPLL0 Translation Profile 0.2 is active.		
				001000	DPLL0 Translation Profile 0.3 is active.		
				010000	DPLL0 Translation Profile 0.4 is active.		
				100000	DPLL0 Translation Profile 0.5 is active.		
0x300A	DPLL1 active profile	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL1 Profile x active		Active translation profile for DPLL1.	0x0	R
				000000	DPLL1 does not have an active translation profile.		
				000001	DPLL1 Translation Profile 1.0 is active.		
				000010	DPLL1 Translation Profile 1.1 is active.		
				000100	DPLL1 Translation Profile 1.2 is active.		
				001000	DPLL1 Translation Profile 1.3 is active.		
				010000	DPLL1 Translation Profile 1.4 is active.		
				100000	DPLL1 Translation Profile 1.5 is active.		

IRQ MAP COMMON READ REGISTERS—REGISTER 0x300B TO REGISTER 0x300F

Table 98. IRQ Map Common Read Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x300B	System clock (SYSCLK)	SYSCLK unlocked	SYSCLK stabilized	SYSCLK locked	SYSCLK calibration deactivated	SYSCLK calibration activated	Watchdog timeout occurred	EEPROM faulted	EEPROM completed	0x00	R
0x300C	Auxiliary DPLL	Reserved		Skew limit exceeded	Temperature warning occurred	Auxiliary DPLL unfaulted	Auxiliary DPLL faulted	Auxiliary DPLL unlocked	Auxiliary DPLL locked	0x00	R
0x300D	REFA	REFAA R divider resynced	REFAA validated	REFAA unfaulted	REFAA faulted	REFA R divider resynced	REFA validated	REFA unfaulted	REFA faulted	0x00	R
0x300E	REFB	REFBB R divider resynced	REFBB validated	REFBB unfaulted	REFBB faulted	REFB R divider resynced	REFB validated	REFB unfaulted	REFB faulted	0x00	R

Table 99. IRQ Map Common Read Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x300B	System clock (SYSCLK)	7	SYSCLK unlocked		System clock unlocked. Read only status of the SYSCLK unlocked IRQ.	0x0	R
		6	SYSCLK stabilized		System clock stable. Read only status of the SYSCLK stabilized IRQ.	0x0	R
		5	SYSCLK locked		System clock locked. Read only status of the SYSCLK locked IRQ.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	SYSCLK calibration deactivated		System clock calibration deactivated. Read only status of the SYSCLK calibration deactivated IRQ.	0x0	R
		3	SYSCLK calibration activated		System clock calibration activated. Read only status of the SYSCLK calibration activated IRQ.	0x0	R
		2	Watchdog timeout occurred		Watchdog timeout occurred. Read only status of the watchdog timer timeout IRQ.	0x0	R
		1	EEPROM faulted		EEPROM faulted. Read only status of the EEPROM faulted IRQ.	0x0	R
		0	EEPROM completed		EEPROM operation complete. Read only status of the EEPROM operation complete IRQ.	0x0	R
0x300C	Auxiliary DPLL	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew limit exceeded		Skew limit exceeded. Read only status of the reference input skew measurement limit exceeded IRQ.	0x0	R
		4	Temperature warning occurred		Temperature range warning.	0x0	R
		3	Auxiliary DPLL unfaulted		Closed-loop SYSCLK compensation DPLL unfaulted. Read only status of the auxiliary DPLL unfaulted IRQ.	0x0	R
		2	Auxiliary DPLL faulted		Closed-loop SYSCLK compensation DPLL faulted. Read only status of the auxiliary DPLL faulted IRQ.	0x0	R
		1	Auxiliary DPLL unlocked		Closed-loop SYSCLK compensation DPLL unlocked. Read only status of the auxiliary DPLL unlocked IRQ.	0x0	R
		0	DPLL locked		Closed-loop SYSCLK compensation DPLL locked. Read only status of the auxiliary DPLL locked IRQ.	0x0	R
0x300D	REFA	7	REFAA R divider resynced		REFAA R divider resynced. Read only status of the REFAA R divider resynced IRQ.	0x0	R
		6	REFAA validated		REFAA validated. Read only status of the REFAA validated IRQ.	0x0	R
		5	REFAA unfaulted		REFAA unfaulted. Read only status of the REFAA unfaulted IRQ.	0x0	R
		4	REFAA faulted		REFAA faulted. Read only status of the REFAA faulted IRQ.	0x0	R
		3	REFA R divider resynced		REFA R divider resynced. Read only status of the REFA R divider resynced IRQ.	0x0	R
		2	REFA validated		REFA validated. Read only status of the REFA validated IRQ.	0x0	R
		1	REFA unfaulted		REFA unfaulted. Read only status of the REFA unfaulted IRQ.	0x0	R
		0	REFA faulted		REFA faulted. Read only status of the REFA faulted IRQ.	0x0	R
0x300E	REFB	7	REFBB R divider resynced		REFBB R divider resynced. Read only status of the REFBB R divider resynced IRQ.	0x0	R
		6	REFBB validated		REFBB validated. Read only status of the REFBB validated IRQ.	0x0	R
		5	REFBB unfaulted		REFBB unfaulted. Read only status of the REFBB unfaulted IRQ.	0x0	R
		4	REFBB faulted		REFBB faulted. Read only status of the REFBB faulted IRQ.	0x0	R
		3	REFB R divider resynced		REFB R divider resynced. Read only status of the REFB R divider resynced IRQ.	0x0	R
		2	REFB validated		REFB validated. Read only status of the REFB validated IRQ.	0x0	R
		1	REFB unfaulted		REFB unfaulted. Read only status of the REFB unfaulted IRQ.	0x0	R
		0	REFB faulted		REFB faulted. Read only status of the REFB faulted IRQ.	0x0	R

IRQ MAP DPLL0 READ REGISTERS—REGISTER 0x3010 TO REGISTER 0x3014

Table 100. IRQ Map DPLL0 Read Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3010	Lock	DPLL0 frequency clamp deactivated	DPLL0 frequency clamp activated	DPLL0 phase slew limiter deactivated	DPLL0 phase slew limiter activated	DPLL0 frequency unlocked	DPLL0 frequency locked	DPLL0 phase unlocked	DPLL0 phase locked	0x00	R
0x3011	State	DPLL0 reference switched	DPLL0 freerun entered	DPLL0 holdover entered	DPLL0 hitless entered	DPLL0 hitless exited	DPLL0 history updated	Reserved	DPLL0 phase step detected	0x00	R
0x3012	Fast acqui-sition	Reserved			DPLL0 N-divider resynced	DPLL0 fast acquisition completed	DPLL0 fast acquisition started	Reserved		0x00	R
0x3013	Active profile	Reserved		DPLL0 Profile 5 activated	DPLL0 Profile 4 activated	DPLL0 Profile 3 activated	DPLL0 Profile 2 activated	DPLL0 Profile 1 activated	DPLL0 Profile 0 activated	0x00	R
0x3014	APLL	Reserved			DPLL0 distribution sync	APLL0 unlocked	APLL0 locked	APLL0 calibration completed	APLL0 calibration started	0x00	R

Table 101. IRQ Map DPLL0 Read Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3010	Lock	7	DPLL0 frequency clamp deactivated		Frequency clamp deactivated. Read only status of the IRQ for DPLL0 frequency clamp deactivated.	0x0	R
		6	DPLL0 frequency clamp activated		Frequency clamp activated. Read only status of the IRQ for DPLL0 frequency clamp activated.	0x0	R
		5	DPLL0 phase slew limiter deactivated		Phase slew limiter deactivated. Read only status of the IRQ for DPLL0 phase slew limiter deactivated.	0x0	R
		4	DPLL0 phase slew limiter activated		Phase slew limiter activated. Read only status of the IRQ for DPLL0 phase slew limiter activated.	0x0	R
		3	DPLL0 frequency unlocked		Frequency unlocked. Read only status of the IRQ for DPLL0 FLD (lock to unlock transition).	0x0	R
		2	DPLL0 frequency locked		Frequency locked. Read only status of the IRQ for DPLL0 FLD (unlock to lock transition).	0x0	R
		1	DPLL0 phase unlocked		Phase unlocked. Read only status of the IRQ for DPLL0 PLD (lock to unlock transition).	0x0	R
		0	DPLL0 phase locked		Phase locked. Read only status of the IRQ for DPLL0 PLD (unlock to lock transition).	0x0	R
0x3011	State	7	DPLL0 reference switched		Reference switched. Read only status of the IRQ for DPLL0 reference input switched.	0x0	R
		6	DPLL0 freerun entered		Freerun mode entered. Read only status of the IRQ for DPLL0 freerun mode entered.	0x0	R
		5	DPLL0 holdover entered		Holdover mode entered. Read only status of the IRQ for DPLL0 holdover mode entered.	0x0	R
		4	DPLL0 hitless entered		Hitless mode entered. Read only status of the IRQ for DPLL0 hitless mode entered.	0x0	R
		3	DPLL0 hitless exited		Hitless mode exited. Read only status of the IRQ for DPLL0 hitless mode exited.	0x0	R
		2	DPLL0 history updated		Holdover history updated. Read only status of the IRQ for DPLL0 tuning word holdover history updated.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DPLL0 phase step detected		Phase step detected. Read only status of the IRQ for DPLL0 reference input phase step detected.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3012	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 N-divider resynced		N-divider resynchronized. Read only status of the IRQ for DPLL0 N-divider resynced.	0x0	R
		3	DPLL0 fast acquisition completed		Fast acquisition completed. Read only status of the IRQ for DPLL0 fast acquisition completed.	0x0	R
		2	DPLL0 fast acquisition started		Fast acquisition started. Read only status of the IRQ for DPLL0 fast acquisition started.	0x0	R
		[1:0]	Reserved		Reserved.	0x0	R
0x3013	Active profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 Profile 5 activated		Profile 5 activated. Read only status of the IRQ for DPLL0 Profile 5 activated.	0x0	R
		4	DPLL0 Profile 4 activated		Profile 4 activated. Read only status of the IRQ for DPLL0 Profile 4 activated.	0x0	R
		3	DPLL0 Profile 3 activated		Profile 3 activated. Read only status of the IRQ for DPLL0 Profile 3 activated.	0x0	R
		2	DPLL0 Profile 2 activated		Profile 2 activated. Read only status of the IRQ for DPLL0 Profile 2 activated.	0x0	R
		1	DPLL0 Profile 1 activated		Profile 1 activated. Read only status of the IRQ for DPLL0 Profile 1 activated.	0x0	R
		0	DPLL0 Profile 0 activated		Profile 0 activated. Read only status of the IRQ for DPLL0 Profile 0 activated.	0x0	R
0x3014	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 distribution sync		Clock distribution synced. Read only status of the IRQ for DPLL0 clock distribution synced.	0x0	R
		3	APLL0 unlocked		Unlock detect. Read only status of the IRQ for APLL0 lock detect (lock to unlock transition).	0x0	R
		2	APLL0 locked		Lock detect. Read only status of the IRQ for APLL0 lock detect (unlock to lock transition).	0x0	R
		1	APLL0 calibration completed		Calibration completed. Read only status of the IRQ for APLL0 calibration completed.	0x0	R
		0	APLL0 calibration started		Calibration started. Read only status of the IRQ for APLL0 calibration started.	0x0	R

IRQ MAP DPLL1 READ REGISTERS—REGISTER 0x3015 TO REGISTER 0x3019

Table 102. IRQ Map DPLL1 Read Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3015	Lock	DPLL1 frequency clamp deactivated	DPLL1 frequency clamp activated	DPLL1 phase slew limiter deactivated	DPLL1 phase slew limiter activated	DPLL1 frequency unlocked	DPLL1 frequency locked	DPLL1 phase unlocked	DPLL1 phase locked	0x00	R
0x3016	State	DPLL1 reference switched	DPLL1 freerun entered	DPLL1 holdover entered	DPLL1 hitless entered	DPLL1 hitless exited	DPLL1 history updated	Reserved	DPLL1 phase step detected	0x00	R
0x3017	Fast acqui-sition	Reserved			DPLL1 N-divider resynced	DPLL1 fast acquisition completed	DPLL1 fast acquisition started	Reserved		0x00	R
0x3018	Active profile	Reserved		DPLL1 Profile 5 activated	DPLL1 Profile 4 activated	DPLL1 Profile 3 activated	DPLL1 Profile 2 activated	DPLL1 Profile 1 activated	DPLL1 Profile 0 activated	0x00	R
0x3019	APLL	Reserved			DPLL1 distribution sync	APLL1 unlocked	APLL1 locked	APLL1 calibration completed	APLL1 calibration started	0x00	R

Table 103. IRQ Map DPLL1 Read Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3015	Lock	7	DPLL1 frequency clamp deactivated		Frequency clamp deactivated. Read only status of the IRQ for DPLL1 frequency clamp deactivated.	0x0	R
		6	DPLL1 frequency clamp activated		Frequency clamp activated. Read only status of the IRQ for DPLL1 frequency clamp activated.	0x0	R
		5	DPLL1 phase slew limiter deactivated		Phase slew limiter deactivated. Read only status of the IRQ for DPLL1 phase slew limiter deactivated.	0x0	R
		4	DPLL1 phase slew limiter activated		Phase slew limiter activated. Read only status of the IRQ for DPLL1 phase slew limiter activated.	0x0	R
		3	DPLL1 frequency unlocked		Frequency unlocked. Read only status of the IRQ for DPLL1 FLD (lock to unlock transition).	0x0	R
		2	DPLL1 frequency locked		Frequency locked. Read only status of the IRQ for DPLL1 FLD (unlock to lock transition).	0x0	R
		1	DPLL1 phase unlocked		Phase unlocked. Read only status of the IRQ for DPLL1 PLD (lock to unlock transition).	0x0	R
		0	DPLL1 phase locked		Phase locked. Read only status of the IRQ for DPLL1 PLD (unlock to lock transition).	0x0	R
0x3016	State	7	DPLL1 reference switched		Reference switched. Read only status of the IRQ for DPLL1 reference input switched.	0x0	R
		6	DPLL1 freerun entered		Freerun mode entered. Read only status of the IRQ for DPLL1 freerun mode entered.	0x0	R
		5	DPLL1 holdover entered		Holdover mode entered. Read only status of the IRQ for DPLL1 holdover mode entered.	0x0	R
		4	DPLL1 hitless entered		Hitless mode entered. Read only status of the IRQ for DPLL1 hitless mode entered.	0x0	R
		3	DPLL1 hitless exited		Hitless mode exited. Read only status of the IRQ for DPLL1 hitless mode exited.	0x0	R
		2	DPLL1 history updated		Holdover history updated. Read only status of the IRQ for DPLL1 tuning word holdover history updated.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DPLL1 phase step detect		Phase step detected. Read only status of the IRQ for DPLL1 reference input phase step detected	0x0	R
0x3017	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 N-divider resynced		N-divider resynchronized. Read only status of the IRQ for DPLL1 N-divider resynchronization.	0x0	R
		3	DPLL1 fast acquisition completed		Fast acquisition completed. Read only status of the IRQ for DPLL1 fast acquisition completed.	0x0	R
		2	DPLL1 fast acquisition started		Fast acquisition started. Read only status of the IRQ for DPLL1 fast acquisition started.	0x0	R
		[1:0]	Reserved		Reserved.	0x0	R
0x3018	Active profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 Profile 5 activated		Profile 5 activated. Read only status of the IRQ for DPLL1 Profile 5 activated.	0x0	R
		4	DPLL1 Profile 4 activated		Profile 4 activated. Read only status of the IRQ for DPLL1 Profile 4 activated.	0x0	R
		3	DPLL1 Profile 3 activated		Profile 3 activated. Read only status of the IRQ for DPLL1 Profile 3 activated.	0x0	R
		2	DPLL1 Profile 2 activated		Profile 2 activated. Read only status of the IRQ for DPLL1 Profile 2 activated.	0x0	R
		1	DPLL1 Profile 1 activated		Profile 1 activated. Read only status of the IRQ for DPLL1 Profile 1 activated.	0x0	R
		0	DPLL1 Profile 0 activated		Profile 0 activated. Read only status of the IRQ for DPLL1 Profile 0 activated.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3019	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 distribution sync		Clock distribution synchronized. Read only status of the IRQ for DPLL1 clock distribution synchronized.	0x0	R
		3	APLL1 unlocked		Unlock detect. Read only status of the IRQ for APLL1 lock detect (lock to unlock transition).	0x0	R
		2	APLL1 locked		Lock detect. Read only status of the IRQ for APLL1 lock detect (unlock to lock transition).	0x0	R
		1	APLL1 calibration completed		Calibration completed. Read only status of the IRQ for APLL1 calibration completed.	0x0	R
		0	APLL1 calibration started		Calibration started. Read only status of the IRQ for APLL1 calibration started.	0x0	R

STATUS READBACK PLL0 REGISTERS—REGISTER 0x3100 TO REGISTER 0x310E

Table 104. STATUS_READBACK_PLL_0 Register Summary

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3100	DPLL0 lock status	Reserved		APLL0 calibration done	APLL0 calibration busy	APLL0 lock	DPLL0 frequency lock	DPLL0 phase lock	Channel 0 all lock	0xXX	R
0x3101	DPLL0 operation	Reserved	DPLL0 active profile			DPLL0 active	DPLL0 reference switch	DPLL0 holdover	DPLL0 freerun	0xXX	R
0x3102	DPLL0 state	Reserved		DPLL0 FACQ done	DPLL0 FACQ active	Reserved	DPLL0 phase slew limit	DPLL0 frequency clamped	DPLL0 history available	0xXX	R
0x3103	DPLL0 tuning word history	DPLL0 tuning word history [7:0]								0xXX	R
0x3104		DPLL0 tuning word history [15:8]								0xXX	R
0x3105		DPLL0 tuning word history [23:16]								0xXX	R
0x3106		DPLL0 tuning word history [31:24]								0xXX	R
0x3107		DPLL0 tuning word history [39:32]								0xXX	R
0x3108		Reserved		DPLL0 tuning word history [45:40]						0xXX	R
0x3109	DPLL0 PLD tub	DPLL0 PLD tub [7:0]								0xXX	R
0x310A		Reserved				DPLL0 PLD tub [11:8]				0x0X	R
0x310B	DPLL0 FLD tub	DPLL0 FLD tub[7:0]								0xXX	R
0x310C		Reserved				DPLL0 FLD tub [11:8]				0x0X	R
0x310D	Channel 0 distribution phase slew active	Reserved		DPLL0 phase slew enable						0xXX	R
0x310E	Channel 0 distribution phase slew error	Reserved		DPLL0 phase control error						0xXX	R

In Table 105, prog in the reset column and RP in the access column mean the bit is read only and live (IO_UPDATE command not needed to read the latest status.)

Table 105. STATUS_READBACK_PLL_0 Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3100	DPLL0 lock status	[7:6]	Reserved		Reserved.	0x0	R
		5	APLL0 calibration done		APLL0 calibration complete. This read only bit is Logic 1 when APLL0 calibration is complete. This bit remains Logic 1 until another APLL0 calibration is issued. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		4	APLL0 calibration busy		APLL0 calibration in progress. This read only bit is Logic 1 when APLL0 calibration is in progress. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		3	APLL0 lock		APLL0 lock. This read only bit is Logic 1 when APLL0 is locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		2	DPLL0 frequency lock		DPLL0 frequency lock. This read only bit is Logic 1 when DPLL0 is frequency locked. All of the bits in this register are live, meaning that their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		1	DPLL0 phase lock		DPLL0 phase lock. This read only bit is Logic 1 when DPLL0 is phase locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		0	Channel 0 all lock		Channel 0 all lock. This read only bit is the logical AND of the APLL0 lock and the DPLL0 phase lock bits in this register. It is Logic 1 when both PLLs are locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
0x3101	DPLL0 operation	7	Reserved		Reserved.	0x0	R
		[6:4]	DPLL0 active profile		DPLL0 active profile. This 3-bit bit field contains the active profile for DPLL0. If DPLL0 is not active, this bit field contains the last active profile. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		3	DPLL0 active		DPLL0 active. This read only bit is Logic 1 when DPLL0 is actively tracking an input reference. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		2	DPLL0 reference switch		DPLL0 input reference switching. This read only bit is Logic 1 when DPLL0 is switching input references. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL0 holdover		DPLL0 is in holdover mode. This read only bit is Logic 1 when DPLL0 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL0 freerun		DPLL0 is in freerun mode. This read only bit is Logic 1 when DPLL0 is in freerun mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3102	DPLL0 state	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 FACQ done		DPLL0 fast acquisition done. This read only bit is Logic 1 when the DPLL0 fast acquisition is completed is complete. It is cleared by writing Logic 1 to the clear DPLL0 fast acquisition done bit. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		4	DPLL0 FACQ active		DPLL0 fast acquisition active. This read only bit is Logic 1 when the DPLL0 fast acquisition logic is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	Reserved		Reserved.	Prog	RP
		2	DPLL0 phase slew limit		DPLL0 phase slew limiter active. This read only bit is Logic 1 when the DPLL0 phase slew limiter is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL0 frequency clamped		DPLL0 frequency clamp is active. This read only bit is Logic 1 when the DPLL0 frequency clamp is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL0 history available		DPLL0 history available. This read only bit is Logic 1 when the DPLL0 holdover history is available. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3103	DPLL0 tuning word history	[7:0]	DPLL0 tuning word history [7:0]		DPLL0 tuning word history. This 46-bit bit field contains the DPLL0 tuning word history that is used while DPLL0 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3104		[7:0]	DPLL0 tuning word history [15:8]			Prog	RP
0x3105		[7:0]	DPLL0 tuning word history [23:16]			Prog	RP
0x3106		[7:0]	DPLL0 tuning word history [31:24]			Prog	RP
0x3107		[7:0]	DPLL0 tuning word history [39:32]			Prog	RP
0x3108		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 tuning word history [45:40]		DPLL0 tuning word history. This 46-bit bit field contains the DPLL0 tuning word history that is used while DPLL0 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3109	DPLL0 PLD tub	[7:0]	DPLL0 PLD tub [7:0]		DPLL0 PLD tub level. This 12-bit bit field contains the DPLL0 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310A		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL0 PLD tub [11:8]		DPLL0 PLD tub level. This 12-bit bit field contains the DPLL0 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310B	DPLL0 FLD tub	[7:0]	DPLL0 FLD tub [7:0]		DPLL0 FLD tub level. This 12-bit bit field contains the DPLL0 FLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310C		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL0 FLD tub [11:8]		DPLL0 FLD tub level. This 12-bit bit field contains the DPLL0 FLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310D	Channel 0 distribution phase slew active	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 phase slew enable		Channel 0 phase slewing active. This 6-bit bit field contains read only bits that are Logic 1 when phase slewing is active on the DPLL0 Q0x dividers, where x is A, AA, B, BB, C, and CC (the C and CC dividers are on Channel 0 only). An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows:	Prog	RP
				0	Logic 1 when phase slewing is active on Divider Q0A.		
				1	Logic 1 when phase slewing is active on Divider Q0AA.		
				2	Logic 1 when phase slewing is active on Divider Q0B.		
				3	Logic 1 when phase slewing is active on Divider Q0BB.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				4	Logic 1 when phase slewing is active on Divider Q0C.		
				5	Logic 1 when phase slewing is active on Divider Q0CC.		
0x310E	Channel 0 distribution phase slew error	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 phase control error		Channel 0 distribution phase control error. This 6-bit bit field contains read only bits that are Logic 1 when the distribution phase slewing logic on the Channel 1 Q0x divider (where x is A, AA, B, BB, C, and CC) is unable to complete the requested phase adjustment. An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows:	Prog	RP
				0	Logic 1 indicates a phase slewing error on Divider Q0A.		
				1	Logic 1 indicates a phase slewing error on Divider Q0AA.		
				2	Logic 1 indicates a phase slewing error on Divider Q0B.		
				3	Logic 1 indicates a phase slewing error on Divider Q0BB.		
				4	Logic 1 indicates a phase slewing error on Divider Q0C.		
				5	Logic 1 indicates a phase slewing error on Divider Q0CC.		

STATUS READBACK PLL1 REGISTERS—REGISTER 0x3200 TO REGISTER 0x320E

Table 106. STATUS_READBACK_PLL_1 Register Summary

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3200	DPLL1 lock status	Reserved		APLL1 calibration done	APLL1 calibration busy	APLL1 lock	DPLL1 frequency lock	DPLL1 phase lock	Channel 1 all lock	0xXX	R
0x3201	DPLL1 operation	Reserved	DPLL1 active profile			DPLL1 active	DPLL1 reference switch	DPLL1 holdover	DPLL1 freerun	0xXX	R
0x3202	DPLL1 state	Reserved		DPLL1 FACQ done	DPLL1 FACQ active	Reserved	DPLL1 phase slew limit	DPLL1 frequency clamped	DPLL1 history available	0xXX	R
0x3203	DPLL1 tuning word history	DPLL1 tuning word history [7:0]								0xXX	R
0x3204		DPLL1 tuning word history [15:8]								0xXX	R
0x3205		DPLL1 tuning word history [23:16]								0xXX	R
0x3206		DPLL1 tuning word history [31:24]								0xXX	R
0x3207		DPLL1 tuning word history [39:32]								0xXX	R
0x3208		Reserved		DPLL1 tuning word history [45:40]						0xXX	R
0x3209	DPLL1 PLD tub	DPLL1 PLD tub [7:0]								0xXX	R
0x320A		Reserved				DPLL1 PLD tub [11:8]				0x0X	R
0x320B	DPLL1 FLD tub	DPLL1 FLD tub [7:0]								0xXX	R
0x320C		Reserved				DPLL1 FLD tub [11:8]				0x0X	R
0x320D	Channel 1 distribution phase slew active	Reserved				DPLL1 phase slew enable				0x0X	R
0x320E	Channel 1 distribution phase slew error	Reserved				DPLL1 phase control error				0x0X	R

In Table 107, prog in the reset column and RP in the access column mean the bit is read only and live (IO_UPDATE command not needed to read the latest status.)

Table 107. STATUS_READBACK_PLL_1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3200	DPLL1 lock status	[7:6]	Reserved		Reserved.	0x0	R
		5	APLL1 calibration done		APLL1 calibration complete. This read only bit is Logic 1 when APLL1 calibration is complete. This bit remains Logic 1 until another APLL1 calibration is issued. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE before reading.	Prog	RP
		4	APLL1 calibration busy		APLL1 calibration in progress. This read only bit is Logic 1 when APLL1 calibration is in progress. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE before reading.	Prog	RP
		3	APLL1 lock		APLL1 lock. This read only bit is Logic 1 when APLL1 is locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE before reading.	Prog	RP
		2	DPLL1 frequency lock		DPLL1 frequency lock. This read only bit is Logic 1 when DPLL1 is frequency locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE before reading.	Prog	RP
		1	DPLL1 phase lock		DPLL1 phase lock. This read only bit is Logic 1 when DPLL1 is phase locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE before reading.	Prog	RP
		0	Channel 1 all lock		Channel 1 all lock. This read only bit is the logical AND of the APLL1 lock and the DPLL1 phase lock bits in this register. It is Logic 1 when both PLLs are locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE before reading.	Prog	RP
0x3201	DPLL1 operation	7	Reserved		Reserved.	0x0	R
		[6:4]	DPLL1 active profile		DPLL1 active profile. This 3-bit bit field contains the active profile for DPLL1. If DPLL1 is not active, this bit field contains the last active profile. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		3	DPLL1 active		DPLL1 active. This read only bit is Logic 1 when DPLL1 is actively tracking an input reference. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		2	DPLL1 reference switch		DPLL1 input reference switching. This read only bit is Logic 1 when DPLL1 is switching input references. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL1 holdover		DPLL1 is in holdover mode. This read only bit is Logic 1 when DPLL1 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL1 freerun		DPLL1 is in freerun mode. This read only bit is Logic 1 when DPLL1 is in freerun mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3202	DPLL1 state	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 FACQ done		DPLL1 fast acquisition done. This read only bit is Logic 1 when the DPLL1 fast acquisition is complete. It is cleared by writing Logic 1 to the clear DPLL1 fast acquisition done bit. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		4	DPLL1 FACQ active		DPLL1 fast acquisition active. This read only bit is Logic 1 when the DPLL1 fast acquisition logic is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		3	Reserved		Reserved.	Prog	RP
		2	DPLL1 phase slew limit		DPLL1 phase slew limiter active. This read only bit is Logic 1 when the DPLL1 phase slew limiter is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL1 frequency clamped		DPLL1 frequency clamp is active. This read only bit is Logic 1 when the DPLL1 frequency clamp is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL1 history available		DPLL1 history available. This read only bit is Logic 1 when the DPLL0 holdover history is available. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3203	DPLL1 tuning word history	[7:0]	DPLL1 turning world history [7:0]		DPLL1 tuning word history. This 46-bit bit field contains the DPLL1 tuning word history that is used while DPLL1 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3204		[7:0]	DPLL1 turning world history [15:8]			Prog	RP
0x3205		[7:0]	DPLL1 turning world history [23:16]			Prog	RP
0x3206		[7:0]	DPLL1 turning world history [31:24]			Prog	RP
0x3207		[7:0]	DPLL1 turning world history [39:32]			Prog	RP
0x3208		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL1 turning world history [45:40]		DPLL1 tuning word history. This 46-bit bit field contains the DPLL1 tuning word history that is used while DPLL1 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3209	DPLL1 PLD tub	[7:0]	DPLL1 PLD tub [7:0]		DPLL1 PLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x320A		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 PLD tub [11:8]		DPLL1 PLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x320B	DPLL1 FLD tub	[7:0]	DPLL1 FLD tub [7:0]		DPLL1 FLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x320C		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 FLD tub [11:8]		DPLL1 FLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x320D	Channel 1 distribution phase slew active	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 phase slew enable		DPLL1 phase slewing active. This 4-bit bit field contains read only bits that are Logic 1 when phase slewing is active on the DPLL1 Q1x dividers, where x is A, AA, B, and BB. An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows:	Prog	RP
				0	Logic 1 when phase slewing is active on Divider Q0A.		
				1	Logic 1 when phase slewing is active on Divider Q1AA.		
				2	Logic 1 when phase slewing is active on Divider Q1B.		
				3	Logic 1 when phase slewing is active on Divider Q1BB.		
0x320E	Channel 1 distribution phase slew error	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 phase control error		DPLL1 distribution phase control error. This 4-bit bit field contains read only bits that are Logic 1 when the distribution phase slewing logic on the DPLL1 Q1x dividers (where x is A, AA, B, and BB) is unable to complete the requested phase adjustment. An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows:	Prog	RP
				0	Logic 1 when phase slewing is active on Divider Q1A.		
				1	Logic 1 when phase slewing is active on Divider Q1AA.		
				2	Logic 1 when phase slewing is active on Divider Q1B.		
				3	Logic 1 when phase slewing is active on Divider Q1BB.		

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners. Information contained within this document is subject to change without notice. Software or hardware provided by Analog Devices may not be disassembled, decompiled or reverse engineered. Analog Devices' standard terms and conditions for products purchased from Analog Devices can be found at: http://www.analog.com/en/content/analog_devices_terms_and_conditions/fca.html

©2017 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
UG16132-0-9/17(0)

ANALOG DEVICES

www.analog.com