3-Channel Clock Generator, 24 Outputs

Data Sheet **AD9531**

FEATURES

- 3 fully integrated PLL/VCO cores (PLL1, PLL2, and PLL3)
- Jitter performance: 0.462 ps rms typical
  - PLL1, fractional-N mode, 12 kHz to 20 MHz bandwidth
- Loss of reference and lock detection for each PLL
- Pin-configurable common frequency translations
- Automatic synchronization of all outputs on power-up
- Manual output synchronization capability
- Package available in an 88-lead LFCSP
- PLL1 details
  - Fractional-N/integer-N modes
  - Optional external VCXO
  - Fixed delay mode for constant static phase offset
  - 2 reference clock inputs
    - Input format: differential/single-ended
    - Frequency range: 9.5 MHz to 260 MHz
    - Reference switching: manual/automatic
  - 10 ultralow jitter HSTL/CMOS outputs up to 400 MHz
- PLL2 details
  - Integer-N mode (1 reference clock input)
    - Input format: differential/single-ended/crystal[1]
    - Frequency range: 9.5 MHz to 250 MHz
  - 12 HSTL/CMOS outputs up to 400 MHz
- PLL3 details
  - Integer-N mode (1 reference clock input)
    - Frequency range: 9.5 MHz to 100 MHz
- Input format: differential/crystal (supports a 25 MHz to 50 MHz AT-cut quartz crystal resonator)
  - 2 HSTL/LVDS/CMOS outputs to 400 MHz/150 MHz (differential/CMOS)

APPLICATIONS

- Radio equipment controller clocking
- Low jitter/phase noise clock generation and distribution
- Clock generation and translation for SONET, 10GE, 10G FC, and other 10 Gbps protocols
- 40 Gbps/100 Gbps networking line cards, including SONET, synchronous ethernet, OTU2/3/4
- Forward error correction (G.710)
- High performance wireless transceivers
- ATE and high performance instrumentation
- Broadband infrastructures
- Ethernet line cards, switches, and routers
- SATA and PCI-express

GENERAL DESCRIPTION

The AD9531 provides a multioutput clock generator function and three on-chip phase-locked loop (PLL) cores with SPI programmable output frequencies and formats.

PLL1 provides two reference inputs and 10 outputs and includes four user selectable loop configurations. The PLL has a fully integrated loop filter requiring only a single external capacitor (or a series RC network). PLL1 provides a wide range of output frequencies up to 400 MHz and is capable of operating with an external voltage controlled crystal oscillator (VCXO) and loop filter, instead of the integrated voltage controlled oscillator (VCO) and loop filter.

PLL2 is an integer-N PLL providing a single reference input and 12 outputs. PLL2 synthesizes output frequencies up to 400 MHz from the REF2_x source and synchronizes the output clocks to the input reference.

PLL3 provides a single reference input and two outputs. PLL3 synthesizes output frequencies up to 400 MHz from the REF3_x source and synchronizes the output clocks to input reference.

The AD9531 is available in an 88-lead LFCSP and is specified over the −40°C to +85°C operating temperature range.

Throughout this data sheet, multifunction pins, such as LOR/M4, are referred to either by the entire pin name or by a single function of the pin (for example, LOR, when only that function is relevant). In other cases, the text and figures of this data sheet contain references to a channel rather than a pin. For example, REF_A refers to the REF_A channel rather than the REF_AP and REF_AN pins. Likewise, OUT3_1 refers to Channel 1 of PLL3 rather than the OUT3_1P and OUT3_1N pins. Additionally, an abbreviated notation for a pin pair replaces an explicit reference to a each pin (for example, REF_Ax signifies the REF_AN and REF_AP pins.).

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REVISION HISTORY

1/16—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

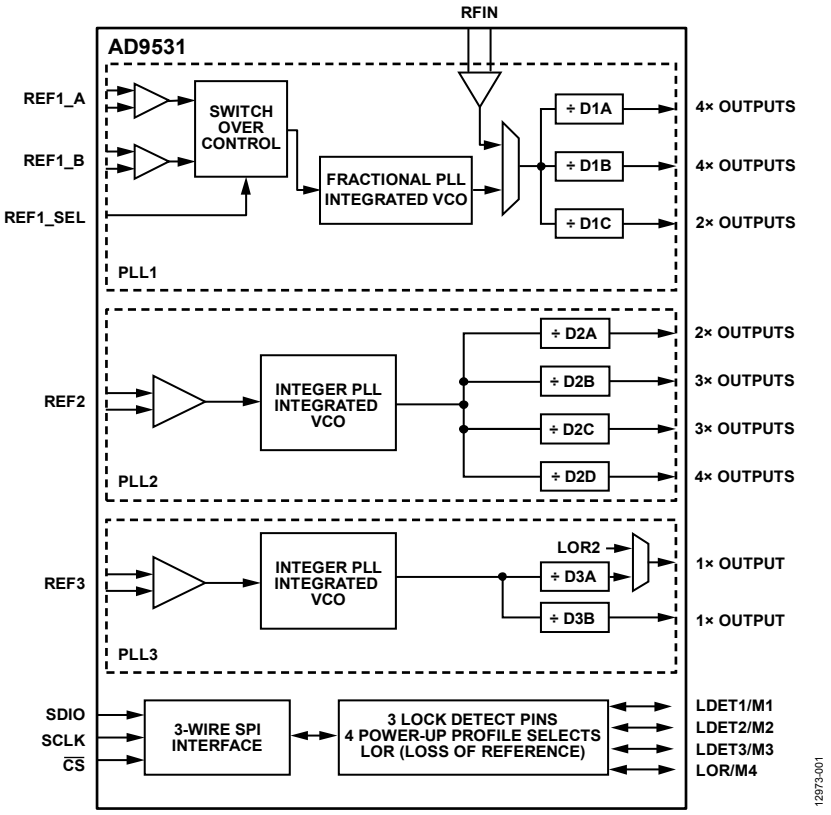


Figure 1.

SPECIFICATIONS

Typical values are given for 3.3 V supplies at 3.3 V ± 5% and 1.8 V supplies at 1.8 V ± 5%; T_A = 25°C. Minimum and maximum values apply over the full variation of supply voltage and T_A (−40°C to +85°C) as listed in Table 1, unless otherwise specified.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
3 V Supply Pins		3.3		V	3.3 V ± 5%
1.8 V Supply Pins		1.8		V	1.8 V ± 5%
TEMPERATURE RANGE, T_A	−40	+25	+85	°C	

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					
Case 1					PLL1: off; PLL2: off; PLL3: off
1.8 V Supply					
PLL1 Pins		6		mA	
PLL2 Pins		19		mA	
PLL3 Pins		1.5		mA	
DVDD		3		mA	
3.3 V Supply					
PLL1 Pins		3.2		mA	
PLL2 Pins		1.3		mA	
PLL3 Pins		0.1		mA	
Case 2					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: off; PLL3: off
1.8 V Supply					
PLL1 Pins		270		mA	
PLL2 Pins		19		mA	
PLL3 Pins		1.5		mA	
DVDD		0.3		mA	
3.3 V Supply					
PLL1 Pins		34		mA	
PLL2 Pins		1.3		mA	
PLL3 Pins		0.1		mA	
Case 3					PLL1: off; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: off
1.8 V Supply					
PLL1 Pins		6		mA	
PLL2 Pins		280		mA	
PLL3 Pins		1.5		mA	
DVDD Pin		0.3		mA	
3.3 V Supply					
PLL1 Pins		3.2		mA	
PLL2 Pins		22		mA	
PLL3 Pins		0.1		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Case 4					PLL1: off; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively); PLL2: off
1.8 V Supply					
PLL1 Pins		6		mA	
PLL2 Pins		19		mA	
PLL3 Pins		72		mA	
DVDD Pin		0.3		mA	
3.3 V Supply					
PLL1 Pins		3.2		mA	
PLL2 Pins		1.3		mA	
PLL3 Pins		0.1		mA	
Case 5					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively)
1.8 V Supply					
PLL1 Pins		270		mA	
PLL2 Pins		280		mA	
PLL3 Pins		72		mA	
DVDD Pin		0.3		mA	
3.3 V Supply					
PLL1 Pins		34		mA	
PLL2 Pins		23		mA	
PLL3 Pins		0.1		mA	
INCREMENTAL SUPPLY CURRENT					
PLL1, External VCXO Configuration					
1.8 V Supply (PLL1 Pins)		−22		mA	
3.3 V Supply (PLL1 Pins)		−27		mA	
PLL3, Dual Loop Configuration					
1.8 V Supply (PLL3 Pins)		36		mA	
3.3 V Supply (PLL3 Pins)		0		mA	

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER CONSUMPTION					Does not include power dissipated in the external resistors
Case 1					PLL1: off; PLL2: off; PLL3 off
1.8 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		35		mW	
PLL3 Pins		2.5		mW	
DVDD Pin		0.5		mW	
3.3 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		4.0		mW	
PLL3 Pins		0.3		mW	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Case 2					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: off; PLL3: off
1.8 V Supply					
PLL1 Pins		480		mW	
PLL2 Pins		35		mW	
PLL3 Pins		2.5		mW	
DVDD Pins		0.5		mW	
3.3 V Supply					
PLL1 Pins		112		mW	
PLL2 Pins		4.0		mW	
PLL3 Pins		0.3		mW	
Case 3					PLL1: off; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: off
1.8 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		500		mW	
PLL3 Pins		2.5		mW	
DVDD Pins		0.5		mW	
3.3 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		73		mW	
PLL3 Pins		0.3		mW	
Case 4					PLL1: off; PLL2: off; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively)
1.8 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		35		mW	
PLL3 Pins		130		mW	
DVDD Pins		0.5			
3.3 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		4.0		mW	
PLL3 Pins		0.3		mW	
Case 5					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively)
1.8 V Supply					
PLL1 Pins		480		mW	
PLL2 Pins		500		mW	
PLL3 Pins		130		mW	
DVDD Pins		0.5		mW	
3.3 V Supply					
PLL1 Pins		112		mW	
PLL2 Pins		73		mW	
PLL3 Pins		0.3		mW	
INCREMENTAL POWER CONSUMPTON					Change in power consumption when a specific circuit block or function is made active (or inactive)
PLL1, External VCXO Configuration					
1.8 V Supply (PLL1 Pins)		−39		mW	
3.3 V Supply (PLL1 Pins)		−89		mW	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL3, Dual Loop Configuration				mW	
1.8 V Supply (PLL3 Pins)		65		mW	
3.3 V Supply (PLL3 Pins)		0		mW	

LDET1/M1, LDET2/M2, LDET3/M3, AND LOR/M4 PINS

In addition to the LOR/M4 pin, a secondary LOR indicator pin is possible via OUT3_0 (see the OUT3_0 Driver section).

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT SPECIFICATIONS					Load current: 1 mA
1.8 V Operating Mode					The 3.3 V mode bit in Register 0x0083 or Register 0x0084 is Logic 0 for the associated pin
Output Voltage					
High	V_{DD} – 0.2			V	Relative to the supply pins (Pin 49, Pin 78, Pin 61, and Pin 6) for LDET1/M1, LDET2/M2, LDET3/M3, and LOR/M4, respectively
Low			0.2	V	
3.3 V Operating Mode					The 3.3 V mode bit in Register 0x0083 or Register 0x0084 is Logic 1 for the associated pin
Output Voltage					
High	2.7			V	
Low			0.2	V	
INPUT SPECIFICATIONS					Applies during a power-on/reset sequence (see the Power-On Reset (POR) section and the Multifunction Pins (LDET1/M1, LDET2/M2, LDET3/M3, LOR/M4) section)
Input High Voltage (V_{IH})	1.2			V	
Input Low Voltage (V_{IL})			0.7	V	
External Resistive Load	3	10	100	kΩ	Required termination to ground or 1.8 V for Logic 0 or Logic 1, respectively
Input Capacitance (C_{IN})		3		pF	

REF1_SEL PIN

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SPECIFICATIONS					
Input High Voltage (V_{IH})	1.4			V	
Input Low Voltage (V_{IL})			1.0	V	
Input Current (I_{INH}, I_{INL})	−2		+2	µA	
Input Capacitance (C_{IN})		3		pF	

PLL1 CHARACTERISTICS

PLL1 Reference Inputs (REF1_A and REF1_B)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					Capacitive coupling required
Input Frequency Range					
×2 Frequency Multiplier					
Bypassed	9.5		260	MHz	
Enabled	9.5		100	MHz	
Input Sensitivity	200			mV p-p	
Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Common-Mode Internally Generated Bias Voltage		1.0		V	
Hysteresis		20		mV	
Differential Input Resistance		19		kΩ	
Differential Input Capacitance		3		pF	
Duty Cycle	40		60	%	Required for input frequencies below 20 MHz; limited by spurious performance when ×2 frequency multiplier is in use
CMOS MODE SINGLE-ENDED INPUT					Single-ended operation is only applicable to the REF1_AP and REF1_BP pins; for both of these inputs, the 2.5 V or 3.3 V mode is selectable via Register 0x0103
Input Frequency Range					
×2 Frequency Multiplier					
Bypassed	9.5		260	MHz	
Enabled	9.5		100	MHz	
Hysteresis		430		mV	
Input Resistance		46		kΩ	
Input Capacitance		3		pF	
Duty Cycle	40		60	%	Required for input frequencies below 20 MHz; limited by spurious performance when ×2 frequency multiplier is in use.
3.3 V Operating Mode					
Input Voltage					
Bias		1.65		V	50% of 3.3 V supply, Pin 23 (VDD1_3V3)
High	2.0			V	
Low			1.3	V	
2.5 V Operating Mode					
Input Voltage					
Bias		1.25		V	38% of 3.3 V supply, Pin 23 (VDD1_3V3)
High	1.5			V	
Low			0.9	V	

PLL1 Distribution Clock Outputs (OUT1_0x to OUT1_9x)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					Specifications assume a 100 Ω termination across the differential output pins
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		120	170	ps	Listed values are for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle					
Up to f_{OUT} = 400 MHz	45	50	55	%	
Differential Output Voltage Swing		950		mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage		870		mV	Output driver static
CMOS MODE					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} – 0.2			V	Relative to the VDD1_03, VDD1_47, and VDD1_89 pins, with the output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA

PLL1 Output Timing Skew Matrix (HSTL Mode)

Entries in Table 8 are typical with units of pico seconds (ps) and only apply with a channel divider input frequency less than 650 MHz. Any blank cell shown in Table 8 indicates an empty space in the matrix.

Table 8.

	Group 1A				Group 1B				Group 1C	
OUT1_x[1]	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0		20	20	20	100	100	100	100	100	100
1			20	20	100	100	100	100	100	100
2				20	100	100	100	100	100	100
3					100	100	100	100	100	100
4						20	20	20	100	100
5							20	20	100	100
6								20	100	100
7									100	100
8										20
9										

[1] OUT1_x refers to one of the 10 output channels associated with PLL1.

PLL1 Output Timing Skew Matrix (CMOS Mode)

Entries in Table 9 are typical with units of pico seconds (ps) and only apply with a channel divider input frequency less than 650 MHz. The typical pin load is 10 pF. Any blank cell shown in Table 9 indicates an empty space in the matrix.

Table 9.

	Group 1A				Group 1B				Group 1C	
OUT1_x[1]	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0		20	20	20	100	100	100	100	100	100
1			20	20	100	100	100	100	100	100
2				20	100	100	100	100	100	100
3					100	100	100	100	100	100
4						20	20	20	100	100
5							20	20	100	100
6								20	100	100
7									100	100
8										20
9										

[1] OUT1_x refers to one of the 10 output channels associated with PLL1.

PLL1 Output Isolation, Group to Group

Table 10.

Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
GROUP TO GROUP ISOLATION					Indicates the worst spur occurring in any channel of the noninterferer groups; all outputs of all groups are active and configured as HSTL
Group 1A Interferer		65		dB	Group 1A = 153.6 MHz, Group 1B = 122.88 MHz, Group 1C = 122.88 MHz
Group 1B Interferer		64		dB	Group 1A = 122.88 MHz, Group 1B = 153.6 MHz, Group 1C = 122.88 MHz
Group 1C Interferer		66		dB	Group 1A = 122.88 MHz, Group 1B = 122.88 MHz, Group 1C = 153.6 MHz

PLL1, Fixed Delay Mode

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RELATIVE INPUT/OUTPUT DELAY					
External VCXO					f_{VCXO} = 122.88 MHz, f_R = 15.36 MHz, f_{OUT} = 15.36 MHz
Group 1A Feedback					From REF1_A/REF1_B to any Group 1A output
Differential Reference	1.60		2.45	ns	
3.3 V CMOS Reference	0.82		1.48	ns	
2.5 V CMOS Reference	0.64		1.37	ns	
Group 1B Feedback					From REF1_A/REF1_B to any Group 1B output
Differential Reference	1.56		2.38	ns	
3.3 V CMOS Reference	0.76		1.41	ns	
2.5 V CMOS Reference	0.64		1.31	ns	
Group 1C Feedback					From REF1_A/REF1_B to any Group 1C output
Differential Reference	1.79		2.60	ns	
3.3 V CMOS Reference	0.94		1.58	ns	
2.5 V CMOS Reference	0.84		1.41	ns	
Internal VCO					f_R = 122.88 MHz, f_{OUT} = 122.88 MHz
Group 1A Feedback					From REF1_A/REF1_B to any Group 1A output
Differential Reference	1.09		2.23	ns	
3.3 V CMOS Reference	0.36		1.64	ns	
2.5 V CMOS Reference	0.27		1.51	ns	
Group 1B Feedback					From REF1_A/REF1_B to any Group 1B output
Differential Reference	1.01		2.16	ns	
3.3 V CMOS Reference	0.28		1.57	ns	
2.5 V CMOS Reference	0.20		1.43	ns	
Group 1C Feedback					From REF1_A/REF1_B to any Group 1C output
Differential Reference	1.14		2.32	ns	
3.3 V CMOS Reference	0.44		1.70	ns	
2.5 V CMOS Reference	0.37		1.56	ns	

PLL1 Internal VCO

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL VCO					
Frequency Range	3500	3686	3900	MHz	
Gain		53		MHz/V	

PLL1 PFD and Charge Pump

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM PFD FREQUENCY					
1.8 V Charge Pump (Internal VCO)					
Integer Mode			260	MHz	
Fractional Mode			60	MHz	
3.3 V Charge Pump (for External VCXO)			40	MHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
3.3 V CHARGE PUMP CURRENT					These charge pump specifications are only applicable to the 3.3 V charge pump, which draws its power from Pin 23 (VDD1_3V3)
I_{CP} Sink/Source					Programmable via Register 0x0101, Bits[D4:D2]
Highest Programmable Value		±5.0		mA	
Lowest Programmable Value		±0.625		mA	
I_{CP} High Impedance Mode Leakage		0.5		nA	
Sink and Source Current Matching		10		%	0.8 V < V_{CP} < V_{DD} − 0.8 V
I_{CP} vs. V_{CP}		11		%	0.8 V < V_{CP} < V_{DD} − 0.8 V
I_{CP} vs. Temperature		2		%	V_{CP} = V_{DD}/2
PLL FIGURE OF MERIT (FOM)		−221		dBc/Hz	Applies to wide loop bandwidth mode (see the PLL1 Loop 2 Wide Bandwidth Configuration section) measured at 500 kHz offset relative to the output frequency under the following conditions: f_R = 245.76 MHz (differential input), f_{OUT} = 122.88 MHz (HSTL output), integer-N PLL mode, internal VCO, and loop bandwidth = 500 kHz

PLL1 RFIN1_x Inputs

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					
Input Frequency Range			400	MHz	
Input Sensitivity	200			mV p-p	Capacitive coupling recommended
Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance (when using a sinusoidal source, for example)
Common-Mode Internally Generated Bias Voltage		0.65		V	
Differential Input Resistance		5.6		kΩ	
Differential Input Capacitance		3		pF	
CMOS MODE, SINGLE-ENDED INPUT					
Input Frequency Range			400	MHz	
Input Voltage					
High	1.2			V	
Low			0.6	V	
Hysteresis		300		mV	
Input Resistance		5		MΩ	
Input Capacitance		3		pF	

PLL1 Jitter Generation

The jitter integration bandwidth is from 12 kHz to 20 MHz.

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ABSOLUTE TIME JITTER					
Fractional Mode		0.462		ps rms	f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 90 kHz
Integer Mode		0.360		ps rms	f_R = 15.36 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 100 kHz
Wide Loop Bandwidth Integer Mode[1]		0.204		ps rms	f_R = 122.88 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 300 kHz
External VCXO Mode		0.145		ps rms	f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 100 Hz
ADDITIVE TIME JITTER					Additive jitter contribution is from the RFIN1_x input to the OUT_x output, excluding the VCXO contribution
External VCXO Mode		0.125		ps rms	f_{VCXO} = 122.88 MHz, f_{OUT} = 122.88 MHz

[1] See the PLL1 Loop 2 Wide Bandwidth Configuration section.

PLL1 Spurious Performance

Entries in Table 16 indicate the worst spur measured between dc and 1 GHz on any PLL1 output for the given conditions.

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS PERFORMANCE					
ROM Profile 4		−85		dBc	PLL1: f_R = 122.88 MHz, f_{LOOP} = 300 kHz; PLL2: f_R = 50 MHz
ROM Profile 5		−85		dBc	PLL1: f_R = 10 MHz, f_{VCXO} = 122.88 MHz, f_{LOOP} = 100 Hz; PLL2: f_R = 50 MHz

PLL1 Start-Up Time

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
START-UP TIME—INTERNAL VCO					Time from application of power (90% of nominal) to first output clock edge after PLL1 is locked and the outputs are synchronized
f_R = 122.88 MHz, f_{OUT} = 122.88 MHz, f_{PFD} = 122.88 MHz, f_{LOOP} = 300 kHz		25		ms	
f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{PFD} = 10 MHz, f_{LOOP} = 90 kHz, Fractional-N PLL Mode		35		ms	
START-UP TIME—EXTERNAL VCXO					Time from application of power (90% of nominal) to first output clock edge after PLL1 is locked
f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{PFD} = 80 kHz, f_{LOOP} = 130 Hz		840		ms	

PLL2 CHARACTERISTICS

PLL2 Reference Input (REF2_x)

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE CLOCK INPUT PATH					
Input Frequency Range	9.5		250	MHz	
Input Sensitivity	200			mV p-p	
Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance
Common-Mode Internally Generated Bias Voltage		1.1		V	
Hysteresis		95		mV	
Differential Input Capacitance		3		pF	
Differential Input Resistance	1			kΩ	
Duty Cycle	45		55	%	Required for input frequencies below 20 MHz when ×2 frequency multiplier is in use
CRYSTAL MOTIONAL RESISTANCE			100	Ω	Use a fundamental mode AT-cut crystal when operating REF2_x as a crystal resonator input

PLL2 Distribution Clock Outputs (OUT2_0x to OUT2_11x)

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					Specifications assume a 100 Ω termination across differential output pins
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		120	170	ps	Listed values are for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle					
Up to f_{OUT} = 400 MHz	45	50	55	%	
Differential Output Voltage Swing		950		mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage		870		mV	Output driver static
CMOS MODE					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} – 0.2			V	Relative to the VDD2_01, VDD2_24, VDD2_57, and VDD2_811 pins, with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA

PLL2 Output Timing Skew Matrix (HSTL Mode)

Entries in Table 20 are typical with units of picoseconds (ps) and only apply with a channel divider input frequency less than 650 MHz. Any blank cell shown in Table 20 indicates an empty space in the matrix.

Table 20.

	Group 2A		Group 2B			Group 2C			Group 2D			
OUT2_x[1]	0	1	2	3	4	5	6	7	8	9	10	11
0		20	100	100	100	100	100	100	100	100	100	100
1			100	100	100	100	100	100	100	100	100	100
2				20	20	100	100	100	100	100	100	100
3					20	100	100	100	100	100	100	100
4						100	100	100	100	100	100	100
5							20	20	100	100	100	100
6								20	100	100	100	100
7									100	100	100	100
8										20	20	20
9											20	20
10												20
11												

[1] OUT2_x refers to one of the 12 output channels associated with PLL2.

PLL2 Output Timing Skew Matrix (CMOS Mode)

Entries in Table 21 are typical with units of picoseconds (ps) and only apply with a channel divider input frequency less than 650 MHz. The typical pin load is 10 pF. Any blank cell shown in Table 21 indicates an empty space in the matrix.

Table 21.

	Group 2A		Group 2B			Group 2C			Group 2D			
OUT2_x[1]	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
0		20	100	100	100	100	100	100	100	100	100	100
1			100	100	100	100	100	100	100	100	100	100
2				20	20	100	100	100	100	100	100	100
3					20	100	100	100	100	100	100	100
4						100	100	100	100	100	100	100
5							20	20	100	100	100	100
6								20	100	100	100	100
7									100	100	100	100
8										20	20	20
9											20	20
10												20
11												

[1] OUT2_x refers to one of the 12 output channels associated with PLL2.

PLL2 Output Isolation, Group to Group

Table 22.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
GROUP TO GROUP ISOLATION					Indicates the worst spur occurring in any channel of the noninterferer groups; all outputs of all groups active and configured as HSTL
Group 2A Interferer		70		dB	Group 2A = 125 MHz, Group 2B = 156.25 MHz, Group 2C = 156.25 MHz, Group 2D = 156.25 MHz
Group 2B Interferer		66		dB	Group 2A = 156.25 MHz, Group 2B = 125 MHz, Group 2C = 156.25 MHz, Group 2D = 156.25 MHz
Group 2C Interferer		65		dB	Group 2A = 156.25 MHz, Group 2B = 156.25 MHz, Group 2C = 125 MHz, Group 2D = 156.25 MHz
Group 2D Interferer		63		dB	Group 2A = 156.25 MHz, Group 2B = 156.25 MHz, Group 2C = 156.25 MHz, Group 2D = 125 MHz

PLL2 VCO and PFD Characteristics

Table 23.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO FREQUENCY RANGE	2400		2500	MHz	An additional 200 ppm margin is allowed beyond these limits to accommodate input reference drift
PLL FIGURE OF MERIT (FOM)		−222		dBc/Hz	Measured at 500 kHz offset from the output frequency under the following conditions: f_R = 50 MHz, 3.3 V CMOS (single-ended input), f_{OUT} = 156.25 MHz, (HSTL output)
PFD FREQUENCY RANGE			125	MHz	

PLL2 Jitter Generation

The jitter integration bandwidth is from 12 kHz to 20 MHz.

Table 24.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
f_R = 25 MHz, f_{OUT} = 156.25 MHz		0.566		ps rms	
f_R = 50 MHz, f_{OUT} = 156.25 MHz		0.337		ps rms	

PLL2 Spurious Performance

Entries in Table 25 indicate the worst spur measured between dc and 1 GHz on any PLL2 output for the given conditions.

Table 25.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS PERFORMANCE					
ROM Profile 4					PLL1: f_R = 122.88 MHz, f_{LOOP} = 300 kHz; PLL2: f_R = 50 MHz
OUT2_0 to OUT2_4		−61		dBc	
OUT2_5 to OUT2_7		−69		dBc	
OUT2_8 to OUT2_11		−78		dBc	
ROM Profile 5					PLL1: f_R = 10 MHz, f_{VCXO} = 122.88 MHz, f_{LOOP} = 100 Hz; PLL2: f_R = 50 MHz; PLL3: f_R = 10 MHz, C_{LOAD} = 10 pF on OUT3_1P
OUT2_0		−76		dBc	
OUT2_1		−65		dBc	
OUT2_2 to OUT2_3		−69		dBc	
OUT2_4 to OUT2_11		−79		dBc	

PLL2 Start-Up Time

Table 26.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
START-UP TIME					The time from the application of power (90% of nominal) to the first output clock edge (PLL2 is locked and outputs are synchronized)
f_R = 25 MHz, f_{OUT} = 156.25 MHz, f_{PFD} = 25 MHz		50		ms	

PLL3 CHARACTERISTICS

PLL3 Reference Input (REF3_x)

Table 27.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT PATH					
Input Frequency Range	9.5		100	MHz	
Input Sensitivity	200			mV p-p	
Minimum Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance
Common-Mode, Internally Generated Bias Voltage		1.16		V	
Hysteresis		70		mV	
Differential Input Capacitance		3		pF	
Differential Input Resistance		4.1		kΩ	
Duty Cycle	47		53	%	Required for input frequencies below 20 MHz when using a frequency scale factor of either 2 or 2/3
CRYSTAL MOTIONAL RESISTANCE			100	Ω	Use a fundamental mode AT-cut crystal when operating REF3_x as a crystal resonator input

PLL3 Outputs OUT3_0

Table 28.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1.8 V SUPPLY (CMOS)					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} − 0.2			V	Relative to VDD3_01 (Pin 66) with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA
3.3 V SUPPLY (CMOS)					
Output Frequency			200	MHz	10 pF load
Rise/Fall Time (20% to 80%)		0.7		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} − 0.2			V	Relative to VDD3_3V3 (Pin 67) with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA

PLL3 Outputs (OUT3_1x)

Table 29.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		120	170	ps	100 Ω termination across the output pins; listed values are for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle	45	50	55	%	
Differential Output Voltage Swing		925		mV	Magnitude of voltage across the pins; output driver static
Common-Mode Output Voltage		850		mV	Output driver static

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS MODE					
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		160		ps	100 Ω termination across the output pair; listed value is for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle	45	50	55	%	
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage swing between the output pins; output driver static
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between the voltage swing of the OUT3_xP pin and the OUT3_xN pin; output driver static
Offset Voltage					
Common-Mode, V_{OS}	1.125	1.26	1.375	V	Output driver static
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between the OUT3_xP pin and the OUT3_xN pin; output driver static
Short-Circuit Output Current		13	24	mA	Output driver static
CMOS MODE					
1.8 V Supply					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} – 0.2			V	Relative to VDD3_01 (Pin 66) with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA
3.3 V Supply					
Output Frequency			200	MHz	10 pF load
Rise/Fall Time (20% to 80%)		0.7		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change (|δv/δt|)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} – 0.2			V	Relative to VDD3_3V3 (Pin 67) with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA

PLL3 VCO and PFD Characteristics

The specifications in Table 30 apply to both the input and output PLLs of PLL3.

Table 30.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO FREQUENCY RANGE	720		805	MHz	An additional 200 ppm margin is allowed beyond these limits to accommodate input reference drift
PLL FIGURE OF MERIT (FOM)		–215		dBc/Hz	Measured at 100 kHz offset from the output frequency under the following conditions: f_R = 10 MHz (3.3 V CMOS single-ended input), f_{OUT} = 125 MHz (HSTL output)
PFD FREQUENCY RANGE	9.5		100	MHz	

PLL3 Spurious Performance

Entries in Table 31 indicate the worst spur measured between dc and 600 MHz on OUT3_1P for the given conditions.

Table 31.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS PERFORMANCE					
ROM Profile 4					PLL1: f_R = 122.88 MHz, f_{LOOP} = 300 kHz; PLL2: f_R = 50 MHz
OUT2_0 to OUT2_4		−61		dBc	
OUT2_5 to OUT2_7		−69		dBc	
OUT2_8 to OUT2_11		−78		dBc	
ROM Profile 5					PLL1: f_R = 10 MHz, f_{VCXO} = 122.88 MHz, f_{LOOP} = 100 Hz; PLL2: f_R = 50 MHz; PLL3: f_R = 10 MHz, C_{LOAD} = 10 pF on OUT3_1P
OUT2_0		−76		dBc	
OUT2_1		−65		dBc	
OUT2_2 to OUT2_3		−69		dBc	
OUT2_4 to OUT2_11		−79		dBc	

PLL3 Jitter Generation

Unless otherwise specified the following test conditions apply: PLL1 configured with OUT1_0 to OUT1_9 operating at 122.88 MHz in HSTL mode; PLL2 configured with f_{REF} = 50 MHz, f_{VCO} = 2.5 GHz, and OUT2_0 to OUT2_11 operating at 125 MHz in HSTL mode; PLL3 configured for single loop operation with OUT3_0 disabled. Measurements are valid with the PLL2 input reference locked to an integer multiple of the PLL3 input reference frequency to within 4.8 ppm.

Table 32.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
f_R = 25 MHz; f_{OUT} = 100 MHz					
OUT1_8x and OUT1_9x Disabled		1.78		ps rms	
OUT1_8x and OUT1_9x Active		3.17		ps rms	
f_R = 10 MHz; f_{OUT} = 125 MHz					
PLL1 and PLL2 Powered Down		2.69		ps rms	
OUT1_8x and OUT1_9x Disabled		2.95		ps rms	
OUT1_8x and OUT1_9x Active		5.20		ps rms	

PLL3 Start-Up Time

The PPL3 start-up time is the time from the application of power (90% of nominal) to the first output clock edge (PLL3 is locked and the outputs are synchronized).

Table 33.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
START-UP TIME					
f_R = 10 MHz, f_{OUT} = 25 MHz, f_{PFD} = 10 MHz		20		ms	

SERIAL CONTROL PORT

Table 34.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT (SCLK, SDIO, $\overline{CS}$)					
1.8 V Supply					DVDD_IO (Pin 18) powered with 1.8 V
Input Voltage					
Logic 1	1.3			V	
Logic 0			0.6	V	
Input Current (I_{INH}, I_{INL})	−2		+2	µA	
Input Capacitance		3		pF	
3.3 V Supply					DVDD_IO (Pin 18) powered with 3.3 V
Input Voltage					
Logic 1	1.3			V	
Logic 0			0.6	V	
Input Current (I_{INH}, I_{INL})	−2		+2	µA	
Input Capacitance		3		pF	
OUTPUT (SDIO)					
1.8 V Supply					DVDD_IO (Pin 18) powered with 1.8 V
Output Voltage					
Logic 1	V_{DD} − 0.2			V	1 mA load current
Logic 0			0.2	V	1 mA load current
3.3 V Supply					DVDD_IO (Pin 18) powered with 3.3 V
Output Voltage					
Logic 1	V_{DD} − 0.2			V	1 mA load current
Logic 0			0.2	V	1 mA load current

Serial Control Port Timing

Table 35.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1.8 V SUPPLY					DVDD_IO (Pin 18) powered with 1.8 V
SCLK					
Clock Rate, $1/t_{SCLK}$			50	MHz	
Pulse Width High, t_{HIGH}	2.1			ns	
Pulse Width Low, t_{LOW}	1.7			ns	
SDIO to SCLK Setup, t_{DS}	0.3			ns	
SCLK to SDIO Hold, t_{DH}	1.0			ns	
SCLK to Valid SDIO, t_{DV}	6.5			ns	
$\overline{CS}$ to SCLK Setup (t_S) and Hold (t_H)	1.1			ns	
$\overline{CS}$ Minimum Pulse Width High	1.4			ns	
3.3 V SUPPLY					DVDD_IO (Pin 18) powered with 3.3 V
SCLK					
Clock Rate, $1/t_{SCLK}$			50	MHz	
Pulse Width High, t_{HIGH}	0.8			ns	
Pulse Width Low, t_{LOW}	2.5			ns	
SDIO to SCLK Setup, t_{DS}	1.8			ns	
SCLK to SDIO Hold, t_{DH}	0.4			ns	
SCLK to Valid SDIO, t_{DV}	6.5			ns	
$\overline{CS}$ to SCLK Setup (t_S) and Hold (t_H)	2.4			ns	
$\overline{CS}$ Minimum Pulse Width High	3.0			ns	

ABSOLUTE MAXIMUM RATINGS

Table 36.

Parameter	Rating
Analog Supply Voltage	
3.3 V Supply Pins	3.6 V
1.8 V Supply Pins	2 V
Maximum Digital Input Voltage	−0.5 V to VDD3 + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

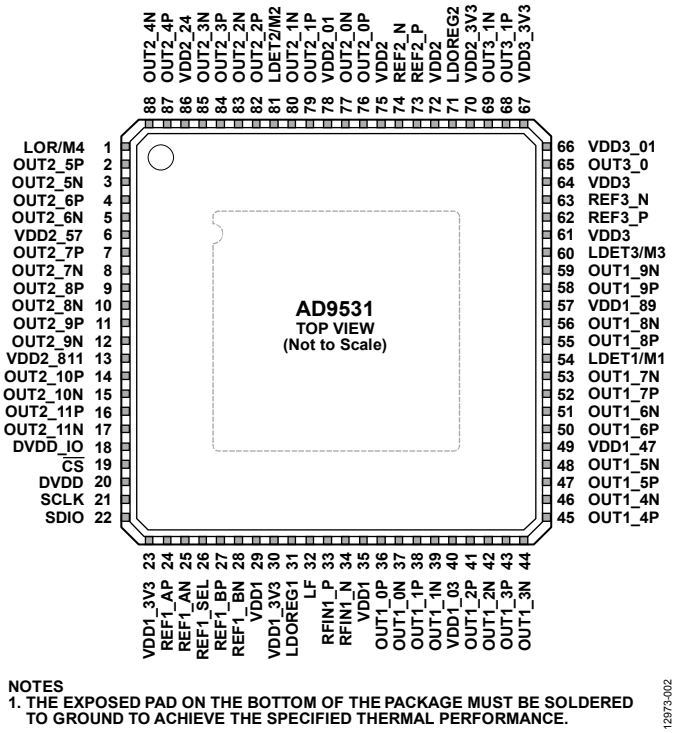


Figure 2. Pin Configuration

Table 37. Pin Function Descriptions

Pin No.	Mnemonic	Supply Domain	Description
1	LOR/M4	1.8 V/3.3 V	Loss of Reference Pin. This is a multifunction pin.
2	OUT2_5P	1.8 V	PLL2 Output 5 (Positive).
3	OUT2_5N	1.8 V	PLL2 Output 5 (Negative).
4	OUT2_6P	1.8 V	PLL2 Output 6 (Positive).
5	OUT2_6N	1.8 V	PLL2 Output 6 (Negative).
6	VDD2_57	1.8 V	PLL2 Power Supply for Channel Outputs OUT2_5 Through OUT2_7.
7	OUT2_7P	1.8 V	PLL2 Output 7 (Positive).
8	OUT2_7N	1.8 V	PLL2 Output 7 (Negative).
9	OUT2_8P	1.8 V	PLL2 Output 8 (Positive).
10	OUT2_8N	1.8 V	PLL2 Output 8 (Negative).
11	OUT2_9P	1.8 V	PLL2 Output 9 (Positive).
12	OUT2_9N	1.8 V	PLL2 Output 9 (Negative).
13	VDD2_811	1.8 V	PLL2 Power Supply for Channel Outputs OUT2_8 Through OUT2_11.
14	OUT2_10P	1.8 V	PLL2 Output 10 (Positive).
15	OUT2_10N	1.8 V	PLL2 Output 10 (Negative).
16	OUT2_11P	1.8 V	PLL2 Output 11 (Positive).
17	OUT2_11N	1.8 V	PLL2 Output 11 (Negative).
18	DVDD_IO	1.8 V/3.3 V	Power Supply for Serial Input/Output Pins.
19	$\overline{CS}$	1.8 V/3.3 V	Chip Select Pin.
20	DVDD	1.8 V	Power Supply for SPI Registers and PLL1 Digital Σ-Δ Modulator (SDM).
21	SCLK	1.8 V/3.3 V	Serial Programming Clock.
22	SDIO	1.8 V/3.3 V	Serial Data Input/Output.
23	VDD1_3V3	3.3 V	PLL1 REF_A/REF_B Input Receiver Power Supply.
24	REF1_AP	3.3 V	PLL1 REF_A Input (Positive). Use this pin when operating the REF_A input in single-ended mode.

Pin No.	Mnemonic	Supply Domain	Description
25	REF1_AN	3.3 V	PLL1 REF_A Input (Negative). When operating the REF_A input in single-ended mode, this pin becomes inoperative (internally disconnected) and must be connected to ground or left floating.
26	REF1_SEL	3.3 V	PLL1 Manual REF_A/REF_B Input Select.
27	REF1_BP	3.3 V	PLL1 REF_B Input (Positive). Use this pin when operating the REF_B input in single-ended mode.
28	REF1_BN	3.3 V	PLL1 REF_B Input (Negative). When operating the REF_B input in single-ended mode, this pin becomes inoperative (internally disconnected) and must be connected to ground or left floating.
29	VDD1	1.8 V	PLL1 Power Supply for the Input Circuitry Following the REF1_A/REF1_B Receivers.
30	VDD1_3V3	3.3 V	PLL1 Power Supply for the Low Dropout (LDO) Input.
31	LDOREG1	3.3 V	PLL1 LDO Regulated Supply for the VCO Core. Connect a 220 nF capacitor between this pin and ground.
32	LF	3.3 V	Loop Filter.
33	RFIN1_P	3.3 V	PLL1 External VCO/VCXO Input (Positive).
34	RFIN1_N	3.3 V	PLL1 External VCO/VCXO Input (Negative).
35	VDD1	1.8 V	PLL1 Power Supply for the Output Distribution Circuitry.
36	OUT1_0P	1.8 V	PLL1 Output 0 (Positive).
37	OUT1_0N	1.8 V	PLL1 Output 0 (Negative).
38	OUT1_1P	1.8 V	PLL1 Output 1 (Positive).
39	OUT1_1N	1.8 V	PLL1 Output 1 (Negative).
40	VDD1_03	1.8 V	PLL1 Power Supply for Channel Outputs OUT1_0 Through OUT1_3.
41	OUT1_2P	1.8 V	PLL1 Output 2 (Positive).
42	OUT1_2N	1.8 V	PLL1 Output 2 (Negative).
43	OUT1_3P	1.8 V	PLL1 Output 3 (Positive).
44	OUT1_3N	1.8 V	PLL1 Output 3 (Negative).
45	OUT1_4P	1.8 V	PLL1 Output 4 (Positive).
46	OUT1_4N	1.8 V	PLL1 Output 4 (Negative).
47	OUT1_5P	1.8 V	PLL1 Output 5 (Positive).
48	OUT1_5N	1.8 V	PLL1 Output 5 (Negative).
49	VDD1_47	1.8 V	PLL1 Power Supply for Channel Outputs OUT1_4 Through OUT1_7.
50	OUT1_6P	1.8 V	PLL1 Output 6 (Positive).
51	OUT1_6N	1.8 V	PLL1 Output 6 (Negative).
52	OUT1_7P	1.8 V	PLL1 Output 7 (Positive).
53	OUT1_7N	1.8 V	PLL1 Output 7 (Negative).
54	LDET1/M1	1.8 V/3.3 V	PLL1 Lock Detect. This is a multifunction pin.
55	OUT1_8P	1.8 V	PLL1 Output 8 (Positive).
56	OUT1_8N	1.8 V	PLL1 Output 8 (Negative).
57	VDD1_89	1.8 V	PLL1 Power Supply for Channel Outputs OUT1_8 Through OUT1_9.
58	OUT1_9P	1.8 V	PLL1 Output 9 (Positive).
59	OUT1_9N	1.8 V	PLL1 Output 9 (Negative).
60	LDET3/M3	1.8 V/3.3 V	PLL3 Lock Detect. This is a multifunction pin.
61	VDD3	1.8 V	PLL3 Power Supply for Input Circuitry of the First PLL in the 2 PLL Cascade of PLL3.
62	REF3_P	1.8 V	PLL3 Reference Input (Positive).
63	REF3_N	1.8 V	PLL3 Reference Input (Negative).
64	VDD3	1.8 V	PLL3 Power Supply for the Output Circuitry of PLL3A and Input Circuitry of PLL3B.
65	OUT3_0	1.8 V/3.3 V	PLL3 Output 0.
66	VDD3_01	1.8 V	PLL3 Power Supply for Channel Outputs OUT3_0 Through OUT3_1.
67	VDD3_3V3	3.3 V	PLL3 Power Supply for the Output Circuitry.
68	OUT3_1P	1.8 V/3.3 V	PLL3 Output 1 (Positive).
69	OUT3_1N	1.8 V/3.3 V	PLL3 Output 1 (Negative).
70	VDD2_3V3	3.3 V	PLL2 Power Supply for the LDO Input.
71	LDOREG2	1.8 V	PLL2 LDO Regulated Supply for the VCO Core. Connect a 220 nF capacitor between this pin and ground.

Pin No.	Mnemonic	Supply Domain	Description
72	VDD2	1.8 V	PLL2 Power Supply for the Input Circuitry.
73	REF2_P	1.8 V	PLL2 Reference Input (Positive).
74	REF2_N	1.8 V	PLL2 Reference Input (Negative).
75	VDD2	1.8 V	PLL2 Power Supply for the Output Circuitry.
76	OUT2_0P	1.8 V	PLL2 Output 0 (Positive).
77	OUT2_0N	1.8 V	PLL2 Output 0 (Negative).
78	VDD2_01	1.8 V	PLL2 Power Supply for Outputs OUT2_0 Through OUT2_1.
79	OUT2_1P	1.8 V	PLL2 Output 1 (Positive).
80	OUT2_1N	1.8 V	PLL2 Output 1 (Negative).
81	LDET2/M2	1.8 V/3.3 V	PLL2 Lock Detect. This is a multifunction pin.
82	OUT2_2P	1.8 V	PLL2 Output 2 (Positive).
83	OUT2_2N	1.8 V	PLL2 Output 2 (Negative).
84	OUT2_3P	1.8 V	PLL2 Output 3 (Positive).
85	OUT2_3N	1.8 V	PLL2 Output 3 (Negative).
86	VDD2_24	1.8 V	PLL2 Power Supply for Outputs OUT2_2 Through OUT2_4.
87	OUT2_4P	1.8 V	PLL2 Output 4 (Positive).
88	OUT2_4N	1.8 V	PLL2 Output 4 (Negative).
	EP		Exposed Pad. The exposed pad on the bottom of the package must be soldered to ground to achieve the specified thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

Nominal supply voltage for V_{DD} = 3.3 V and 1.8 V, unless otherwise noted. Jitter integration bandwidth = 12 kHz to 20 MHz.

In the Typical Performance Characteristics section, the following terminology is used: f_R is the device input reference clock frequency, f_{OUT} is the device output clock frequency, LBW is the loop bandwidth of PLLx, and LBW × 2 is the loop bandwidth of PLLx with the ×2 multiplier enabled.

PLL1 CHARACTERISTICS

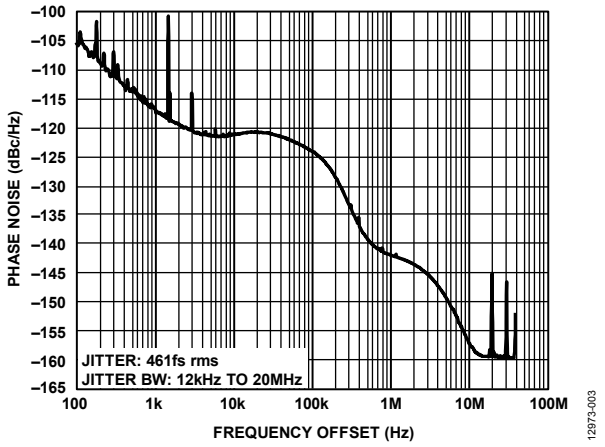


Figure 3. Absolute Phase Noise, f_R = 10 MHz, f_{OUT} = 122.88 MHz, 3.3 V CMOS Single-Ended Input, HSTL Output, Fractional-N PLL Mode, Internal VCO, LBW = 100 kHz

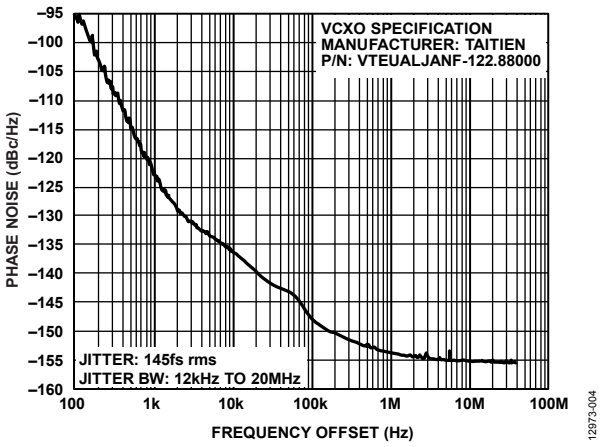


Figure 4. Absolute Phase Noise, f_R = 10 MHz, f_{OUT} = 122.88 MHz, 3.3 V CMOS Single-Ended Input, HSTL Output, Integer-N PLL Mode, External VCO, LBW = 100 Hz

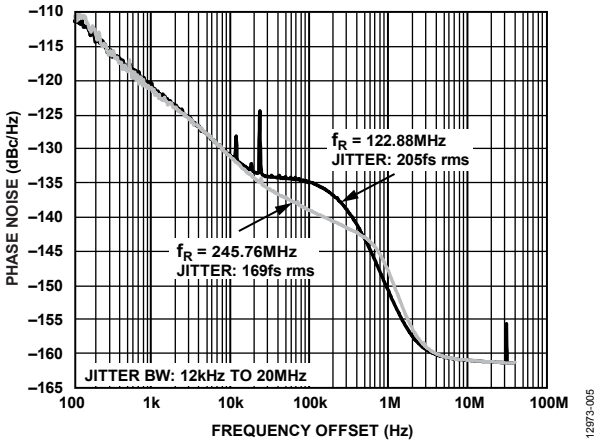


Figure 5. Absolute Phase Noise, f_R = 122.88 MHz and 245.76 MHz, f_{OUT} = 122.88 MHz, Differential Input, HSTL Output, Integer-N PLL Mode, Internal VCO, Wide Bandwidth Mode, LBW = 300 kHz, LBW × 2 = 565 kHz

PLL2 CHARACTERISTICS

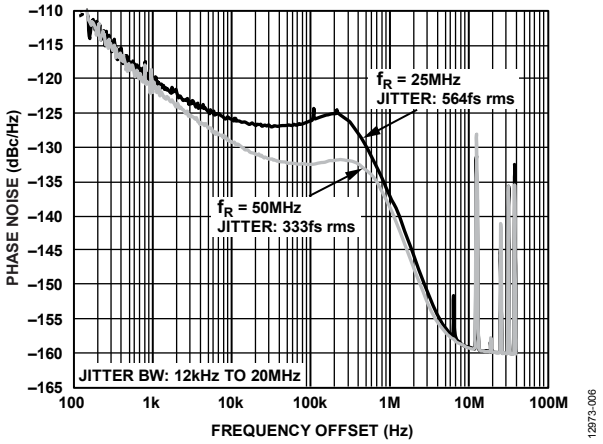


Figure 6. Absolute Phase Noise, f_R = 25 MHz and 50 MHz, f_{OUT} = 156.25 MHz, 3.3 V CMOS Single-Ended Input, HSTL Output

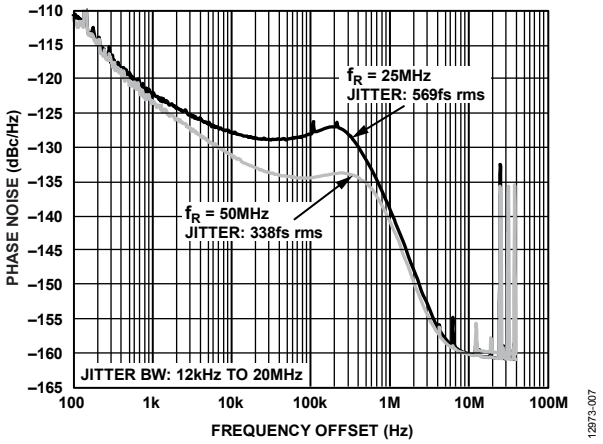


Figure 7. Absolute Phase Noise, f_R = 25 MHz and 50 MHz, f_{OUT} = 125 MHz, 3.3 V CMOS Single-Ended Input, HSTL Output

PLL3 CHARACTERISTICS

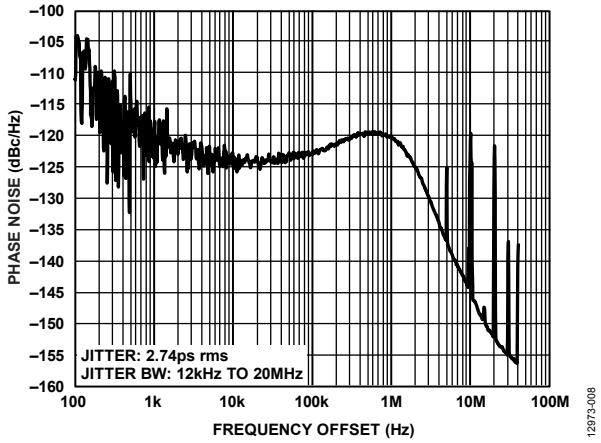


Figure 8. Absolute Phase Noise, f_R = 10 MHz, f_{OUT} = 125 MHz, 3.3 V CMOS Single-Ended Input, HSTL Output

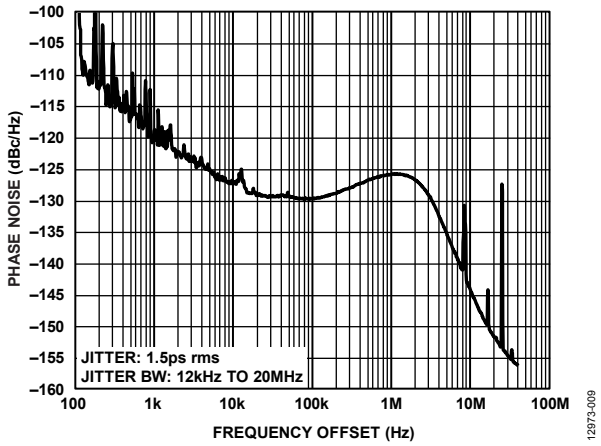


Figure 9. Absolute Phase Noise, f_R = 25 MHz, f_{OUT} = 133 MHz, 3.3 V CMOS Single-Ended Input, HSTL Output

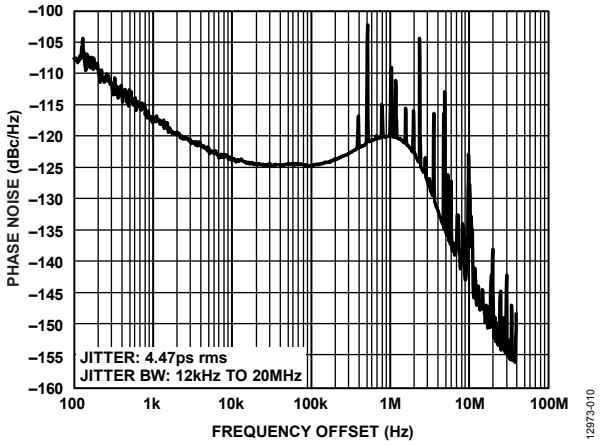


Figure 10. Absolute Phase Noise, f_R = 19.2 MHz, f_{OUT} = 125 MHz, 3.3 V CMOS Single-Ended Input, HSTL Output

GENERAL CHARACTERISTICS

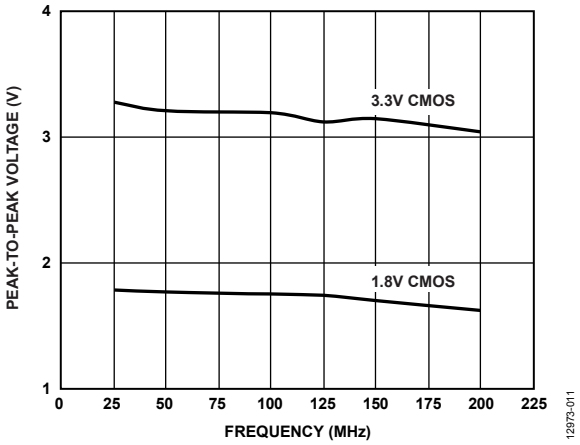


Figure 11. CMOS Output—Amplitude (Peak-to-Peak Voltage) vs. Frequency

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave has a continuous and even progression of phase with time from 0° to 360° for each cycle. A sine wave as a real-world signal, however, exhibits a certain amount of variation in its phase progression over time relative to the ideal sine wave. This variation is phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, characterized statistically by a normal (Gaussian) distribution.

In the frequency domain, an ideal sine wave exhibits a discrete spectral line. Phase jitter, however, blurs the ideal spectral line because it distributes some of the energy of the sine wave throughout the frequency spectrum, resulting in a continuous, rather than discrete, power spectrum. This power spectrum usually appears in the literature as a table of values given in units of dBc/Hz at various offset frequencies from the frequency of the sine wave (carrier). The units, dBc/Hz, represent a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth at some specified offset frequency from the carrier and relative to the power in the carrier. In fact, the c in dBc is an abbreviation for carrier and signifies decibels relative to the carrier.

It is important to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is integrated phase noise and relates phase noise (a frequency domain parameter) over the given bandwidth to jitter (a time domain parameter).

Phase noise has a detrimental effect on the performance of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and radio frequency (RF) mixers. Phase noise lowers the achievable dynamic range of the converters and mixers, although it affects these various devices in different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect appears as time jitter, which is a variation of the instants of zero crossing of a sine wave (or a variation in the occurrence of the edges of a square wave relative to their ideal position in time). In both cases, timing jitter is variations relative to the ideal timing instants. Because time jitter variations are random in nature, they carry units of seconds root mean square (rms), which corresponds to the standard deviation (σ) of a normal (Gaussian) distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter allows the highest possible performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise attributable to the device or subsystem in question. That is, additive phase noise is phase noise exhibited only by the device in question and effectively disregards the phase noise contributions of other sources (like external oscillators or clock sources). This disregarded phase noise makes it possible to predict the impact of the device in question on the total system phase noise when used in conjunction with the various oscillators and clock sources (each contributing its own phase noise to the total). In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the same as additive phase noise, except it is applicable to the time domain rather than the frequency domain.

THEORY OF OPERATION

The AD9531 includes three independent, fully integrated PLLs that enable three separate frequency translations (PLL1, PLL2, and PLL3 in Figure 1). The device has a serial programming interface (SPI) that allows full control of its many features, as well as multifunction pins enabling the device to power up in one of 16 possible predefined configurations.

Because PLL1, PLL2, and PLL3 are functionally independent, their descriptions appear in the following three distinct sections:

- The PLL1—Integer/Fractional-N PLL section
- The PLL1 Lock Detector section
- The PLL3 Integer-N PLL section

PLL1—INTEGER/FRACTIONAL-N PLL

PLL1 is a fractional-N PLL that is also capable of operating in integer mode (see Figure 12).

PLL1 provides two independent reference clock input signals. The AD9531 supports differential and single-ended operation for both reference clocks. PLL1 provides 10 outputs segregated into three groups. Each group has a dedicated channel divider, allowing the device to produce three different output frequencies simultaneously. Note that PLL1 is capable of several different loop configurations; this data sheet describes each configuration separately.

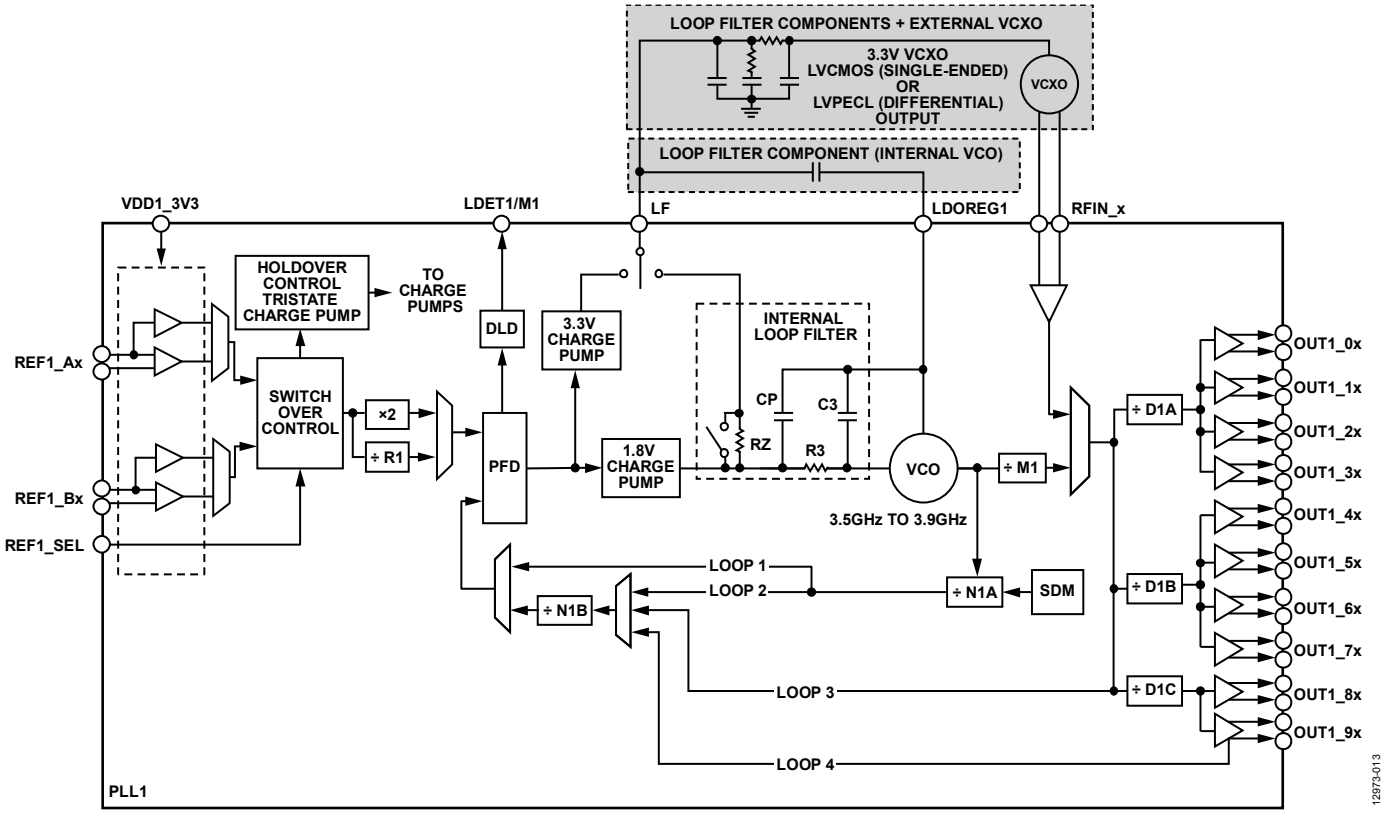


Figure 12. PLL1 Block Diagram

PLL1 LOOP CONFIGURATIONS

The selection of the various PLL1 loop configurations depends on the following three criteria:

- The fixed delay bits (Register 0x0101, Bits[D6:D5]).
- The external oscillator (VXCO) mode bits (Register 0x0101, Bits[D1:D0]).
- The N1B divider value.

A summary of the criteria necessary to select the various loop configurations is shown in Table 38.

Table 38. PLL1 Loop Configurations[1]

Register 0x0101				
Bits[D6:D5]	Bits[D1:D0]	N1B	Loop	VCO
0	0	0 or 1	1	Internal
0	0	>1	2	Internal
0	>0	X	3	External
>0	0	X	4	Internal
>0	>0	X	4	External

[1] X means don't care.

PLL1 Loop 1 Configuration (Integrated VCO)

In the Loop 1 configuration, the loop bandwidth of PLL1 is constant at a nominal value of 100 kHz. The PFD of the PLL drives a 1.8 V charge pump, which automatically changes its output current proportional to the value of N1A, thereby keeping the loop bandwidth constant regardless of the frequency translation ratio.

The VCO frequency is a function of the PFD input frequency (see the PLL1 Reference Frequency Scaling section) and the values programmed into the registers associated with N1A, N1A fraction, and N1A modulus.

$$f_{VCO} = f_{PFD} \times \left(N1A + \frac{N1A\ Fraction}{N1A\ Modulus} \right)$$

where:
f_{VCO} is the frequency of the VCO.
f_{PFD} is the frequency at the input to the PFD.
N1A is an element of the following set: {N_{MIN}, N_{MIN} + 1, ... 255}, where N_{MIN} = 15 for integer-N operation and N_{MIN} = 80 for fractional-N operation.
N1A Fraction is an element of the following set: {0, 1 ... 1,048,574}.
N1A Modulus is an element of the following set, but with the constraint of *N1A Fraction* < *N1A Modulus*: {1, 2 ... 1,048,575}.
OUT1_x and is an element of the following set: {1, 2 ... 256}.

Note that programming N1A fraction to 0 disables the SDM and configures PLL1 as an integer-N PLL. Integer-N operation yields the best performance in terms of phase noise, spurs, and jitter.

The overall frequency translation equation for Loop 1 is as follows:

$$f_{OUT1} = \frac{f_{REF}}{R1} \times \frac{\left(N1A + \frac{N1A\ Fraction}{N1A\ Modulus} \right)}{M1 \times D1}$$

where:
f_{OUT1} is the frequency at OUT1_x.
f_{REF} is the frequency of the active reference (REF_1A or REF_1B).
R1 is an element of the following set: {½, 1, 4, 5 ... 4,095}. The value of ½ is the result of selecting the ×2 reference multiplier (by programming the R1 divider to a value of 0).
M1 is an element of the following set: {3, 4 ... 11}.
D1 is the channel divider (D1A, D1B, or D1C) associated with

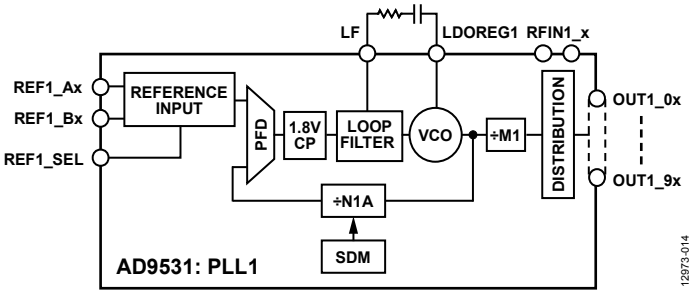


Figure 13. PLL1 Loop 1 Configuration

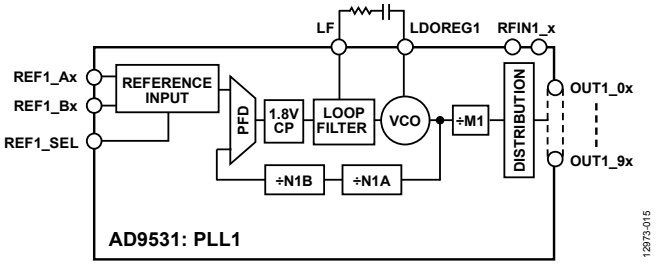


Figure 14. PLL1 Loop 2 Configuration

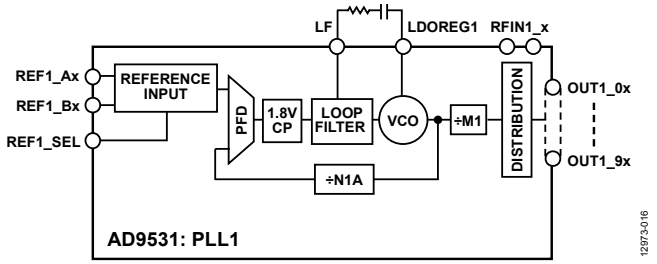


Figure 15. PLL1 Loop 2 Wide Bandwidth Configuration

PLL1 Loop 2 Configuration (Integrated VCO)

Loop 2 consists of the N1A and N1B dividers in cascade, allowing lower PFD frequencies than in the Loop 1 configuration. In this configuration, the charge pump current is constant at 1200 µA (there is no automatic scaling as in the Loop 1 configuration). Furthermore, an internal switch shorts RZ in the integrated loop filter and automatically sets the integrated pole capacitor (C_P) to 50 pF. This particular internal loop filter configuration provides the flexibility to set the response zero and first pole frequency of the loop filter (via an external RC network) to accommodate a low PFD rate. Note that Loop 2 configures PLL1 as an integer-N PLL only.

The VCO frequency is a function of the PFD input frequency (see the PLL1 Reference Frequency Scaling section) and the values programmed into the registers associated with N1A and N1B.

$$f_{VCO} = f_{PFD} \times N1A \times N1B$$

where:
N1A is an element of the following set: {15, 16 ... 255}.
N1B is an element of the following set: {4, 5 ... 4095}.

The overall frequency translation equation for Loop 2 is as follows:

$$f_{OUT1} = \frac{f_{REF}}{R1} \times \frac{N1A \times N1B}{M1 \times D1}$$

where:
f_{OUT1} is the frequency at OUT1_x.
f_{REF} is the frequency of the active reference (REF_1A or REF_1B).
R1 is an element of the following set: {½, 1, 4, 5 ... 4,095}. The value of ½ is the result of selecting the ×2 reference multiplier (by programming the R1 divider to a value of 0).
OUT1_x and is also an element of the following set: {1, 2 ... 256}.

PLL1 Loop 2 Wide Bandwidth Configuration

To select the Loop 2 wide bandwidth configuration configure the device for Loop 1 operation per Table 38, but set the wide bandwidth mode bit (Register 0x0102, Bit D3) to Logic 1.

The Loop 2 wide bandwidth configuration is for applications requiring improved jitter performance. It is identical to the standard Loop 2 configuration in most respects. However, there are two significant differences. First, N1B is not part of the feedback path. Second, although not shown in Figure 15, the SDM drives the N1A divider as in the Loop 1 configuration. In the Loop 2 wide bandwidth configuration however, the SDM tends to degrade jitter performance significantly. Therefore, when using the Loop 2 wide bandwidth configuration, it is best to operate in integer-N mode, which accounts for the exclusion of the SDM from Figure 15.

The VCO frequency is a function of the PFD input frequency (see the PLL1 Reference Frequency Scaling section) and the value programmed into the register associated with N1A.

$$f_{VCO} = f_{PFD} \times N1A$$

where *N1A* is an element of the following set: {15, 16 ... 255}.

The overall frequency translation equation for Loop 2 wide bandwidth is as follows:

$$f_{OUT1} = \frac{f_{REF}}{R1} \times \frac{N1A}{M1 \times D1}$$

where:
f_{OUT1} is the frequency at OUT1_x.
f_{REF} is the frequency of the active reference (REF_1A or REF_1B).
R1 is an element of the following set: {½, 1, 4, 5 ... 4,095}. The value of ½ is the result of selecting the ×2 reference multiplier (by programming the R1 divider to a value of 0).
M1 is an element of the following set: {3, 4 ... 11}.
D1 is the channel divider (D1A, D1B, or D1C) associated with OUT1_x and is also an element of the following set: {1, 2 ... 256}.

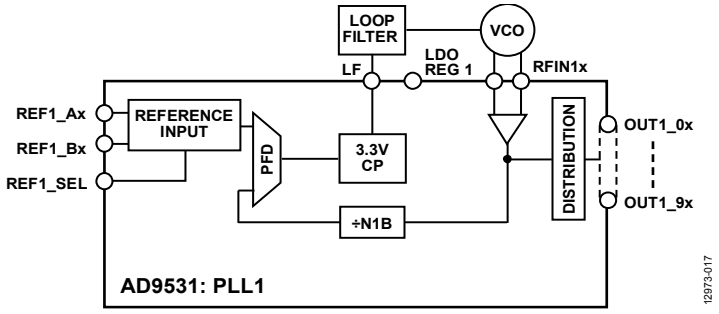


Figure 16. PLL1 Loop 3 Configuration

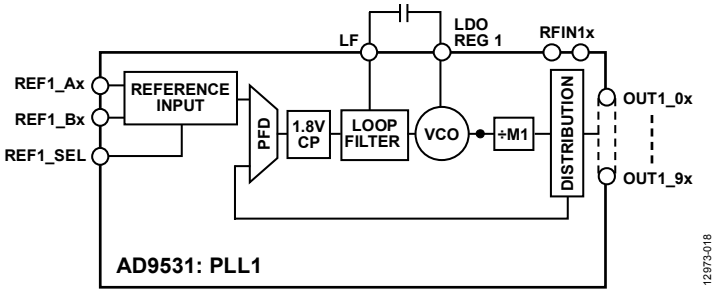


Figure 17. PLL1 Internal Loop 4 Configuration

PLL1 Loop 3 Configuration (External VCXO)

The Loop 3 configuration enables the RFIN receiver and the 3.3 V charge pump. Note that an external loop filter is required between the LF pin and the control input of the external VCXO.

The VCXO frequency is a function of the PFD input frequency (see the PLL1 Reference Frequency Scaling section) and the value programmed into the register associated N1B.

$$f_{VCXO} = f_{PFD} \times N1B$$

where *N1B* is an element of the following set: {1, 4, 5 ... 4,095}.

The overall frequency translation equation for Loop 3 is as follows:

$$f_{OUT1} = \frac{f_{REF}}{R1} \times \frac{N1B}{D1}$$

where:
f_{OUT1} is the frequency at OUT1_x.
f_{REF} is the frequency of the active reference (REF_1A or REF_1B).
R1 is an element of the following set: {½, 1, 4, 5 ... 4,095}. The value of ½ is the result of selecting the ×2 reference multiplier (by programming the R1 divider to a value of 0).
D1 is the channel divider (D1A, D1B, or D1C) associated with OUT1_x and is also an element of the following set: {1, 2 ... 256}.

PLL1 Loop 4 Configuration (Integrated VCO or External VCXO)

The Loop 4 configuration has two variants: internal and external. The internal configuration uses the internal VCO, whereas the external configuration relies on an external VCXO. Note that the Loop 4 configuration bypasses the N1B divider, which the block diagram of PLL1 (see Figure 12) does not explicitly show.

The Loop 4 configuration provides a fixed delay function, which results from the channel dividers being synchronized to each other and the input to the PFD originating from one of the output drivers (per Register 0x0101, Bits[D6:D5]). That is, the feedback reference point of the PLL is one of the outputs, which yields the fixed delay function. The fixed delay function effectively edge aligns all the outputs (OUT1_x) with the reference input because, by design, the internal delay of the reference path closely matches the internal feedback delay from the channel dividers.

Internal Loop 4 Configuration

In the internal Loop 4 configuration, the feedback divider consists of M1 and one of the channel dividers (D1A, D1B, or D1C) in cascade. The particular channel divider included in the feedback path depends on the fixed delay bits per Table 57.

$$f_{VCO} = f_{PFD} \times (M1 \times D1)$$

where:
M1 is an element of the following set: {3, 4 ... 11}.
D1 is the channel divider (D1A, D1B, or D1C) associated with OUT1_x. *D1* is also an element of the following set: {1, 2 ... 256}.

The overall frequency translation equation for Loop 4 using the internal VCO is as follows:

$$f_{OUT1} = \frac{f_{REF}}{R1} \times M1 \times D1$$

where:
f_{OUT1} is the frequency at OUT1_x.
f_{REF} is the frequency of the active reference (REF_1Ax or REF_1Bx).
R1 is an element of the following set: {½, 1, 4, 5 ... 4,095}. The value of ½ is the result of selecting the ×2 reference multiplier (by programming the R1 divider to a value of 0).
Note that internal Loop 4 configuration still allows calibration of the internal VCO, but requires special treatment (see the PLL1 Internal VCO Calibration section).

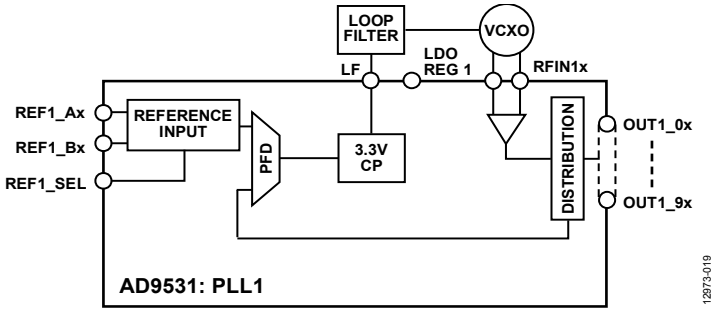


Figure 18. PLL1 External Loop 4 Configuration

External Loop 4 Configuration

In the external Loop 4 configuration, the feedback divider consists of one of the channel dividers (D1A, D1B, or D1C). The particular channel divider included in the feedback path, D1x, depends on the fixed delay bits (Register 0x0101, Bits[D6:D5]). Note that M1 is not part of the feedback path in this configuration. The external configuration uses the 3.3 V charge pump and an external loop filter and VCXO.

$$f_{VCXO} = f_{PFD} \times D1$$

where *D1* is the channel divider (D1A, D1B, or D1C) associated with OUT1_x. *D1* is also an element of the following set: {1, 2 ... 256}.

The overall frequency translation equation for Loop 4 using an external VCXO is as follows:

$$f_{OUT1} = \frac{f_{REF}}{R1} \times D1$$

where:
f_{OUT1} is the frequency at OUT1_x.
f_{REF} is the frequency of the active reference (REF_1Ax or REF_1Bx).
R1 is an element of the following set: {½, 1, 4, 5 ... 4,095}. The value of ½ is the result of selecting the ×2 reference multiplier (by programming the R1 divider to a value of 0).

PLL1 REFERENCE CLOCK INPUTS (REF1_Ax/REF1_Bx)

Two pairs of pins, REF1_Ax and REF1_Bx, provide access to the reference clock receivers. To accommodate input signals with slow rising and falling edges, both the differential and single-ended input receivers use hysteresis. Hysteresis also ensures that a disconnected or floating input does not cause the receiver to oscillate.

When configured for differential operation (see Figure 19 and Table 57), the input receivers accommodate only ac-coupled input signals. The input receivers are capable of accepting ac-coupled LVDS and 2.5 V or 3.3 V LVPECL signals. The receiver is internally dc biased to handle ac-coupled operation. Note that the receivers do not have an internal resistive termination (50 Ω or 100 Ω, for example).

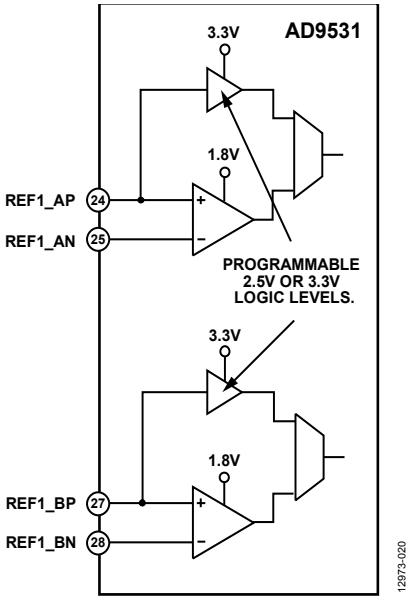


Figure 19. PLL1 Reference Clock Receivers

When configured for single-ended operation (see Figure 19 and Table 57), the REF1_AP and/or REF1_BP inputs have a user-programmable input voltage range of 3.3 V or 2.5 V. These pins possess an internal bias of 1.65 V or 1.25 V (for 3.3 V and 2.5 V operation, respectively) via an internal resistor of approximately 46 kΩ. This configuration allows either dc coupling (typical) or ac coupling, with ac coupling preferred for 3.3 V operation. Note that, when operating in single-ended mode, the REF1_AN and/or REF1_BN pins are nonfunctional; therefore, connect these pins directly to ground to avoid parasitic coupling of stray signals.

PLL1 REFERENCE FREQUENCY SCALING

The frequency of the active reference is scalable via the R1 bits in Register 0x0104 and Register 0x0105 (see Table 58). This configuration allows the user to scale the reference frequency to satisfy the input range of the PFD. The frequency appearing at the input to the PFD of PLL1 depends on the frequency of the active reference (REF_1A or REF_1B), scaled according to the following criteria: when R1 = 0, the PFD frequency is twice the active reference frequency. That is, the ×2 frequency multiplier is active. A value of 1, 2, or 3 for R1 effectively bypasses the divider, making the PFD frequency the same as the active reference frequency. The remaining values of R1 (4 to 4095)

cause the PFD frequency to be the active reference frequency, divided by the value of R1.

Note that, when the ×2 frequency multiplier is in use, the active reference signal must have a duty cycle close to 50%. Otherwise, spurious artifacts (or harmonics) may propagate through the signal path and appear at the output of PLL1.

PLL1 PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMPS

The PFD determines the phase difference between the edges of the reference divider output and the edges of the feedback divider output. The maximum operating frequency of the PFD depends on the operating mode of the PLL (see Table 39).

Table 39. Maximum PFD Rate for PLL1

PLL Mode	Maximum PFD Rate (MHz)
Integer-N	260
Fractional-N	50

The charge pump circuit provides two pulse-width modulated output signals: an up pulse and a down pulse. These up/down pulses drive the charge pump circuit. The instantaneous phase error determines the amount of charge delivered from the charge pump to the loop filter. The closed-loop of the PLL tends to drive the frequency and phase difference between the two PFD input signals toward zero.

The AD9531 PLL1 contains two separate charge pumps. One is a 1.8 V charge pump that controls the internal VCO, and the other is a 3.3 V charge pump that drives an external loop filter and VCXO (the VCXO is 3.3 V compliant). The 1.8 V charge pump current is not user-programmable because the PLL1 control logic automatically sets the 1.8 V charge pump current as required. The 3.3 V charge pump, however, is user-programmable in increments of 625 µA up to 5 mA via Register 0x0101, Bits[D4:D2].

PLL1 LOOP FILTER

A loop filter affects the dynamic characteristics (for example, lock time and stability) of a PLL. When using an external VCXO, a completely external loop filter is required, as shown in Figure 12. Conversely, when using the internal VCO, the integrated loop filter of the AD9531 requires only a single external capacitor or a series RC combination connected between the LF pin and the LDOREG1 pin. For a summary of the loop filter component values, see Table 40.

Table 40. PLL1 Loop Filter Component Values

Component	Loop 1	Loop 2	Loop 2 Wide Bandwidth
R_Z	2.75 kΩ	0 Ω	0 Ω
R_Z (External)	1 kΩ	Application specific	1 kΩ
C_Z (External)	2.7 nF	Application specific	2.7 nF
C_P	50 pF	50 pF	50 pF
R3	2 kΩ	2 kΩ	285 Ω
C3	50 pF	50 pF	50 pF

The PLL1 Loop 1 configuration relies on dynamic charge pump current control to maintain a constant loop bandwidth of approximately 50 kHz, independent of the value of the N1A feedback divider. The Loop 2 and internal Loop 4 configurations, however, use static charge pump current; therefore, the bandwidth depends on the feedback divider value.

PLL1 INTERNAL VCO

PLL1 incorporates a low phase noise, LC tank VCO. This VCO has 256 frequency bands spanning from 3500 MHz to 3900 GHz. At power-up, a VCO calibration cycle begins; this cycle selects the proper band based on the feedback divider value (see the PLL1 Internal VCO Calibration section).

The internal VCO has an integrated LDO linear voltage regulator that isolates the VCO from possible external supply voltage variations. The regulated LDO voltage appears at the LDOREG1 pin. To ensure stability, connect a 220 nF capacitor between this pin and ground. This LDO uses anyCAP™ technology from Analog Devices, Inc., making it insensitive to the type capacitor used for bypassing purposes.

Note that using the LDOREG1 pin to power an external circuit may compromise VCO performance.

PLL1 VCO DIVIDER (M1)

The internal VCO operates in the 4 GHz range; this range is too high to clock the output channel dividers. The purpose of the M1 divider is to scale down the internal VCO frequency to an acceptable range for the output channel dividers. The M1 divider is programmable over a range of 3 to 11.

Under normal operation, there is no need for the user to reset the M1 divider manually because the VCO calibration process (see the PLL1 Internal VCO Calibration section) automatically resets M1.

However, when the user wants to change the M1 divider without recalibrating the PLL1 VCO, the user must execute the following sequence:

1. Reset the M1 divider (write Register 0x010F, Bits[D3:D0] = 0xF).
2. Issue an input/output update (write Register 0x0005, Bit D0 = 1).
3. Program the new M1 divider value.
4. Issue an input/output update (write Register 0x0005, Bit D0 = 1).

PLL1 EXTERNAL VCXO INPUT (RFIN1_x)

The RFIN1_P and RFIN1_N pins are configurable in both differential and single-ended operation via Register 0x0101, Bits[D1:D0]. In differential mode, the pins are internally self biased, and the input signal is ac-coupled via capacitors. In single-ended mode, only one input is operational, either RFIN1_P or RFIN1_N, but not both (see Table 57 for details). Note that the single-ended receivers possess hysteresis and have no internal bias.

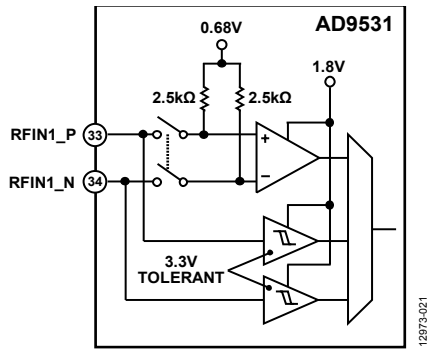


Figure 20. RFIN1_P/RFIN1_N Equivalent Input Circuit

When using an external VCXO with a 3.3 V CMOS single-ended output, however, it is best to use the differential input mode to minimize duty cycle distortion. For more information, see the Interfacing to the RFIN1_x Pins section under Applications Information.

PLL1 CLOCK DISTRIBUTION

PLL1 Output Groups

The clock distribution section exists as three groups of outputs, Group 1A, Group 1B, and Group 1C, with each group having several output drivers that share a channel divider. Group 1A consists of output drivers for OUT1_0 through OUT1_3 and the D1A channel divider. Group 1B consists of output drivers for OUT1_4 through OUT1_7 and the D1B channel divider. Group 1C consists of output drivers for OUT1_8, OUT1_9, and the D1C channel divider.

PLL1 Channel Dividers

The three channel dividers—D1A, D1B, and D1C—are programmable from a factor of 0 to a factor of 255, corresponding to divide ratios ranging from 1 to 256. Note that each channel divider has duty cycle correction for odd divide ratios.

PLL1 Output Power-Down

The ten output drivers (OUT1_0x through OUT1_9x) have independent power-down control via the SPI registers. Each driver has a dedicated power-down bit in its appropriate control register. In addition, setting all three logic mode bits of a particular driver to Logic 0 powers down the output driver.

Note that powering down all the drivers in a group also powers down the channel divider associated with that group. For example, powering down output drivers OUT1_4x through OUT1_7x automatically powers down D1B.

PLL1 Output Operating Mode

The user has independent control of the operating mode of each of the ten output channels via the logic mode bits for PLL1 in the register map. Table 41 summarizes the operating modes.

For LVPECL applications, use HSTL mode and ac-couple the output signal.

Table 41. PLL1 Output Mode Selection

Logic Mode, Bits [2:0]	Description
000	Disable
001	HSTL
010	Undefined
011	Undefined
100	1.8 V CMOS, OUT1_xP active, OUT1_xN active
101	1.8 V CMOS, OUT1_xP active, OUT1_xN disabled
110	1.8 V CMOS, OUT1_xP disabled, OUT1_xN active
111	Undefined

PLL1 Output Polarity

When the user programs a particular output for 1.8 V CMOS mode, the polarity of the driver associated with that output is also programmable (via the polarity bits for PLL1 in the register map). That is, the logical sense of the output pin, OUT1_xP or OUT1_xN, is invertible. Table 42 summarizes the polarity options (normal vs. inverted) for both the positive and negative pins of the particular 1.8 V CMOS output.

Table 42. Output Polarity, 1.8 V CMOS Mode Only

Polarity, Bits[1:0]	Description
00	OUT1_xP normal, OUT1_xN inverted
01	OUT1_xP normal, OUT1_xN normal
10	OUT1_xP inverted, OUT1_xN inverted
11	OUT1_xP inverted, OUT1_xN normal

PLL1 Output Clock Divider Synchronization (Sync)

The sync function allows the user to control the reset of the channel dividers (D1x) so that they can be phase aligned with each other. Upon assertion of a sync signal, the sync block holds the channel dividers reset and disables the clock signals at their inputs. The clocks driving the channel dividers resume on the falling edge of the sync signal. Therefore, the sync signal is a single, positive pulse with both edges necessary to perform output synchronization.

After the sync block receives a falling edge, it allows the channel dividers to start up in a known state, even in the absence of an input clock.

When using PLL1 in any of the internal VCO operating modes, the calibration complete and lock detect signals within the control logic of PLL1 gate the sync function (see the Automatic Output Synchronization section). Therefore, the output channel dividers do not synchronize until PLL1 locks, a VCO calibration sequence executes successfully, and a sync pulse occurs.

Manually force a sync pulse by writing the following register sequence:

1. Register 0x0100, Bit D2 = 1 to set the manual sync bit.
2. Register 0x0005, Bit D0 = 1 to assert the input/output update bit.
3. Register 0x0100, Bit D2 = 0 to clear the manual sync bit.
4. Register 0x0005, Bit D0 =1 to assert the input/output update bit.

Note that, if assertion of a sync pulse occurs prior to the PLL lock and the successful completion of the VCO calibration, then synchronization of the channel dividers does not occur until both conditions are satisfied. Otherwise, the channel dividers synchronize coincident with the falling edge of the sync pulse.

PLL1 HOLDOVER MODE AND FREERUN MODE

PLL1 Holdover Mode

When the AD9531 enters holdover mode, whether invoked manually or automatically, a reset state is in effect for the PFD and charge pump (either the 1.8 V or the 3.3 V charge pump, per the prevailing loop configuration). This mode places the charge pump in a tristate condition, effectively freezing the state of charge on the capacitors in the loop filter (either internal or external per the prevailing loop configuration). By holding the current state of charge on the loop filter, the VCO control voltage remains essentially constant, thereby holding the VCO output frequency at the value it maintained upon entering holdover mode.

Although the VCO frequency remains constant under these conditions, it is subject to frequency drift caused by charge injection or bleed off, for example, the capacitor leakage current or the charge pump leakage current.

PLL1 Freerun Mode

The most important fact regarding freerun mode is that it only applies to the external loop configurations (Loop 3 or external Loop 4). When the device enters freerun mode, whether invoked automatically or manually, it operates much the same as it does in holdover mode. However, in this case the device only acts on the 3.3 V charge pump. In addition to the charge pump entering a tristate condition, an internal resistor connects the LF pin to an internal voltage equal to half the 3.3 V supply. The internal resistor, combined with the tristate condition of the charge pump, effectively holds the VCO control voltage at a constant 1.65 V.

Manual Holdover Mode/Freerun Mode

Force the device into holdover mode at any time by setting the holdover bit (Register 0x0102, Bit D6). Note that, if one of the internal loop configurations is in effect, setting the freerun bit (Register 0x0102, Bit D7) also forces holdover mode. Be aware, however, that in this case, the PLL1 freerun bit (Register 0x0082, Bit D2) is true, even though the device is technically in holdover mode.

Force the device into freerun mode at any time (assuming an external loop configuration is in effect) by setting the freerun bit (Register 0x0102, Bit D7).

Automatic Holdover Mode/Freerun Mode

The AD9531 supports automatic transition to holdover mode when the enable autohold bit (Register 0x0102, Bit D1) is Logic 1 and the freerun vs. holdover bit (Register 0x0102, Bit D2) is Logic 0. An automatic transition to holdover happens when the appropriate LOR states of REF1_A and/or REF1_B occur. Specifically, if the enable autoswitch bit (Register 0x0102, Bit D0) is Logic 0, the automatic transition to holdover occurs when the selected reference (see the Manual Reference Selection section) indicates LOR (REF1_Ax or REF1_Bx, as the case may be). However, if the enable auto switch bit is Logic 1, then both REF1_A and REF1_B must indicate LOR before an automatic transition to holdover occurs.

Automatic transition to freerun mode occurs in identically the same manner as an automatic transition to holdover, but only when an external loop configuration is in effect and both the enable autohold bit and the freerun vs. holdover bit are both Logic 1 (Register 0x0102, Bits[D2:D1]).

PLL1 REFERENCE SELECTION—MANUAL AND AUTOMATIC

Manual Reference Selection

Manual reference selection allows the user to control whether REF1_A or REF1_B is the active reference. Manual control is possible via both hardware (the REF1_SEL pin) and software (by means of the SPI port, Register 0x0102, Bits[D5:D4]).

Hardware-based manual reference selection uses the REF1_SEL pin to make REF1_A or REF1_B the active reference. Logic 0 selects REF1_A, whereas Logic 1 selects REF1_B.

Note that programming the device for automatic reference switching via the enable autoswitch bit disables the functionality of the REF1_SEL pin.

Software-based manual reference selection via the SPI port uses the enable reference select and reference select bits of Register 0x0102. When the enable reference select bit is Logic 0, manual reference selection via the SPI port is disabled. When the enable reference select bit is Logic 1, the reference select bit selects REF1_A or REF1_B as the active reference: Logic 0 selects REF1_A, whereas Logic 1 selects REF1_B.

Note that manual reference selection via the SPI port overrides the automatic reference selection function as well as manual reference selection via hardware using the REF1_SEL pin.

Automatic Reference Selection

Automatic reference selection allows the device to select a reference automatically based on the LOR status of PLL1 (see the Loss of Reference (LOR) section). Automatic reference selection is in effect when the enable auto switch bit is Logic 1.

Upon LOR indication, the device decides whether to switch references. If the active reference indicates LOR and the alternate reference does not, the device automatically switches to the alternate reference. Otherwise, the currently selected reference remains the active reference.

When an automatic reference switch occurs, the new reference becomes the active reference and the other the alternate reference, which allows the device to switch back and forth between the two references as required. Be aware, however, that manual reference selection via Register 0x0102, Bits[D5:D4] overrides this automatic switching feature.

Note that the automatic reference switch feature is nonrevertive. For example, suppose that REF1_A is the active reference, but its LOR becomes active, which triggers a reference switch from REF1_A to REF1_B (assuming REF1_B does not indicate LOR). This switch makes REF1_B the active reference. Then, suppose REF1_A subsequently becomes available (meaning its LOR clears). At this point, instead of the device preferentially reverting to REF1_A, it retains REF1_B as the active reference until REF1_B indicates LOR, whereupon a switch back to REF1_A occurs (assuming REF1_A does not indicate LOR).

PLL1 INTERNAL VCO CALIBRATION

When Loop 1 (integer or fractional-N mode), Loop 2, or the internal variant of Loop 4 is in effect, the internal VCO is subject to calibration. Calibration centers the VCO control voltage at the VCO frequency established after the PLL locks, allowing the VCO sufficient operating range to maintain lock over extremes of temperature and voltage (as long as the loop parameters do not change).

At power-up, the VCO calibration sequence automatically executes, as long as the multifunction pins select a profile that includes a VCO calibration command. Otherwise, the user must do so manually via the PLL1 manual calibrate bit (Bit D1 in Register 0x0100).

VCO calibration requires the presence of a reference signal. Therefore, assuming a signal is present at the REF1_A and/or REF1_B inputs, the VCO calibration controller awaits indication of a valid reference signal. Note that, in the absence of a reference signal, the device remains in VCO calibration mode until a valid reference is present. Validation of an input signal initiates the VCO calibration sequence, which allows the loop to lock and selects the appropriate VCO frequency band.

When the loop parameters change (a new reference frequency or different feedback divider value, for example), it is necessary to manually initiate a VCO calibration sequence. To accomplish this, write the following register sequence:

1. Register 0x0100, Bit D1 = 0 clears the manual calibrate bit.
2. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.
3. Register 0x0100, Bit D1 = 1 sets the manual calibrate bit.
4. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.

Note that, when the internal variant of Loop 4 is in effect, VCO calibration requires special treatment. This is because the M1 and D1x dividers stop during VCO calibration (a result of the automatic sync function imposed during calibration), which prevents the calibration circuitry from receiving the required feedback clock edges. Therefore, the calibration controller detects that Loop 4 is in effect and automatically switches to the Loop 1 configuration to perform the VCO calibration sequence. Upon completion of the calibration sequence, the calibration controller automatically restores the Loop 4 configuration.

Note that, because the calibration controller uses the Loop 1 configuration, the N1A divider is necessarily in the feedback path during the calibration sequence. Therefore, the user must program the value of the N1A divider before initiating a calibration sequence in the Loop 4 configuration, such that

$$N1A = M1 \times D1x$$

That is, N1A must match the product of the M1 divider and the selected channel divider (D1A, D1B, or D1C, as assigned per the fixed delay bits of Register 0x0101, Bits[D6:D5]). Programming N1A to the correct value ensures the calibration controller sets the correct charge-pump current for the Loop 4 configuration.

Note that, during a VCO calibration sequence, the calibration controller holds the distribution section in sync mode (channel dividers reset and output drivers are static) until the calibration terminates. Therefore, no output signals appear until the VCO calibration sequence terminates as indicated by a Logic 1 to Logic 0 transition of the PLL1 calibration in progress bit (Register 0x0080, Bit D4).

The VCO calibration process requires approximately 172,000 cycles of the PFD to complete. Therefore, the calibration time (t_{VCO_CAL}) depends on the input frequency to the PFD as follows:

$$t_{VCO_CAL} = \frac{1.72 \times 10^5}{f_{PFD}}$$

Figure 21 shows a flowchart demonstrating a robust PLL1 VCO calibration procedure. The procedure terminates with an optional output synchronization sequence. In the flowchart, the terms CAL_COUNT and Timer represent variables in the software code that a programmer may use to implement the flowchart.

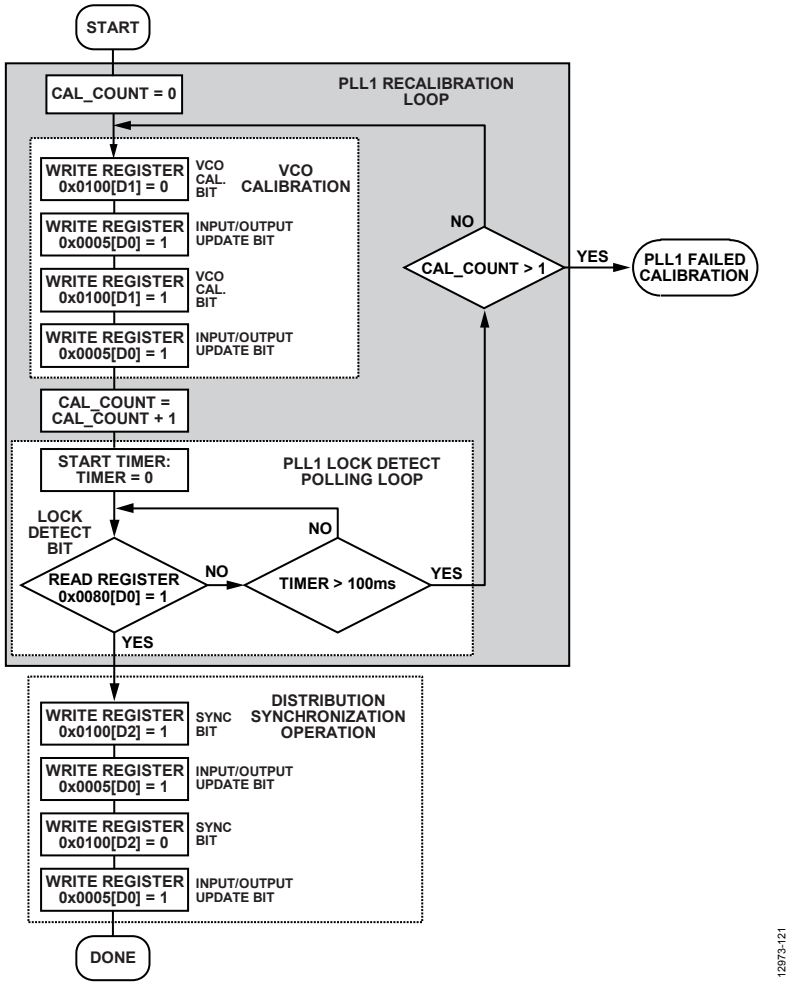


Figure 21. PLL1 VCO Calibration Flowchart

PLL1 Σ-Δ MODULATOR

The N1A feedback divider of PLL1 has an accompanying third-order SDM that allows integer plus fractional frequency translation. This feature, however, only applies to the Loop 1 configuration.

The integer part of the feedback divider ratio is the N1A divider, whereas the fractional part depends on 20-bit fractional and modulus values appearing in the N1A fractional register and the N1A modulus register, respectively (see Table 58). The total feedback divider ratio is expressed as

$$N1A_{Total} = N1A + \frac{N1A\ fraction}{N1A\ modulus}$$

Note that the minimum value of N1A depends on the value of N1A fraction (see the details for N1A in Table 58) because the value of N1A determines integer-N (N1A fraction = 0) or fractional-N (NA1 fraction > 0) operation.

PLL1 LOCK DETECTOR

The lock detector in PLL1 is a digital frequency detector. It effectively averages the frequency difference between the feedback and reference inputs to the PFD over an interval spanning 2^{16} PFD cycles and indicates a lock condition when the average difference is less than 32 ppm. Therefore, the minimum time necessary to detect a lock condition (t_{LDET}) depends on the PFD frequency as follows:

$$t_{LDET} = \frac{2^{16}}{f_{PFD}}$$

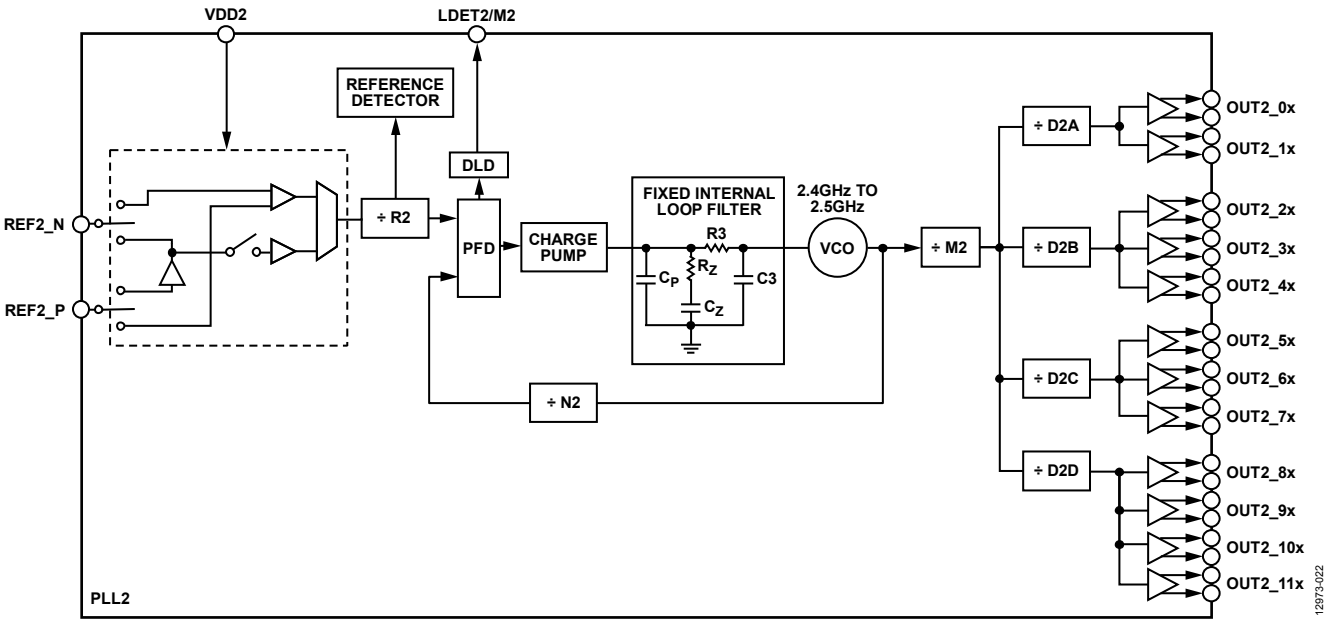


Figure 22. PLL2 Block Diagram

PLL2—INTEGER-N PLL

PLL2 is a fully integrated integer-N PLL that includes a VCO and internal loop filter (see Figure 22). PLL2 has a single reference input supporting either a differential clock signal or a crystal resonator. PLL2 has an output distribution section supporting twelve outputs segregated into four groups. Each group has a dedicated channel divider, allowing the device to produce four different output frequencies simultaneously.

PLL2 reduces the reference input frequency (f_{REF}) via the R2 divider by an integer factor (see the PLL2 Reference Divider (R2) section), setting the frequency at the input to the PFD.

$$f_{PFD} = \frac{f_{REF}}{R2}$$

where *R2* is an element of the following set: {1, 2 ... 16}.

The PLL core scales the PFD frequency up by an integer multiple per the feedback divider, N2, yielding the VCO frequency.

$$f_{VCO} = f_{PFD} \times N2$$

where *N2* is an element of the following set: {20, 21 ... 255}.

The VCO divider, M2, and the channel dividers (D2x) produce the final output frequency, f_{OUT2}.

$$f_{OUT2} = \frac{f_{VCO}}{M2 \times D2}$$

where:
f_{OUT2} is the frequency at OUT2_x.
D2 is the channel divider (D2A, D2B, D2C, or D2D) associated with OUT2_x.
M2 is an element of the following set: {3, 4 ... 11}.
D2 is an element of the following set: {1, 2 ... 256}.

By substitution, the overall frequency translation is

$$f_{OUT2} = \frac{f_{REF}}{R2} \times \frac{N2}{M2 \times D2}$$

PLL2 REFERENCE CLOCK INPUT (REF2_P/REF2_N)

The differential receiver associated with the REF2_P and REF2_N pins has a 1.8 V supply. Typically, the user drives the reference input with a differential signal compatible with 1.8 V logic levels. For applications with a 3.3 V CMOS reference, see the Driving REF2 or REF3 with 3.3 V CMOS Logic in the Applications Information section for more details.

PLL2 REFERENCE DIVIDER (R2)

The function of R2 is to reduce the reference frequency to a range suitable for the phase detector (125 MHz, maximum). R2 divides by an integer factor ranging from 1 to 16 (see Table 63).

PLL2 PFD AND CHARGE PUMP

The PLL2 PFD determines the phase difference between the edges of the reference divider output and edges of the feedback divider output. The circuit provides two pulse-width modulated output signals: an up pulse and a down pulse. These up/down pulses drive the charge pump circuit. The instantaneous phase error determines the amount of charge delivered from the charge pump to the loop filter. The closed-loop of the PLL tends to drive the frequency and phase difference between the two PFD input signals toward 0.

The control logic associated with PLL2 sets the charge pump current based on the value of the feedback divider, N2, to maintain a nearly constant loop bandwidth of 500 kHz, nominal.

PLL2 LOOP FILTER

PLL2 has a fully integrated loop filter. The loop filter components (see Table 43) establish the nominal operating parameters of a 500 kHz closed-loop bandwidth and a 60° phase margin. Because the control logic for PLL2 adjusts the charge pump current based on N2, the bandwidth and phase margin remain relatively constant, regardless of the value of N2.

Table 43. PLL2 Loop Filter Component Values

Component	Value
C_Z	180 pF
R_Z	7 kΩ
C_P	12.5 pF
R3	250 Ω
C3	2.5 pF

PLL2 VCO

PLL2 incorporates a low phase noise, LC tank VCO. This VCO has 64 frequency bands spanning from 2350 GHz to 2510 GHz.

At power-up, the VCO calibration sequence automatically executes as long as the multifunction pins select a profile that includes a VCO calibration command. Otherwise, the user must do so manually via the PLL2 manual calibrate bit in the register map (Bit D1 in Register 0x0200).

VCO calibration requires the presence of a reference signal. Therefore, assuming a signal is present at the REF2_x input, the VCO calibration controller awaits indication of a valid reference signal. Note that, in the absence of a reference signal, the device remains in VCO calibration mode until a valid reference is present. Validation of an input signal initiates the VCO calibration sequence, which allows the loop to lock and selects the appropriate VCO frequency band.

When the loop parameters change (a new reference frequency or different feedback divider value, for example), it is necessary to manually initiate a VCO calibration sequence. To accomplish this, write the following register sequence:

1. Register 0x0200, Bit D1 = 0 clears the manual calibrate bit.
2. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.
3. Register 0x0200, Bit D1 = 1 sets the manual calibrate bit.
4. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.

The VCO calibration process requires approximately 800,000 cycles of the PFD to complete. Therefore, the calibration time (t_{VCO_CAL}) depends on the input frequency to the PFD as follows:

$$t_{VCO_CAL} = \frac{8 \times 10^5}{f_{PFD}}$$

Figure 23 shows a flowchart demonstrating a robust PLL2 VCO calibration procedure. The procedure terminates with an optional output synchronization sequence. In the flowchart, the terms CAL_COUNT and Timer represent variables in the software code that a programmer may use to implement the flowchart.

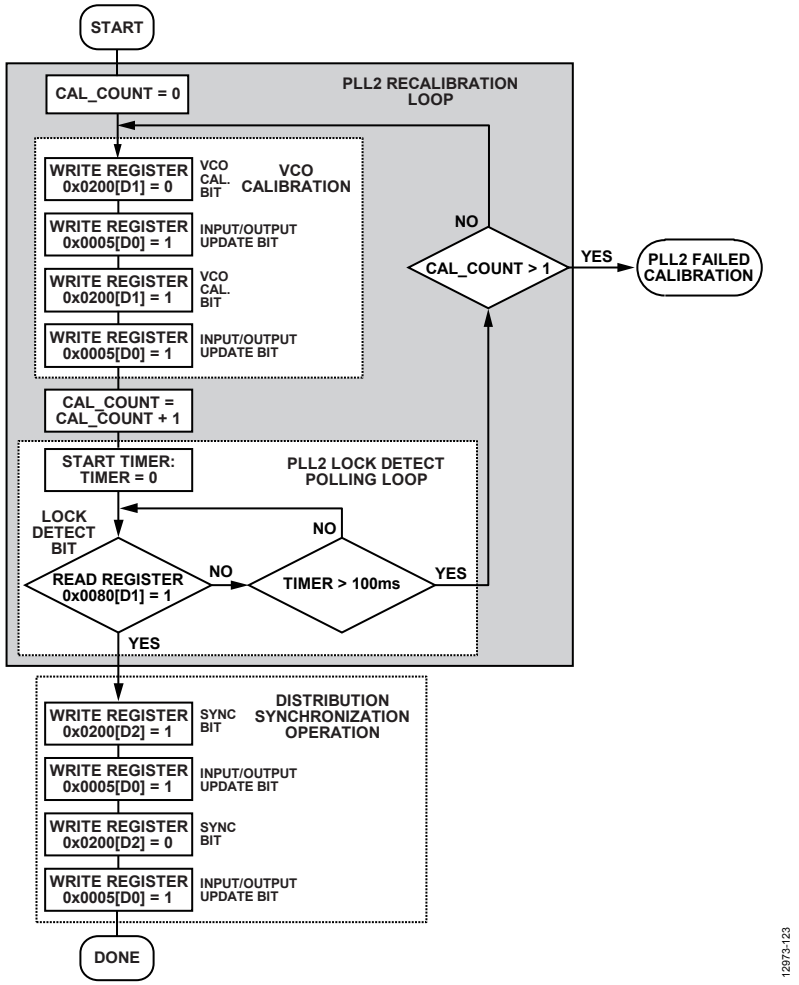


Figure 23. PLL2 VCO Calibration Flowchart

PLL2 VCO DIVIDER (M2)

The internal VCO operates in the 2.4 GHz to 2.5 GHz range; this range is too high to clock the output channel dividers. The purpose of the M2 divider is to scale down the VCO frequency to an acceptable range for the output channel dividers. The M2 divider is program-mable over a range of 3 to 11 via Register 0x0204, Bits[D3:D0].

Under normal operation, there is no need for the user to reset the M2 divider manually because the VCO calibration process (see the PLL2 VCO section) automatically resets M2.

However, when the user wants to change the M2 divider without recalibrating the PLL2 VCO, the user must execute the following sequence:

1. Reset the M2 divider (write Register 0x0204, Bits[D3:D0] = 0xF).
2. Issue an input/output update (write Register 0x0005, Bit D0 = 1).
3. Program the new M2 divider value.
4. Issue an input/output update (write Register 0x0005, Bit D0 =1).

PLL2 FEEDBACK DIVIDER (N2)

The N2 feedback divider is programmable over a useable range of 13 to 255 via Register 0x0203, Bits[D7:D0]. N2 sets the frequency multiplication factor from the input of the PFD input to the output of the VCO.

PLL2 CLOCK DISTRIBUTION

PLL2 Output Groups

The clock distribution section exists as three groups of outputs (Group 2A, Group 2B, Group 2C, and Group 2D), with each group having several output drivers that share a channel divider. Group 2A consists of the D2A channel divider and the output drivers for OUT2_0 and OUT2_1. Group 2B consists of the D2B channel divider and the output drivers for OUT2_2 through OUT2_4. Group 2C consists of the D2C channel divider and the output drivers for OUT2_5 through OUT2_7. Group 2D consists of the D2D channel divider and the output drivers for OUT2_8 and OUT2_11.

PLL2 Channel Dividers

The four channel dividers (D2A, D2B, D2C, and D2D) are programmable from 0 to 255, corresponding to the divide ratios of 1 to 256. Note that each channel divider has duty cycle correction for odd divide ratios.

PLL2 Output Power-Down

The twelve output drivers (OUT2_0 through OUT2_11) have independent power-down control via the SPI registers. Each driver has a dedicated power-down bit in its appropriate control register. In addition, setting all three logic mode bits of a particular driver to Logic 0 powers down the output driver.

Note that powering down all the drivers in a group also powers down the channel divider associated with that group. For example, powering down output drivers OUT2_2x through OUT2_4x automatically powers down D2B as well.

PLL2 Output Mode

The user has independent control of the operating mode of each of the twelve output channels via the logic mode bits for PLL2 in the register map. Table 44 summarizes the operating modes.

Use HSTL mode and ac-couple the output signal for LVPECL applications.

Table 44. PLL2 Output Mode Selection

Logic Mode [2:0]	Description
000	Disable
001	HSTL
010	Undefined
011	Undefined
100	1.8 V CMOS, OUT2_xP active, OUT2_xN active
101	1.8 V CMOS, OUT2_xP active, OUT2_xN disabled
110	1.8 V CMOS, OUT2_xP disabled, OUT2_xN active
111	Undefined

PLL2 Output Polarity

When programming a particular output for 1.8 V CMOS mode, the polarity of the driver associated with that output is also programmable (via the polarity bits for PLL2 in the register map). That is, the logical sense of the output pin, OUT2_xP or OUT2_xN, is invertible. Table 45 summarizes the polarity options (normal vs. inverted) for both the positive and negative pins of the particular 1.8 V CMOS output.

Table 45. Output Polarity, 1.8 V CMOS Mode Only

Polarity, Bits[1:0]	Description
00	OUT1_xP normal, OUT1_xN inverted
01	OUT1_xP normal, OUT1_xN normal
10	OUT1_xP inverted, OUT1_xN inverted
11	OUT1_xP inverted, OUT1_xN normal

PLL2 Output Clock Divider Synchronization

The sync function allows the user to control the reset of the channel dividers (D2x) so that they can be phase aligned with each other. Upon assertion of a sync signal, the sync block holds the channel dividers reset and disables the clock signals at their inputs. The clocks driving the channel dividers resume on the falling edge of the sync signal. Therefore, the sync signal is a single, positive pulse with both edges necessary to perform output synchronization.

After the sync block receives a falling edge, it allows the channel dividers to start up in a known state, even in the absence of an input clock.

The sync function is gated by the calibration complete and lock detect signals within the control logic of PLL2 (see the Automatic Output Synchronization section). Therefore, the output channel dividers do not synchronize until PLL2 locks, a VCO calibration sequence executes successfully, and a sync pulse occurs.

The user can manually force a sync pulse by writing the following register sequence:

1. Register 0x0200, Bit D2 = 1 sets the manual sync bit.
2. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.
3. Register 0x0200, Bit D2 = 0 clears the manual sync bit.
4. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.

Note that, if assertion of a sync pulse occurs prior to the PLL lock and the successful completion of the VCO calibration, synchronization of the channel dividers does not occur until both conditions are satisfied. Otherwise, the channel dividers synchronize coincident with the falling edge of the sync pulse.

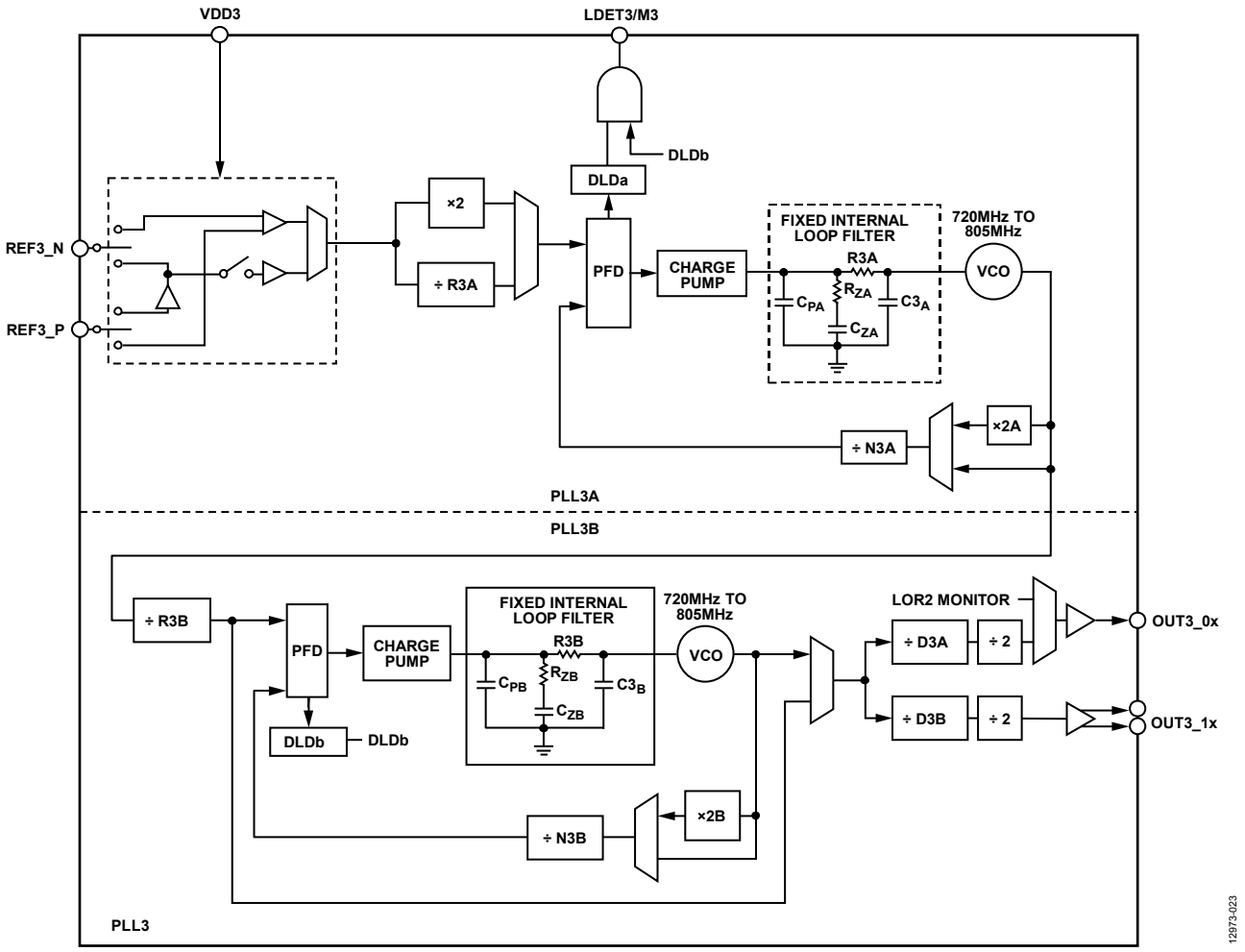


Figure 24. PLL3 Block Diagram

PLL3 INTEGER-N PLL

PLL3 consists of two, cascaded integer-N PLLs (PLL3A and PLL3B), each with a loop bandwidth in the range of approximately 2 MHz. A detailed block diagram of PLL3 is shown in Figure 24.

PLL3 REFERENCE CLOCK INPUT (REF3_P/REF3_N)

The differential receiver associated with the REF3_P and REF3_N pins has a 1.8 V supply. Typically, the user drives the reference input with a differential signal compatible with 1.8 V logic levels. For applications with a 3.3 V CMOS reference, see the Driving REF2 or REF3 with 3.3 V CMOS Logic section in Applications Information for more details.

The PLL3 reference clock input also supports direct connection to a crystal resonator. This feature is in effect when the XTAL amplifier bit (Register 0x0300, Bit D4) is Logic 1. For applications using a crystal resonator at the reference clock input, see the Using REF2 or REF3 with a Crystal Resonator section in Applications Information for more details.

PLL3 INPUT FREQUENCY SCALING

The input frequency applied at REF3 is scalable via R3A per Register 0x0301, Bits[D3:D0] (see Table 69). This feature allows the user to scale the reference frequency to satisfy the input range of the PFD. The available frequency scaling factors are as follows: 2, 1, 2/3, 1/2, 1/3, 1/4, 1/6, and 1/8. Programming Register 0x0301, Bits[D3:D0] with a value of 0 disables in the input reference section.

When using the ×2 frequency multiplier in the input reference section (a frequency scale factor of either 2 or 2/3), the REF3 signal must have a duty cycle close to 50%. Otherwise, spurious artifacts (harmonics) may propagate through the signal path and appear at the output of PLL3.

PLL3 PFD AND CHARGE PUMPS

The PFD determines the phase difference between the edges of the reference divider output and the edges of the feedback divider output. The circuit provides two pulse-width modulated output signals: an up pulse and a down pulse. These up/down pulses drive the charge pump circuit. The instantaneous phase error determines the amount of charge delivered from the charge pump to the loop filter. The closed-loop of the PLL tends to drive the frequency and phase difference between the two PFD input signals toward 0.

The control logic associated with PLL3A and PLL3B sets the respective charge pump current based on the value of the

feedback dividers (N3A or N3B) to maintain a nearly constant loop bandwidth of 2 MHz, nominal.

PLL3 LOOP FILTERS

The loop filters associated with PLL3A and PLL3B are identical and have a third-order response characteristic. The control logic associated with PLL3A and PLL3B selects the appropriate component values of the respective loop filter based on the value of the respective feedback divider (N3A and N3B). This, in conjunction with control of the respective charge pump current, yields a nearly constant loop bandwidth. That is, the closed-loop bandwidth of PLL3A and PLL3B is a function of the value of N3A and N3B, respectively, per Table 46.

Table 46. PLL3A/PLL3B Closed-Loop Bandwidth

N3A, N3B[1]	Nominal Closed-Loop Bandwidth (MHz)
Less than 24	3.5
24 to 47	1.75
Greater than 47	1.0

[1] Table 46 shows that, based on the value of the divider, N3A affects the loop bandwidth of PLL3A and N3B affects the loop bandwidth of PLL3B.

PLL3 VCOs

The VCOs associated with PLL3A and PLL3B are identical and have a frequency range of 745 MHz to 805 MHz. Each has a nominal gain of 750 MHz/V.

PLL3 FEEDBACK DIVIDERS

The feedback dividers associated with PLL3A and PLL3B (N3A and N3B, respectively) are identical, with divide ranges according to Register 0x0302 and Register 0x0304 (see Table 69). Programming a value of 0 bypasses the associated PLL. Therefore, when N3A = 0, the scaled reference input frequency appears at the input to R3B and when N3B = 0, the output frequency of the R3B divider appears at the input to the D3A and D3B channel dividers.

PLL3B REFERENCE DIVIDER (R3B)

The R3B reference divider is between PLL3A and PLL3B. R3B scales the output frequency of the VCO from PLL3A down to a range suitable for the PFD of PLL3B. The integer factor, R3B, is variable via Register 0x0303, Bits[D7:D0], per Table 69.

PLL3 CLOCK DISTRIBUTION

Channel Dividers

The two channel dividers (D3A and D3B) are programmable, providing divide ratios from 1 to 16 (see Table 70 and Table 71 for details). Note that each channel divider has a fixed divide by 2 divider at its output. Therefore, the overall channel divide ratio is always even and spans a range of 2 to 32.

The channel dividers power down when their associated output drivers power down.

Output Clock Divider Synchronization

The sync function allows the user to control the reset of the channel dividers (D3x) so that they can be phase aligned with each other. Upon assertion of a sync signal, the sync block holds the channel dividers reset and disables the clock signals at their inputs. The clocks driving the channel dividers resume on the falling edge of the sync signal. Therefore, the sync signal is a single, positive pulse with both edges necessary to perform output synchronization.

After the sync block receives a falling edge, it allows the channel dividers to start up in a known state even in the absence of an input clock.

The sync function is gated by the lock detect signals within the control logic of PLL3 (see the Automatic Output Synchronization section). Therefore, the output channel dividers do not synchronize until PLL3A and PLL3B locks and a sync pulse occurs.

The user can manually force a sync pulse by writing the following register sequence:

1. Register 0x0300, Bit D2 = 1 sets the manual sync bit.
2. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.
3. Register 0x0300, Bit D2 = 0 clears the manual sync bit.
4. Register 0x0005, Bit D0 = 1 asserts the input/output update bit.

Note that, if assertion of a sync pulse occurs prior to PLL3 lock, synchronization of the channel dividers does not occur until the lock condition is satisfied. Otherwise, the channel dividers synchronize coincident with the falling edge of the sync pulse.

OUT3_0 Driver

OUT3_0 utilizes a CMOS driver, which normally functions as an output clock signal for PLL3 and is capable of 1.8 V or 3.3 V CMOS logic levels as determined by Register 0x0306, Bit D3. In addition to controlling the output logic levels, the user also has control over the logical sense of OUT3_0, which is invertible via Register 0x0306, Bit D1. Furthermore, the OUT3_0 driver has independent power-down control via Register 0x0306, Bit D0.

OUT3_0 may function as an optional second LOR pin, as well (see the Loss of Reference (LOR) section). Note that, when using OUT3_0 as an LOR pin, Register 0x0306, Bits[D3:D0] are ineffective.

OUT3_1 Driver

OUT3_1 has multiple output driver operating modes, as shown in Table 47 (see Register 0x0308, Bits[D6:D3]). These modes include HSTL, LVDS, and 1.8 V or 3.3 V CMOS mode.

For LVPECL applications, use HSTL mode and ac-couple the output signal.

Table 47. OUT3_1 Output Modes

Logic Mode, Bits[3:0]	Description
0000	Disabled
0001	HSTL
0010	LVDS
0011	Undefined
0100	1.8 V CMOS, OUT3_1P active, OUT3_1N active
0101	1.8 V CMOS, OUT3_1P active, OUT3_1N disabled
0110	1.8 V CMOS, OUT3_1P disabled, OUT3_1N active
0111 to 1011	Undefined
1100	3.3 V CMOS, OUT3_1P active, OUT3_1N active
1101	3.3 V CMOS, OUT3_1P active, OUT3_1N disabled
1110	3.3 V CMOS, OUT3_1P disabled, OUT3_1N active
1111	Undefined

When the user programs OUT3_1 for 1.8 V or 3.3 V CMOS mode, the polarity of the driver is also programmable (via the polarity bits for PLL3 in the register map). That is, the logical sense of the output pin, OUT3_1P or OUT3_1N, is invertible. Table 48 summarizes the polarity options (normal vs. inverted).

Table 48. Output Polarity, 1.8 V or 3.3 V CMOS Only

Polarity, Bits[1:0]	Description
00	OUT3_1P normal, OUT3_1N inverted
01	OUT3_1P normal, OUT3_1N normal
10	OUT3_1P inverted, OUT3_1N inverted
11	OUT3_1P inverted, OUT3_1N normal

Furthermore, the OUT3_1 driver has independent power-down control via Register 0x0308, Bit D0.

ADDITIONAL FEATURES

POWER-ON RESET (POR)

Applying power to the AD9531 causes an internal power-on reset (POR) event. The POR event expires approximately 20 ms after the supply voltages reach 80% of their nominal value. The POR event allows the device to initialize to a known state at power-up by initiating a ROM load sequence (see the ROM Profiles section). Note that the POR event is critical to the operation of the multifunction pins.

ROM PROFILES

The AD9531 has an integrated ROM partitioned into 64 groups. Each group constitutes a ROM profile. Each ROM profile stores data that maps to particular SPI registers and establishes the register default values. That is, the register default values depend on the current ROM profile selection. Therefore, the ROM label for the default value is in the Register Map for those registers mapped to the ROM.

At power-up, one of the first 16 ROM profiles is loaded into the register map per the multifunction pins (see the Multifunction Pins (LDET1/M1, LDET2/M2, LDET3/M3, LOR/M4) section for more information). However, the user can select any one of the 64 possible ROM profiles by writing the desired profile value (from 0 to 63) into Register 0x000E, Bits[D5:D0] (this register does not require an input/output update). Writing to Register 0x000E results in an immediate download of the ROM profile contents into the register map and a reset of all PLLs. This reset means that each PLL must be calibrated and synchronized (as applicable), unless the ROM profile contains the requisite calibrate and sync commands.

A listing of the register default values associated with each ROM profile appears in the ROM Profile Data section. Furthermore, reading Register 0x000E allows the user to obtain the index value of the most recently loaded ROM profile.

MULTIFUNCTION PINS (LDET1/M1, LDET2/M2, LDET3/M3, LOR/M4)

During a POR event, the LDET1/M1, LDET2/M2, LDET3/M3, and LOR/M4 pins function as inputs and constitute four ROM profile select pins. The logic level on these pins during the POR event constitutes a 4-bit binary word, M4-M3-M2-M1, that selects one of the first 16 ROM profiles, with M4 denoting the most significant bit (MSB) and M1 the least significant bit (LSB). For example, during a POR event, if the logic level on the pins, M4-M3-M2-M1, is 0-1-0-0, respectively, then the AD9531 automatically loads ROM Profile 4.

Upon expiration of the POR event, the multifunction pins revert from Mx inputs to LDETx and LOR outputs. Note that, when the LDETx and LOR pins function as output signals, each pin is independently capable of 1.8 V or 3.3 V CMOS logic levels. The output logic level for each pin depends on its associated 3.3 V mode bit in Register 0x0083 and Register 0x0084.

When configuring these multifunction pins for 3.3 V operation, the pins make use of a booster circuit that generates 3.3 V from internally available 1.8 V supply domains. This generation has an impact on the 3.3 V operating mode of the LOR/M1 pin in particular, as it requires PLL2 to be active (powered up). The reason for this requirement is that the LOR/M1 pin uses the internal 1.8 V supply domain associated with PLL2. Therefore, powering down PLL2 shuts down the 1.8 V source that supplies the booster circuit of the LOR/M1 pin. Furthermore, when operating the LOR or LDETx pins in 3.3 V mode, it is best to program the logical sense of the pin such that it is normally in a Logic 0 state. That is, when using the LOR pin in 3.3 V mode, program the pin to produce Logic 0 during normal operation (when an LOR condition does not exist). Likewise, when using the LDETx pins in 3.3 V mode, program them to produce Logic 0 during normal operation (when a lock condition exists).

Using the Mx Pins with 1.8 V, 3.3 V, or 1.5 V CMOS Logic

A functional diagram of a representative Mx pin is shown in Figure 25. During a POR event (see the Power-On Reset (POR) section), S1 is in the POR position, which connects each Mx pin to its own internal 1.8 V CMOS receiver. After a POR event, S1 is in the NORM position, which connects each Mx pin to its own internal CMOS driver (capable of either 1.8 V or 3.3 V logic levels, per Register 0x0083 and Register 0x0084). Therefore, except for the brief interval of time during a POR event, the Mx pins operate with S1 in the NORM position, which constitutes normal device operation.

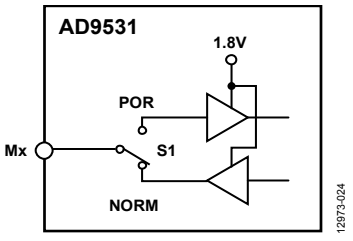


Figure 25. Functional Diagram of an Mx Pin

See the Interfacing to the Multifunction Pins section in the Applications Information section for details on interfacing the Mx pins to 1.8 V, 3.3 V, or 1.5 V CMOS logic.

LOSS OF REFERENCE (LOR)

Each of the PLLs within the AD9531 (PLL1, PLL2, and PLL3) is capable of LOR detection. The LOR detectors effectively report the absence of a reference clock or a reference clock with a significantly low frequency.

LOR Detection

Figure 26 is a functional diagram of an LOR detector. Each reference input (REF) has a dedicated LOR detector. The LOR detectors consist primarily of a pair of edge detectors and timers, with the timers having a nominal period of 500 ns.

There are two important features regarding the LOR detectors:

- LOR is not a latched status signal (it is memoryless).
- LOR is asserted following any of the four indicated reset events and is not deasserted until the LOR detector detects the input signal (REF).

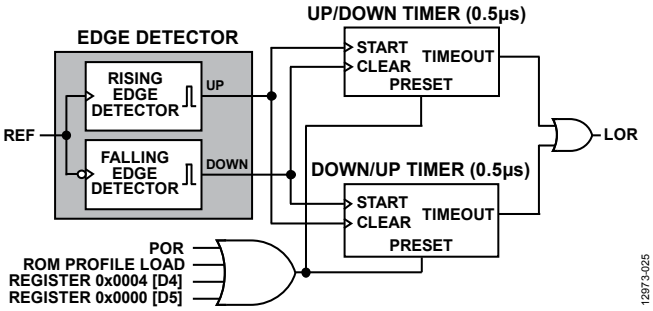


Figure 26. LOR Detector

The edge detector independently monitors both the rising and falling edges of the REF signal. Each rising edge generates an up pulse and each falling edge a down pulse. The up and down pulses trigger the start and clear inputs to the two timers. The up/down timer effectively monitors the positive half cycles of REF, while the down/up counter effectively monitors the negative half cycles of REF. If any positive or negative half cycle of REF extends beyond the nominal period of the associated timer (~500 ns), the timer times out resulting in the assertion of LOR.

LOR Status

The LOR status is available via the SPI port, the LOR/M4 pin, as well as optionally via the OUT3_0 pin by making any of the bits in Register 0x0085, Bits[D4:D0] bits Logic 1.

SPI port indication of LOR for each PLL is available via Register 0x0081. Note that, in the case of PLL1, the LOR status of both REF1_A and REF1_B is available, regardless of which reference is the active reference. The identity of the active reference is available via Register 0x0082, Bit 0, where Logic 0 indicates REF1_A as the active reference, and Logic 1 indicates REF1_B as the active reference.

The LOR/M4 pin provides a hardware indication of the composite LOR status of the device. There are five possible LOR indications as follows:

- REF1_A LOR
- REF1_B LOR
- REF1 active LOR
- REF2 LOR
- REF3 LOR

REF1_A LOR, REF1_B LOR, and REF1 active LOR indicate the LOR status of PLL1. Specifically, REF1_A and REF1_B LOR indicate the LOR state of the designated reference, even if the designated reference is not the active reference. Alternatively, REF1 Active LOR indicates the LOR state of the active reference (REF1_A or REF1_B as applicable).

REF2 LOR indicates the LOR state of PLL2.

REF3 LOR indicates the LOR state. Note that PLL3 is a cascade of two PLLs. The first of the two PLLs in the cascade is the only PLL that provides LOR indication.

Pin indication of LOR is composite in that any combination of the five possible LOR indications previously noted can be logically OR'd via Register 0x0084, Bits[D4:D0] and Register 0x0085, Bits[D4:D0]. Register 0x0084 controls the LOR/M4 pin, while Register 0x0085 controls the OUT3_0 pin.

Because of the logical OR functionality of the LOR bits, when all the LOR bits of Register 0x0084 are Logic 0, the LOR/M4 pin is tristate. Making any of the bits Logic 1, however, enables the associated LOR detector(s) to indicate a loss of reference in a logical OR sense on the LOR/M4 pin.

In the case of Register 0x0085, when all the LOR bits are Logic 0, the OUT3_0 pin functions normally (that is, as an output of PLL3). Making any of the bits Logic 1 enables the associated LOR detector(s) to indicate a loss of reference in a logical OR sense on the OUT3_0 pin.

The LOR/M4 pin indicates a logical true state for a loss of reference condition (per the LOR bits of Register 0x0084). The actual logic level (Logic 0 or Logic 1) depends on the invert bit (Register 0x0084, Bit D5). When the invert bit is Logic 0, an LOR condition of true appears on the LOR/M4 pin as Logic 1, while a false condition appears as Logic 0. When the invert bit is Logic 1, an LOR condition of true appears on the LOR/M4 pin as Logic 0, while a false condition appears as Logic 1. The same is true for the OUT3_0 pin when it functions as an LOR indicator, but with the invert bit located in Register 0x0085, Bit D5.

PLL LOCK DETECTION (LDETx)

PLL1, PLL2, and PLL3 each possess a built in digital lock detector (DLD). PLL1 has a frequency lock detector, whereas PLL2 and PLL3 have phase lock detectors. Each DLD senses the activity of its associated PFD to determine if the PLL has acquired a lock con-dition. The DLDs possess hysteresis to minimize chatter in the lock detect signal as the loop acquires lock and crosses through an internal lock/unlock threshold.

The DLDs indicate a logical true state for a lock condition and a logical false state for an unlock condition. The actual logic level (Logic 0 or Logic 1) at an LDETx pin depends on the invert bit for that particular LDET indicator (Register 0x0083, Bit D4, Bit D2, or Bit D0). When the invert bit is Logic 0, a true DLD condition appears on an LDETx pin as Logic 1, and a false condition appears as Logic 0. When the invert bit is Logic 1, a true DLD condition appears on an LDETx pin as Logic 0, and a false condition appears as Logic 1.

Furthermore, each of the LDETx pins may be set to 3.3 V logic (instead of 1.8 V logic) by setting the appropriate 3.3 V mode bit in Register 0x0083.

AUTOMATIC OUTPUT SYNCHRONIZATION

The output distribution sections associated with PLL1, PLL2, and PLL3 can have their output channels synchronized so that all channels of a particular PLL start producing clock signals at the same instant. The manual sync bit in the register map of a particular PLL controls the synchronization function for that particular PLL, as explained in the output synchronization section of the individual PLL descriptions.

However, output synchronization occurs automatically as the end result of a reset event, as defined by one of the following conditions:

- A POR event
- A ROM profile load
- A soft reset (Register 0x0000, Bit D5 = 1)
- A hardware reset (Register 0x0004, Bit D4 = 1)

Figure 27, Figure 28, and Figure 29 contain flow diagrams showing the reset sequence for each PLL. Each sequence begins with a reset event and terminates with the synchronization of the output channels.

The flowcharts shown in Figure 27, Figure 28, and Figure 29 apply only to a reset event. That is, independent functions included within the flow of the reset sequence, such as calibrate or sync, are accessible via the programming registers, even after the reset sequence terminates. However, when accessed after the termination of the reset sequence, they behave as independent functions and do not follow the reset sequence flow.

Figure 27 shows the reset sequence for PLL1. The REF1 pass and REF1 fail events apply to REF1_A and/or REF1_B, per the contents of Register 0x0084, Bits[D2:D0]. These bits determine whether LOR indication is for REF1_A only, REF1_B only, or the active reference (REF1_A or REF1_B, per the reference switching controls). Though not explicitly shown in Figure 27, the flowchart assumes implementation of the features in Figure 21 to ensure a more robust calibration sequence.

Figure 28 shows the reset sequence for PLL2. The PLL2 flowchart is similar to the PLL1 flowchart shown in Figure 27, except for the absence of the external VCXO and fixed delay dependencies. Though not explicitly shown in Figure 28, the flowchart assumes implementation of the features in Figure 23 to ensure a more robust calibration sequence.

Figure 29 shows the reset sequence for PLL3. The PLL3 flowchart is similar to the PLL2 flowchart shown in Figure 28, except for the absence of a calibration dependency.

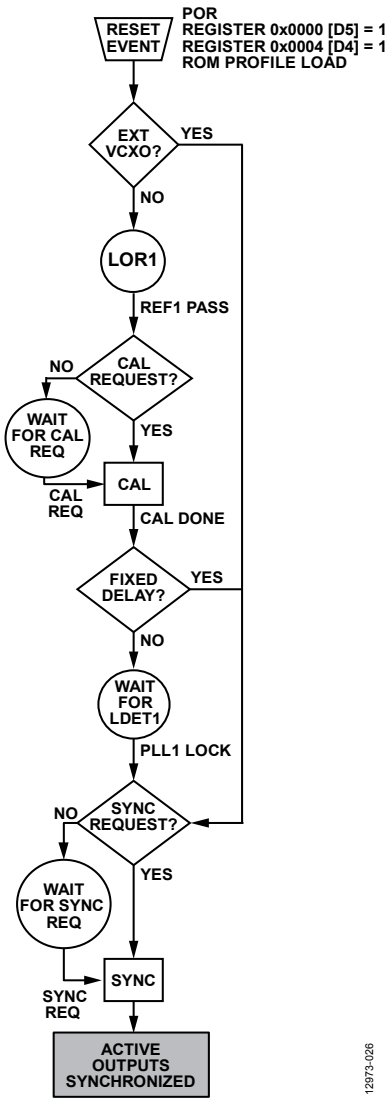


Figure 27. PLL1 Reset Sequence Flowchart

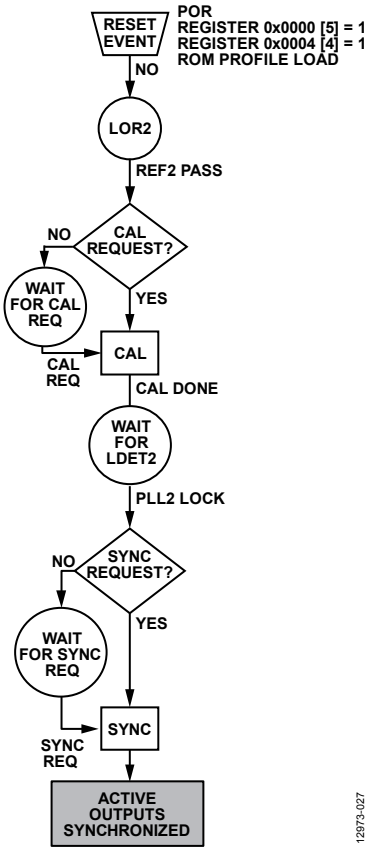


Figure 28. PLL2 Reset Sequence Flowchart

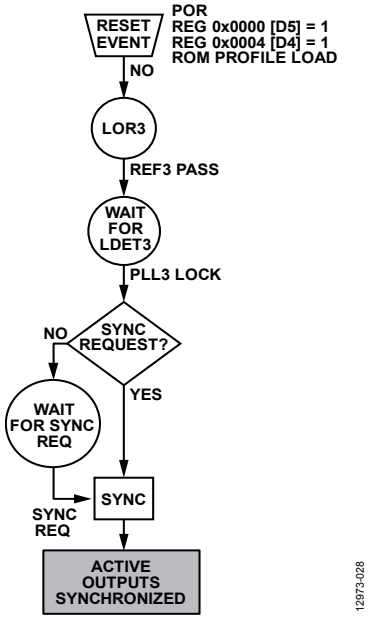


Figure 29. PLL3 Reset Sequence Flowchart

SERIAL CONTROL PORT

The AD9531 serial control port is a flexible, synchronous, serial communications port that allows an easy interface to many industry-standard microcontrollers and microprocessors. The serial port supports single or multiple byte transfers, as well as MSB first or LSB first data transfer formats. Note that the AD9531 serial control port does not have dedicated input and output data pins, but only a single bidirectional SDIO pin.

The serial control port has two types of registers: read only register and writable registers. Read only registers are nonbuffered and ignore write commands. Most writable registers are buffered (also referred to as mirrored) and require an input/output update to transfer the new values from a temporary buffer on the chip to the actual register. To invoke an input/output update, write a 1 to the input/output update bit in Register 0x0005, Bit D0. Because any number of bytes of data can be changed before issuing an update command, the update simultaneously enables all register changes that occur after any previous update.

The serial port physical interface can operate from 1.8 V to 3.3 V based on the voltage provided on the DVDD_IO pin. The default output drive strength is intended for 1.8 V operation, but a strength reduction option is possible via Register 0x0004, Bit D1.

SERIAL CONTROL PORT PIN DESCRIPTIONS

SCLK (serial data clock) is the serial shift clock. This pin is an input and synchronizes the serial control port read and write cycles. The serial port captures write data bits on the rising edge of SCLK, and delivers read data bits on the falling edge of SCLK.

SDIO (digital serial data input/output) is the serial data pin.

$\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDIO is in a high impedance state (note that $\overline{CS}$ must not be left floating). See the Operation of the Serial Control Port section for information on the use of the $\overline{CS}$ pin in a communication cycle.

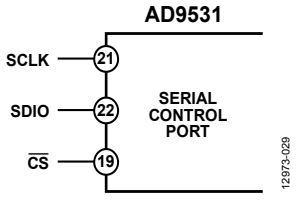


Figure 30. Serial Control Port

OPERATION OF THE SERIAL CONTROL PORT

Framing a Communication Cycle with $\overline{CS}$

The $\overline{CS}$ line gates the communication cycle (a write or a read operation). Set $\overline{CS}$ to Logic 0 to initiate a communication cycle.

The $\overline{CS}$ stall high function is supported in modes where three or fewer bytes of data (plus instruction data) are transferred. Bits[W1:W0] of the Instruction Word (16 Bits) (see Table 50) must be set to 00, 01, or 10 (see Table 49).

In these modes, $\overline{CS}$ may temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer. During this period, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort before the complete transfer of all the data, it is necessary to reset the state machine by either completing the remaining transfer or by returning the $\overline{CS}$ line low for at least one complete SCLK cycle (but fewer than eight SCLK cycles). A rising edge on the $\overline{CS}$ pin on a nonbyte boundary terminates the serial transfer and flushes the buffer.

Table 49. Byte Transfer Count

W1	W0	Bytes to Transfer (Excluding the 2-Byte Instruction)
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

In streaming mode (Bits[W1:W0] = 11), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). At the end of the last byte to be transferred, set $\overline{CS}$ to Logic 1 to end the stream mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9531. The first part writes a 16-bit instruction word into the AD9531, coincident with the first 16 SCLK rising edges. The Instruction Word (16 Bits) (see Table 50) provides the AD9531 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write Operation

If the instruction word is for a write operation (Bit I15 = 0), the second part is the transfer of data into the serial control port buffer of the AD9531. The length of the transfer (1, 2, or 3 bytes or streaming mode) is indicated by two bits (Bits[W1:W0]) in the instruction word. The length of the transfer indicated by Bits[W1:W0] does not include the 2-byte instruction word. Pull $\overline{CS}$ high after each sequence of eight bits to stall the bus (except after the last byte, where this ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is pulled low. Stalling on nonbyte boundaries resets the serial control port. Note that stalling via the $\overline{CS}$ pin is not applicable in streaming mode.

Read Operation

If the instruction word is for a read operation (Bit I15 = 1), the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N = 1, 2, 3, or 4, as determined by Bits[W1:W0]. In this case, the value of 4 is used for streaming mode, where four or more words are transferred per read. The serial port delivers the readback data to the SDIO pin on the falling edge of SCLK.

By default, a read request reads the register value that is currently in use by the AD9531. However, setting Register 0x0004, Bit D0 = 1 causes the buffered registers to be read instead. The buffered registers are the registers that take effect during the next input/output update.

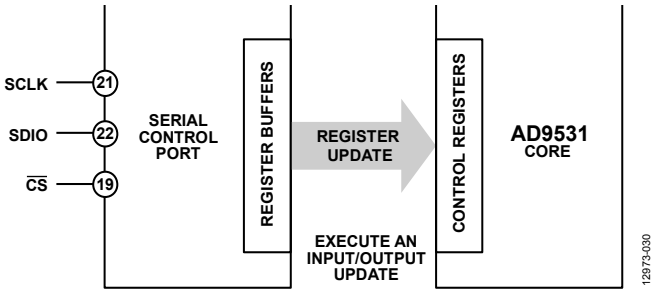


Figure 31. Relationship Between the Serial Control Port Register Buffers and the Control Registers

INSTRUCTION WORD (16 BITS)

The MSB of the instruction word (see Table 50) is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits, W1 and W0, are the transfer length in bytes. The final 13 bits are the address bits (Address Bits[A12:A0]), at which the read or write operation begins.

For a write operation, the instruction word is followed by the number of bytes of data indicated by Bits[W1:W0], which is interpreted according to Table 49.

Address Bits[A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communication cycle. The AD9531 uses all of the 13-bit address space. For multibyte transfers, this address is the starting byte address.

MSB/LSB FIRST TRANSFERS

The AD9531 instruction word and byte data can be MSB first or LSB first. The default for the AD9531 is MSB first. Activate the LSB first mode by setting Register 0x0000, Bit D6 = 1 (an input/output update is not required). Immediately after writing Register 0x0000, Bit D6 = 1, all serial control port operations are changed to LSB first order.

When MSB first mode is active, the instruction word and data bytes must occur in MSB to LSB order. Multibyte data transfers in MSB first format start with an instruction word that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from high address to low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first mode is active, the instruction word and data bytes must occur in LSB to MSB order. Multibyte data transfers in LSB first format start with an instruction word that includes the register address of the least significant data byte followed by multiple data bytes. In LSB first mode, the serial control port internal address generator increments for each data byte of the multibyte transfer cycle.

In summary, for MSB first (default) multibyte input/output operations, the AD9531 serial control port internal address generator decrements, whereas for LSB first multibyte input/output operations, it increments. Furthermore, the serial port controller does not skip unused addresses for multibyte input/output operations. Write the default value to a reserved register, or write Logic 0 to unused registers. It is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unused) registers.

Table 50. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	**I14**	**I13**	**I12**	**I11**	**I10**	**I9**	**I8**	**I7**	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 51. Definition of Terms Used in the Serial Control Port Timing Diagrams (See Figure 32 Through Figure 37)

Parameter	Description
t_{SCLK}	Period of SCLK
t_{DV}	Read data valid time (the time from the falling edge of SCLK to valid data on SDIO)
t_{DS}	Setup time between data and the rising edge of SCLK
t_{DH}	Hold time between data and the rising edge of SCLK
t_S	Setup time between $\overline{CS}$ and SCLK
t_H	Hold time between $\overline{CS}$ and SCLK
t_{HIGH}	Minimum period that SCLK can be in a logic high state
t_{LOW}	Minimum period that SCLK can be in a logic low state

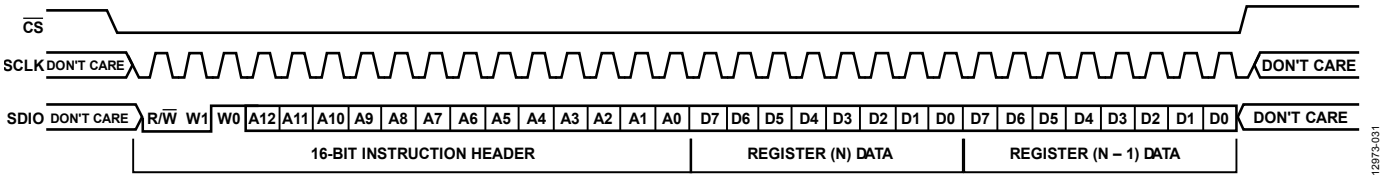


Figure 32. Serial Control Port Write—MSB First, 16-Bit Instruction, Two Bytes Data

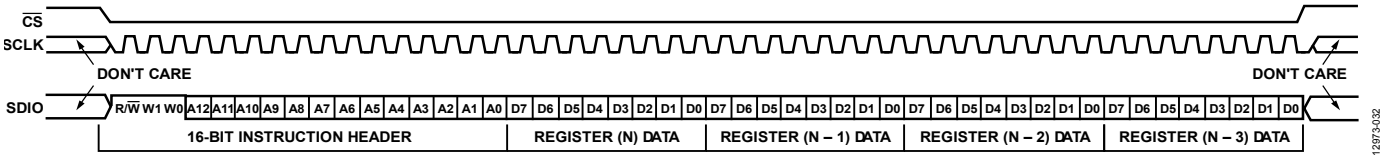


Figure 33. Serial Control Port Read—MSB First, 16-Bit Instruction, Four Bytes Data

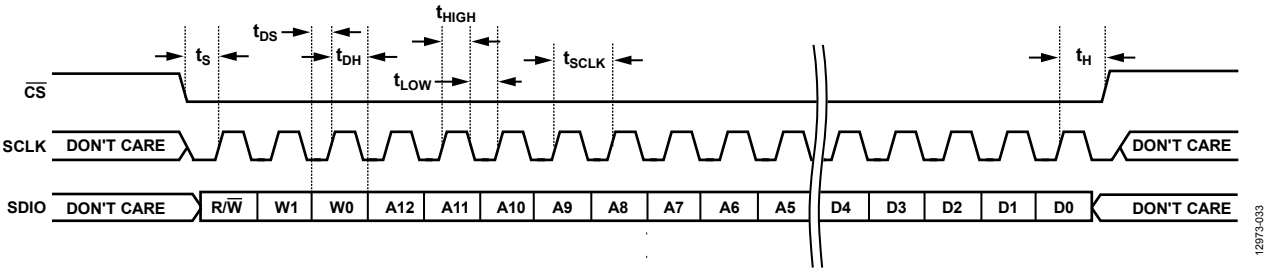


Figure 34. Serial Control Port Write Timing Diagram—MSB First, 16-Bit Instruction, Timing Measurements

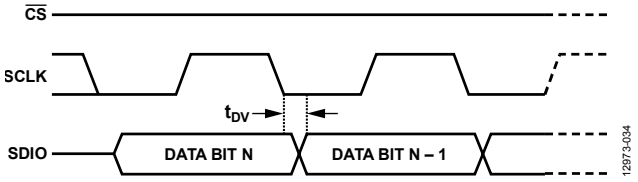


Figure 35. Timing Diagram for a Serial Control Port Register Read

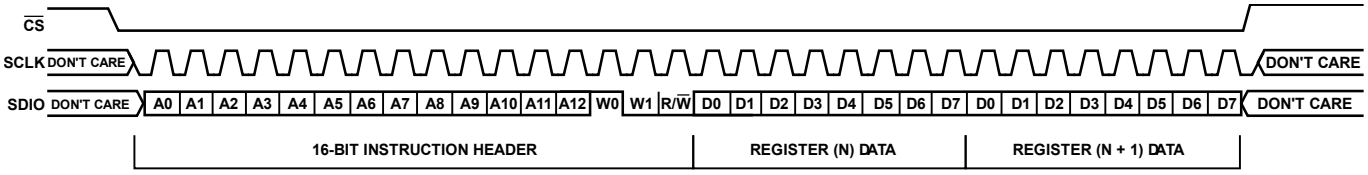


Figure 36. Serial Control Port Write—LSB First, 16-Bit Instruction, Two Bytes Data

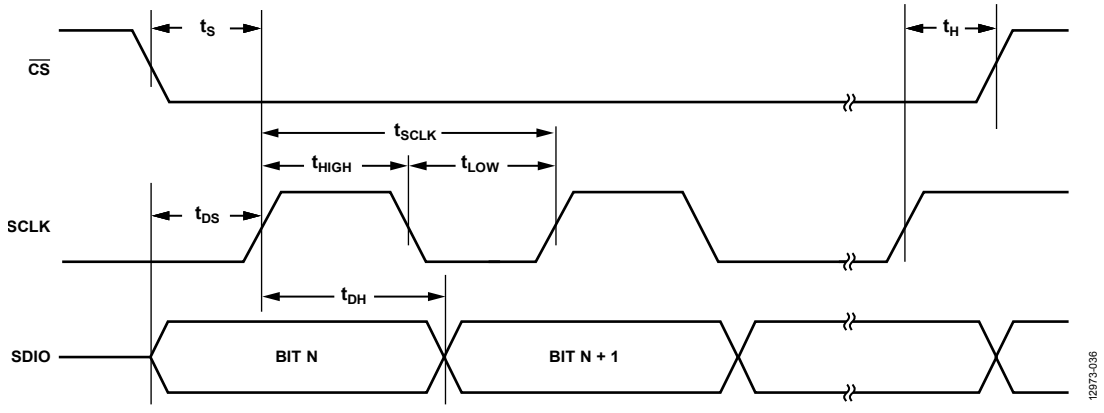


Figure 37. Serial Control Port Timing for a Serial Control Port Register Write

REGISTER MAP

Registers are generic with normal read/write capability unless otherwise noted in the option column (Opt.) as follows:

- A means automatically cleared.
- B means buffered register (requires an input/output update).
- R means read only.
- X means execute ROM load on register write.
- N/A means not applicable.

The user must avoid writing to register addresses not listed in Table 52. Such undocumented addresses may have reserved functionality and writing to them may cause abnormal device behavior.

Bits labeled unused have no associated physical hardware; therefore, writing to these bits has no effect.

Bits labelled reserved may have associated hardware. When writing to reserved bits, use the values in the default column (Def.).

In the default column,

- Values are hexadecimal, unless otherwise noted.
- Values with an R prefix indicate that the default values originate from the ROM and the digits following the R prefix indicate the ROM indices associated with the register bits (see the ROM Profile Data section).
- The "spec" default value (Register 0x0004) is Logic 0 for all bits except the D1 bit, which uses ROM default R639 (see the ROM Profile Data section).
- The "pin" default value (Register 0x000E) indicates that the multifunction pins set the default value as described in the Multifunction Pins (LDET1/M1, LDET2/M2, LDET3/M3, LOR/M4) section.

Table 52. Register Map

Reg. Addr. (Hex)	Opt.	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def.
Serial Port Control Registers											
0x0000	N/A	SPI control	Unused	LSB first	Soft reset	Unused					0x00
0x0004	N/A	Serial port options	Unused			Hardware reset	Unused		Reduce SPI strength	Read buffer register	Spec
0x0005	A	Input/output (I/O) update	Unused							I/O update	0x00
Device and ROM Profile Identification Registers											
0x000A	R	Device ID	Device ID, Bits[31:24]								0x10
0x000B	R		Device ID, Bits[23:16]								0x00
0x000C	R		Device ID, Bits[15:8]								0x08
0x000D	R		Device ID, Bits[7:0]								0x00
0x000E	X	Profile	Reserved		ROM profile, Bits[5:0]						Pin
Status Registers											
0x0080	R	Status	Reserved		PLL2 calibration in progress	PLL1 calibration in progress	Reserved	PLL3 lock detect	PLL2 lock detect	PLL1 lock detect	N/A
0x0081	R		Unused				REF3 LOR	REF2 LOR	REF1B LOR	REF1A LOR	N/A
0x0082	R		Unused				Reserved	PLL1 freerun	PLL1 holdover	PLL1 active reference	N/A
LDET/LOR Control Registers											
0x0083	B	LDET	Reserved		LDET3 3.3 V mode	LDET3 invert	LDET2 3.3 V mode	LDET2 invert	LDET1 3.3 V mode	LDET1 invert	ROM
0x0084	B	LOR	Reserved	3.3 V mode	Invert	REF3 LOR	REF2 LOR	Active REF1 LOR	REF1B LOR	REF1A LOR	ROM
0x0085	B	LOR2	Reserved	3.3 V mode	Invert	REF3 LOR	REF2 LOR	Active REF1 LOR	REF1B LOR	REF1A LOR	ROM
PLL1 Registers											
0x0100	B	PLL1 General Registers	Unused				Reserved	Manual sync	Manual calibrate	Power-down	ROM
0x0101	B		Enable M1 during VCO calibration	Fixed delay, Bits[1:0]		3.3 V charge pump current, Bits[2:0]			External oscillator (VCXO) mode, Bits[1:0]		ROM
0x0102	B		Freerun	Holdover	Enable reference select	Reference select	Wide bandwidth mode	Freerun vs. holdover	Enable autohold	Enable autoswitch	ROM
0x0103	B		VCO calibration reset	REF1B input mode, Bits[1:0]		REF1B power-down	Reserved	REF1A input mode, Bits[1:0]		REF1A power-down	ROM

Reg. Addr. (Hex)	Opt.	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def.
0x0104	B	PLL1 frequency translation registers	R1, Bits[7:0]								ROM
0x0105	B		Unused				R1, Bits[11:8]				ROM
0x0106	B		N1A, Bits[7:0]								ROM
0x0107	B		N1A fraction, Bits[7:0]								ROM
0x0108	B		N1A fraction, Bits[15:8]								ROM
0x0109	B		Reserved				N1A fraction, Bits[19:16]				ROM
0x010A	B		N1A modulus, Bits[7:0]								ROM
0x010B	B		N1A modulus, Bits[15:8]								ROM
0x010C	B		Reserved				N1A modulus, Bits[19:16]				ROM
0x010D	B		N1B, Bits[7:0]								ROM
0x010E	B		Unused				N1B, Bits[11:8]				ROM
0x010F	B		Unused				M1, Bits[3:0]				ROM
0x0110	B	D1A	D1A, Bits[7:0]								ROM
0x0111	B	OUT1_0	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0112	B	OUT1_1	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0113	B	OUT1_2	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0114	B	OUT1_3	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0115	B	D1B	D1B, Bits[7:0]								ROM
0h0116	B	OUT1_4	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0117	B	OUT1_5	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0118	B	OUT1_6	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0119	B	OUT1_7	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x011A	B	D1C	D1C [7:0]								ROM
0x011B	B	OUT1_8	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x011C	B	OUT1_9	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
PLL2 Registers											
0x0200	B	PLL2 general registers	Unused		Reserved	XTAL amplifier	Reserved	Manual sync	Manual calibrate	Power-down	ROM
0x0201	B		Unused				Manual charge pump current	Charge pump current, Bits[2:0]			ROM
0x0202	B	PLL2 frequency translation registers	Unused				R2, Bits[3:0]				ROM
0x0203	B		N2, Bits[7:0]								ROM
0x0204	B		Unused				M2, Bits[3:0]				ROM
0x0205	B	D2A	D2A, Bits[7:0]								ROM
0x0206	B	OUT2_0	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0207	B	OUT2_1	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x0208	B	D2B	D2B, Bits[7:0]								ROM
0x0209	B	OUT2_2	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x020A	B	OUT2_3	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x020B	B	OUT2_4	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM
0x020C	B	D2C	D2C [7:0]								ROM
0x020D	B	OUT2_5	Unused			Logic mode, Bits[2:0]		Polarity, Bits[1:0]		Power-down	ROM

Reg. Addr. (Hex)	Opt.	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def.
0x020E	B	OUT2_6	Unused		Logic mode, Bits[2:0]			Polarity, Bits[1:0]		Power-down	ROM
0x020F	B	OUT2_7	Unused		Logic mode, Bits[2:0]			Polarity, Bits[1:0]		Power-down	ROM
0x0210	B	D2D	D2D [7:0]								ROM
0x0211	B	OUT2_8	Unused		Logic mode, Bits[2:0]			Polarity, Bits[1:0]		Power-down	ROM
0x0212	B	OUT2_9	Unused		Logic mode, Bits[2:0]			Polarity, Bits[1:0]		Power-down	ROM
0x0213	B	OUT2_10	Unused		Logic mode, Bits[2:0]			Polarity, Bits[1:0]		Power-down	ROM
0x0214	B	OUT2_11	Unused		Logic mode, Bits[2:0]			Polarity, Bits[1:0]		Power-down	ROM
PLL3 Registers											
0x0300	B	PLL3 general registers	Unused		Reserved	XTAL amplifier	Reserved	Manual sync	Reserved	Power-down	ROM
0x0301	B	PLL3 frequency translation registers	Unused		×2B	×2A	Reference scaling, Bits[3:0]				ROM
0x0302	B		N3A, Bits[7:0]								ROM
0x0303	B		R3B, Bits[7:0]								ROM
0x0304	B		N3B, Bits[7:0]								ROM
0x0305	B	OUT3_0	Reserved				D3A, Bits[3:0]				ROM
0x0306	B		Unused				3.3 V mode	Reserved	Invert	Power-down	ROM
0x0307	B	OUT3_1	Reserved				D3B, Bits[3:0]				ROM
0x0308	B		Unused	Logic mode, Bits[3:0]				Polarity, Bits[1:0]		Power-down	ROM

REGISTER MAP DETAILS

Control bit functions are active high and register address values are hexadecimal, unless otherwise noted.

SERIAL PORT CONTROL REGISTERS—REGISTER 0x0000 TO REGISTER 0x0005

Table 53. Serial Port Control Register Details

Address	Bits	Bit Name	Description
0x0000	D7	Unused	Unused.
	D6	LSB first	Bit order for the SPI port. 0 (default): most significant bit first and, for multibyte transfers, most significant byte first with autodecrement register addressing. 1: least significant bit first and, for multibyte transfers, least significant byte first with autoincrement register addressing.
	D5	Soft reset	Software initiated reset. This bit restores register contents to the current ROM profile values.
	[D4:D0]	Unused	Unused.
0x0004	[D7:D5]	Unused	Unused.
	D4	Hardware reset	Software initiated hardware reset. This bit resets the internal device hardware without changing the current register contents. This bit does not autoclear; therefore, for proper device operation, first write a Logic 1 then, a Logic 0.
	[D3:D2]	Unused	Unused.
	D1	Reduce SPI strength	Alters the strength of the SPI port control pins. The default value for this bit resides in the ROM. 0: normal SPI strength. 1: reduced SPI strength.
	D0	Read buffer register	Read cycle target (SPI or buffered register(s)). 0 (default): read cycles apply to the SPI registers. 1: read cycles apply to the buffered registers.
0x0005	[D7:D1]	Unused	Unused.
	D0	I/O update	Software initiated input/output update. This is an autoclearing bit.

DEVICE IDENTIFICATION AND ROM PROFILE REGISTERS—REGISTER 0x000A TO REGISTER 0x000E

Register 0x000A to Register 0x000D are read-only. Writing to Register 0x000E invokes a ROM load sequence.

Table 54. Device Identification and ROM Profile Register Details

Address	Bits	Bit Name	Description
0x000A	[D7:D0]	Device ID [31:24]	Most significant byte of the device ID.
0x000B	[D7:D0]	Device ID [23:16]	Next byte of the device ID.
0x000C	[D7:D0]	Device ID [15:8]	Next byte of the device ID.
0x000D	[D7:D0]	Device ID [7:0]	Least significant byte of the device ID.
0x000E	[D7:D6]	Reserved	Reserved.
	[D5:D0]	ROM profile	Reading this register provides the index value of the most recently loaded ROM profile. Writing to the register selects one of 64 possible ROM profiles. The contents of this register are initially set at power-up as described in the Multifunction Pins (LDET1/M1, LDET2/M2, LDET3/M3, LOR/M4) section. Note that writing to this register loads the specified ROM profile, thereby updating the value of all registers identified by ROM in the default column of the Register Map. The contents of a register with ROM in the default column of the Register Map depend on the ROM profile number identified by the bits in this register (see the ROM Profile Data section).

STATUS REGISTERS—REGISTER 0x0080 TO REGISTER 0x0082

Register 0x0080 to Register 0x0082 are read-only.

Table 55. Status Register Details

Address	Bits	Bit Name	Description
0x0080	[D7:D6]	Reserved	Reserved.
	D5	PLL2 calibration in progress	This bit reflects the state of the PLL2 calibration controller. Logic 1 indicates that the PLL2 internal VCO calibration is in progress.
	D4	PLL1 calibration in progress	This bit reflects the state of the PLL1 calibration controller. Logic 1 indicates that the PLL1 internal VCO calibration is in progress.
	D3	Reserved	Reserved.
	D2	PLL3 lock detect	This bit reflects the state of the lock detector for PLL3. Logic 1 indicates a lock condition for PLL3.
	D1	PLL2 lock detect	This bit reflects the state of the lock detector for PLL2. Logic 1 indicates a lock condition for PLL2.
	D0	PLL1 lock detect	This bit reflects the state of the lock detector for PLL1. Logic 1 indicates a lock condition for PLL1.
0x0081	[D7:D4]	Unused	Unused.
	D3	REF3 LOR	Logic 1 indicates a loss of reference condition for PLL3. Only the first of the two cascaded PLLs of PLL3 provides the LOR status.
	D2	REF2 LOR	Logic 1 indicates a loss of reference condition for PLL2.
	D1	REF1B LOR	Logic 1 indicates a loss of reference condition for PLL1 REF1_B.
	D0	REF1A LOR	Logic 1 indicates a loss of reference condition for PLL1 REF1_A.
0x0082	[D7:D4]	Unused	Unused.
	D3	Reserved	Reserved.
	D2	PLL1 freerun	This bit indicates (Logic 1) PLL1 is in freerun mode.
	D1	PLL1 holdover	This bit indicates (Logic 1) PLL1 is in holdover mode.
	D0	PLL1 active reference	This bit indicates the currently active reference. Logic 0 indicates REF1_A is the currently active reference. Logic 1 indicates REF1_B is the currently active reference.

LDET/LOR CONTROL REGISTERS—REGISTER 0x0083 TO REGISTER 0x0085

Register 0x0083 controls the three LDETx pins. Register 0x0084 controls the LOR pin, where Bits[D4:D0] provide logical OR indication of the various loss of reference detectors at the LOR pin. Register 0x0085 controls the OUT3_0 pin of PLL3, where Bits[D4:D0] provide logical OR indication of the various loss of referenced detectors on the OUT3_0 pin. When Register 0x0085, Bits[D4:D0] = 00000, the OUT3_0 pin functions normally (that is, as the output of PLL3).

Table 56. LDETx/LOR Control Register Details

Address	Bits	Bit Name	Description
0x0083	[D7:D6]	Reserved	Reserved.
	D5	LDET3 3.3 V mode	0: LDET3/M3 pin, 1.8 V mode. 1: LDET3/M3 pin, 3.3 V mode.
	D4	LDET3 invert	0: LDET3/M3 pin normal (active high logic). 1: LDET3/M3 pin inverted (active low logic).
	D3	LDET2 3.3 V mode	0: LDET2/M2 pin, 1.8 V mode. 1: LDET2/M2 pin, 3.3 V mode.
	D2	LDET2 invert	0: LDET2/M2 pin normal (active high logic). 1: LDET2/M2 pin inverted (active low logic).
	D1	LDET1 3.3 V mode	0: LDET1/M1 pin, 1.8 V mode. 1: LDET1/M1 pin, 3.3 V mode.
	D0	LDET1 invert	0: LDET1/M1 pin normal (active high logic). 1: LDET1/M1 pin inverted (active low logic).
0x0084	D7	Reserved	Reserved.
	D6	3.3 V mode	0: LOR/M4 pin, 1.8 V mode. 1: LOR/M4 pin, 3.3 V mode.
	D5	Invert	0: LOR/M4 pin normal (active high logic). 1: LOR/M4 pin inverted (active low logic).

Address	Bits	Bit Name	Description
	D4	REF3 LOR	0: disallows loss of reference indication on the LOR/M4 pin by PLL3. 1: allows loss of reference indication on the LOR/M4 pin by PLL3.
	D3	REF2 LOR	0: disallows loss of reference indication on the LOR/M4 pin by PLL2. 1: allows loss of reference indication on the LOR/M4 pin by PLL2.
	D2	Active REF1 LOR	0: disallows loss of reference indication on the LOR/M4 pin by the active reference of PLL1. 1: allows loss of reference indication on the LOR/M4 pin by the active reference (REF1_A or REF1_B) of PLL1.
	D1	REF1B LOR	0: disallows loss of reference indication on the LOR/M4 pin by REF1_B of PLL1. 1: allows loss of reference indication on the LOR/M4 pin by REF1_B of PLL1.
	D0	REF1A LOR	0: disallows loss of reference indication on the LOR/M4 pin by REF1_A of PLL1. 1: allows loss of reference indication on the LOR/M4 pin by REF1_A of PLL1.
0x0085	D7	Reserved	Reserved.
	D6	3.3 V mode	This bit controls the output drive voltage of OUT3_0 when any bit of Register 0x0085, Bits[D4:D0] is Logic 1. In this case, OUT3_0 is a static logic output indicating LOR status per the drive voltage specified at this bit location (the drive voltage specified by this bit overrides Register 0x0306, Bit D3). 0: OUT3_0 pin = 1.8 V mode LOR indication. 1: OUT3_0 pin = 3.3 V mode LOR indication.
	D5	Invert	This bit controls the logical sense of OUT3_0 when any bit of Register 0x0085, Bits[D4:D0] is Logic 1. In this case, OUT3_0 is a static logic output indicating LOR status with the logical sense specified at this bit location (the logical sense specified by this bit overrides Register 0x0306, Bit D1). 0: OUT3_0 pin normal (active high logic). 1: OUT3_0 pin inverted (active low logic).
	D4	REF3 LOR	0: disallows loss of reference indication on the OUT3_0 pin by PLL3. 1: allows loss of reference indication on the OUT3_0 pin by PLL3.
	D3	REF2 LOR	0: disallows loss of reference indication on the OUT3_0 pin by PLL2. 1: allows loss of reference indication on the OUT3_0 pin by PLL2.
	D2	Active REF1 LOR	0: disallows loss of reference indication on the OUT3_0 pin by the active reference of PLL1. 1: allows loss of reference indication on the OUT3_0 pin by active reference of PLL1.
	D1	REF1B LOR	0: disallows loss of reference indication on the OUT3_0 pin by REF1_B of PLL1. 1: allows loss of reference indication on the OUT3_0 pin by REF1_B of PLL1.
	D0	REF1A LOR	0: disallows loss of reference indication on the OUT3_0 pin by REF1_A of PLL1. 1: allows loss of reference indication on the OUT3_0 pin by REF1_A of PLL1.

PLL1 REGISTERS

PLL1 General Registers—Register 0x0100 to Register 0x0103

Table 57. PLL1 General Register Details

Address	Bits	Bit Name	Description
0x0100	[D7:D4]	Unused	Unused.
	D3	Reserved	Reserved.
	D2	Manual sync	Write Logic 1 to this bit to arm the distribution synchronization circuit, then write Logic 0 to cause the distribution channel dividers to synchronize (synchronization occurs on the falling edge of this bit).
	D1	Manual calibrate	Logic 1 causes the VCO calibration sequence to execute for PLL1. For robustness, write to this bit in three operations: Logic 0, Logic 1, then Logic 0 with an input/output update following each operation.
	D0	Power-down	Logic 1 causes a full power-down of PLL1.
0x0101	D7	Enable M1 during VCO calibration	0: normal operation (default). The M1 divider is in a reset state during calibration to ensure a defined set of initial conditions at power-up or following a device reset. 1: causes the M1 divider to remain active during PLL1 VCO calibration. Allows the user to observe the calibration process at the clock outputs of PLL1.

Address	Bits	Bit Name	Description
	[D6:D5]	Fixed delay [1:0]	These bits select a particular output distribution group when using the fixed delay function (see the PLL1 Loop 4 Configuration section). 00: disables the fixed delay function. 01: selects OUT1_0x (Group 1A outputs) as the fixed delay feedback source. 10: selects OUT1_4x (Group 1B outputs) as the fixed delay feedback source. 11: selects OUT1_8x (Group 1C outputs) as the fixed delay feedback source.
	[D4:D2]	3.3 V charge pump current [2:0]	These bits establish the charge pump current for the 3.3 V charge pump of PLL1 (used for controlling an external VCXO). 000: 625 µA. 001: 1250 µA. 010: 1875 µA. 011: 2500 µA. 100: 3125 µA. 101: 3750 µA. 110: 4375 µA. 111: 5000 µA.
	[D1:D0]	External oscillator (VCXO) mode [1:0]	These bits determine the functionality of the RFIN_1P/RFIN_1N pins when using an external loop configuration (see the PLL1 Loop Configurations section). 00: disables the external VCXO function. 01: single-ended input (RFIN_1P). 10: single-ended input (RFIN_1N). 11: differential input.
0x0102	D7	Freerun	Logic 1 forces PLL1 into freerun mode, but only if an external loop configuration is in effect. Otherwise, Logic 1 forces PLL1 into holdover mode.
	D6	Holdover	Logic 1 forces PLL1 into holdover mode.
	D5	Enable reference select	0: disables the functionality of the reference select bit. 1: enables the functionality of the reference select bit.
	D4	Reference select	This bit is ineffective when Register 0x0102, Bit D5 = 0. 0: forces REF1_A to be the active reference for PLL1. 1: forces REF1_B to be the active reference for PLL1.
	D3	Wide bandwidth mode	See the PLL1 Loop 2 Wide Bandwidth Configuration section for details. 0: disables the wide bandwidth mode. 1: enables the wide bandwidth mode.
	D2	Freerun vs. holdover	Logic 1 allows automatic transition to freerun mode instead of holdover mode. This transition is only effective when the enable auto hold bit is set and an external loop configuration is in effect.
	D1	Enable autohold	Logic 1 activates the control logic that allows automatic transition to holdover mode when conditions warrant this transition.
	D0	Enable autoswitch	Logic 1 activates the control logic that allows automatic switching to an alternate reference upon LOR indication of the active reference.
0x0103	D7	VCO calibration reset	0: normal operation (default). 1: resets the PLL1 VCO calibration circuitry. This is a fail-safe control bit. Normally, a reset of the calibration circuitry automatically occurs at the start of calibration.
	[D6:D5]	REF1B input mode [1:0]	These bits set the configuration of the REF1_B input reference. 00: differential input (REF1_BP/REF1_BN inputs active). 01: 3.3 V CMOS single-ended (REF1_BP active, REF1_BN disabled). 10: not applicable. 11: 2.5 V CMOS single-ended (REF1_BP active, REF1_BN disabled).
	D4	REF1B power-down	Logic 1 powers down the REF1_BP/REF1_BN inputs.
	D3	Reserved	Reserved.

Address	Bits	Bit Name	Description
	[D2:D1]	REF1A input mode [1:0]	These bits set the configuration of the REF1_A input reference. 00: differential input (REF1_AP/REF1_AN inputs active). 01: 3.3 V CMOS single-ended (REF1_AP active, REF1_AN disabled). 10: not applicable. 11: 2.5 V CMOS single-ended (REF1_AP active, REF1_AN disabled).
	D0	REF1A power-down	Logic 1 powers down the REF1_AP/REF1_AN inputs.

PLL1 Frequency Translation Registers—Register 0x0104 to Register 0x010F

Table 58. PLL1 Frequency Translation Register Details

Address	Bits	Bit Name	Description
0x0104	[D7:D0]	R1 [7:0]	R1 divider Bit D7 to Bit D0 (LSB). See Register 0x0105, Bits[D3:D0] for details.
0x0105	[D7:D4]	Unused	Unused.
	[D3:D0]	R1 [11:8]	R1 divider Bit D11 (MSB) to Bit D8. The value of R1, Bits[D11:D0] results in the following behavior: 0: multiplies the input frequency by a factor of 2. 1 to 3: passes the input frequency unaltered (R1 divider bypass). 4 to 4095: divides the input frequency by this value.
0x0106	[D7:D0]	N1A [7:0]	N1A Bit D7 (MSB) to Bit D0 (LSB). The value of N1A [7:0] results in the following behavior, depending on the operating mode (integer-N or fractional-N): For integer-N mode, 0 to 14: not applicable. 15 to 255: divide by this value. For fractional-N mode, 0 to 79: not applicable. 80 to 255: divide by this value.
0x0107	[D7:D0]	N1A fraction [7:0]	N1A Fraction Bit D7 to Bit D0 (LSB). See Register 0x0109, Bits[D3:D0] for details.
0x0108	[D7:D0]	N1A fraction [15:8]	N1A Fraction Bit D15 to Bit D8. See Register 0x0109, Bits[D3:D0] for details.
0x0109	[D7:D4]	Reserved	Reserved.
	[D3:D0]	N1A fraction [19:16]	N1A Fraction Bit D19 (MSB) to Bit D16. The value of N1A fraction [19:0] results in the following behavior: 0: enables integer mode (disables the Σ-Δ modulator). 1 to 1048574: enables fractional-N mode (Σ-Δ modulator active).
0x010A	[D7:D0]	N1A modulus [7:0]	N1A Modulus Bit D7 to Bit D0 (LSB). See Register 0x010C, Bits[D3:D0] for details.
0x010B	[D7:D0]	N1A modulus [15:8]	N1A Modulus Bit D8 to Bit D15. See Register 0x010C, Bits[D3:D0] for details.
0x010C	[D7:D4]	Reserved	Reserved.
	[D3:D0]	N1A modulus [19:16]	N1A Modulus Bit D19 (MSB) to Bit D16. N1A Modulus [19:0] must be greater than N1A fraction (1,048,575 maximum).
0x010D	[D7:D0]	N1B [7:0]	N1B Bit D7 to Bit D0 (LSB). See Register 0x010E, Bits[D3:D0] for details.
0x010E	[D7:D4]	Unused	Unused.
	[D3:D0]	N1B [11:8]	N1B Bit D11 (MSB) to Bit D8. The value of N1B [11:0] results in the following behavior: 0 to 1: disallows the Loop 2 configuration and bypasses the N1B divider. 2 to 3: undefined. 4 to 4095: divides the by this value. The Loop 4 configuration bypasses the N1B divider regardless of the value of N1B [11:0].
0x010F	[D7:D4]	Unused	Unused.
	[D3:D0]	M1 [3:0]	M1 Bit D3 (MSB) to Bit D0. The value of the M1 [3:0] bits results in the following behavior: 0 to 2: disable. 3 to 11: divide by this value. 12 to 14: disables VCO calibration after changing the value of M1. 15: M1 divider reset state. If the user intends to change the M1 divider without performing a subsequent PLL1 VCO calibration, then program this value (followed by an input/output update) before programming the new M1 divider value (followed by an input/output update). An input/output update is writing Register 0x0005, Bit D0 = 1. The procedure given here is unnecessary if the user performs a PLL1.

Registers for PLL1 Group 1A Outputs, OUT1_0x to OUT1_3x—Register 0x0110 to Register 0x0114

Table 59. PLL1 Group 1A Outputs Register Details

Address	Bits	Bit Name	Description
0x0110	[D7:D0]	D1A [7:0]	D1A divider Bit D7 (MSB) to Bit D0 (LSB). The divide factor is the value of D1A [7:0] + 1. D1A powers down when all four of the associated output drivers power down, whether via the power-down bit or via the logic mode bits.
0x0111	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	These bits configure the OUT1_0x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_0P active, OUT1_0N active. 101: 1.8 V CMOS, OUT1_0P active, OUT1_0N disabled. 110: 1.8 V CMOS, OUT1_0P disabled, OUT1_0N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_0x polarity as follows (applies to CMOS only): 00: OUT1_0P normal, OUT1_0N inverted. 01: OUT1_0P normal, OUT1_0N normal. 10: OUT1_0P inverted, OUT1_0N inverted. 11: OUT1_0P inverted, OUT1_0N normal.
	D0	Power-down	0: OUT1_0x driver active. 1: OUT1_0x driver powered down.
0x0112	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT1_1x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_1P active, OUT1_1N active. 101: 1.8 V CMOS, OUT1_1P active, OUT1_1N disabled. 110: 1.8 V CMOS, OUT1_1P disabled, OUT1_1N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_1x polarity as follows (applies to CMOS only): 00: OUT1_1P normal, OUT1_1N inverted. 01: OUT1_1P normal, OUT1_1N normal. 10: OUT1_1P inverted, OUT1_1N inverted. 11: OUT1_1P inverted, OUT1_1N normal.
	D0	Power-down	0: OUT1_1x driver active. 1: OUT1_1x driver powered down.
0x0113	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT1_2x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_2P active, OUT1_2N active. 101: 1.8 V CMOS, OUT1_2P active, OUT1_2N disabled. 110: 1.8 V CMOS, OUT1_2P disabled, OUT1_2N active. 111: undefined.

Address	Bits	Bit Name	Description
	[D2:D1]	Polarity [1:0]	Configure OUT1_2x polarity as follows (applies to CMOS only): 00: OUT1_2P normal, OUT1_2N inverted. 01: OUT1_2P normal, OUT1_2N normal. 10: OUT1_2P inverted, OUT1_2N inverted. 11: OUT1_2P inverted, OUT1_2N normal.
	D0	Power-down	0: OUT1_2x driver active. 1: OUT1_2x driver powered down.
0x0114	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT1_3x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_3P active, OUT1_3N active. 101: 1.8 V CMOS, OUT1_3P active, OUT1_3N disabled. 110: 1.8 V CMOS, OUT1_3P disabled, OUT1_3N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_3x polarity as follows (applies to CMOS only): 00: OUT1_3P normal, OUT1_3N inverted. 01: OUT1_3P normal, OUT1_3N normal. 10: OUT1_3P inverted, OUT1_3N inverted. 11: OUT1_3P inverted, OUT1_3N normal.
	D0	Power-down	0: OUT1_3x driver active. 1: OUT1_3x driver powered down.

Registers for PLL1 Group 1B Outputs, OUT1_4x to OUT1_7x—Register 0x0115 to Register 0x0119

Table 60. PLL1 Group 1B Outputs Register Details

Address	Bits	Bit Name	Description
0x0115	[D7:D0]	D1B [7:0]	D1B divider Bit D7 (MSB) to Bit D0 (LSB). The divide factor is the value of D1B [7:0] + 1. D1B powers down when all four of the associated output drivers power down, whether via the power-down bit or via the logic mode bits.
0x0116	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT1_4x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_4P active, OUT1_4N active. 101: 1.8 V CMOS, OUT1_4P active, OUT1_4N disabled. 110: 1.8 V CMOS, OUT1_4P disabled, OUT1_4N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_4x polarity as follows (applies to CMOS only): 00: OUT1_4P normal, OUT1_4N inverted. 01: OUT1_4P normal, OUT1_4N normal. 10: OUT1_4P inverted, OUT1_4N inverted. 11: OUT1_4P inverted, OUT1_4N normal.
	D0	Power-down	0: OUT1_4x driver active. 1: OUT1_4x driver powered down.

Address	Bits	Bit Name	Description
0x0117	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure OUT1_5x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_5P active, OUT1_5N active. 101: 1.8 V CMOS, OUT1_5P active, OUT1_5N disabled. 110: 1.8 V CMOS, OUT1_5P disabled, OUT1_5N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_5x polarity as follows (applies to CMOS only): 00: OUT1_5P normal, OUT1_5N inverted. 01: OUT1_5P normal, OUT1_5N normal. 10: OUT1_5P inverted, OUT1_5N inverted. 11: OUT1_5P inverted, OUT1_5N normal.
	D0	Power-down	0: OUT1_5x driver active. 1: OUT1_5x driver powered down.
0x0118	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure OUT1_6 output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_6P active, OUT1_6N active. 101: 1.8 V CMOS, OUT1_6P active, OUT1_6N disabled. 110: 1.8 V CMOS, OUT1_6P disabled, OUT1_6N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_6x polarity as follows (applies to CMOS only): 00: OUT1_6P normal, OUT1_6N inverted. 01: OUT1_6P normal, OUT1_6N normal. 10: OUT1_6P inverted, OUT1_6N inverted. 11: OUT1_6P inverted, OUT1_6N normal.
	D0	Power-down	0: OUT1_6x driver active. 1: OUT1_6x driver powered down.
0x0119	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT1_7x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_7P active, OUT1_7N active. 101: 1.8 V CMOS, OUT1_7P active, OUT1_7N disabled. 110: 1.8 V CMOS, OUT1_7P disabled, OUT1_7N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_7x polarity as follows (applies to CMOS only): 00: OUT1_7P normal, OUT1_7N inverted. 01: OUT1_7P normal, OUT1_7N normal. 10: OUT1_7P inverted, OUT1_7N inverted. 11: OUT1_7P inverted, OUT1_7N normal.
	D0	Power-down	0: OUT1_7x driver active. 1: OUT1_7x driver powered down.

Registers for PLL1 Group 1C Outputs, OUT1_8x to OUT1_9x—Register 0x011A to Register 0x011C

Table 61. PLL1 Group 1C Outputs

Address	Bits	Bit Name	Description
0x011A	[D7:D0]	D1C [7:0]	D1C divider Bit D7 (MSB) to Bit D0 (LSB). The divide factor is the value of D1C [7:0] + 1. D1C powers down when all four of the associated output drivers power down, whether via the power-down bit or via the logic mode bits.
0x011B	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure OUT1_8x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_8P active, OUT1_8N active. 101: 1.8 V CMOS, OUT1_8P active, OUT1_8N disabled. 110: 1.8 V CMOS, OUT1_8P disabled, OUT1_8N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_8 polarity (applies to CMOS, only) as follows: 00: OUT1_8P normal, OUT1_8N inverted. 01: OUT1_8P normal, OUT1_8N normal. 10: OUT1_8P inverted, OUT1_8N inverted. 11: OUT1_8P inverted, OUT1_8N normal.
	D0	Power-down	0: OUT1_8x driver active. 1: OUT1_8x driver powered down.
0x011C	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT1_9x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT1_9P active, OUT1_9N active. 101: 1.8 V CMOS, OUT1_9P active, OUT1_9N disabled. 110: 1.8 V CMOS, OUT1_9P disabled, OUT1_9N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT1_9x polarity as follows (applies to CMOS only): 00: OUT1_9P normal, OUT1_9N inverted. 01: OUT1_9P normal, OUT1_9N normal. 10: OUT1_9P inverted, OUT1_9N inverted. 11: OUT1_9P inverted, OUT1_9N normal.
	D0	Power-down	0: OUT1_9x driver active. 1: OUT1_9x driver powered down.

PLL2 REGISTERS

PLL2 General Registers—Register 0x0200 Register 0x0201

Table 62. PLL2 General Register Details

Address	Bits	Bit Name	Description
0x0200	[D7:D6]	Unused	Unused.
	D5	Reserved	Reserved.
	D4	XTAL amplifier	0: configures REF_2P/REF_2N as a differential clock input pair. 1: configures REF_2P/REF_2N as a crystal resonator input. REF_2P/REF_2N is the amplifier input/output, respectively.
	D3	Reserved	Reserved.
	D2	Manual sync	Write Logic 1 to arm the distribution synchronization circuit, then write Logic 0 to cause the distribution channel dividers to synchronize (synchronization occurs on the falling edge of this bit).
	D1	Manual calibrate	Logic 1 causes the VCO calibration sequence to execute for PLL2. For robustness, write to this bit as three operations: Logic 0, Logic 1, then Logic 0.
	D0	Power-down	Logic 1 causes a full power-down of PLL2.
0x0201	[D7:D4]	Unused	Unused.
	D3	Manual charge pump current	0: automatic charge pump current control (recommended). 1: enable manual charge pump current control via Register 0x0201, Bits[D2:D0].
	[D2:D0]	Charge pump current [2:0]	Charge pump current control bits. These bits are ineffective when Register 0x0201, Bit D3 = 0. 000: 125 µA. 001: 250 µA. 010: 375 µA. 011: 500 µA. 100: 625 µA. 101: 750 µA. 110: 875 µA. 111: 1000 µA.

PLL2 Frequency Translation Registers—Register 0x0202 to Register 0x0204

Table 63. PLL2 Frequency Translation Register Details

Address	Bits	Bit Name	Description
0x0202	[D7:D4]	Unused	Unused.
	[D3:D0]	R2 [3:0]	R2 divider Bit D3 (MSB) to Bit D0. The value of R2 [3:0] results in the following behavior: 0: divides the input frequency by 16. 1 to 15: divides the input frequency by this value.
0x0203	[D7:D0]	N2 [7:0]	N2 Bit D7 (MSB) to Bit D0 (LSB). The value of N2 [7:0] results in the following behavior: 0 to 19: not applicable. 20 to 255: divides by this value.
0x0204	[D7:D4]	Unused	Unused.
	[D3:D0]	M2 [3:0]	M2 Bit D3 (MSB) to Bit D0. The value of the M2 [3:0] bits results in the following behavior: 0 to 2: disabled. 3 to 11: divides by this value. 12 to 14: disable. 15: M2 divider reset state. If the user intends to change the M2 divider without performing a subsequent PLL2 VCO calibration, then program this value (followed by an input/output update) before programming the a new M2 divider value (followed by an input/output update). An input/output update is writing Register 0x0005, Bit D0 = 1. The procedure given here is unnecessary if the user performs a PLL2 VCO calibration after changing the value of M2.

Registers for PLL2 Group 2A Outputs, OUT2_0x to OUT2_1x—Register 0x0205 to Register 0x0207

Table 64. PLL2 Group 2A Outputs Register Details

Address	Bits	Bit Name	Description
0x0205	[D7:D0]	D2A [7:0]	D2A divider Bit D7 (MSB) to Bit D0 (LSB). The divide factor is the value of D2A [7:0] + 1. D2A powers down when all four of the associated output drivers power down, whether via the power-down bit or via the logic mode bits.
0x0206	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_0x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_0P active, OUT2_0N active. 101: 1.8 V CMOS, OUT2_0P active, OUT2_0N disabled. 110: 1.8 V CMOS, OUT2_0P disabled, OUT2_0N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_0x polarity as follows (applies to CMOS only): 00: OUT2_0P normal, OUT2_0N inverted. 01: OUT2_0P normal, OUT2_0N normal. 01: OUT2_0P normal, OUT2_0N normal. 11: OUT2_0P inverted, OUT2_0N normal.
	0	Power-down	0: OUT2_0x driver active. 1: OUT2_0x driver powered down.
0x0207	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_1x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_1P active, OUT2_1N active. 101: 1.8 V CMOS, OUT2_1P active, OUT2_1N disabled. 110: 1.8 V CMOS, OUT2_1P disabled, OUT2_1N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_1x polarity as follows (applies to CMOS only): 00: OUT2_1P normal, OUT2_1N inverted. 01: OUT2_1P normal, OUT2_1N normal. 10: OUT2_1P inverted, OUT2_1N inverted. 11: OUT2_1P inverted, OUT2_1N normal.
	D0	Power-down	0: OUT2_1x driver active. 1: OUT2_1x driver powered down.

Registers for PLL2 Group 2B Outputs, OUT2_2x to OUT2_4x—Register 0x0208 to Register 0x020B

Table 65. PLL2 Group 2B Outputs Register Details

Address	Bits	Bit Name	Description
0x0208	[D7:D0]	D2B [7:0]	D2B divider Bit D7 (MSB) to Bit D0 (LSB). The divide factor is the value of D2B [7:0] + 1. D2B powers down when all four of the associated output drivers power down whether via the power-down bit or via the logic mode bits.
0x0209	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure OUT2_2x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_2P active, OUT2_2N active. 101: 1.8 V CMOS, OUT2_2P active, OUT2_2N disabled. 110: 1.8 V CMOS, OUT2_2P disabled, OUT2_2N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_2x polarity as follows (applies to CMOS only): 00: OUT2_2P normal, OUT2_2N inverted. 01: OUT2_2P normal, OUT2_2N normal. 10: OUT2_2P inverted, OUT2_2N inverted. 11: OUT2_2P inverted, OUT2_2N normal.
	D0	Power-down	0: OUT2_2x driver active. 1: OUT2_2x driver powered down.
0x020A	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_3x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_3P active, OUT2_3N active. 101: 1.8 V CMOS, OUT2_3P active, OUT2_3N disabled. 110: 1.8 V CMOS, OUT2_3P disabled, OUT2_3N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_3x polarity as follows (applies to CMOS only): 00: OUT2_3P normal, OUT2_3N inverted. 01: OUT2_3P normal, OUT2_3N normal. 10: OUT2_3P inverted, OUT2_3N inverted. 11: OUT2_3P inverted, OUT2_3N normal.
	D0	Power-down	0: OUT2_3x driver active. 1: OUT2_3x driver powered down.
0x020B	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_4x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_4P active, OUT2_4N active. 101: 1.8 V CMOS, OUT2_4P active, OUT2_4N disabled. 110: 1.8 V CMOS, OUT2_4P disabled, OUT2_4N active. 111: undefined.

Address	Bits	Bit Name	Description
	[D2:D1]	Polarity [1:0]	Configure OUT2_4x polarity as follows (applies to CMOS only): 00: OUT2_4P normal, OUT2_4N inverted. 01: OUT2_4P normal, OUT2_4N normal. 10: OUT2_4P inverted, OUT2_4N inverted. 11: OUT2_4P inverted, OUT2_4N normal.
	D0	Power-down	0: OUT2_4x driver active. 1: OUT2_4x driver powered down.

Registers for PLL2 Group 2C Outputs, OUT2_5x to OUT2_7x—Register 0x020C to Register 0x020F

Table 66. PLL2 Group 2C Outputs Register Details

Address	Bits	Bit Name	Description
0x020C	[D7:D0]	D2C [7:0]	D2C divider Bit D7 (MSB) to Bit D0 (LSB). The divide factor is the value of D2C [7:0] + 1. D2C powers down when all four of the associated output drivers power down, whether via the power-down bit or via the logic mode bits.
0x020D	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_5x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_5P active, OUT2_5N active. 101: 1.8 V CMOS, OUT2_5P active, OUT2_5N disabled. 110: 1.8 V CMOS, OUT2_5P disabled, OUT2_5N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_5x polarity as follows (applies to CMOS only): 00: OUT2_5P normal, OUT2_5N inverted. 01: OUT2_5P normal, OUT2_5N normal. 10: OUT2_5P inverted, OUT2_5N inverted. 11: OUT2_5P inverted, OUT2_5N normal.
	D0	Power-down	0: OUT2_5x driver active. 1: OUT2_5x driver powered down.
0x020E	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_6x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_6P active, OUT2_6N active. 101: 1.8 V CMOS, OUT2_6P active, OUT2_6N disabled. 110: 1.8 V CMOS, OUT2_6P disabled, OUT2_6N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_6x polarity as follows (applies to CMOS only): 00: OUT2_6P normal, OUT2_6N inverted. 01: OUT2_6P normal, OUT2_6N normal. 10: OUT2_6P inverted, OUT2_6N inverted. 11: OUT2_6P inverted, OUT2_6N normal.
	D0	Power-down	0: OUT2_6x driver active. 1: OUT2_6x driver powered down.

Address	Bits	Bit Name	Description
0x020F	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_7x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_7P active, OUT2_7N active. 101: 1.8 V CMOS, OUT2_7P active, OUT2_7N disabled. 110: 1.8 V CMOS, OUT2_7P disabled, OUT2_7N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_7x polarity as follows (applies to CMOS only): 00: OUT2_7P normal, OUT2_7N inverted. 01: OUT2_7P normal, OUT2_7N normal. 10: OUT2_7P inverted, OUT2_7N inverted. 11: OUT2_7P inverted, OUT2_7N normal.
	D0	Power-down	0: OUT2_7x driver active. 1: OUT2_7x driver powered down.

Registers for PLL2 Group 2D Outputs, OUT2_8x to OUT2_11x—Register 0x0210 to Register 0x0214

Table 67. PLL2 Group 2D Outputs Register Details

Address	Bits	Bit Name	Description
0x0210	[D7:D0]	D2D [7:0]	D2D divider Bit D7 (MSB) to Bit D0 (LSB). The divide factor is the value of D2D [7:0] + 1. D2D powers down when all four of the associated output drivers power down, whether via the power-down bit or via the logic mode bits.
0x0211	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_8x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_8P active, OUT2_8N active. 101: 1.8 V CMOS, OUT2_8P active, OUT2_8N disabled. 110: 1.8 V CMOS, OUT2_8P disabled, OUT2_8N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_8x polarity as follows (applies to CMOS only): 00: OUT2_8P normal, OUT2_8N inverted. 01: OUT2_8P normal, OUT2_8N normal. 10: OUT2_8P inverted, OUT2_8N inverted. 11: OUT2_8P inverted, OUT2_8N normal.
	D0	Power-down	0: OUT2_8x driver active. 1: OUT2_8x driver powered down.
0x0212	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure OUT2_9 output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_9P active, OUT2_9N active. 101: 1.8 V CMOS, OUT2_9P active, OUT2_9N disabled. 110: 1.8 V CMOS, OUT2_9P disabled, OUT2_9N active. 111: undefined.

Address	Bits	Bit Name	Description
	[D2:D1]	Polarity [1:0]	Configure OUT2_9x polarity as follows (applies to CMOS only): 00: OUT2_9P normal, OUT2_9N inverted. 01: OUT2_9P normal, OUT2_9N normal. 10: OUT2_9P inverted, OUT2_9N inverted. 11: OUT2_9P inverted, OUT2_9N normal.
	D0	Power-down	0: OUT2_9x driver active. 1: OUT2_9x driver powered down.
0x0213	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_10x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_10P active, OUT2_10N active. 101: 1.8 V CMOS, OUT2_10P active, OUT2_10N disable. 110: 1.8 V CMOS, OUT2_10P disable, OUT2_10N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_10x polarity as follows (applies to CMOS only): 00: OUT2_10P normal, OUT2_10N inverted. 01: OUT2_10P normal, OUT2_10N normal. 10: OUT2_10P inverted, OUT2_10N inverted. 11: OUT2_10P inverted, OUT2_10N normal.
	D0	Power-down	0: OUT2_10x driver active. 1: OUT2_10x driver powered down.
0x0214	[D7:D6]	Unused	Unused.
	[D5:D3]	Logic mode [2:0]	Configure the OUT2_11x output driver as follows: 000: disabled. 001: HSTL. 010: undefined. 011: undefined. 100: 1.8 V CMOS, OUT2_11P active, OUT2_11N active. 101: 1.8 V CMOS, OUT2_11P active, OUT2_11N disabled. 110: 1.8 V CMOS, OUT2_11P disabled, OUT2_11N active. 111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT2_11x polarity as follows (applies to CMOS only): 00: OUT2_11P normal, OUT2_11N inverted. 01: OUT2_11P normal, OUT2_11N normal. 10: OUT2_11P inverted, OUT2_11N inverted. 11: OUT2_11P inverted, OUT2_11N normal.
	D0	Power-down	0: OUT2_11x driver active. 1: OUT2_11x driver powered down.

PLL3 REGISTERS

PLL3 General Register—Register 0x0300

Table 68. PLL3 General Register Details

Address	Bits	Bit Name	Description
0x0300	[D7:D6]	Unused	Unused.
	D5	Reserved	Reserved.
	D4	XTAL amplifier	0: configures REF_3P/REF_3N as a differential clock input pair. 1: configures REF_3P/REF_3N as a crystal resonator input. REF_3P/REF_3N is amplifier input/output, respectively.
	D3	Reserved	Reserved.
	D2	Manual sync	Write Logic 1 to arm the distribution synchronization circuit, then write Logic 0 to cause the distribution channel dividers to synchronize (synchronization occurs on the falling edge of this bit).
	D1	Reserved	Reserved.
	D0	Power-down	Logic 1 causes a full power-down of PLL3.

PLL3 Frequency Translation Registers—Register 0x0301 to Register 0x0304

Table 69. PLL3 Frequency Translation Register Details

Address	Bits	Bit Name	Description
0x0301	[D7:D6]	Unused	Unused.
	D5	×2B	Logic 1 enables the ×2 VCO frequency multiplier of PLL3B.
	D4	×2A	Logic 1 enables the ×2 VCO frequency multiplier of PLL3A.
	[D3:D0]	Reference scaling [3:0]	Reference scaling, Bit D3 (MSB) to Bit D0 (LSB). The value of the reference scaling bits results in the following behavior: 0: disables reference input section. 1: passes the input frequency unaltered (bypasses R3A). 2: divides the input frequency by 1.5. 3: divides the input frequency by 2. 4: divides the input frequency by 3. 5: divides the input frequency by 4. 6: divides the input frequency by 6. 7: divides the input frequency by 8. 8 to 15: multiplies the input frequency by a factor of 2.
0x0302	[D7:D0]	N3A [7:0]	N3A Bit D7 (MSB) to Bit D0 (LSB). The value of N3A [7:0] results in the following behavior (avoid values not included in the following ranges): 0: bypasses PLL3A. 8 to 80: divides by this value when ×2A = 0. 15 to 161: divides by this value when ×2A = 1.
0x0303	[D7:D0]	R3B [7:0]	R3B Bit D7 (MSB) to Bit D0 (LSB). The value of R3B [7:0] results in the following behavior (avoid values not included in the following ranges): 0: bypasses R3B divider. 2 to 10: divides by this value when N3 = 0. 8 to 80: divides by this value when N3 ≠ 0.
0x0304	[D7:D0]	N3B [7:0]	N3B Bit D7 (MSB) to Bit D0 (LSB). The value of N3B [7:0] results in the following behavior (avoid values not included in the following ranges): 0: bypasses PLL3B. 8 to 80: divides by this value when ×2B = 0. 15 to 161: divides by this value when ×2B = 1.

PLL3 OUT3_0 Registers—Register 0x0305 to Register 0x0306

Table 70. PLL3 OUT3_0 Register Details

Address	Bits	Bit Name	Description
0x0305	[D7:D4]	Reserved	Reserved.
	[D3:D0]	D3A [3:0]	D3A divider, Bit D3 (MSB) to Bit D0 (LSB). The actual channel divide value is twice the value indicated in this table, due to the fixed divide by 2 that follows D3A. D3A powers down when the OUT3_0 driver powers down. The value of D3A [3:0] results in the following behavior: 0: divides by 16. 1 to 15: divides by this value.
0x0306	[D7:D4]	Unused	Unused.
	D3	3.3 V mode	This bit is only effective when Register 0x0085, Bits[D4:D0] = 00000. 0: 1.8 V CMOS output driver. 1: 3.3 V CMOS output driver.
	D2	Reserved	Reserved.
	D1	Invert	0: OUT3_0 normal logic output. 1: OUT3_0 inverted logic output.
	D0	Power-down	This bit is only effective when Register 0x0085, Bits[D4:D0] = 00000. 0: OUT3_0 driver active. 1: OUT3_0 driver powered down.

PLL3 OUT3_1x Registers—Register 0x0307 to Register 0x0308

Table 71. PLL OUT3_1 Register Details

Address	Bits	Bit Name	Description
0x0307	[D7:D4]	Reserved	Reserved.
	[D3:D0]	D3B [3:0]	D3B divider Bit D3 (MSB) to Bit D0 (LSB). The actual channel divide value is twice the value indicated in this table, due to the fixed divide by 2 that follows D3B. D3B powers down when the OUT3_1x driver powers down. The value of D3B [3:0] results in the following behavior: 0: divides by 16. 1 to 15: divides by this value.
0x0308	D7	Unused	Unused.
	[D6:D3]	Logic mode [3:0]	Configure OUT3_1 output driver as follows: 0000: disabled. 0001: HSTL. 0010: LVDS. 0011: undefined. 0100: 1.8 V CMOS, OUT3_1P active, OUT3_1N active. 0101: 1.8 V CMOS, OUT3_1P active, OUT3_1N disabled. 0110: 1.8 V CMOS, OUT3_1P disabled, OUT3_1N active. 0111 to 1011: undefined. 1100: 3.3 V CMOS, OUT3_1P active, OUT3_1N active. 1101: 3.3 V CMOS, OUT3_1P active, OUT3_1N disabled. 1110: 3.3 V CMOS, OUT3_1P disabled, OUT3_1N active. 1111: undefined.
	[D2:D1]	Polarity [1:0]	Configure OUT3_1 polarity as follows (applies to CMOS only): 00: OUT3_1P normal, OUT3_1N inverted. 01: OUT3_1P normal, OUT3_1N normal. 10: OUT3_1P inverted, OUT3_1N inverted. 11: OUT3_1P inverted, OUT3_1N normal.
	D0	Power-down	0: OUT3_1x driver active. 1: OUT3_1x driver powered down.

ROM PROFILE DATA

The tables in this section contain the ROM contents organized in columns by the ROM profile number (as defined by the value contained in Register 0x000E, Bits[D5:D0]). The leftmost column of the table contains the register address.

The ROM profile contents appear as 8-bit hexadecimal values. Avoid loading reserved ROM profiles. Reserved profiles are noted in Table 72, Table 73, Table 74, and Table 75.

ROM PROFILE 0 TO ROM PROFILE 15

Table 72. ROM Contents for ROM Profile 0 to ROM Profile 15

	ROM Profile Number						
Register Address	**0**	**1**	**2**	**3**	**4**	**5**	**6 … 15**
Status Controls							
0x0083	0x0A	0x2A	0x00	0x00	0x00	0x00	These profiles are all reserved
0x0084	0x41	0x41	0x01	0x01	0x01	0x01	
0x0085	0x42	0x42	0x02	0x02	0x02	0x02	
PLL1							
0x0100	0x02	0x00	0x02	0x00	0x02	0x00	These profiles are all reserved
0x0101	0x00	0x0D	0x00	0x0D	0x00	0x0D	
0x0102	0x08	0x00	0x08	0x00	0x08	0x00	
0x0103	0x00	0x22	0x00	0x22	0x00	0x22	
0x0104	0x01	0x7D	0x01	0x7D	0x01	0x7D	
0x0105	0x00	0x00	0x00	0x00	0x00	0x00	
0x0106	0x1E	0x00	0x1E	0x00	0x1E	0x00	
0x0107	0x00	0x00	0x00	0x00	0x00	0x00	
0x0108	0x00	0x00	0x00	0x00	0x00	0x00	
0x0109	0x00	0x00	0x00	0x00	0x00	0x00	
0x010A	0x00	0x00	0x00	0x00	0x00	0x00	
0x010B	0x00	0x00	0x00	0x00	0x00	0x00	
0x010C	0x00	0x00	0x00	0x00	0x00	0x00	
0x010D	0x00	0x00	0x00	0x08	0x00	0x00	
0x010E	0x00	0x06	0x00	0x07	0x00	0x06	
0x010F	0x03	0x00	0x03	0x00	0x03	0x00	
0x0110	0x09	0x00	0x07	0x00	0x09	0x00	
0x0111	0x08	0x08	0x08	0x08	0x08	0x08	
0x0112	0x08	0x08	0x08	0x08	0x08	0x08	
0x0113	0x08	0x08	0x08	0x08	0x08	0x08	
0x0114	0x08	0x08	0x08	0x08	0x08	0x08	
0x0115	0x09	0x00	0x07	0x00	0x09	0x00	
0x0116	0x08	0x08	0x08	0x08	0x08	0x08	
0x0117	0x08	0x08	0x08	0x08	0x08	0x08	
0x0118	0x08	0x08	0x08	0x08	0x08	0x08	
0x0119	0x08	0x08	0x08	0x08	0x08	0x08	
0x011A	0x09	0x00	0x07	0x00	0x09	0x00	
0x011B	0x08	0x08	0x08	0x08	0x08	0x08	
0x011C	0x08	0x08	0x08	0x08	0x08	0x08	

	ROM Profile Number						
Register Address	**0**	**1**	**2**	**3**	**4**	**5**	**6 … 15**
PLL2							
0x0200	0x02	0x02	0x02	0x02	0x02	0x02	These profiles are all reserved
0x0201	0x00	0x00	0x00	0x00	0x00	0x00	
0x0202	0x01	0x01	0x01	0x01	0x01	0x01	
0x0203	0x032	0x032	0x032	0x032	0x032	0x032	
0x0204	0x04	0x04	0x04	0x04	0x04	0x04	
0x0205	0x04	0x03	0x03	0x03	0x04	0x03	
0x0206	0x08	0x08	0x08	0x08	0x08	0x08	
0x0207	0x08	0x08	0x08	0x08	0x08	0x08	
0x0208	0x03	0x04	0x03	0x03	0x03	0x04	
0x0209	0x08	0x08	0x08	0x08	0x08	0x08	
0x020A	0x08	0x08	0x08	0x08	0x08	0x08	
0x020B	0x08	0x08	0x08	0x08	0x08	0x08	
0x020C	0x04	0x04	0x03	0x03	0x04	0x04	
0x020D	0x08	0x08	0x08	0x08	0x08	0x08	
0x020E	0x08	0x08	0x08	0x08	0x08	0x08	
0x020F	0x08	0x08	0x08	0x08	0x08	0x08	
0x0210	0x04	0x04	0x03	0x03	0x04	0x04	
0x0211	0x08	0x08	0x08	0x08	0x08	0x08	
0x0212	0x08	0x08	0x08	0x08	0x08	0x08	
0x0213	0x08	0x08	0x08	0x08	0x08	0x08	
0x0214	0x08	0x08	0x08	0x08	0x08	0x08	
PLL3							
0x0300	0x01	0x00	0x01	0x00	0x01	0x00	These profiles are all reserved
0x0301	0x00	0x01	0x00	0x01	0x00	0x01	
0x0302	0x00	0x4B	0x00	0x4B	0x00	0x4B	
0x0303	0x00	0x00	0x00	0x00	0x00	0x00	
0x0304	0x00	0x00	0x00	0x00	0x00	0x00	
0x0305	0x00	0x00	0x00	0x00	0x00	0x00	
0x0306	0x00	0x01	0x00	0x01	0x00	0x01	
0x0307	0x00	0x0F	0x00	0x0F	0x00	0x0F	
0x0308	0x00	0x28	0x00	0x28	0x00	0x28	
0x0309	0x00	0x00	0x00	0x00	0x00	0x00	
0x030A	0x00	0x00	0x00	0x00	0x00	0x00	
0x030B	0x00	0x00	0x00	0x00	0x00	0x00	
0x030C	0x00	0x00	0x00	0x00	0x00	0x00	
0x030D	0x00	0x00	0x00	0x00	0x00	0x00	
0x030E	0x00	0x00	0x00	0x00	0x00	0x00	

ROM PROFILE 16 TO ROM PROFILE 31

Table 73. ROM Contents for ROM Profile 16 to ROM Profile 31

Register Address	**ROM Profile Number 16 … ROM Profile Number 31**
Status Controls	
0x0083	These profiles are all reserved
0x0084	
0x0085	

Register Address	ROM Profile Number 16 … ROM Profile Number 31
PLL1	
0x0100	These profiles are all reserved
0x0101	
0x0102	
0x0103	
0x0104	
0x0105	
0x0106	
0x0107	
0x0108	
0x0109	
0x010A	
0x010B	
0x010C	
0x010D	
0x010E	
0x010F	
0x0110	
0x0111	
0x0112	
0x0113	
0x0114	
0x0115	
0x0116	
0x0117	
0x0118	
0x0119	
0x011A	
0x011B	
0x011C	
PLL2	
0x0200	These profiles are all reserved
0x0201	
0x0202	
0x0203	
0x0204	
0x0205	
0x0206	
0x0207	
0x0208	
0x0209	
0x020A	
0x020B	
0x020C	
0x020D	
0x020E	
0x020F	
0x0210	
0x0211	
0x0212	
0x0213	
0x0214	

Register Address	ROM Profile Number 16 … ROM Profile Number 31
PLL3	
0x0300	These profiles are all reserved
0x0301	
0x0302	
0x0303	
0x0304	
0x0305	
0x0306	
0x0307	
0x0308	
0x0309	
0x030A	
0x030B	
0x030C	
0x030D	
0x030E	

ROM PROFILE 32 TO ROM PROFILE 47

Table 74. ROM Contents for ROM Profile 32 to ROM Profile 47

	ROM Profile Number 32 … ROM Profile Number 47															
Register Address	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
Status Controls																
0x0083	These profiles are all reserved															
0x0084																
0x0085																
PLL1																
0x0100	These profiles are all reserved															
0x0101																
0x0102																
0x0103																
0x0104																
0x0105																
0x0106																
0x0107																
0x0108																
0x0109																
0x010A																
0x010B																
0x010C																
0x010D																
0x010E																
0x010F																
0x0110																
0x0111																
0x0112																
0x0113																
0x0114																
0x0115																
0x0116																
0x0117																
0x0118																
0x0119																

Register Address	ROM Profile Number 32 … ROM Profile Number 47															
	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
0x011A																
0x011B																
0x011C																
PLL2																
0x0200	These profiles are all reserved															
0x0201																
0x0202																
0x0203																
0x0204																
0x0205																
0x0206																
0x0207																
0x0208																
0x0209																
0x020A																
0x020B																
0x020C																
0x020D																
0x020E																
0x020F																
0x0210																
0x0211																
0x0212																
0x0213																
0x0214																
PLL3																
0x0300	These profiles are all reserved															
0x0301																
0x0302																
0x0303																
0x0304																
0x0305																
0x0306																
0x0307																
0x0308																
0x0309																
0x030A																
0x030B																
0x030C																
0x030D																
0x030E																

ROM PROFILE 48 TO ROM PROFILE 63

Table 75. ROM Contents for ROM Profile 48 to ROM Profile 63

Register Address	ROM Profile Number 48 … ROM Profile Number 63
Status Controls	
0x0083	These profiles are all reserved
0x0084	
0x0085	
PLL1	
0x0100	These profiles are all reserved
0x0101	
0x0102	
0x0103	
0x0104	
0x0105	
0x0106	
0x0107	
0x0108	
0x0109	
0x010A	
0x010B	
0x010C	
0x010D	
0x010E	
0x010F	
0x0110	
0x0111	
0x0112	
0x0113	
0x0114	
0x0115	
0x0116	
0x0117	
0x0118	
0x0119	
0x011A	
0x011B	
0x011C	

Register Address	ROM Profile Number 48 … ROM Profile Number 63
PLL2	
0x0200	These profiles are all reserved
0x0201	
0x0202	
0x0203	
0x0204	
0x0205	
0x0206	
0x0207	
0x0208	
0x0209	
0x020A	
0x020B	
0x020C	
0x020D	
0x020E	
0x020F	
0x0210	
0x0211	
0x0212	
0x0213	
0x0214	
PLL3	
0x0300	These profiles are all reserved
0x0301	
0x0302	
0x0303	
0x0304	
0x0305	
0x0306	
0x0307	
0x0308	
0x0309	
0x030A	
0x030B	
0x030C	
0x030D	
0x030E	

THERMAL PERFORMANCE

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 76. Thermal Parameters for the AD9531 88-Lead LFCSP Package

Symbol	Thermal Characteristic Using a JEDEC51-7 Plus JEDEC51-5 2S2P Test Board[1]	Value[2]	Unit
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air)	18	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	16	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)	14	°C/W
θ_{JB}	Junction-to-board thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-8 (moving air)	9	°C/W
θ_{JC}	Junction-to-case thermal resistance (die to heat sink) per MIL-Std 883, Method 1012.1	1.0	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.1	°C/W

[1] The exposed pad on the bottom of the package must be soldered to ground to achieve the specified thermal performance.
[2] Results are from simulations. The printed circuit board (PCB) is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

The AD9531 is specified for a case temperature (T_{CASE}). To prevent exceeding T_{CASE}, use an airflow source. Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is the value as indicated in Table 76.
PD is the power dissipation (see Table 3).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

APPLICATIONS INFORMATION

INTERFACING TO THE MULTIFUNCTION PINS

Figure 38 and Figure 39 demonstrate using the Mx pins with a 1.8 V CMOS logic. For proper operation during a POR event, the internal buffer requires a nominal 10 kΩ resistor to pull-up to 1.8 V (Logic 1) or pull-down to ground (Logic 0). After a POR event (with S1 in the NORM position), the internal CMOS driver forces the appropriate 1.8 V logic levels across the 10 kΩ pull-up or pull-down resistor.

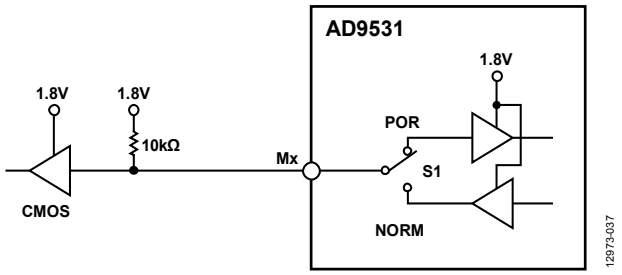


Figure 38. Using an Mx Pin with a 1.8 V CMOS Logic, Pull-Up Connection

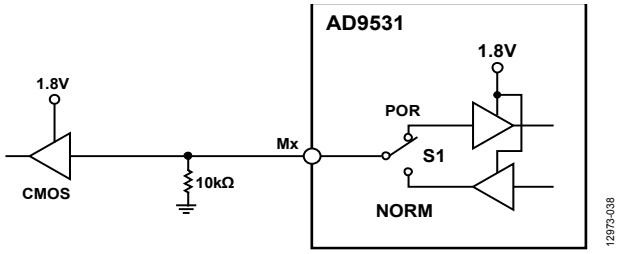


Figure 39. Using an Mx Pin with a 1.8 V CMOS Logic, Pull-Down Connection

Figure 40 and Figure 41 demonstrate using the Mx pins with a 3.3 V CMOS logic. For proper operation during a POR event, the internal buffer requires a nominal 10 kΩ resistor to pull-up to 1.8 V (Logic 1) or pull-down to ground (Logic 0). After a POR event (normal operation), the internal CMOS driver forces the appropriate 3.3 V logic levels across the 10 kΩ pull-up or pull-down resistor. Note that interfacing to 3.3 V CMOS requires programming the 3.3 V mode bit to Logic 1 for the associated pin function (LDETx or LOR).

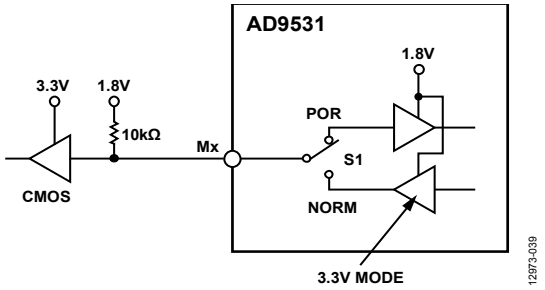


Figure 40. Using an Mx Pin with a 3.3 V Logic, Pull-Up Configuration

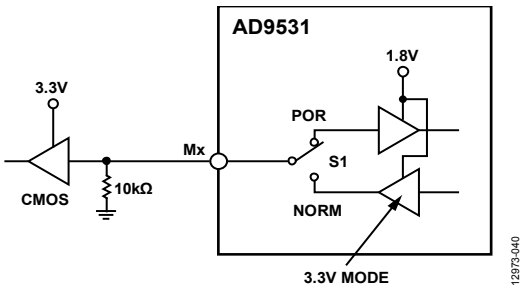


Figure 41. Using an Mx Pin with a 3.3 V Logic, Pull-Down Configuration

Figure 42 and Figure 43 demonstrate using the Mx pins with a 1.5 V CMOS logic in a pull-down configuration. A resistive voltage divider is necessary to properly translate a Logic 1 produced by the internal driver during normal operation from 1.8 V to 1.5 V. Therefore, the ratio of the resistors is 5:1. Note the external resistors have no impact on a Logic 1 produced by the internal driver.

The primary design constraint is the load current (I_L) that the driver must supply for a condition of Logic 1. Assuming the input of the external CMOS gate exhibits high impedance, then all the load current flows through the 5R resistor, which must drop 1.5 V. This implies $5R = 1.5\ V/I_L$ or $R = 0.3\ V/I_L$. Therefore, choose a reasonable load current, such as 1 mA, for example. This load current yields R = 300 Ω and 5R = 1.5 kΩ.

During a POR event, the pull-down configuration provides the internal buffer with a 1.8 kΩ termination to ground, which the internal buffer interprets as Logic 0. Alternately, during normal operation, the internal 1.8 V driver delivers a 1.5 V Logic 1 to the external CMOS gate with 1 mA of load current.

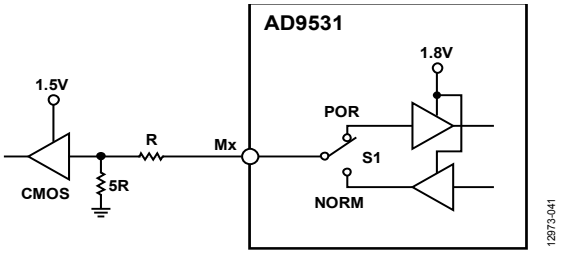


Figure 42. Using an Mx Pin with 1.5 V Logic, Pull-Down Configuration During a POR Event

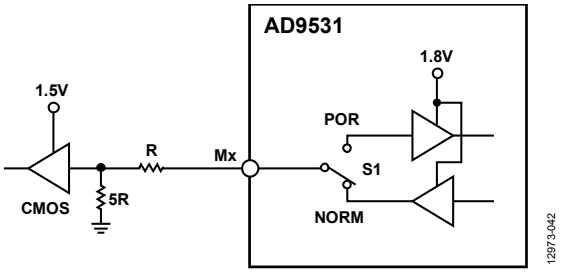


Figure 43. Using an Mx Pin with 1.5 V Logic, Pull-Down Configuration During Normal Operation

Figure 44 and Figure 45 demonstrate using the Mx pins with a 1.5 V CMOS logic in a pull-up configuration. A three resistor arrangement is necessary to satisfy two design criteria as follows:

- Translate a 1.8 V Logic 1, produced by the internal driver, to 1.5 V for the external CMOS gate during normal operation.
- Provide the desired Logic 1 pull-up to the internal buffer during a POR event.

The primary design constraint on the pull-up resistor (R_U) is the Logic 0 load current (I_L) it imposes on the internal driver during normal operation. Assuming the external CMOS gate exhibits high impedance, then $R_U = 1.8\ V/I_L$. Therefore, choose a reasonable load current, such as 1 mA, for example. This yields $R_U = 1.8\ k\Omega$.

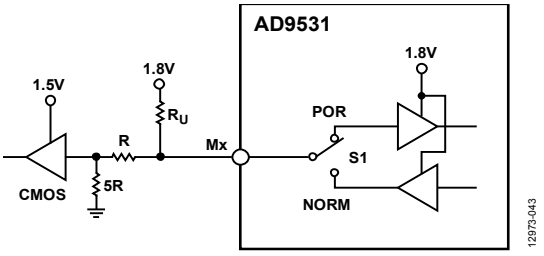


Figure 44. Using an Mx Pin with a 1.5 V Logic, Pull-Up Configuration During a POR Event

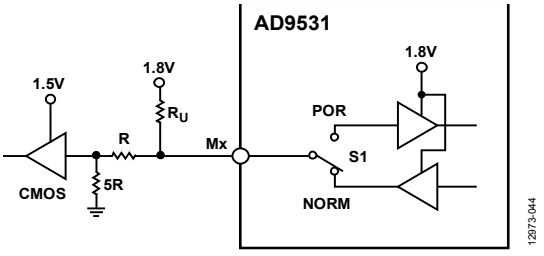


Figure 45. Using an Mx Pin with a 1.5 V Logic, Pull-Up Configuration During Normal Operation

In the pull-down case, the series and pull-down resistors must exhibit a 5:1 ratio to provide the desired 1.8 V to 1.5 V Logic 1 translation between the internal driver and the external CMOS gate during normal operation. Therefore, the respective R and 5R label for the series and pull-down resistors.

The design goal is to have at least 1.2 V (that is, 2/3 of 1.8 V) on the Mx pin during a POR event to constitute the desired Logic 1. R_U, R, and 5R form a voltage divider. This divider sets up the following necessary design constraint:

$$1.8\ V \times \frac{R + 5R}{R_U + R + 5R} > 1.2\ V$$

Because $R_U = 1.8\ V/I_L$, the above constraint simplifies to $R > 0.6/I_L$ and having chosen $I_L = 1$ mA, the result is $R > 600\ \Omega$. Therefore, choose a convenient value such as $R = 1\ k\Omega$. This implies that $5R = 5\ k\Omega$.

INTERFACING TO THE RFIN1_x PINS

Figure 46 is the recommended method for interfacing an external VCXO with a 3.3 V CMOS single-ended output to the RFIN1_x pins. Even though the VCXO has a single-ended output, it is best to configure the RFIN1_x input for differential input mode to minimize duty cycle distortion. This circuit works well as long as the stray PCB capacitance (C_S) is less than 10 pF and the VCXO frequency is in the range of 120 MHz.

The 0.1 µF capacitor on the RFIN1_N input provides a suitable ac ground reference for the two 5 pF capacitors, which serve as a voltage divider for the rising and falling signal edges delivered by the VCXO output. Typically, the CMOS drivers of most VCXOs tend to have low output drive capability to minimize output switching noise and EMI. Therefore, choose small divider capacitor values to avoid excessive loading of the CMOS output driver of the VCXO.

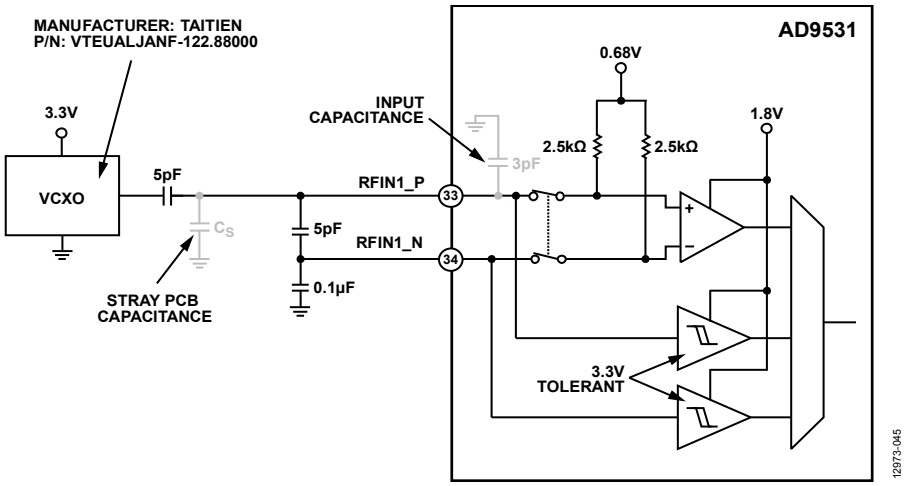


Figure 46. Connecting an External 3.3 V CMOS VCXO Single-Ended Output to the RFIN1_x Pins

DRIVING REF2 OR REF3 WITH 3.3 V CMOS LOGIC

For applications with a 3.3 V CMOS driver as the reference source, a single-ended to differential conversion is necessary, as shown in Figure 47.

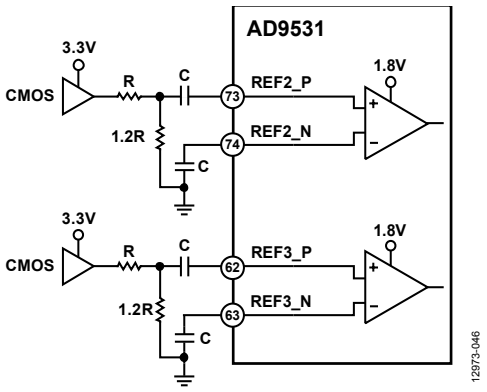


Figure 47. Interfacing the REF2 or REF3 Inputs to 3.3 V CMOS

Choose the value of R and C in Figure 47 based on the input frequency, f_{REF}. Typically, choose R to limit the current load on the CMOS driver as given by $R = 1.5/I_{LOAD}$. Then, choose C based on the input frequency such that $C > 10/(R \times f_{REF})$. The remaining shunt resistor is 1.2× the value of R and provides the necessary voltage scaling from 3.3 V to 1.8 V.

For example, I_{LOAD} = 1 mA and f_{REF} = 25 MHz results in R = 1.5 kΩ (R_{SHUNT} = 1.8 kΩ) and C > 270 pF.

USING REF2 OR REF3 WITH A CRYSTAL RESONATOR

For applications using a crystal resonator as the reference input, the XTAL amplifier bit in the appropriate programming register must be set to Logic 1. Register 0x0200, Bit D4 applies to PLL2 and Register 0x0300, Bit D4 applies to PLL3.

Figure 48 shows a typical crystal connection for both the PLL2 and PLL3 reference inputs. The internal input circuitry converts to an amplifier configuration to promote oscillation of the crystal resonator. The value of the shunt capacitors (C) connected to the crystal depends on the crystal manufacturer load capacitance (C_{LOAD}) specification for parallel resonance, as follows:

$$C = 2 \times C_{LOAD}$$

For example, a C_{LOAD} specification of 10 pF means that the value of each of the two capacitors connected to the crystal is 20 pF.

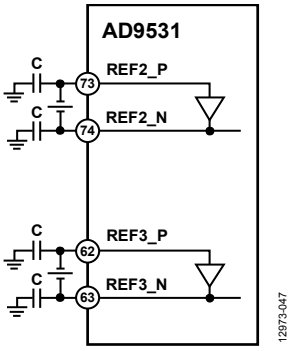


Figure 48. Interfacing the REF2 or REF3 Inputs to a Crystal Resonator

OUTLINE DIMENSIONS

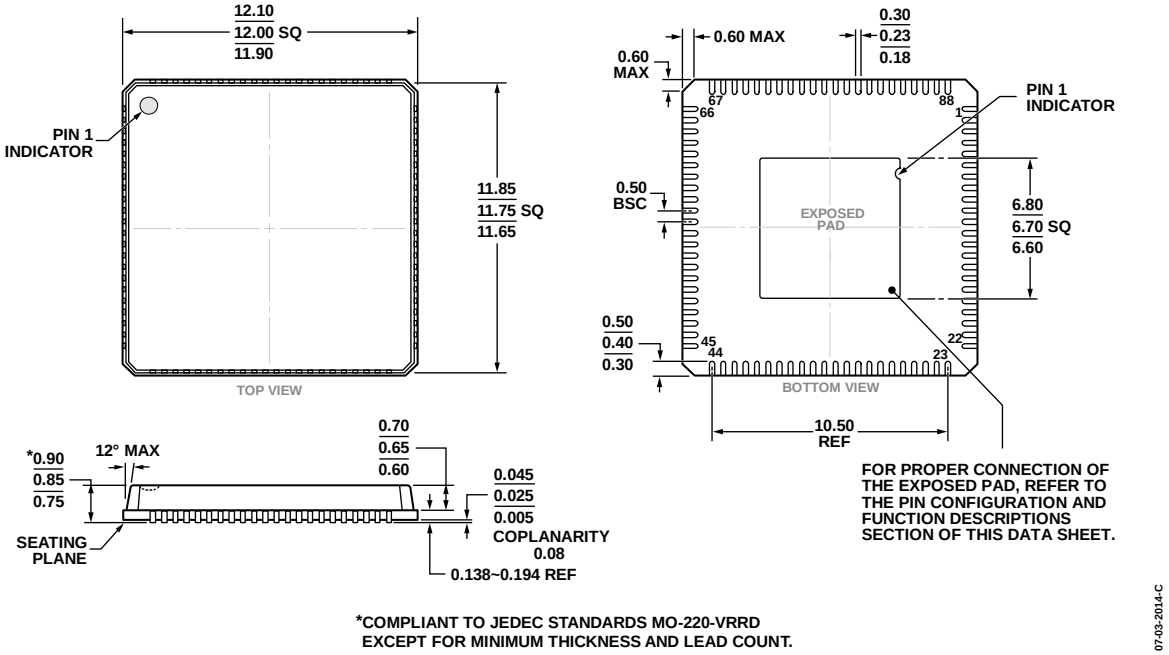


Figure 49. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
12 mm × 12 mm Body, Very Thin Quad
(CP-88-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9531BCPZ	−40°C to +85°C	88-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-88-5
AD9531BCPZ-REEL7	−40°C to +85°C	88-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-88-5
AD9531/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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