Jitter Cleaner and Clock Generator with 14 Differential or 29 LVCMOS Outputs

Data Sheet **AD9523**

FEATURES

- Output frequency: <1 MHz to 1 GHz
- Start-up frequency accuracy: <±100 ppm (determined by VCXO reference accuracy)
- Zero delay operation
  - Input-to-output edge timing: <150 ps
- 14 outputs: configurable LVPECL, LVDS, HSTL, and LVCMOS
- 14 dedicated output dividers with jitter-free adjustable delay
- Adjustable delay: 63 resolution steps of ½ period of VCO output divider
- Output-to-output skew: <50 ps
- Duty cycle correction for odd divider settings
- Automatic synchronization of all outputs on power-up
- Absolute output jitter: <200 fs at 122.88 MHz
  - Integration range: 12 kHz to 20 MHz
- Distribution phase noise floor: −160 dBc/Hz
- Digital lock detect
- Nonvolatile EEPROM stores configuration settings
- SPI- and I^2C-compatible serial control port
- Dual PLL architecture
  - PLL1
    - Low bandwidth for reference input clock cleanup with external VCXO
    - Phase detector rate up to130 MHz
    - Redundant reference inputs
    - Automatic and manual reference switchover modes
      - Revertive and nonrevertive switching
    - Loss of reference detection with holdover mode
    - Low noise LVCMOS output from VCXO used for RF/IF synthesizers
  - PLL2
    - Phase detector rate up to 259 MHz
    - Integrated low noise VCO

APPLICATIONS

- LTE and multicarrier GSM base stations
- Wireless and broadband infrastructure
- Medical instrumentation
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- Low jitter, low phase noise clock distribution
- Clock generation and translation for SONET, 10Ge, 10G FC, and other 10 Gbps protocols
- Forward error correction (G.710)
- High performance wireless transceivers
- ATE and high performance instrumentation

FUNCTIONAL BLOCK DIAGRAM

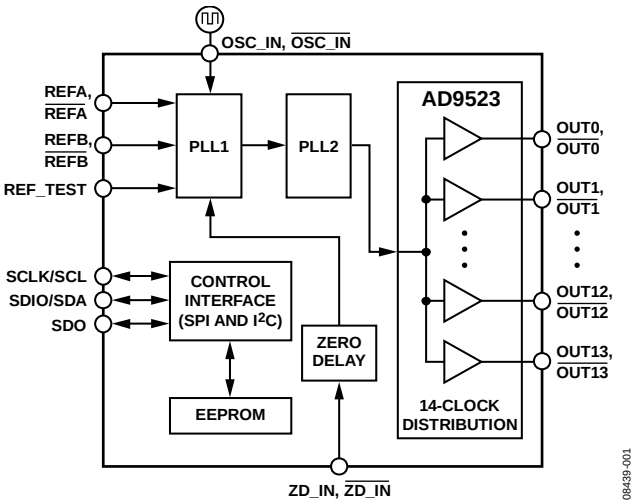


Figure 1.

GENERAL DESCRIPTION

The AD9523 provides a low power, multi-output, clock distribution function with low jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 3.6 GHz to 4.0 GHz.

The AD9523 is designed to support the clock requirements for long term evolution (LTE) and multicarrier GSM base station designs. It relies on an external VCXO to provide the reference jitter cleanup to achieve the restrictive low phase noise requirements necessary for acceptable data converter SNR performance.

The input receivers, oscillator, and zero delay receiver provide both single-ended and differential operation. When connected to a recovered system reference clock and a VCXO, the device generates 14 low noise outputs with a range of 1 MHz to 1 GHz, and one dedicated buffered output from the input PLL (PLL1). The frequency and phase of one clock output relative to another clock output can be varied by means of a divider phase select function that serves as a jitter-free coarse timing adjustment in increments that are equal to half the period of the signal coming out of the VCO.

An in-package EEPROM can be programmed through the serial interface to store user-defined register settings for power-up and chip reset.

Rev. D
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REVISION HISTORY

9/15—Rev. C to Rev. D

Changes to Features Section 1
Changes to Table 7 6
Changes to Table 12 8
Added Operating Temperature Range Parameter and Junction Temperature Parameter, Table 17 11
Changes to Figure 21 17
Changes to Figure 22 and Overview Section 19
Changes to PLL1 Reference Clock Inputs Section and PLL1 Loop Filter Section 20
Added OSC_IN Input Section 20
Changes to PLL2 General Description Section 22
Changes to VCO and VCO Calibration Section 23
Changes to Zero Delay Operation Section 26
Added Power Supply Sequencing Section 27
Deleted Figure 32; Renumbered Sequentially 29
Changes to SPI Instruction Word (16 Bits) Section 32
Changes to Writing to the EEPROM Section and Reading from the EEPROM Section 35
Changes to Programming the EEPROM Buffer Segment Section 36
Added Device Initialization Flow Charts Section, Figure 44, and Figure 45; Renumbered Sequentially 38
Changes to Table 31 44
Changes to Table 40 49
Changes to Table 47 52

2/13—Rev. B to Rev. C

Deleted VDD1.8_PLL2 ..... Throughout
Changes to Data Sheet Title 1
Added T_J of 115°C, Table 1 4
Changed VDD3_PLL1, Supply Voltage for PLL1 Typical Parameter from 22 mA to 37 mA and Changed VDD3_PLL1, Supply Voltage for PLL1 Maximum Parameter from 25.2 mA to 43 mA, Table 2 4
Changes to Table 3 5
Added PLL1 Characteristics Section and Table 7; Renumbered Sequentially 6
Changes to Table 9 Summary Statement 7
Changes to Pin 7 Description, Table 19 13
Changed Pin 69 from VDD1.8_PLL2 to NC, Table 19 15
Changes to Figure 23 21
Changes to Clock Distribution Synchronization Section 25
Changes to Figure 29 26
Added Reset Modes Section and Lock Detect Section 26
Added Power-Down Mode Section 27
Changes to Pin Descriptions Section and Read Section 31
Added Figure 38; Renumbered Sequentially 33
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Changed Bit 6 Name from Status PLL2 Feedback Clock to Status PLL1 Feedback Clock, Table 54 52

3/11—Rev. A to Rev. B

Added Table Summary, Table 8 7
Changes to EEPROM Operations Section and Writing to the EEPROM Section 34
Changes to 0x01A, Bits[4:3], Table 30 39
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11/10—Rev. 0 to Rev. A

Change to General Description 1
Changes to Table Summary, Table 1 3
Change to Input High Voltage and Input Low Voltage Parameters and Added Input Threshold Voltage Parameter, Table 4 4
Change to Junction Temperature Rating, Table 16; Changes to Thermal Resistance Section 11
Changes to Table 18 12
Added Figure 14, Renumbered Sequentially 16
Edits to Figure 15, Figure 17, and Figure 19 17
Changes to VCO Calibration Section 22
Changed Output Mode Heading to Multimode Output Drivers; Changes to Multimode Output Drivers Section; Added Figure 26 23
Added Power Dissipation and Thermal Considerations Section; Added Table 29, Renumbered Sequentially 35
Changes to Table 34, Table 35, Table 36, and Table 38 43
Changes to Address 0x192, Table 50 48
Changes to Table 52 49
Changes to Table 54 50

7/10—Revision 0: Initial Version

SPECIFICATIONS

f_{VCXO} = 122.88 MHz single ended, REFA and REFB on differential at 30.72 MHz, f_{VCO} = 3932.16 MHz, doubler is off, channel control low power mode off, divider phase = 1, unless otherwise noted. Typical is given for VDD = 3.3 V ± 5% and T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full VDD and T_A (−40°C to +85°C) variation, as listed in Table 1.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDD3_PLL1, Supply Voltage for PLL1		3.3		V	3.3 V ± 5%
VDD3_PLL2, Supply Voltage for PLL2		3.3		V	3.3 V ± 5%
VDD3_REF, Supply Voltage Clock Output Drivers Reference		3.3		V	3.3 V ± 5%
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		3.3		V	3.3 V ± 5%
VDD1.8_OUT[x:y],[1] Supply Voltage Clock Dividers		1.8		V	1.8 V ± 5%
TEMPERATURE					
Ambient Temperature Range, T_A	−40	+25	+85	°C	
Junction Temperature, T_J			115	°C	

[1] x and y are the pair of differential outputs that share the same power supply. For example, VDD3_OUT[0:1] is Supply Voltage Clock Output OUT0, $\overline{OUT0}$ (Pin 68 and Pin 67, respectively) and Supply Voltage Clock Output OUT1, $\overline{OUT1}$ (Pin 65 and Pin 64, respectively).

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLIES OTHER THAN CLOCK OUTPUT DRIVERS					
VDD3_PLL1, Supply Voltage for PLL1		37	43	mA	Decreases by 9 mA typical if REFB is turned off
VDD3_PLL2, Supply Voltage for PLL2		67	77.7	mA	
VDD3_REF, Supply Voltage Clock Output Drivers Reference					
LVPECL Mode		5	6	mA	Only one output driver turned on; for each additional output that is turned on, the current increments by 1.2 mA maximum
LVDS Mode		4	4.8	mA	Only one output driver turned on; for each additional output that is turned on, the current increments by 1.2 mA maximum
HSTL Mode		3	3.6	mA	Values are independent of the number of outputs turned on
CMOS Mode		3	3.6	mA	Values are independent of the number of outputs turned on
VDD1.8_OUT[x:y],[1] Supply Voltage Clock Dividers[2]		3.5	4.2	mA	Current for each divider: f = 245.76 MHz
CLOCK OUTPUT DRIVERS					
LVDS Mode, 7 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		16	17.4	mA	f = 61.44 MHz
LVDS Mode, 3.5 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		5	6.2	mA	f = 245.76 MHz
LVPECL Mode					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		17	18.9	mA	f = 122.88 MHz
HSTL Mode, 16 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		21	24.0	mA	f = 122.88 MHz
HSTL Mode, 8 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		14	16.3	mA	f = 122.88 MHz
CMOS Mode (Single-Ended)					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		2	2.4	mA	f = 15.36 MHz, 10 pF load

[1] x and y are the pair of differential outputs that share the same power supply. For example, VDD3_OUT[0:1] is Supply Voltage Clock Output OUT0, $\overline{OUT0}$ (Pin 68 and Pin 67, respectively) and Supply Voltage Clock Output OUT1, $\overline{OUT1}$ (Pin 65 and Pin 64, respectively).
[2] The current for Pin 63 (VDD1_OUT[0:3]) is 2× that of the other VDD11.8_OUT[x:y] pairs.

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					Does not include power dissipated in termination resistors
Typical Configuration		876	970	mW	Clock distribution outputs running as follows: seven LVPECL outputs at 122.88 MHz, three LVDS outputs (3.5 mA) at 61.44 MHz, three LVDS outputs (3.5 mA) at 245.76 MHz, one CMOS 10 pF load at 122.88 MHz, and one differential input reference at 30.72 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 3932.16 MHz; PLL2 BW = 530 kHz, doubler is off
$\overline{PD}$, Power-Down		101	132.2	mW	$\overline{PD}$ pin pulled low, with typical configuration conditions
INCREMENTAL POWER DISSIPATION					
Low Power Typical Configuration		389	450	mW	Absolute total power with clock distribution; one LVPECL output running at 122.88 MHz; one differential input reference at 30.72 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 3932.16 MHz; doubler is off
Output Distribution, Driver On					Incremental power increase (OUT1) from low power typical
LVDS		15.3	18.4	mW	Single 3.5 mA LVDS output at 245.76 MHz
		47.8	55.4	mW	Single 7 mA LVDS output at 61.44 MHz
LVPECL		50.1	54.9	mW	Single LVPECL output at 122.88 MHz
HSTL		40.2	46.3	mW	Single 8 mA HSTL output at 122.88 MHz
		43.7	50.3	mW	Single 16 mA HSTL output at 122.88 MHz
CMOS		6.6	7.9	mW	Single 3.3 V CMOS output at 15.36 MHz
		9.9	11.9	mW	Dual complementary 3.3 V CMOS output at 122.88 MHz
		9.9	11.9	mW	Dual in-phase 3.3 V CMOS output at 122.88 MHz

REFA, $\overline{REFA}$, REFB, $\overline{REFB}$, OSC_IN, $\overline{OSC_IN}$, AND ZD_IN, $\overline{ZD_IN}$ INPUT CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					
Input Frequency Range			400	MHz	
Input Slew Rate (OSC_IN)	400			V/µs	Minimum limit imposed for jitter performance
Common-Mode Internally Generated Input Voltage	0.6	0.7	0.8	V	
Input Common-Mode Range	1.025		1.475	V	For dc-coupled LVDS (maximum swing)
Differential Input Voltage, Sensitivity Frequency < 250 MHz	100			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding of unused input; the instantaneous voltage on either pin must not exceed the 1.8 V dc supply rails
Differential Input Voltage, Sensitivity Frequency > 250 MHz	200			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding of unused input; the instantaneous voltage on either pin must not exceed the 1.8 V dc supply rails
Differential Input Resistance		4.8		kΩ	
Differential Input Capacitance		1		pF	
Duty Cycle					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	1			ns	
Pulse Width High	1			ns	
CMOS MODE SINGLE-ENDED INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	1.62			V	
Input Low Voltage			0.52	V	
Input Threshold Voltage		1.0		V	When ac coupling to the input receiver, the user must dc bias the input to 1 V; the single-ended CMOS input is 3.3 V compatible
Input Capacitance		1		pF	
Duty Cycle					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	1.6			ns	
Pulse Width High	1.6			ns	

OSC_CTRL OUTPUT CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
High	VDD3_PLL1 – 0.15			V	R_{LOAD} > 20 kΩ
Low			150	mV	

REF_TEST INPUT CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF_TEST INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	

PLL1 CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL1 FIGURE OF MERIT (FOM)		−226		dBc/Hz	
MAXIMUM PFD FREQUENCY					
Antibacklash Pulse Width					High is the initial PLL1 antibacklash pulse width setting. The user must program Register 0x019[4] = 1b to enable SPI control of the antibacklash pulse width to the setting defined in Register 0x019[3:2] and Table 40.
Minimum			130	MHz	
Low			90	MHz	
High			65	MHz	
Maximum			45	MHz	

PLL1 OUTPUT CHARACTERISTICS

Table 8.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM OUTPUT FREQUENCY		250		MHz	
Rise/Fall Time (20% to 80%)		387	665	ps	15 pF load
Duty Cycle	45	50	55	%	f = 250 MHz
OUTPUT VOLTAGE HIGH					Output driver static
	VDD3_PLL1 – 0.25			V	Load current = 10 mA
	VDD3_PLL1 – 0.1			V	Load current = 1 mA
OUTPUT VOLTAGE LOW					Output driver static
			0.2	V	Load current = 10 mA
			0.1	V	Load current = 1 mA

[1] CMOS driver strength = strong (see Table 52).

DISTRIBUTION OUTPUT CHARACTERISTICS (OUT0, $\overline{OUT0}$ TO OUT13, $\overline{OUT13}$)

Duty cycle performance is specified with the invert divider bit set to 1, and the divider phase bits set to 0.5. (For example, for Channel 0, 0x190[7] = 1 and 0x192[7:2] = 1.) Output Voltage Reference VDD in Table 9 refers to the 3.3 VDD3_OUT[x:y] supply.

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL MODE					
Maximum Output Frequency		1		GHz	Minimum VCO/maximum dividers
Rise Time/Fall Time (20% to 80%)		117	147	ps	100 Ω termination across output pair
Duty Cycle	47	50	52	%	f < 500 MHz
	43	48	52	%	f = 500 MHz to 800 MHz
	40	49	54	%	f = 800 MHz to 1 GHz
Differential Output Voltage Magnitude	643	775	924	mV	Voltage across pins, output driver static
Common-Mode Output Voltage	VDD – 1.5	VDD – 1.4	VDD – 1.25	V	Output driver static
SCALED HSTL MODE, 16 mA					
Maximum Output Frequency		1		GHz	Minimum VCO/maximum dividers
Rise Time/Fall Time (20% to 80%)		112	141	ps	100 Ω termination across output pair
Duty Cycle	47	50	52	%	f < 500 MHz
	44	48	51	%	f = 500 MHz to 800 MHz
	40	49	54	%	f = 800 MHz to 1 GHz
Differential Output Voltage Magnitude	1.3	1.6	1.7	V	Voltage across pins, output driver static; nominal supply
Supply Sensitivity		0.6		mV/mV	Change in output swing vs. VDD3_OUT[x:y] ($\Delta V_{OD}/\Delta VDD3$)
Common-Mode Output Voltage	VDD – 1.76	VDD – 1.6	VDD – 1.42	V	
LVDS MODE, 3.5 mA					
Maximum Output Frequency		1		GHz	
Rise Time/Fall Time (20% to 80%)		138	161	ps	100 Ω termination across output pair
Duty Cycle	48	51	53	%	f < 500 MHz
	43	49	53	%	f = 500 MHz to 800 MHz
	41	49	55	%	f = 800 MHz to 1 GHz
Differential Output Voltage Magnitude					
Balanced	247		454	mV	Voltage across pins; output driver static
Unbalanced			50	mV	Absolute difference between voltage magnitude of normal pin and inverted pin
Common-Mode Output Voltage	1.125		1.375	V	Output driver static
Common-Mode Difference			50	mV	Voltage difference between output pins; output driver static
Short-Circuit Output Current		3.5	24	mA	Output driver static
CMOS MODE					
Maximum Output Frequency		250		MHz	
Rise Time/Fall Time (20% to 80%)		387	665	ps	15 pF load
Duty Cycle	45	50	55	%	f = 250 MHz
Output Voltage High					Output driver static
	VDD – 0.25			V	Load current = 10 mA
	VDD – 0.1			V	Load current = 1 mA
Output Voltage Low					Output driver static
			0.2	V	Load current = 10 mA
			0.1	V	Load current = 1 mA

TIMING ALIGNMENT CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					Delay off on all outputs; maximum deviation between rising edges of outputs; all outputs are on, unless otherwise noted
Between Outputs in Same Group[1]					
LVPECL, HSTL, and LVDS					
Between LVPECL, HSTL, and LVDS Outputs		30	183	ps	
CMOS					
Between CMOS Outputs		100	300	ps	Single-ended true phase high-Z mode
Mean Delta Between Groups[1]		50			
Adjustable Delay	0		63	Steps	Resolution step; for example, 8 × 0.5/1 GHz
Resolution Step		500		ps	½ period of 1 GHz
Zero Delay					
Between Input Clock Edge on REFA or REFB to ZD_IN Input Clock Edge, External Zero Delay Mode		150	500	ps	PLL1 settings: PFD = 7.68 MHz, I_{CP} = 63.5 µA, R_{ZERO} = 10 kΩ, antibacklash pulse width is at maximum, BW = 40 Hz, REFA and ZD_IN are set to differential mode

[1] There are three groups of outputs. They are as follows: the top outputs group: OUT0, OUT1, OUT2, OUT3; the right outputs group: OUT4, OUT5, OUT6, OUT7, OUT8, OUT9; and the bottom outputs group: OUT10, OUT11, OUT12, OUT13.

JITTER AND NOISE CHARACTERISTICS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT ABSOLUTE RMS TIME JITTER					Application example based on a typical setup (see Table 3); f = 122.88 MHz
LVPECL Mode, HSTL Mode, LVDS Mode					
		125		fs	Integrated BW = 200 kHz to 5 MHz
		136		fs	Integrated BW = 200 kHz to 10 MHz
		169		fs	Integrated BW = 12 kHz to 20 MHz
		212		fs	Integrated BW = 10 kHz to 61 MHz
		223		fs	Integrated BW = 1 kHz to 61 MHz

PLL2 CHARACTERISTICS

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON CHIP)					
Frequency Range	3600		4000	MHz	
Gain		45		MHz/V	
PLL2 FIGURE OF MERIT (FOM)		−226		dBc/Hz	
MAXIMUM PFD FREQUENCY					
Antibacklash Pulse Width					High is the initial PLL2 antibacklash pulse width setting. The user must program Register 0x0F2[4] = 1b to enable SPI control of the antibacklash pulse width to the setting defined in Register 0x0F2[3:2] and Table 47.
Minimum			259	MHz	
Low			200	MHz	
High			135	MHz	
Maximum			80	MHz	

LOGIC INPUT PINS—$\overline{PD}$, EEPROM_SEL, REF_SEL, $\overline{RESET}$, $\overline{SYNC}$

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Input High	2.0			V	
Input Low			0.8	V	
INPUT LOW CURRENT		±80	±250	µA	The minus sign indicates that, due to the internal pull-up resistor, current is flowing out of the AD9523
CAPACITANCE		3		pF	
$\overline{RESET}$ TIMING					
Pulse Width Low	50			ns	
Inactive to Start of Register Programming	100			ns	
$\overline{SYNC}$ TIMING					
Pulse Width Low	1.5			ns	High speed clock is CLK input signal

STATUS OUTPUT PINS—STATUS1, STATUS0

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Output High	2.94			V	
Output Low			0.4	V	

SERIAL CONTROL PORT—SPI MODE

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 40 kΩ pull-up resistor
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		30		µA	
Input Logic 0		−110		µA	The minus sign indicates that, due to the internal pull-up resistor, current is flowing out of the AD9523
Input Capacitance		2		pF	
SCLK (INPUT) IN SPI MODE					SCLK has an internal 40 kΩ pull-down resistor in SPI mode but not in I^2C mode
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		240		µA	
Input Logic 0		1		µA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT IS IN BIDIRECTIONAL MODE)					
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		1		µA	
Input Logic 0		1		µA	
Input Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{HIGH}	8			ns	
Pulse Width Low, t_{LOW}	12			ns	
SDIO to SCLK Setup, t_{DS}	3.3			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			14	ns	
$\overline{CS}$ to SCLK Setup, t_S	10			ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	6			ns	

SERIAL CONTROL PORT—I²C MODE

VDD = VDD3_REF, unless otherwise noted.

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (WHEN INPUTTING DATA)					
Input Logic 1 Voltage	0.7 × VDD			V	
Input Logic 0 Voltage			0.3 × VDD	V	
Input Current with an Input Voltage Between 0.1 × VDD and 0.9 × VDD	−10		+10	µA	
Hysteresis of Schmitt Trigger Inputs	0.015 × VDD			V	
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SPIKE}			50	ns	
SDA (WHEN OUTPUTTING DATA)					
Output Logic 0 Voltage at 3 mA Sink Current			0.4	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX} with a Bus Capacitance from 10 pF to 400 pF	20 + 0.1 C_B[1]		250	ns	
TIMING					Note that all I²C timing values are referred to VIH_{MIN} (0.3 × VDD) and VIL_{MAX} levels (0.7 × VDD)
Clock Rate (SCL, f_{I2C})			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition, $t_{SET;STR}$	0.6			µs	
Hold Time (Repeated) Start Condition, $t_{HLD;STR}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for Stop Condition, $t_{SET;STP}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_{RISE}	20 + 0.1 C_B[1]		300	ns	
SCL, SDA Fall Time, t_{FALL}	20 + 0.1 C_B[1]		300	ns	
Data Setup Time, $t_{SET;DAT}$	100			ns	
Data Hold Time, $t_{HLD;DAT}$	100		880	ns	This is a minor deviation from the original I²C specification of 0 ns minimum[2]
Capacitive Load for Each Bus Line, C_B[1]			400	pF	

[1] C_B is the capacitance of one bus line in picofarads (pF).
[2] According to the original I²C specification, an I²C master must also provide a minimum hold time of 300 ns for the SDA signal to bridge the undefined region of the SCL falling edge.

ABSOLUTE MAXIMUM RATINGS

Table 17.

Parameter	Rating
VDD3_PLL1, VDD3_PLL2, VDD3_REF, VDD3_OUT, LDO_VCO to GND	−0.3 V to +3.6 V
REFA, $\overline{\text{REFA}}$, $\overline{\text{REFIN}}$, REFB, $\overline{\text{REFB}}$ to GND	−0.3 V to +3.6 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to +3.6 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$, OUT10, $\overline{\text{OUT10}}$, OUT11, $\overline{\text{OUT11}}$, OUT12, $\overline{\text{OUT12}}$, OUT13, $\overline{\text{OUT13}}$ to GND	−0.3 V to +3.6 V
$\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, $\overline{\text{PD}}$ to GND	−0.3 V to +3.6 V
STATUS0, STATUS1 to GND	−0.3 V to +3.6 V
SP0, SP1, EEPROM_SEL to GND	−0.3 V to +3.6 V
VDD1.8_OUT, LDO_PLL1, LDO_PLL2 to GND	2 V
Operating Temperature Range	−40°C to +85°C
Junction Temperature	115°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 18. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
72-Lead LFCSP, 10 mm × 10 mm	0	21.3	1.7	12.6	0.1	°C/W
	1.0	20.1			0.2	°C/W
	2.5	18.1			0.3	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

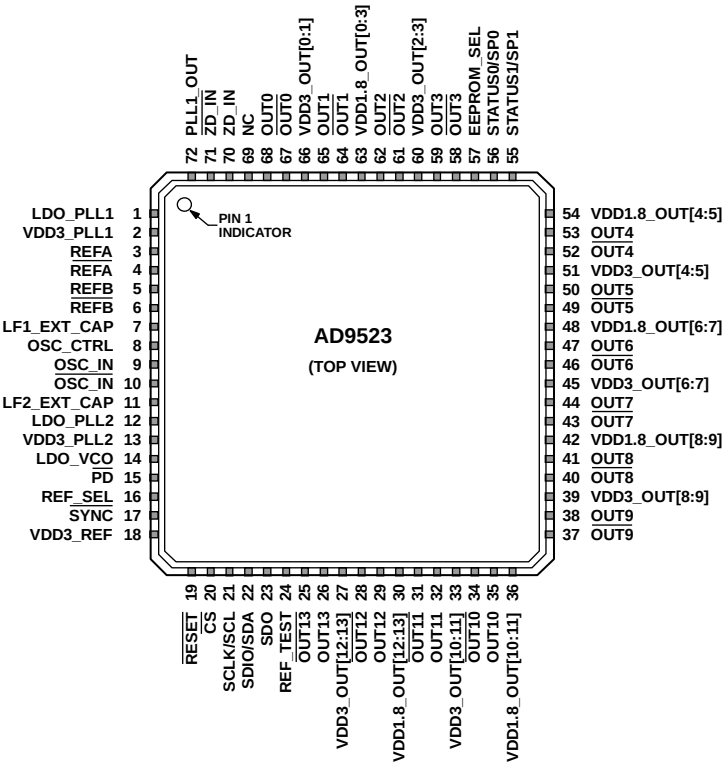
For information about power dissipation, refer to the Power Dissipation and Thermal Considerations section.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT. ON EXISTING PCB DESIGNS, IT IS ACCEPTABLE TO LEAVE PIN 69 CONNECTED TO 1.8V SUPPLY.
2. THE EXPOSED PADDLE IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

Figure 2. Pin Configuration

Table 19. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	LDO_PLL1	P/O	1.8 V Internal LDO Regulator Decoupling Pin for PLL1. Connect a 0.47 µF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
2	VDD3_PLL1	P	3.3 V Supply PLL1. Use the same supply as VCXO.
3	REFA	I	Reference Clock Input A. Along with $\overline{\text{REFA}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
4	$\overline{\text{REFA}}$	I	Complementary Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3V CMOS input.
5	REFB	I	Reference Clock Input B. Along with $\overline{\text{REFB}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
6	$\overline{\text{REFB}}$	I	Complementary Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
7	LF1_EXT_CAP	O	PLL1 External Loop Filter Capacitor. Connect a loop filter capacitor to this pin and to ground.
8	OSC_CTRL	O	Oscillator Control Voltage. Connect this pin to the voltage control pin of the external oscillator.
9	OSC_IN	I	PLL1 Oscillator Input. Along with $\overline{\text{OSC_IN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
10	$\overline{\text{OSC_IN}}$	I	Complementary PLL1 Oscillator Input. Along with OSC_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
11	LF2_EXT_CAP	O	PLL2 External Loop Filter Capacitor Connection. Connect a capacitor to this pin and LDO_VCO.

Pin No.	Mnemonic	Type[1]	Description
12	LDO_PLL2	P/O	LDO Decoupling Pin for PLL2 1.8 V Internal Regulator. Connect a 0.47 µF decoupling capacitor from this pin to ground. Note that for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
13	VDD3_PLL2	P	3.3 V Supply for PLL2.
14	LDO_VCO	P/O	2.5 V LDO Internal Regulator Decoupling Pin for VCO. Connect a 0.47 µF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
15	$\overline{PD}$	I	Chip Power-Down, Active Low. This pin has an internal 40 kΩ pull-up resistor.
16	REF_SEL	I	Reference Input Select. This pin has an internal 40 kΩ pull-down resistor.
17	$\overline{SYNC}$	I	Manual Synchronization. This pin initiates a manual synchronization and has an internal 40 kΩ pull-up resistor.
18	VDD3_REF	P	3.3 V Supply for Output Clock Drivers Reference.
19	$\overline{RESET}$	I	Digital Input, Active Low. Resets internal logic to default states. This pin has an internal 40 kΩ pull-up resistor.
20	$\overline{CS}$	I	Serial Control Port Chip Select, Active Low. This pin has an internal 40 kΩ pull-up resistor.
21	SCLK/SCL	I	Serial Control Port Clock Signal for SPI Mode (SCLK) or I^2C Mode (SCL). Data clock for serial programming. This pin has an internal 40 kΩ pull-down resistor in SPI mode but is high impedance in I^2C mode.
22	SDIO/SDA	I/O	Serial Control Port Bidirectional Serial Data In/Data Out for SPI Mode (SDIO) or I^2C Mode (SDA).
23	SDO	O	Serial Data Output. Use this pin to read data in 4-wire mode (high impedance in 3-wire mode). There is no internal pull-up/pull-down resistor on this pin.
24	REF_TEST	I	Test Input to PLL1 Phase Detector.
25	$\overline{OUT13}$	O	Complementary Square Wave Clocking Output 13. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
26	OUT13	O	Square Wave Clocking Output 13. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
27	VDD3_OUT[12:13]	P	3.3 V Supply for Output 12 and Output 13 Clock Drivers.
28	$\overline{OUT12}$	O	Complementary Square Wave Clocking Output 12. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
29	OUT12	O	Square Wave Clocking Output 12. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
30	VDD1.8_OUT[12:13]	P	1.8 V Supply for Output 12 and Output 13 Clock Dividers.
31	$\overline{OUT11}$	O	Complementary Square Wave Clocking Output 11. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
32	OUT11	O	Square Wave Clocking Output 11. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
33	VDD3_OUT[10:11]	P	3.3 V Supply for Output 10 and Output 11 Clock Drivers.
34	$\overline{OUT10}$	O	Complementary Square Wave Clocking Output 10. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
35	OUT10	O	Square Wave Clocking Output 10. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
36	VDD1.8_OUT[10:11]	P	1.8 V Supply for Output 10 and Output 11 Clock Dividers.
37	$\overline{OUT9}$	O	Complementary Square Wave Clocking Output 9. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
38	OUT9	O	Square Wave Clocking Output 9. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
39	VDD3_OUT[8:9]	P	3.3 V Supply for Output 8 and Output 9 Clock Drivers.
40	$\overline{OUT8}$	O	Complementary Square Wave Clocking Output 8. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
41	OUT8	O	Square Wave Clocking Output 8. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
42	VDD1.8_OUT[8:9]	P	1.8 V Supply for Output 8 and Output 9 Clock Dividers.
43	$\overline{OUT7}$	O	Complementary Square Wave Clocking Output 7. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
44	OUT7	O	Square Wave Clocking Output 7. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
45	VDD3_OUT[6:7]	P	3.3 V Supply for Output 6 and Supply Output 7 Clock Drivers.

Pin No.	Mnemonic	Type[1]	Description
46	$\overline{\text{OUT6}}$	O	Complementary Square Wave Clocking Output 6. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
47	OUT6	O	Square Wave Clocking Output 6. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
48	VDD1.8_OUT[6:7]	P	1.8 V Supply for Output 6 and Output 7 Clock Dividers.
49	$\overline{\text{OUT5}}$	O	Complementary Square Wave Clocking Output 5. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
50	OUT5	O	Square Wave Clocking Output 5. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
51	VDD3_OUT[4:5]	P	3.3 V Supply for Output 4 and Output 5 Clock Drivers.
52	$\overline{\text{OUT4}}$	O	Complementary Square Wave Clocking Output 4. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
53	OUT4	O	Square Wave Clocking Output 4. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
54	VDD1.8_OUT[4:5]	P	1.8 V Supply for Output 4 and Output 5 Clock Dividers.
55	STATUS1/SP1	I/O	Lock Detect and Other Status Signals (STATUS1)/I²C Address (SP1). This pin has an internal 40 kΩ pull-down resistor.
56	STATUS0/SP0	I/O	Lock Detect and Other Status Signals (STATUS0)/I²C Address (SP0). This pin has an internal 40 kΩ pull-down resistor.
57	EEPROM_SEL	I	EEPROM Select. Setting this pin high selects the register values stored in the internal EEPROM to be loaded at reset and/or power-up. Setting this pin low causes the AD9523 to load the hard-coded default register values at power-up/reset. This pin has an internal 40 kΩ pull-down resistor.
58	$\overline{\text{OUT3}}$	O	Complementary Square Wave Clocking Output 3. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
59	OUT3	O	Square Wave Clocking Output 3. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
60	VDD3_OUT[2:3]	P	3.3 V Supply for Output 2 and Output 3 Clock Drivers.
61	$\overline{\text{OUT2}}$	O	Complementary Square Wave Clocking Output 2. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
62	OUT2	O	Square Wave Clocking Output 2. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
63	VDD1.8_OUT[0:3]	P	1.8 V Supply for Output 0, Output 1, Output 2, and Output 3 Clock Dividers.
64	$\overline{\text{OUT1}}$	O	Complementary Square Wave Clocking Output 1. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
65	OUT1	O	Square Wave Clocking Output 1. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
66	VDD3_OUT[0:1]	P	3.3 V Supply for Output 0 and Output 1 Clock Drivers.
67	$\overline{\text{OUT0}}$	O	Complementary Square Wave Clocking Output 0. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
68	OUT0	O	Square Wave Clocking Output 0. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
69	NC	P	This pin is not connected internally (see Figure 2).
70	ZD_IN	I	External Zero Delay Clock Input. Along with $\overline{\text{ZD_IN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
71	$\overline{\text{ZD_IN}}$	I	Complementary External Zero Delay Clock Input. Along with ZD_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
72	PLL1_OUT	O	Single-Ended CMOS Output from PLL1. This pin has settings for weak and strong in Register 0x1BA[4] (see Table 52).
EP	EP, GND	GND	Exposed Paddle. The exposed paddle is the ground connection on the chip. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

[1] P is power, I is input, O is output, I/O is input/output, P/O is power/output, and GND is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

f_{VCXO} = 122.88 MHz, REFA differential at 30.72 MHz, f_{VCO} = 3686.4 MHz, and doubler is off, unless otherwise noted.

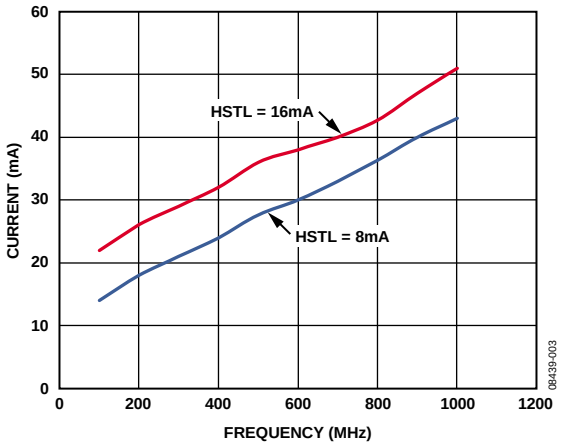


Figure 3. VDD3_OUT[x:y] Current (Typical) vs. Frequency; HSTL Mode, 16 mA and 8 mA

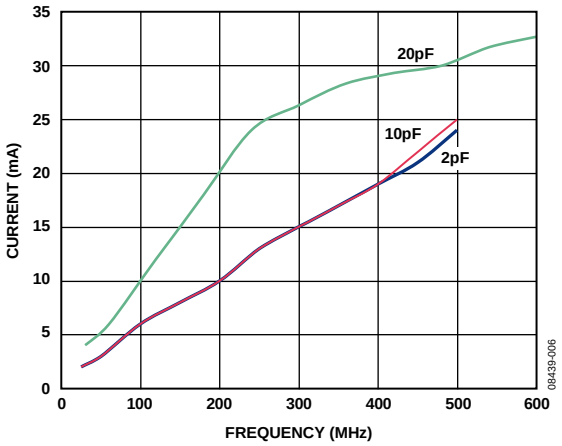


Figure 6. VDD3_OUT[x:y] Current (Typical) vs. Frequency; CMOS Mode, 20 pF, 10 pF, and 2 pF Load

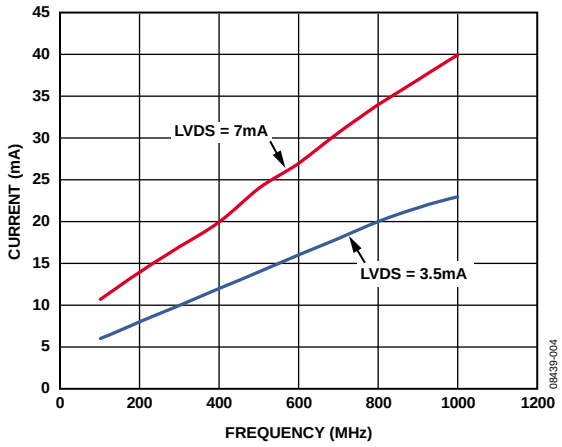


Figure 4. VDD3_OUT[x:y] Current (Typical) vs. Frequency; LVDS Mode, 7 mA and 3.5 mA

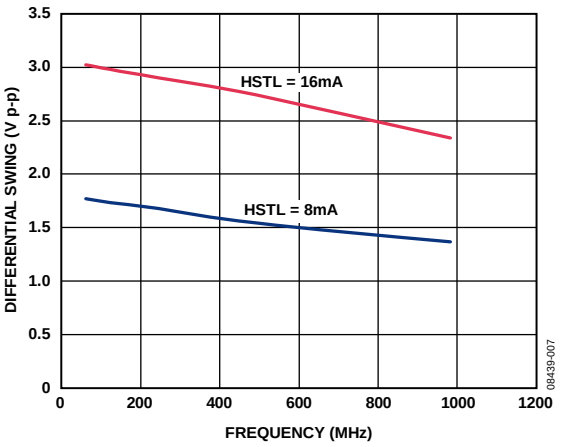


Figure 7. Differential Voltage Swing vs. Frequency; HSTL Mode, 16 mA and 8 mA

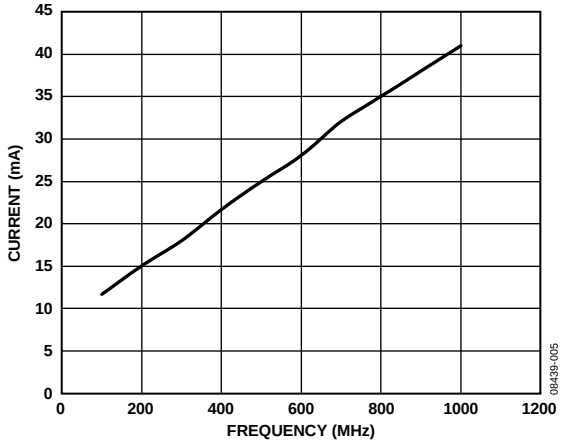


Figure 5. VDD3_OUT[x:y] Current (Typical) vs. Frequency, LVPECL Mode

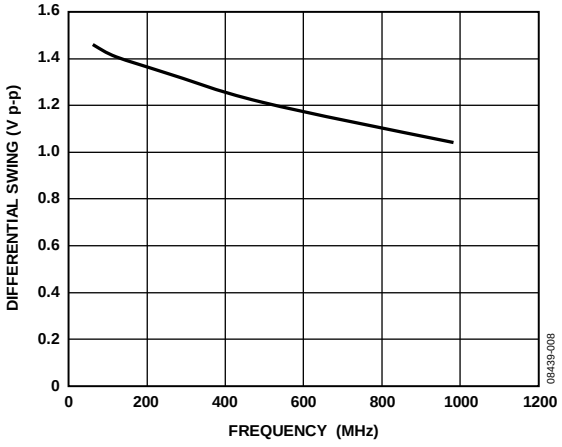


Figure 8. Differential Voltage Swing vs. Frequency, LVPECL Mode

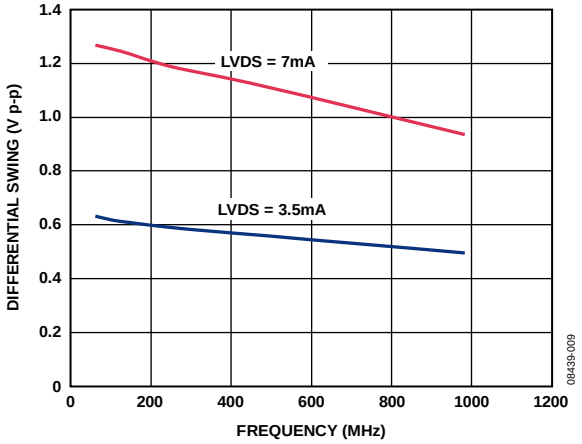


Figure 9. Differential Voltage Swing vs. Frequency; LVDS Mode, 7 mA and 3.5 mA

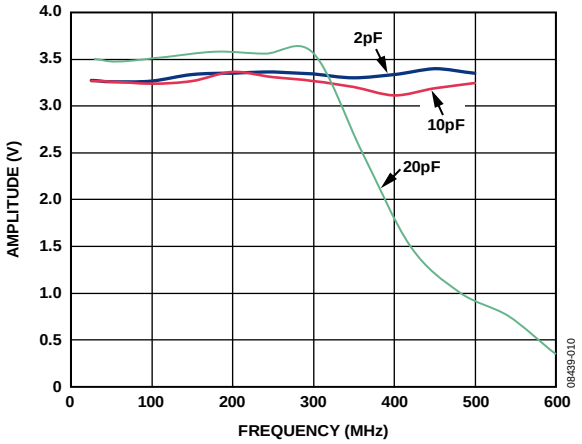


Figure 10. Amplitude vs. Frequency and Capacitive Load; CMOS Mode, 2 pF, 10 pF, and 20 pF

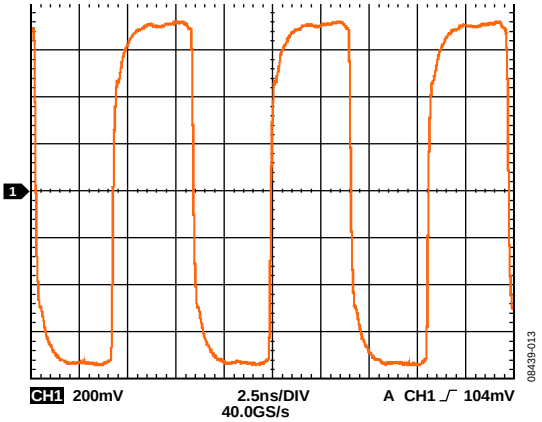


Figure 11. Output Waveform (Differential), LVPECL at 122.88 MHz

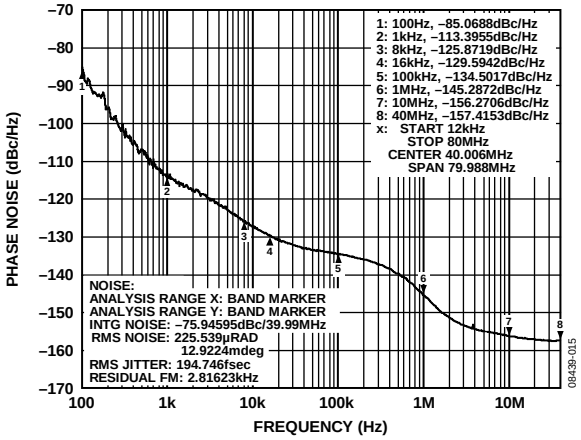


Figure 12. Phase Noise, Output = 184.32 MHz (VCXO = 122.88 MHz, Crystek VCXO CVHD-950)

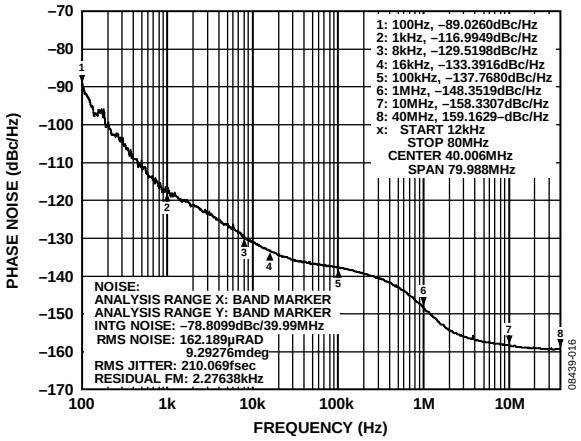


Figure 13. Phase Noise, Output = 122.88 MHz (VCXO = 122.88 MHz, Crystek VCXO CVHD-950; Doubler Is Off)

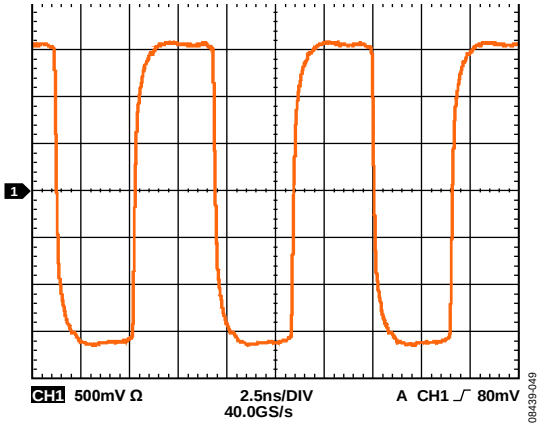


Figure 14. Output Waveform (Differential), HSTL at 16 mA, 122.88 MHz

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

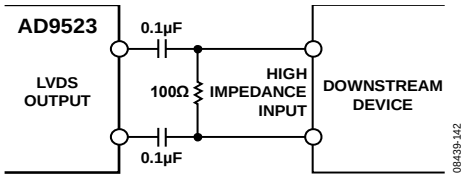


Figure 15. AC-Coupled LVDS Output Driver

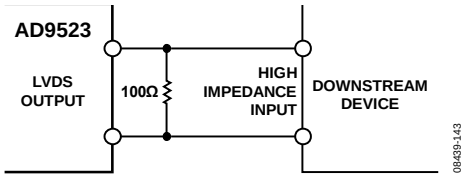


Figure 16. DC-Coupled LVDS Output Driver

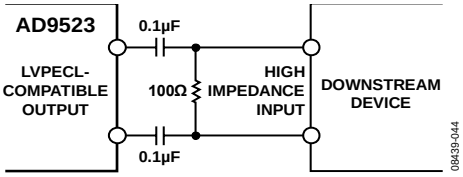


Figure 17. AC-Coupled LVPECL Output Driver

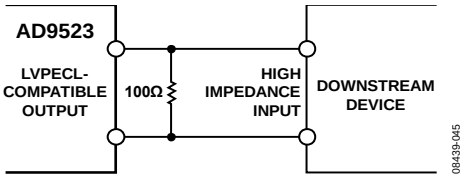


Figure 18. DC-Coupled LVPECL Output Driver

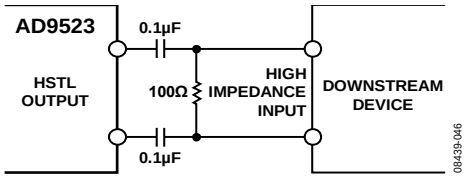


Figure 19. AC-Coupled HSTL Output Driver

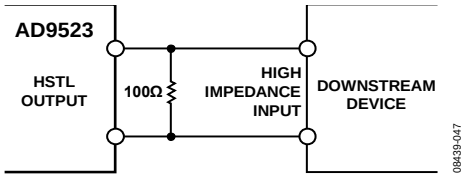


Figure 20. DC-Coupled HSTL Output Driver

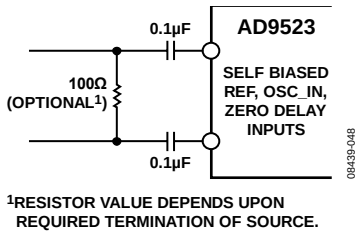


Figure 21. REF, OSC_IN, and Zero Delay Input Differential Mode

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma (Σ) of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

DETAILED BLOCK DIAGRAM

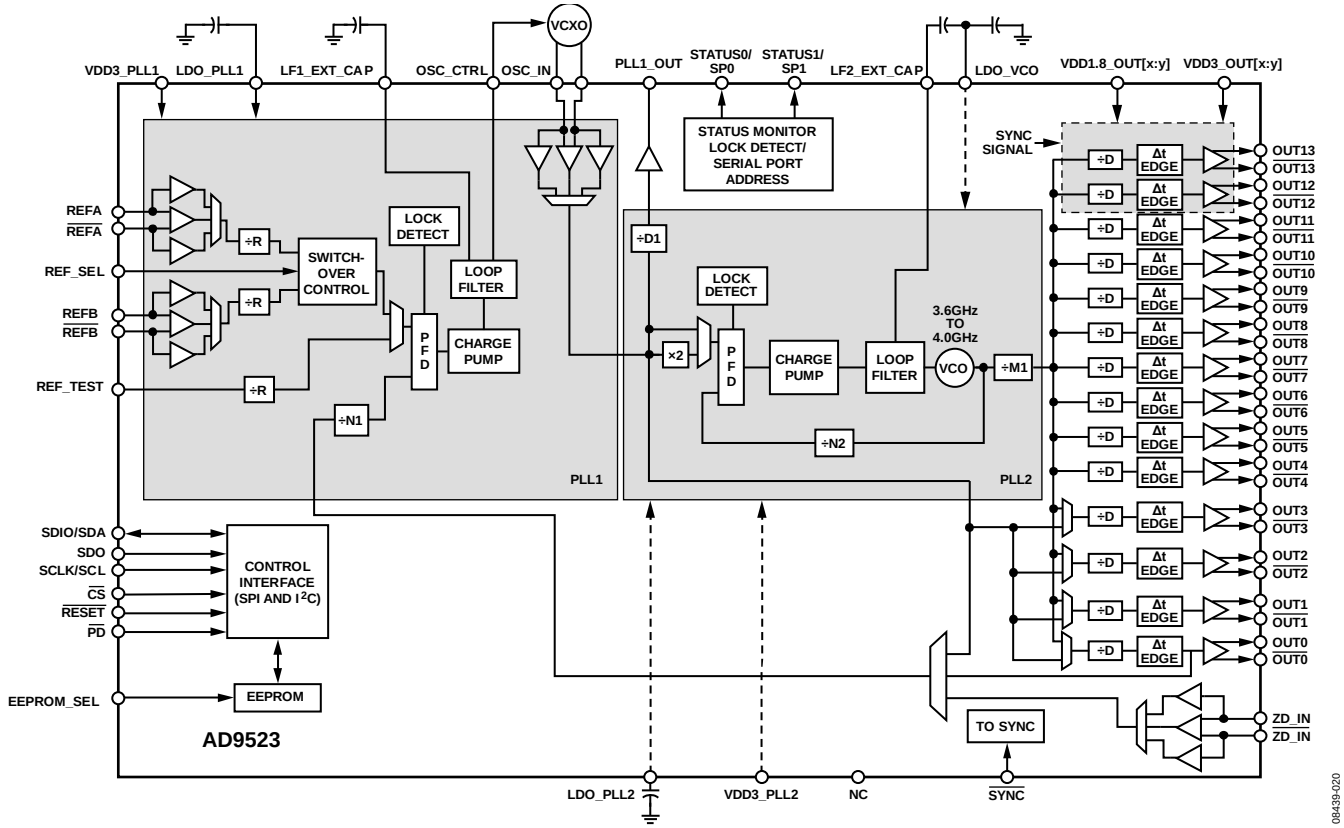


Figure 22. Top Level Diagram

OVERVIEW

The AD9523 is a clock generator that employs integer-N-based phase-locked loops (PLL). The device architecture consists of two cascaded PLL stages. The first stage, PLL1, consists of an integer division PLL that uses an external voltage-controlled crystal oscillator (VCXO) of up to 250 MHz. PLL1 has a narrow-loop bandwidth that provides initial jitter cleanup of the input reference signal. The second stage, PLL2, is a frequency multiplying PLL that translates the first stage output frequency to a range of 3.6 GHz to 4.0 GHz. PLL2 incorporates an integer-based feedback divider that enables integer frequency multiplication. Programmable integer dividers (1 to 1024) follow PLL2, establishing a final output frequency of 1 GHz or less.

The AD9523 includes reference signal processing blocks that enable a smooth switching transition between two reference inputs. This circuitry automatically detects the presence of the reference input signals. If only one input is present, the device uses it as the active reference. If both are present, one becomes the active reference and the other becomes the backup reference. If the active reference fails, the circuitry automatically switches to the backup reference (if available), making it the new active reference. A register setting determines what action to take if the failed reference is once again available: either stay on Reference B or revert to Reference A. If neither reference can be used, the AD9523 supports a holdover mode. A reference select pin (REF_SEL, Pin 16) is available to manually select which input reference is active (see Table 43). The accuracy of the holdover is dependent on the external VCXO frequency stability at half supply voltage.

Any of the divider settings are programmable via the serial programming port, enabling a wide range of input/output frequency ratios under program control. The dividers also include a programmable delay to adjust the timing of the output signals, if required.

The 14 outputs are compatible with LVPECL, LVDS, HSTL, and 1.8 V CMOS logic levels (see the Input/Output Termination Recommendations section). All differential output logic settings require a single 100 Ω differential termination.

The loop filters of each PLL are integrated and programmable. Only a single external capacitor for each of the two PLL loop filters is required.

The AD9523 operates over the extended industrial temperature range of −40°C to +85°C.

COMPONENT BLOCKS—INPUT PLL (PLL1)

PLL1 General Description

Fundamentally, the input PLL (referred to as PLL1) consists of a phase/frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop.

PLL1 has the flexibility to operate with a loop bandwidth of approximately 10 Hz to 100 Hz. This relatively narrow loop bandwidth gives the AD9523 the ability to suppress jitter that appears on the input references (REFA and REFB). The output of PLL1 then becomes a low jitter phase-locked version of the reference input system clock.

PLL1 Reference Clock Inputs

The AD9523 features two separate PLL1 differential reference clock inputs, REFA and REFB. These inputs can be configured to operate in full differential mode or single-ended CMOS mode.

In differential mode, these pins are internally self biased. If REFA or REFB is driven single-ended in differential mode, the unused side ($\overline{\text{REFA}}$, $\overline{\text{REFB}}$) should be decoupled via a suitable capacitor to a quiet ground. Figure 21 shows the recommended differential input termination to REFA or REFB. It is possible to dc couple to these inputs, but the dc operation point should be set as specified in the Specifications tables.

To operate either the REFA or the REFB inputs in 3.3 V CMOS mode, set Register 0x01A[6:5] and Register 0x01B[1:0] (see Table 41 and Table 40). The single-ended inputs can be driven by either a dc-coupled CMOS level signal or an ac-coupled sine wave or square wave.

The differential reference input receiver is powered down when the differential reference input is not selected, or when the PLL is powered down. The single-ended buffers power-down when the PLL is powered down, when their respective individual power-down registers are set, or when the differential receiver is selected.

The REFB R divider uses the same value as the REFA R divider unless Register 0x01C[7], the enable REFB R divider independent division control bit, is programmed as shown in Table 43.

OSC_IN Input

The OSC_IN receiver connects to the PLL1 feedback divider and to the PLL2 PFD through an optional doubler. This input receiver is identical to the PLL1 REFA and REFB receivers. Control bits for this receiver are located in Register 0x01A[1:0]. Figure 21 shows the recommended differential input termination to the OSC_IN receiver.

The OSC_IN receiver is powered down when the PLL1 power-down bit is set (Register 0x233[2] = 1b). When using the AD9523 in a mode of operation that bypasses PLL1, the PLL1 power-down bit must be disabled (Register 0x233[2] = 0b).

PLL1 Loop Filter

The PLL1 loop filter requires the connection of an external capacitor from LF1_EXT_CAP (Pin 7) to ground. The value of the external capacitor depends on the use of an external VCXO, as well as such configuration parameters as input clock rate and desired bandwidth. Normally, a 0.3 µF capacitor allows the loop bandwidth to range from 10 Hz to 100 Hz and ensures loop stability over the intended operating parameters of the device (see Table 44 for R_{ZERO} values). The operating loop bandwidth (LBW) of PLL1 can be used as a metric to estimate the time required for the PLL to phase lock. In general, PLL1 is phase locked within 10 loop bandwidth time constants, τ_{LBW}, where $\tau_{LBW} = 1/LBW$. Therefore, PLL_TO (see Figure 44) equals $10 \times \tau_{LBW}$.

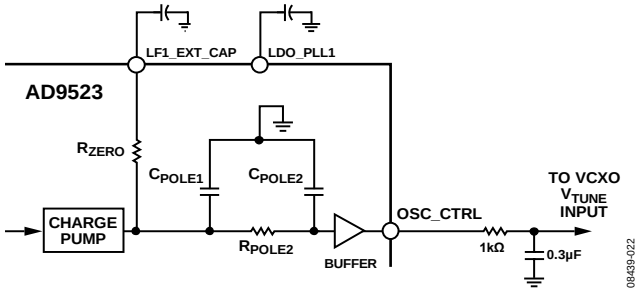


Figure 23. PLL1 Loop Filter

Table 20. PLL1 Loop Filter Programmable Values

R_{ZERO} (kΩ)	C_{POLE1} (nF)	R_{POLE2} (kΩ)	C_{POLE2} (nF)	LF1_EXT_CAP[1] (µF)
883	1.5 fixed	165 fixed	0.337 fixed	0.3
677				
341				
135				
10				
External				

[1] External loop filter capacitor.

An external RC low-pass filter should be used at the OSC_CTRL output. The values shown in Figure 23 add an additional low-pass pole at ~530 Hz. This RC network filters the noise associated with the OSC_CTRL buffer to achieve the best noise performance at the 1 kHz offset region.

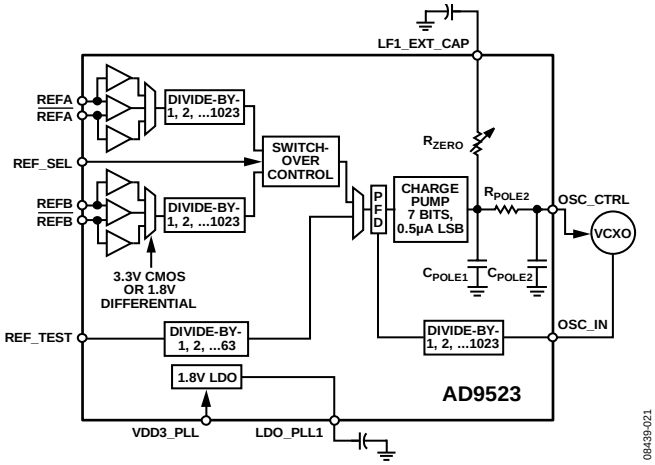


Figure 24. Input PLL (PLL1) Block Diagram

PLL1 Input Dividers

Each reference input feeds a dedicated reference divider block. The input dividers provide division of the reference frequency in integer steps from 1 to 1023. They provide the bulk of the frequency prescaling that is necessary to reduce the reference frequency to accommodate the bandwidth that is typically desired for PLL1.

PLL1 Reference Switchover

The reference monitor verifies the presence/absence of the prescaled REFA and REFB signals (that is, after division by the input dividers). The status of the reference monitor guides the activity of the switchover control logic. The AD9523 supports automatic and manual PLL reference clock switching between REFA (the REFA and $\overline{\text{REFA}}$ pins) and REFB (the REFB and $\overline{\text{REFB}}$ pins). This feature supports networking and infrastructure applications that require redundant references.

There are several configurable modes of reference switchover. Manual reference switchover is achieved either via a programming register setting or by using the REF_SEL pin. Automatic reference switchover occurs when REFA disappears and there is a reference on REFB.

Automatic reference switchover can be set to work as follows:

- Nonrevertive: stay on REFB. Switch from REFA to REFB when REFA disappears, but do not switch back to REFA if it reappears. If REFB disappears, then go back to REFA.
- Revert to REFA: switch from REFA to REFB when REFA disappears. Return to REFA from REFB when REFA returns.

See Table 43 for the PLL1 miscellaneous control register bit settings.

PLL1 Holdover

In the absence of both input references, the device enters holdover mode. Holdover is a secondary function that is provided by PLL1. Because PLL1 has an external VCXO available as a frequency source, it continues to operate in the absence of the input reference signals. When the device switches to holdover, the charge pump tristates. The device continues operating in this mode until a reference signal becomes available. Then the device exits holdover mode, and PLL1 resynchronizes with the active reference. In addition to tristate, the charge pump can be forced to $V_{CC}/2$ during holdover (see Table 43, Register 0x01C[6]).

COMPONENT BLOCKS—OUTPUT PLL (PLL2)

PLL2 General Description

The output PLL (referred to as PLL2) consists of an optional input reference doubler, phase/frequency detector (PFD), a partially integrated analog loop filter (see Figure 25), an integrated voltage controlled oscillator (VCO), and a feedback divider. The VCO produces a nominal 3.8 GHz signal with an output divider that is capable of division ratios of 4 to 11.

The PFD of the output PLL drives a charge pump that increases, decreases, or holds constant the charge stored on the loop filter capacitors (both internal and external). The stored charge results in a voltage that sets the output frequency of the VCO. The feedback loop of the PLL causes the VCO control voltage to vary in a way that phase locks the PFD input signals. The gain of PLL2 is proportional to the current delivered by the charge pump. The loop filter bandwidth is chosen to reduce noise contributions from PLL sources that could degrade phase noise requirements.

The output PLL has a VCO with multiple bands spanning a range of 3.6 GHz to 4.0 GHz. However, the actual operating frequency within a particular band depends on the control voltage that appears on the loop filter capacitor. The control voltage causes the VCO output frequency to vary linearly within the selected band. This frequency variability allows the control loop of the output PLL to synchronize the VCO output signal with the reference signal applied to the PFD. Typically, the device automatically selects the appropriate band as part of its calibration process (invoked via the VCO control register at Address 0x0F3). The VCO is designed to operate over temperature extremes including when the VCO is calibrated at one temperature extreme and operated within another.

Input 2× Frequency Multiplier

The 2× frequency multiplier provides the option to double the frequency at the PLL2 input. This allows the user to take advantage of a higher frequency at the input to the PLL (PFD) and, thus, allows for reduced in-band phase noise and greater separation between the frequency generated by the PLL and the modulation spur associated with PFD. However, increased reference spur separation results in harmonic spurs introduced by the frequency multiplier that increase as the duty cycle deviates from 50% at the OSC_IN inputs. Therefore, beneficial use of the frequency multiplier is application-specific. Typically, a VCXO with proper interfacing has a duty cycle that is approximately 50% at the OSC_IN inputs. Note that the maximum output frequency of the 2× frequency multipliers must not exceed the maximum PFD rate that is specified in Table 12.

PLL2 Feedback Divider

PLL2 has a feedback divider (N divider) that enables it to provide integer frequency up-conversion. The PLL2 N divider is a combination of a prescaler (P) and two counters, A and B. The total divider value is

$$N = (P \times B) + A$$

where $P = 4$.

The feedback divider is a dual modulus prescaler architecture, with a nonprogrammable P that is equal to 4. The value of the B counter can be from 4 to 63, and the value of the A counter can be from 0 to 3. However, due to the architecture of the divider, there are constraints, as listed in Table 46.

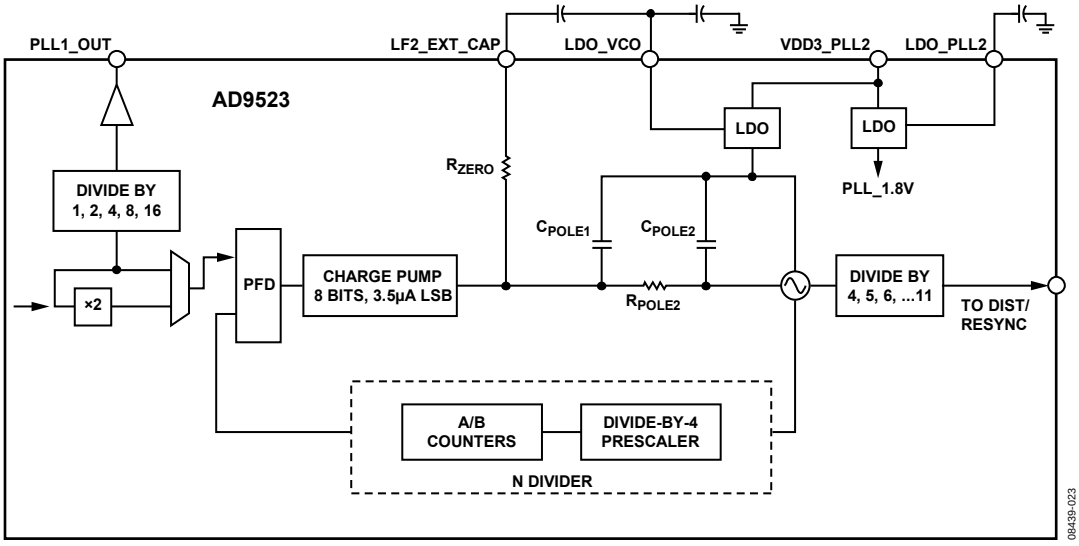


Figure 25. Output PLL (PLL2) Block Diagram

PLL2 Loop Filter

The PLL2 loop filter requires the connection of an external capacitor from LF2_EXT_CAP (Pin 11) to LDO_VCO (Pin 14), as illustrated in Figure 25. The value of the external capacitor depends on the operating mode and the desired phase noise performance. For example, a loop bandwidth of approximately 500 kHz produces the lowest integrated jitter. A lower bandwidth produces lower phase noise at 1 MHz but increases the total integrated jitter.

Table 21. PLL2 Loop Filter Programmable Values

R_{ZERO} (Ω)	C_{POLE1} (pF)	R_{POLE2} (Ω)	C_{POLE2} (pF)	LF2_EXT_CAP[1] (pF)
3250	48	900	Fixed at 16	Typical at 1000
3000	40	450		
2750	32	300		
2500	24	225		
2250	16			
2100	8			
2000	0			
1850				

[1] External loop filter capacitor.

VCO Divider

The VCO divider provides frequency division between the internal VCO and the clock distribution. The VCO divider can be set to divide by 4, 5, 6, 7, 8, 9, 10, or 11.

VCO and VCO Calibration

The AD9523 on-chip VCO must be manually calibrated to ensure proper operation over process and temperature. A VCO calibration is accomplished by transitioning the calibrate VCO bit (Register 0x0F3[1]) from 0 to 1 (this bit is not self clearing). The setting can be performed as part of the initial setup before executing the IO_UPDATE bit (Register 0x234[1] = 1b). A readback bit, VCO calibration in progress (Register 0x22D[0]), indicates when a VCO calibration is in progress by returning a logic true (Register 0x22D[1] = 1b). If the EEPROM is in use, setting the calibrate VCO bit to 1 before saving the register settings to the EEPROM ensures that the VCO calibrates automatically after the EEPROM has loaded. After calibration, it is recommended to initiate a distribution sync (see the Clock Distribution Synchronization section).

Note that the calibrate VCO bit defaults to 0. This bit must change from 0 to 1 to initiate a calibration sequence. Therefore, any subsequent calibrations require the following sequence:

1. Register 0x0F3[1] = 0b (calibrate VCO bit)
2. Register 0x234[0] = 1b (IO_UPDATE bit)
3. Register 0x0F3[1] = 1b (calibrate VCO bit)
4. Register 0x234[0] =1b (IO_UPDATE bit)

VCO calibration is controlled by a calibration controller that runs off the OSC_IN input clock. The calibration requires that PLL2 be set up properly to lock the PLL2 loop and that the OSC_IN clock be present.

During power-up or reset, the distribution section is automatically held in sync until the first VCO calibration is finished. Therefore, no outputs can occur until VCO calibration is complete and PLL2 is locked. This default functionality can be overwritten using Register 0x0F3[4].

Initiate a VCO calibration under the following conditions:

- After changing any of the PLL2 B counter and A counter settings or after a change in the PLL2 reference clock frequency. This means that a VCO calibration should be initiated any time that a PLL2 register or reference clock changes such that a different VCO frequency is the result.
- Whenever system calibration is desired. The VCO is designed to operate properly over extremes of temperature even when it is first calibrated at the opposite extreme. However, a VCO calibration can be initiated at any time, if desired.

CLOCK DISTRIBUTION

The clock distribution block provides an integrated solution for generating multiple clock outputs based on frequency dividing the PLL2 VCO divider output. The distribution output consists of 14 channels (OUT0 to OUT13). Each of the output channels has a dedicated divider and output driver, as shown in Figure 27. The AD9523 also has the capability to route the VCXO output to four of the outputs (OUT0 to OUT3).

Clock Dividers

The output clock distribution dividers are referred to as D0 to D13, corresponding to output channels OUT0 through OUT13, respectively. Each divider is programmable with 10 bits of division depth that is equal to 1 to 1024. Dividers have duty cycle correction to always give a 50% duty cycle, even for odd divides.

Output Power-Down

Each of the output channels offers independent control of the power-down functionality via the Channel 0 to Channel 13 control registers (see Table 51). Each output channel has a dedicated power-down bit for powering down the output driver. However, if all 14 outputs are powered down, the entire distribution output enters a deep sleep mode. Although each channel has a channel power-down control signal, it may sometimes be desirable to power down an output driver while maintaining the divider's synchronization with the other channel dividers. This is accomplished by placing the output in tristate mode (this works in CMOS mode, as well).

Multimode Output Drivers

The user has independent control of the operating mode of each of the fourteen output channels via the Channel 0 to Channel 13 control registers (see Table 51). The operating mode control includes the following:

- Logic family and pin functionality
- Output drive strength
- Output polarity

The four least significant bits (LSBs) of each of the 14 Channel 0 to Channel 13 control registers comprise the driver mode bits. The mode value selects the desired logic family and pin functionality of an output channel, as listed in Table 51. This driver design allows a common 100 Ω external resistor for all the different driver modes of operation that are illustrated in Figure 26.

If the output channel is ac-coupled to the circuit to be clocked, changing the mode varies the voltage swing to determine sensitivity to the drive level. For example, in LVDS mode, a current of 3.5 mA causes a 350 mV peak voltage. Likewise, in LVPECL mode, a current of 8 mA causes an 800 mV peak voltage at the 100 Ω load resistor. Using any termination other than those specified in the Input/Output Termination Recommendations section may results in damage or decrease end of life performance.

In addition to the four mode bits, each of the 14 Channel 0 to Channel 13 control registers includes the following control bits:

- Invert divider output. Enables the user to choose between normal polarity and inverted polarity. Normal polarity is the default state. Inverted polarity reverses the representation of Logic 0 and Logic 1, regardless of the logic family.
- Ignore sync. Makes the divider ignore the $\overline{\text{SYNC}}$ signal from any source.
- Power down channel. Powers down the entire channel.
- Lower power mode.
- Driver mode.
- Channel divider.
- Divider phase.

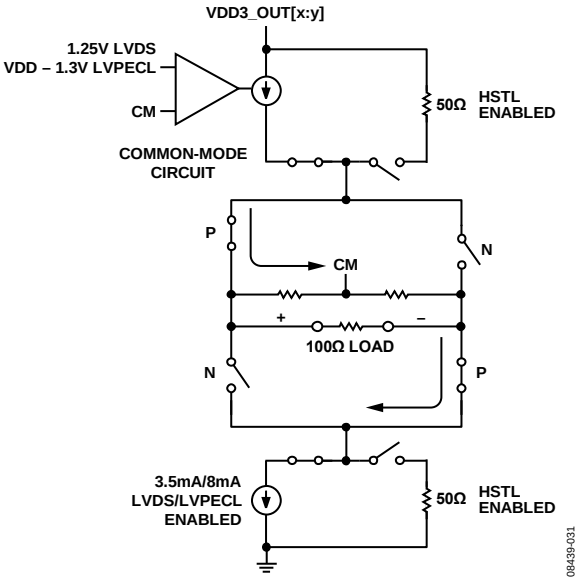


Figure 26. Multimode Driver

Clock Distribution Synchronization

A block diagram of the clock distribution synchronization functionality is shown in Figure 27. The synchronization sequence begins with the primary synchronization signal, which ultimately results in delivery of a synchronization strobe to the clock distribution logic.

As indicated, the primary synchronization signal originates from one of the following sources:

- Direct synchronization source via the sync dividers bit (see Register 0x232[0] in Table 55)
- Device pin, $\overline{\text{SYNC}}$ (Pin 17)

An automatic synchronization of the divider is initiated the first time that PLL2 locks after a power-up or reset event. Subsequent lock/unlock events do not initiate a resynchronization of the distribution dividers unless they are preceded by a power-down or reset of the part. Both sources of the primary synchronization signal are logic OR'd; therefore, any one of them can synchronize the clock distribution output at any time.

When using the sync dividers bit, the user first sets and then clears the bit. The synchronization event is the clearing operation (that is, the Logic 1 to Logic 0 transition of the bit). The dividers are all automatically synchronized to each other when PLL2 is ready. The dividers support programmable phase offsets from 0 to 63 steps, in half periods of the input clock (for example, the VCO divider output clock). The phase offsets are incorporated in the dividers through a preset for the first output clock period of each divider. Phase offsets are sup-ported only by programming the initial phase and divide value and then issuing a sync to the distribution (automatically at startup or manually, if desired).

When using the $\overline{\text{SYNC}}$ pin (Pin 17), there are 11 VCO divider output pipe line delays plus one period of the clock from the rising edge of $\overline{\text{SYNC}}$ to the clock output. There is at least one extra VCO divider period of uncertainty because the $\overline{\text{SYNC}}$ signal and the VCO divider output are asynchronous.

In normal operation, the phase offsets are already programmed through the EEPROM or the SPI/I²C port before the AD9523 starts to provide outputs. Although the user cannot adjust the phase offsets while the dividers are operating, it is possible to adjust the phase of all the outputs together without powering down PLL1 and PLL2. This is accomplished by programming the new phase offset, using Register 0x192[7:2] (see Table 51) and then issuing a divider sync signal by using the $\overline{\text{SYNC}}$ pin or the sync dividers bit (Register 0x232[0]). All outputs that are not programmed to ignore the sync are disabled temporarily while the sync is active. Note that, if an output is used for the zero delay path, it also disappears momentarily. However, this is desirable because it ensures that all the synchronized outputs have a deterministic phase relationship with respect to the zero delay output and, therefore, also with respect to the input.

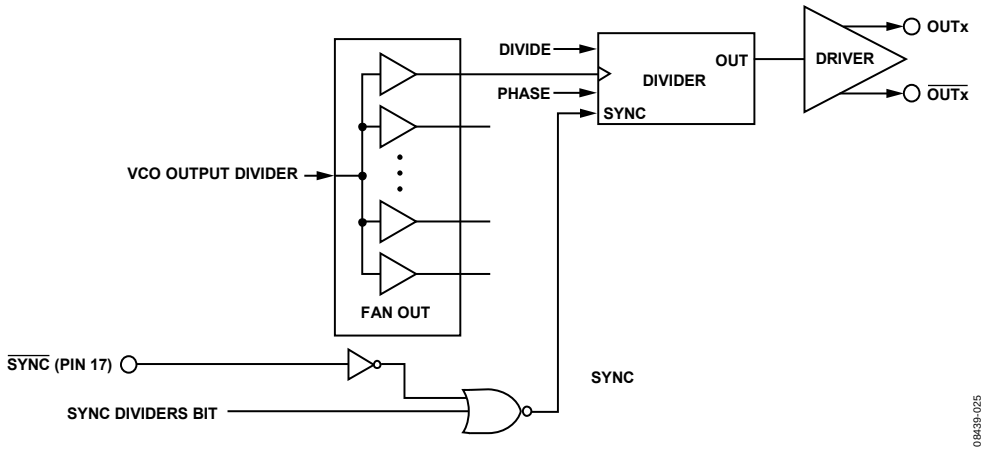


Figure 27. Clock Output Synchronization Block Diagram

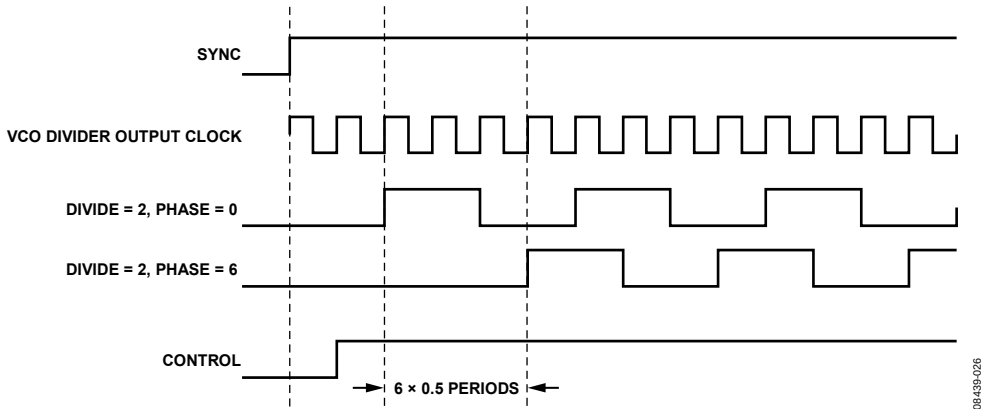


Figure 28. Clock Output Synchronization Timing Diagram

ZERO DELAY OPERATION

Zero delay operation aligns the phase of the output clocks with the phase of the external PLL reference input. The OUT0 output is designed to be used as the output for zero delay. There are two zero delay modes on the AD9523: internal and external (see Figure 29). Note that the external delay mode provides better matching than the internal delay mode because the output drivers are included in the zero delay path.

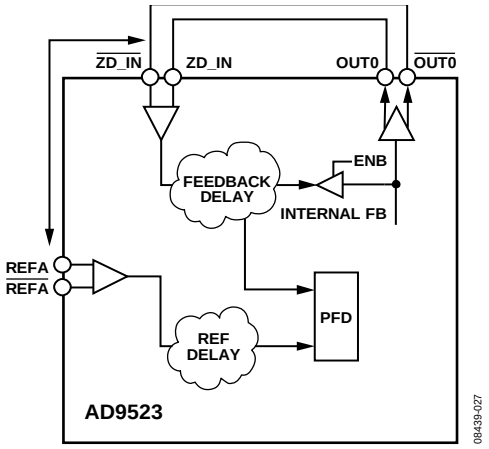


Figure 29. Zero Delay Function

Internal Zero Delay Mode

The internal zero delay function of the AD9523 is achieved by feeding the output of Channel Divider 0 back to the PLL1 N divider. Register 0x01B[5] is used to select internal zero delay mode (see Table 42). In the internal zero delay mode, the output of Channel Divider 0 is routed back to the PLL1 (N divider) through a mux. PLL1 synchronizes the phase/edge of the output of Channel Divider 0 with the phase/edge of the reference input.

Because the channel dividers are synchronized to each other, the outputs of the channel divider are synchronous with the reference input.

External Zero Delay Mode

The external zero delay function of the AD9523 is achieved by feeding OUT0 back to the ZD_IN input and, ultimately, back to the PLL1 N divider. In Figure 29, the change in signal routing for external zero delay is external to the AD9523.

Register 0x01B[5] is used to select the external zero delay mode. In external zero delay mode, OUT0 must be routed back to PLL1 (the N divider) through the ZD_IN and $\overline{\text{ZD_IN}}$ pins.

PLL1 synchronizes the phase/edge of the feedback output clock with the phase/edge of the reference input. Because the channel dividers are synchronized to each other, the clock outputs are synchronous with the reference input. Both the reference path delay and the feedback delay from ZD_IN are designed to have the same propagation delay from the output drivers and PLL components to minimize the phase offset between the clock output and the reference input to achieve zero delay.

LOCK DETECT

The PLL1 and PLL2 lock detectors issue an unlock condition when the frequency error is greater than the threshold of the lock detector. When the PLL is unlocked, there is a random phase between the reference clock and feedback clock. Due to the random phase relationship that exists, the unlock condition can take between $2^{15} \times T_{PFD}$ cycles to $1 \times T_{PFD}$ cycles. A lock condition always takes $2^{16} \times T_{PFD}$ to lock, but can potentially take $2^{31} \times T_{PFD}$ cycles depending on how big the phase jump is and when it occurs in relation to the lock detect restart.

RESET MODES

The AD9523 has a power-on reset (POR) and several other ways to apply a reset condition to the chip.

Power-On Reset

During chip power-up, a power-on reset pulse is issued when the 3.3 V supply reaches ~2.6 V (<2.8 V) and restores the chip either to the setting stored in the EEPROM (EEPROM pin = 1) or to the on-chip setting (EEPROM pin = 0). At power-on, the AD9523 executes a sync operation, which brings the outputs into phase alignment according to the default settings. The output drivers are held in sync for the duration of the internally generated power-up sync timer (~70 ms). The outputs begin to toggle after this period.

Reset via the $\overline{\text{RESET}}$ Pin

$\overline{\text{RESET}}$, a reset (an asynchronous hard reset is executed by briefly pulling $\overline{\text{RESET}}$ low), restores the chip either to the setting stored in the EEPROM (EEPROM pin = 1) or to the on-chip setting (EEPROM pin = 0). A reset also executes a sync operation, which brings the outputs into phase alignment according to the default settings. When the EEPROM is inactive (EEPROM pin = 0), it takes ~2 µs for the outputs to begin toggling after $\overline{\text{RESET}}$ is issued. When the EEPROM is active (EEPROM pin = 1), it takes ~40 ms for the outputs to toggle after $\overline{\text{RESET}}$ is brought high.

Reset via the Serial Port

The serial port control register allows for a reset by setting Bit 2 and Bit 5 in Register 0x000. When Bit 2 and Bit 5 are set, the chip enters a reset mode and restores the chip either to the setting stored in the EEPROM (EEPROM pin = 1) or to the on-chip setting (EEPROM pin = 0), except for Register 0x000. Except for the self-clearing bits, Bit 2 and Bit 5, Register 0x000 retains its previous value prior to reset. During the internal reset, the outputs hold static. Bit 2 and Bit 5 are self-clearing. However, the self-clearing operation does not complete until an additional serial port SCLK cycle completes, and the AD9523 is held in reset until Bit 2 and Bit 5 self-clear.

Reset to Settings in EEPROM when EEPROM Pin = 0 via the Serial Port

The serial port control register allows the chip to be reset to settings in the EEPROM when the EEPROM pin = 0 via Register 0xB02[1]. This bit is self-clearing. This bit does not have any effect when the EEPROM pin = 1. It takes ~40 ms for the outputs to begin toggling after the SOFT_EEPROM register is cleared.

POWER-DOWN MODE

Chip Power-Down via $\overline{PD}$

Place the AD9523 into a power-down mode by pulling the $\overline{PD}$ pin low. Power-down turns off most of the functions and currents inside the AD9523. The chip remains in this power-down state until $\overline{PD}$ is returned to a logic high state. When taken out of power-down mode, the AD9523 returns to the settings programmed into its registers prior to the power-down, unless the registers are changed by new programming while the $\overline{PD}$ pin is held low.

POWER SUPPLY SEQUENCING

The AD9523 has multiple power supply domains that operate with 3.3 V, and the output supply domain that operates on 1.8 V. To ensure proper device operation, bring the 1.8 V supplies high and stable prior to or simultaneously with the 3.3 V supplies. It is recommended to hold the $\overline{RESET}$ pin low while both supply domains settle to ensure that the 3.3 V supplies do not lead the 1.8 V supplies.

SERIAL CONTROL PORT

The AD9523 serial control port is a flexible, synchronous serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. The AD9523 serial control port is compatible with most synchronous transfer formats, including I²C, Motorola® SPI, and Intel® SSR protocols. The AD9523 I²C implementation deviates from the classic I²C specification in two specifications, and these deviations are documented in Table 16. The serial control port allows read/write access to all registers that configure the AD9523.

SPI/I²C PORT SELECTION

The AD9523 has two serial interfaces, SPI and I²C. Users can select either the SPI or I²C depending on the states (logic high, logic low) of the two logic level input pins, SP1 and SP0, when power is applied or after a $\overline{\text{RESET}}$ (each pin has an internal 40 kΩ pull-down resistor). When both SP1 and SP0 are low, the SPI interface is active. Otherwise, I²C is active with three different I²C slave address settings (seven bits wide), as shown in Table 22. The five MSBs of the slave address are hardware coded as 11000, and the two LSBs are determined by the logic levels of the SP1 and SP0 pins.

Table 22. Serial Port Mode Selection

SP1	SP0	Address
Low	Low	SPI
Low	High	I²C: 1100000
High	Low	I²C: 1100001
High	High	I²C: 1100010

I²C SERIAL PORT OPERATION

The AD9523 I²C port is based on the I²C fast mode standard. The AD9523 supports both I²C protocols: standard mode (100 kHz) and fast mode (400 kHz).

The AD9523 I²C port has a 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). In an I²C bus system, the AD9523 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device, meaning that no clock is generated by the AD9523. The AD9523 uses direct 16-bit (two bytes) memory addressing instead of traditional 8-bit (one byte) memory addressing.

I²C Bus Characteristics

Table 23. I²C Bus Definitions

Abbreviation	Definition
S	Start
Sr	Repeated start
P	Stop
A	Acknowledge
$\overline{\text{A}}$	No acknowledge
W	Write
R	Read

One pulse on the SCL clock line is generated for each data bit that is transferred.

The data on the SDA line must not change during the high period of the clock. The state of the data line can change only when the clock on the SCL line is low.

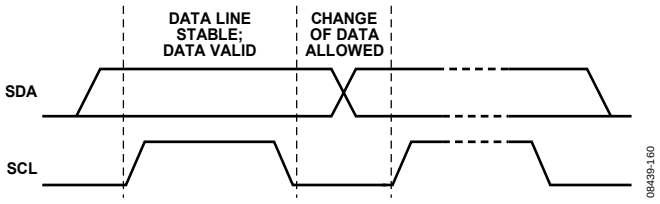


Figure 30. Valid Bit Transfer

A start condition is a transition from high to low on the SDA line while SCL is high. The start condition is always generated by the master to initialize the data transfer.

A stop condition is a transition from low to high on the SDA line while SCL is high. The stop condition is always generated by the master to end the data transfer.

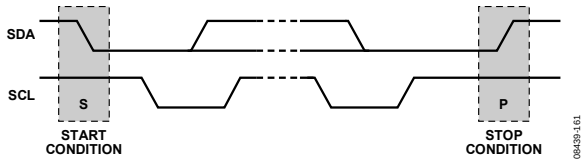


Figure 31. Start and Stop Conditions

A byte on the SDA line is always eight bits long. An acknowledge bit must follow every byte. Bytes are sent MSB first.

The acknowledge bit is the ninth bit attached to any 8-bit data byte. An acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has been received. The acknowledge bit is accomplished by pulling the SDA line low during the ninth clock pulse after each 8-bit data byte.

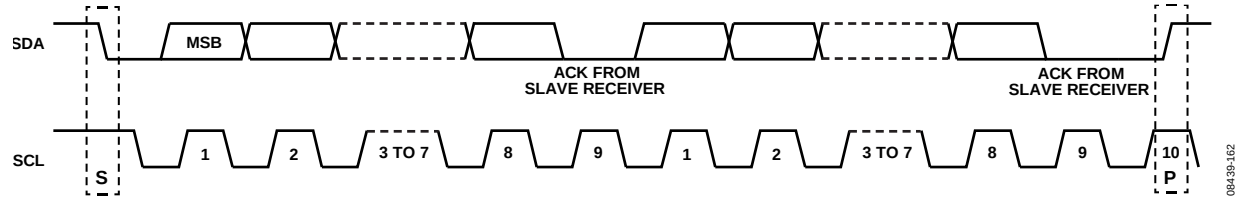


Figure 32. Data Transfer Process (Master Write Mode, 2-Byte Transfer)

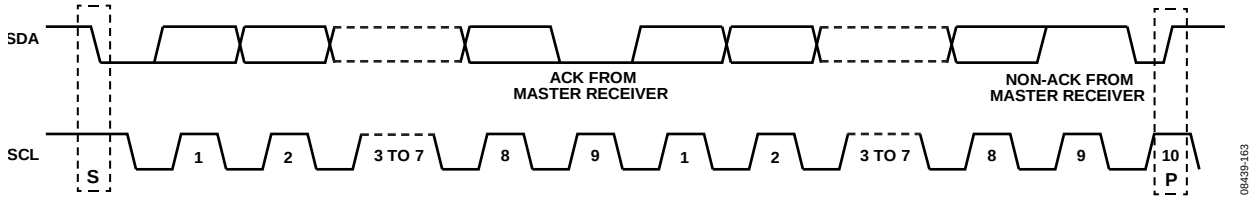


Figure 33. Data Transfer Process(Master Read Mode, 2-Byte Transfer)

The no acknowledge bit is the ninth bit attached to any 8-bit data byte. A no acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has not been received. The no acknowledge bit is accomplished by leaving the SDA line high during the ninth clock pulse after each 8-bit data byte.

Data Transfer Process

The master initiates data transfer by asserting a start condition, which indicates that a data stream follows. All I²C slave devices connected to the serial bus respond to the start condition.

The master then sends an 8-bit address byte over the SDA line, consisting of a 7-bit slave address (MSB first), plus a R/$\overline{W}$ bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 is write, 1 is read).

The peripheral whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master (transmitter) writes to the slave device (receiver). If the R/$\overline{W}$ bit is 1, the master (receiver) reads from the slave device (transmitter).

The format for these commands is described in the Data Transfer Format section.

Data is then sent over the serial bus in the format of nine clock pulses, one data byte (eight bits) from either master (write mode) or slave (read mode), followed by an acknowledge bit from the receiving device. The number of bytes that can be transmitted per transfer is unrestricted. In write mode, the first two data bytes immediately after the slave address byte are the internal memory (control registers) address bytes with the high address byte first. This addressing scheme gives a memory address of up to $2^{16} - 1 = 65,535$. The data bytes after these two memory address bytes are register data written into the control registers. In read mode, the data bytes after the slave address byte are register data read from the control registers. A single I²C transfer can contain multiple data bytes that can be read from or written to control registers whose address is automatically incremented starting from the base memory address.

When all data bytes are read or written, stop conditions are established. In write mode, the master (transmitter) asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the slave device (receiver). In read mode, the master device (receiver) receives the last data byte from the slave device (transmitter) but does not pull it low during the ninth clock pulse. This is known as a no acknowledge bit. Upon receiving the no acknowledge bit, the slave device knows that the data transfer is finished and releases the SDA line. The master then takes the data line low during the low period before the 10th clock pulse and high during the 10th clock pulse to assert a stop condition.

A repeated start (Sr) condition can be used in place of a stop condition. Furthermore, a start or stop condition can occur at any time, and partially transferred bytes are discarded.

For an I²C data write transfer containing multiple data bytes, the peripheral drives a no acknowledge for the data byte that follows a write to Register 0x234, thereby ending the I²C transfer. For an I²C data read transfer containing multiple data bytes, the peripheral drives data bytes of 0x00 for subsequent reads that follow a read from Register 0x234.

Data Transfer Format

Send byte format. The send byte protocol is used to set up the register address for subsequent commands.

S	Slave Address	W	A	RAM Address High Byte	A	RAM Address Low Byte	A	P

Write byte format. The write byte protocol is used to write a register address to the RAM, starting from the specified RAM address.

S	Slave Address	W	A	RAM Address High Byte	A	RAM Address Low Byte	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	A	P

Receive byte format. The receive byte protocol is used to read the data byte(s) from the RAM, starting from the current address.

S	Slave Address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

Read byte format. The combined format of the send byte and the receive byte.

S	Slave Address	W	A	RAM Address High Byte	A	RAM Address Low Byte	A	Sr	Slave Address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

I²C Serial Port Timing

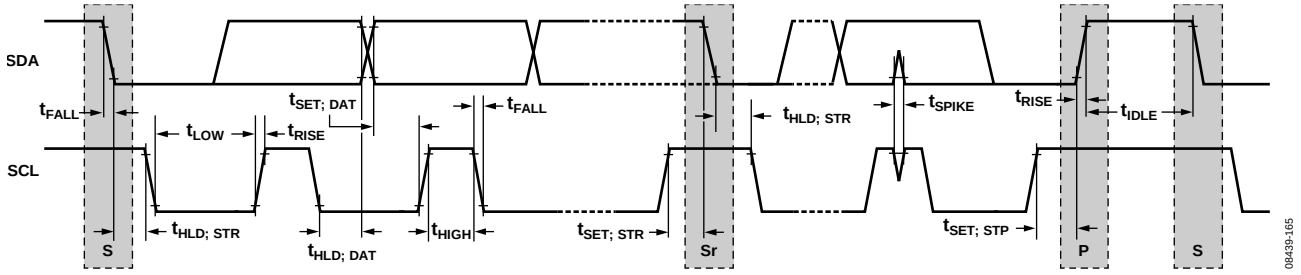


Figure 34. I²C Serial Port Timing

Table 24. I²C Timing Definitions

Parameter	Description
f_{I2C}	I²C clock frequency
t_{IDLE}	Bus idle time between stop and start conditions
$t_{HLD; STR}$	Hold time for repeated start condition
$t_{SET; STR}$	Setup time for repeated start condition
$t_{SET; STP}$	Setup time for stop condition
$t_{HLD; DAT}$	Hold time for data
$t_{SET; DAT}$	Setup time for data
t_{LOW}	Duration of SCL clock low
t_{HIGH}	Duration of SCL clock high
t_{RISE}	SCL/SDA rise time
t_{FALL}	SCL/SDA fall time
t_{SPIKE}	Voltage spike pulse width that must be suppressed by the input filter

SPI SERIAL PORT OPERATION

Pin Descriptions

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 40 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin and acts either as an input only (unidirectional mode) or as an input/output (bidirectional mode). The AD9523 defaults to the bidirectional input/output mode.

SDO (serial data out) is used only in the unidirectional input/output mode as a separate output pin for reading back data.

$\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, the SDO and SDIO pins enter a high impedance state. The $\overline{CS}$ pin is internally pulled up by a 40 kΩ resistor to VDD3_REF.

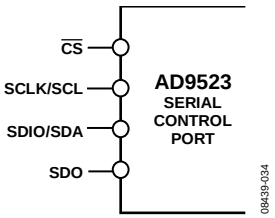


Figure 35. Serial Control Port

SPI Mode Operation

In SPI mode, single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9523 serial control port can be configured for a single bidirectional input/output pin (SDIO only) or for two unidirectional input/output pins (SDIO/SDO). By default, the AD9523 is in bidirectional mode. Short instruction mode (8-bit instructions) is not supported. Only long (16-bit) instruction mode is supported.

A write or a read operation to the AD9523 is initiated by pulling $\overline{CS}$ low.

The $\overline{CS}$ stalled high mode is supported in data transfers where three or fewer bytes of data (plus instruction data) are transferred (see Table 25). In this mode, the $\overline{CS}$ pin can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can go high only on byte boundaries; however, it can go high during either phase (instruction or data) of the transfer.

During this period, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset either by completing the remaining transfers or by returning $\overline{CS}$ low for at least one complete SCLK cycle (but fewer than eight SCLK cycles). Raising the $\overline{CS}$ pin on a nonbyte boundary terminates the serial transfer and flushes the buffer. In streaming mode (see Table 25), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the SPI MSB/LSB First Transfers section). $\overline{CS}$ must be raised at the end of the last byte to be transferred, thereby ending streaming mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9523. The first part writes a 16-bit instruction word into the AD9523, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9523 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation, the second part is the transfer of data into the serial control port buffer of the AD9523. Data bits are registered on the rising edge of SCLK.

The length of the transfer (one, two, or three bytes or streaming mode) is indicated by two bits (W1, W0) in the instruction byte. When the transfer is one, two, or three bytes but not streaming, $\overline{CS}$ can be raised after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Raising the $\overline{CS}$ pin on a nonbyte boundary resets the serial control port. During a write, streaming mode does not skip over reserved or blank registers, and the user can write 0x00 to the reserved register addresses.

Because data is written into a serial control port buffer area, and not directly into the actual control registers of the AD9523, an additional operation is needed to transfer the serial control port buffer contents to the actual control registers of the AD9523, thereby causing them to become active. The update registers operation consists of setting the self-clearing IO_UPDATE bit, Register 0x234[0] (see Table 57). Any number of data bytes can be changed before executing an update registers operation. The update registers simultaneously actuates all register changes that have been written to the buffer since any previous update.

Read

The AD9523 supports only the long instruction mode. If the instruction word is for a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by Bits[W1:W0]. If N = 4, the read operation is in streaming mode, continuing until $\overline{CS}$ is raised. During an SPI read, serial data on SDIO (or SDO in the case of 4-wire mode) transitions on the SCLK falling edge, and is normally sampled on the SCLK rising edge. To read the last bit correctly, the SPI host must be able to tolerate a zero hold time. In cases where zero hold time is not possible, the user can either use streaming mode and delay the rising edge of $\overline{CS}$, or sample the serial data on the SCLK falling edge. However, to sample the data correctly on the SCLK falling edge, the user must ensure that

the setup time is greater than t_{DV} (time data valid). Streaming mode does not skip over reserved or blank registers.

The default mode of the AD9523 serial control port is the bidirectional mode. In bidirectional mode, both the sent data and the readback data appear on the SDIO pin. It is also possible to set the AD9523 to unidirectional mode. In unidirectional mode, the readback data appears on the SDO pin.

A readback request reads the data that is in the serial control port buffer area or the data that is in the active registers (see Figure 36).

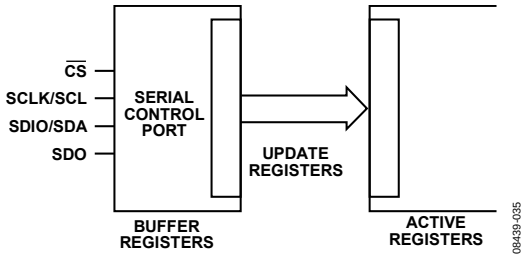


Figure 36. Relationship Between Serial Control Port Buffer Registers and Active Registers

SPI INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits ([W1:W0]) indicate the length of the transfer in bytes. The final 13 bits are the address ([A12:A0]) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits[W1:W0] (see Table 25).

Table 25. Byte Transfer Count

W1	W0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

Bits[A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. In MSB first mode, subsequent bytes decrement the address.

SPI MSB/LSB FIRST TRANSFERS

The AD9523 instruction word and byte data can be MSB first or LSB first. Any data written to Register 0x000 must be mirrored: Bit 7 is mirrored to Bit 0, Bit 6 to Bit 1, Bit 5 to Bit 2, and Bit 4 to Bit 3. This makes it irrelevant whether LSB first or MSB first is in effect. The default for the AD9523 is MSB first.

When LSB first is set by Register 0x000[1] and Register 0x000[6], it takes effect immediately because it affects only the operation of the serial control port and does not require that an update be executed.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first mode is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte, followed by multiple data bytes. In a multibyte transfer cycle, the internal byte address generator of the serial port increments for each byte.

The AD9523 serial control port register address decrements from the register address just written toward 0x000 for multibyte input/output operations if MSB first mode is active (default). If LSB first mode is active, the register address of the serial control port increments from the address just written toward 0x234 for multibyte input/output operations. Unused addresses are not skipped for these operations.

For multibyte accesses that cross Address 0x234 or Address 0x000 in MSB first mode, the SPI internally disables writes to subsequent registers and returns zeros for reads to subsequent registers.

Streaming mode always terminates when crossing address boundaries (as shown in Table 26).

Table 26. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
MSB First	Decrement	…, 0x001, 0x000, stop

Table 27. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

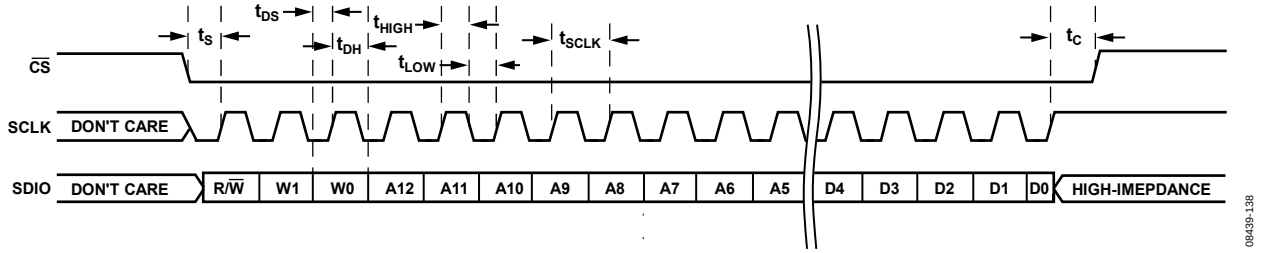


Figure 37. Serial Control Port Read—MSB First, 16-Bit Instruction, One Byte of Data

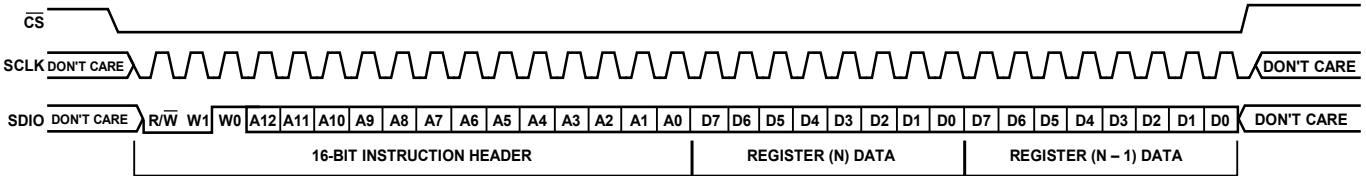


Figure 38. Serial Control Port Write—MSB First, 16-Bit Instruction, Two Bytes of Data

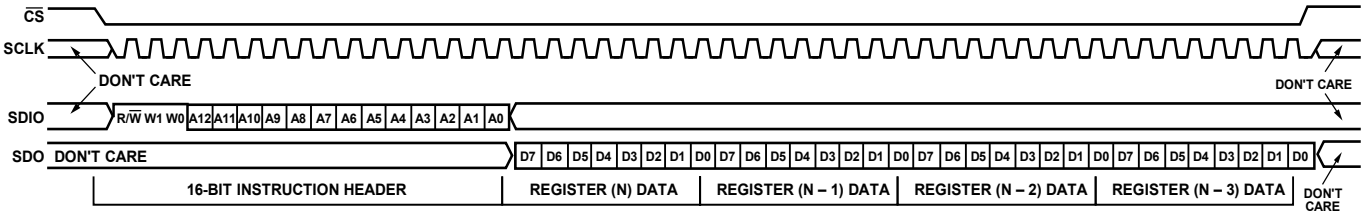


Figure 39. Serial Control Port Read—MSB First, 16-Bit Instruction, Four Bytes of Data

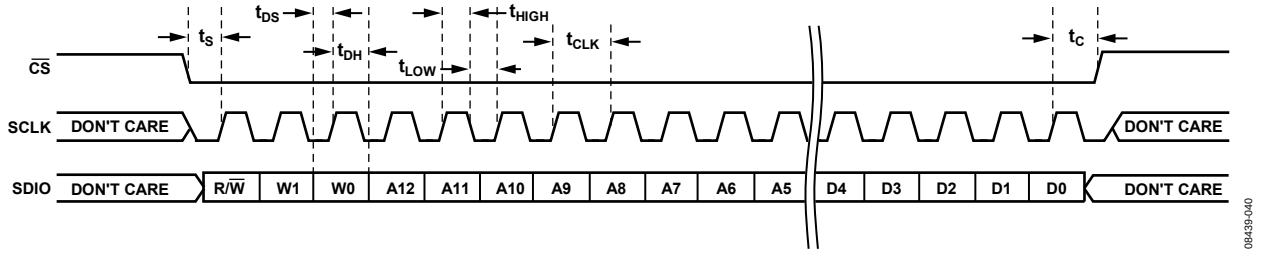


Figure 40. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

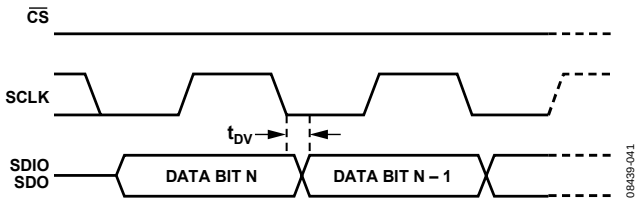


Figure 41. Timing Diagram for Serial Control Port Register Read

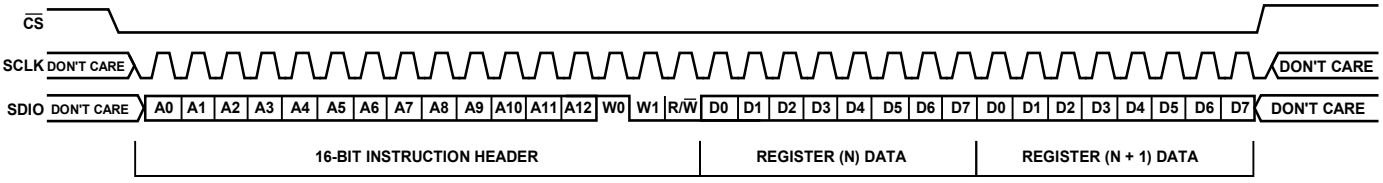


Figure 42. Serial Control Port Write—LSB First, 16-Bit Instruction, Two Bytes of Data

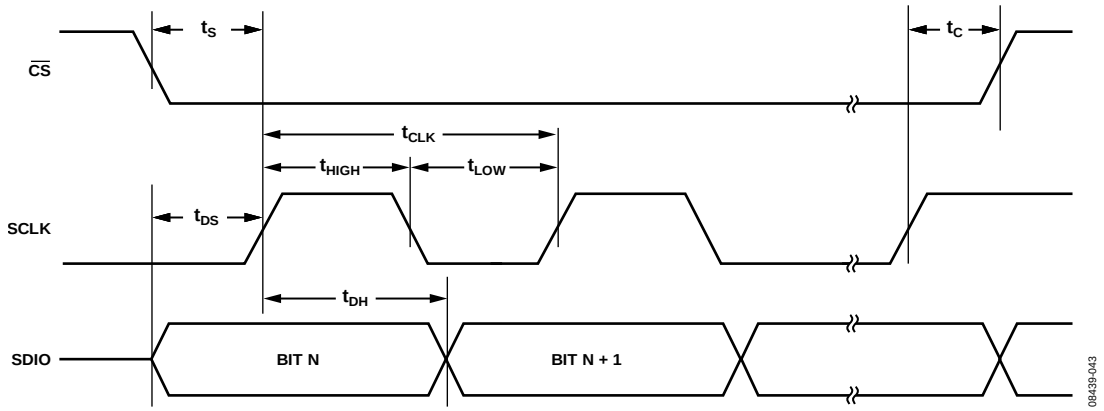


Figure 43. Serial Control Port Timing—Write

Table 28. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and SCLK rising edge (start of communication cycle)
t_C	Setup time between the SCLK rising edge and $\overline{CS}$ rising edge (end of communication cycle)
t_{HIGH}	Minimum period that SCLK should be in a logic high state
t_{LOW}	Minimum period that SCLK should be in a logic low state
t_{DV}	SCLK to valid SDIO and SDO (see Figure 41)

EEPROM OPERATIONS

The AD9523 contains an internal EEPROM (nonvolatile memory). The EEPROM can be programmed by the user to create and store a user-defined register setting file when the power is off. This setting file can be used for power-up and chip reset as a default setting. The EEPROM size is 512 bytes. Descriptions of the EEPROM registers that control EEPROM operation can be found in Table 58 and Table 59.

During the data transfer process, the write and read registers are generally not available via the serial port, except for one readback bit: STATUS_EEPROM (Register 0xB00[0]).

To determine the data transfer state through the serial port in SPI mode, users can read the value of the STATUS_EEPROM bit (1 = data transfer in process, and 0 = data transfer complete).

In I²C mode, the user can address the AD9523 slave port with the external I²C master (send an address byte to the AD9523). If the AD9523 responds with a no acknowledge bit, the data transfer was not received. If the AD9523 responds with an acknowledge bit, the data transfer process is complete. The user can monitor the STATUS_EEPROM bit or use Register 0x232[4] to program the STATUS0 pin to monitor the status of the data transfer (see Table 55).

To transfer all 512 bytes to the EEPROM, it takes approximately 46 ms. To transfer the contents of the EEPROM to the active register, it takes approximately 40 ms.

$\overline{\text{RESET}}$, a hard reset (an asynchronous hard reset is executed by briefly pulling $\overline{\text{RESET}}$ low), restores the chip either to the setting stored in the EEPROM (the EEPROM pin = 1) or to the on-chip setting (the EEPROM pin = 0). A hard reset also executes a SYNC operation, which brings the outputs into phase alignment according to the default settings. When the EEPROM is inactive (the EEPROM pin = 0), it takes ~2 µs for the outputs to begin toggling after $\overline{\text{RESET}}$ is issued. When the EEPROM is active (the EEPROM pin = 1), it takes ~40 ms for the outputs to toggle after $\overline{\text{RESET}}$ is brought high.

WRITING TO THE EEPROM

The EEPROM cannot be programmed directly through the serial port interface. To program the EEPROM and store a register setting file, follow these steps:

1. Program the AD9523 registers to the desired circuit state. If the user wants PLL2 to lock automatically after power-up, the calibrate VCO bit (Register 0x0F3[1]) must be set to 1. This allows VCO calibration to start automatically after register loading. Note that a valid input reference signal must be present during VCO calibration.
2. Program the EEPROM buffer registers to the necessary settings as described in the Programming the EEPROM Buffer Segment section.
3. Set the enable EEPROM write bit (Register 0xB02[0]) to 1 to enable the EEPROM.
4. Set the REG2EEPROM bit (Register 0xB03[0]) to 1.
5. Set the IO_UPDATE bit (Bit 0, Register 0x234[0]) to 1. This starts the process of writing data into the EEPROM to create the EEPROM setting file. This enables the EEPROM controller to transfer the current register values, as well as the memory address and instruction bytes from the EEPROM buffer segment, into the EEPROM. After the write process is completed, the internal controller sets the REG2EEPROM bit back to 0.
6. The STATUS_EEPROM bit (Register 0xB00[0]) indicates the data transfer status between the EEPROM and the control registers (1 = data transfer in process, and 0 = data transfer complete). At the beginning of the data transfer, the STATUS_EEPROM bit is set to 1 by the EEPROM controller and cleared to 0 at the end of the data transfer. The user can access STATUS_EEPROM via the STATUS0 pin when the STATUS0 pin is programmed to monitor the STATUS_EEPROM bit. Alternatively, the user can monitor the STATUS_EEPROM bit directly.
7. When the data transfer is complete (STATUS_EEPROM = 0), set the enable EEPROM write bit (Register 0xB02[0]) to 0. Clearing the enable EEPROM write bit to 0 disables writing to the EEPROM.

To ensure that the data transfer has completed correctly, verify that the EEPROM data error bit (Register 0xB0[0]) is 0. A value of 1 in this bit indicates a data transfer error. When an EEPROM save/load transfer is complete, wait a minimum of 10 µs before starting the next EEPROM save/load transfer.

READING FROM THE EEPROM

The following reset related events can start the process of restoring the settings stored in the EEPROM to the control registers. When the EEPROM_SEL pin is set high, do any of the following to initiate an EEPROM read:

1. Power up the AD9523.
2. Perform a hardware chip reset by pulling the $\overline{\text{RESET}}$ pin low and then releasing $\overline{\text{RESET}}$.
3. Set the self clearing soft reset bit (Bit 5, Register 0x000) to 1.

When the EEPROM_SEL pin is set low, set the self clearing SOFT_EEPROM bit (Register 0xB02[1]) to 1. The AD9523 then starts to read the EEPROM and loads the values into the AD9523 registers. If the EEPROM_SEL pin is low during reset or power-up, the EEPROM is not active, and the AD9523 default values are loaded instead.

When using the EEPROM to automatically load the AD9523 register values and lock the PLL, the calibrate VCO bit (Register 0x0F3[1]) must be set to 1 when the register values are written to the EEPROM. This allows VCO calibration to start automatically after register loading. A valid input reference signal must be present during VCO calibration.

To ensure that the data transfer has completed correctly, verify that the EEPROM data error bit (Register 0xB0[0]) is set to 0.

A value of 1 in this bit indicates a data transfer error. When an EEPROM save/load transfer is complete, wait a minimum of 10 µs before starting the next EEPROM save/load transfer.

PROGRAMMING THE EEPROM BUFFER SEGMENT

The EEPROM buffer segment is a register space that allows the user to specify which groups of registers are stored to the EEPROM during EEPROM programming. Normally, this segment does not need to be programmed by the user. The default power-up values for the EEPROM buffer segment allow the user to store all of the register values from Register 0x000 to Register 0x234 to the EEPROM.

For example, if the user wants to load only the output driver settings from the EEPROM without disturbing the PLL register settings currently stored in the EEPROM, the EEPROM buffer segment can be modified to include only the registers that apply to the output drivers and exclude the registers that apply to the PLL configuration.

There are two parts to the EEPROM buffer segment: register section definition groups and operational codes. Each register section definition group contains the starting address and number of bytes to be written to the EEPROM. Note that any register within the EEPROM buffer segment can be defined as a part of a definition group or an operational code.

If the AD9523 register map were continuous from Address 0x000 to Address 0x234, only one register section definition group would consist of a starting address of 0x000 and a length of 563 bytes. However, the AD9523 register map is noncontiguous, and the EEPROM is only 512 bytes long. Therefore, the register section definition group tells the EEPROM controller how the AD9523 register map is segmented.

There are three operational codes: IO_UPDATE, end-of-data, and pseudo-end-of-data. It is important that the EEPROM buffer segment always have either an end-of-data or a pseudo-end-of-data operational code and that an IO_UPDATE operation code appear at least once before the end-of-data operational code.

Register Section Definition Group

The register section definition group is used to define a continuous register section for the EEPROM profile. It consists of three bytes. The first byte defines how many continuous register bytes are in this group. If the user inputs 0x000 in the first byte, it means there is only one byte in this group. If the user inputs 0x001, it means there are two bytes in this group. The maximum number of registers in one group is 128.

The next two bytes are the high byte and low byte of the memory address (16 bits) of the first register in this group.

IO_UPDATE (Operational Code 0x80)

The EEPROM controller uses this operational code to generate an IO_UPDATE signal to update the active control register bank from the buffer register bank during the download process.

At a minimum, there should be at least one IO_UPDATE operational code after the end of the final register section definition group. This is needed so that at least one IO_UPDATE occurs after all of the AD9523 registers are loaded when the EEPROM is read. If this operational code is absent during a write to the EEPROM, the register values loaded from the EEPROM are not transferred to the active register space, and these values do not take effect after they are loaded from the EEPROM to the AD9523.

End-of-Data (Operational Code 0xFF)

The EEPROM controller uses the end-of-data operational code to terminate the data transfer process between EEPROM and the control register during the upload and download process. The last item appearing in the EEPROM buffer segment should be either this operational code or the pseudo-end-of-data operational code.

Pseudo-End-of-Data (Operational Code 0xFE)

The AD9523 EEPROM buffer segment has 23 bytes that can contain up to seven register section definition groups. If the user wants to define more than seven register section definition groups, the pseudo-end-of-data operational code can be used. During the upload process, when the EEPROM controller receives the pseudo-end-of-data operational code, it halts the data transfer process, clears the REG2EEPROM bit (Bit 0, Register 0xB03), and enables the AD9523 serial port. The user can then program the EEPROM buffer segment again and reinitiate the data transfer process by setting the REG2EEPROM bit to 1 and the IO_UPDATE bit (Bit 0, Register 0x234) to 1. The internal I^2C master then begins writing to the EEPROM, starting from the EEPROM address held from the last writing.

This sequence enables more discrete instructions to be written to the EEPROM than would otherwise be possible due to the limited size of the EEPROM buffer segment. It also permits the user to write to the same register multiple times with a different value each time.

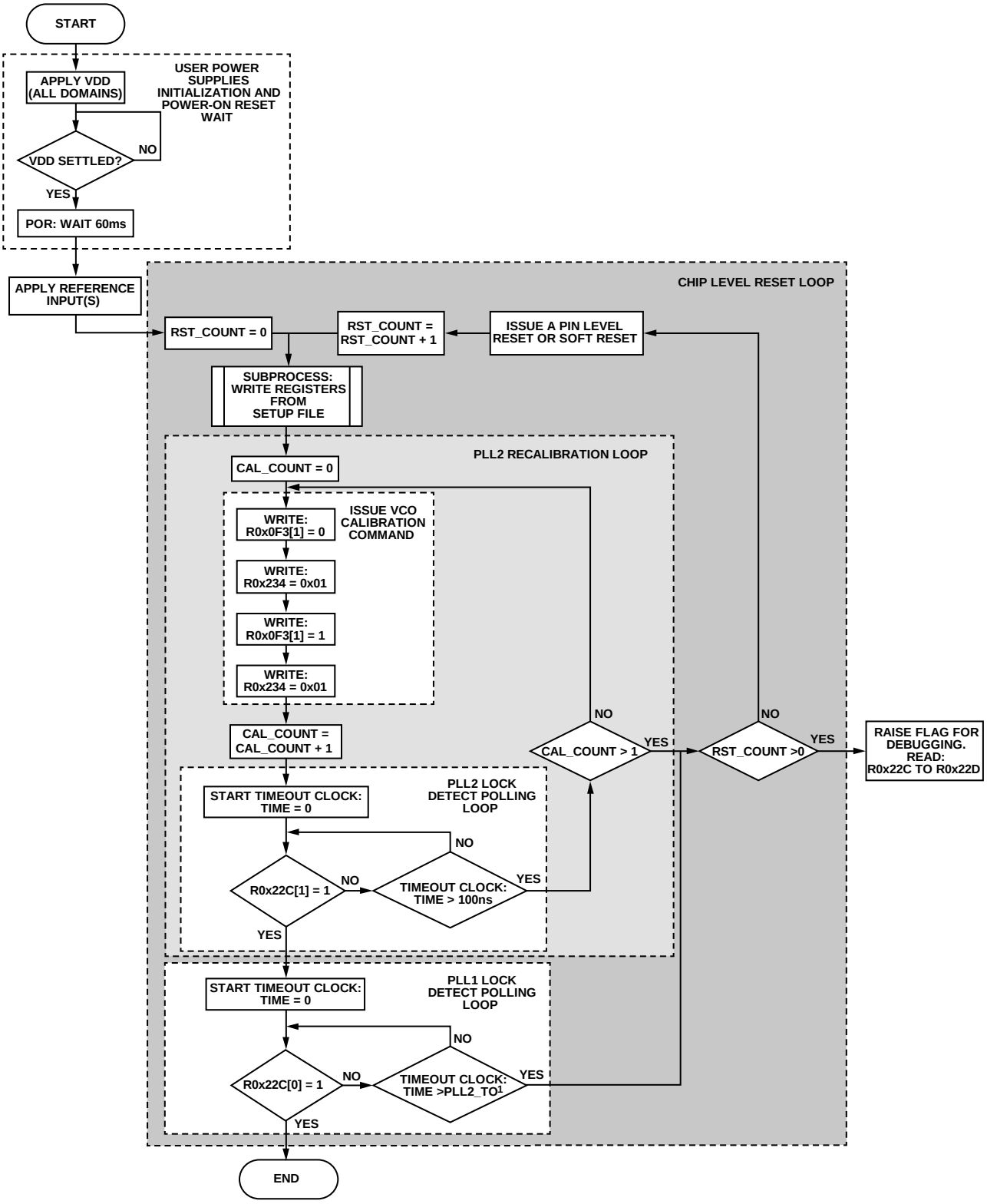
Table 29. Example of an EEPROM Buffer Segment

Register Address (Hex)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Start EEPROM Buffer Segment								
0xA00	0	Number of bytes of the first group of registers (Bits[6:0])						
0xA01	Address of the first group of registers (Bits[15:8])							
0xA02	Address of the first group of registers (Bits[7:0])							
0xA03	0	Number of bytes of the second group of registers (Bits[6:0])						
0xA04	Address of the second group of registers (Bits[15:8])							
0xA05	Address of the second group of registers (Bits[7:0])							
0xA06	0	Number of bytes of the third group of registers (Bits[6:0])						
0xA07	Address of the third group of registers (Bits[15:8])							
0xA08	Address of the third group of registers (Bits[7:0])							
0xA09	IO_UPDATE operational code (0x80)							
0xA0A	End-of-data operational code (0xFF)							

DEVICE INITIALIZATION FLOW CHARTS

The flowcharts in this section show a typical AD9523 initialization routine using an evaluation software generated setup file (.stp) and calibration routines designed for robust system startup. Other valid start up sequences exist and, as such, these flow charts are provided as recommendations.

The count variables (RST_COUNT and CAL_COUNT) in the AD9523 device initialization flow chart act as system level count limits for the loop to prevent an infinite loop. These count variables are not AD9523 device settings or status readbacks.



[1]PLL2_TO IS A CALCULATED TIMEOUT VALUE. SEE THE THEORY OF OPERATION, COMPONENT BLOCKS—INPUT PLL (PLL1) FOR ITS FORMULA.

Figure 44. AD9523 Device Initialization

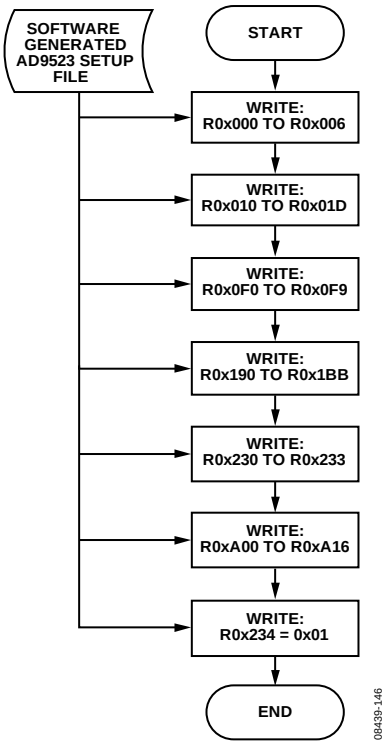


Figure 45. Subprocess: Write Registers from Setup File

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9523 is a multifunctional, high speed device that targets a wide variety of clock applications. The numerous innovative features contained in the device each consume incremental power. If all outputs are enabled in the maximum frequency and mode that have the highest power, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management are critical elements in the proper application of the AD9523 device.

The AD9523 device is specified to operate within the industrial temperature range of −40°C to +85°C. This specification is conditional, however, such that the absolute maximum junction temperature is not exceeded (as specified in Table 17). At high operating temperatures, extreme care must be taken when operating the device to avoid exceeding the junction temperature and potentially damaging the device.

A maximum junction temperature is listed in Table 1 with the ambient operating range. The ambient range and maximum junction temperature specifications ensure the performance of the device, as guaranteed in the Specifications section.

Many variables contribute to the operating junction temperature within the device, including

- Selected driver mode of operation
- Output clock speed
- Supply voltage
- Ambient temperature

The combination of these variables determines the junction temperature within the AD9523 device for a given set of operating conditions.

The AD9523 is specified for an ambient temperature (T_A). To ensure that T_A is not exceeded, an airflow source can be used.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the user at the top center of the package.
Ψ_{JT} is the value from Table 18.
PD is the power dissipation of the AD9523.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of Ψ_{JB} are provided for package comparison and PCB design considerations.

CLOCK SPEED AND DRIVER MODE

Clock speed directly and linearly influences the total power dissipation of the device and, therefore, the junction temperature. Two operating frequencies are listed under the incremental power dissipation parameter in Table 3. Using linear interpretation is a sufficient approximation for frequencies not listed in the table. When calculating power dissipation for thermal consideration, the amount of power dissipated in the 100 Ω resistor must be removed. If using the data in Table 2, this power is already removed. If using the current vs. frequency graphs provided in the Typical Performance Characteristics section, the power into the load must be subtracted, using the following equation:

$$\frac{Differential\ \ Output\ Voltage\ Swing^2}{100\ \Omega}$$

EVALUATION OF OPERATING CONDITIONS

The first step in evaluating the operating conditions is to determine the maximum power consumption (PD) internal to the AD9523. The maximum PD excludes power dissipated in the load resistors of the drivers because such power is external to the device. Use the power dissipation specifications listed in Table 3 to calculate the total power dissipated for the desired configuration. The base typical configuration parameter in Table 3 lists a power of 428 mW, which includes one LVPECL output at 122.88 MHz. If the frequency of operation is not listed in Table 3, see the Typical Performance Characteristics section, current vs. frequency and driver mode to calculate the power dissipation; then add 20% for maximum current draw. Remove the power dissipated in the load resistor to achieve the most accurate power dissipation internal to the AD9523. See Table 30 for a summary of the incremental power dissipation from the base power configuration for two different examples.

Table 30. Temperature Gradient Examples

Description	Mode	Frequency (MHz)	Maximum Power (mW)
Example 1			
Base Typical Configuration			428
Output Driver	6 × LVPECL	122.88	330
Output Driver	6 × LVDS	245.76	110
Total Power			868
Example 2			
Base Typical Configuration			428
Output Driver	13 × LVPECL	983.04	2066
Total Power			2500

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient. For this example, a thermal impedance of θ_{JA} = 20.1°C/W was used.

Example 1

(868 mW × 20.1°C/W) = 17.4°C

With an ambient temperature of 85°C, the junction temperature is

T_J = 85°C + 17.4°C = 102°C

This junction temperature is below the maximum allowable.

Example 2

(2500 mW × 20.1°C/W) = 50.2°C

With an ambient temperature of 85°C, the junction temperature is

T_J = 85°C + 50°C = 135°C

This junction temperature exceeds the maximum allowable range. To operate in the condition of Example 2, the ambient temperature must be lowered to 65°C.

THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES

See the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, for more information about mounting devices with an exposed paddle.

CONTROL REGISTERS

CONTROL REGISTER MAP

Register addresses that are not listed in Table 31 are not used, and writing to those registers has no effect. Registers that are marked as reserved must never have their values changed. When writing to registers with bits that are marked reserved, the user must take care to always write the default value for the reserved bits.

Table 31. Control Register Map

Addr (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
Serial Port Configuration										
0x000	SPI mode serial port configuration	SDO active	LSB first/ address increment	Soft reset	Reserved	Reserved	Soft reset	LSB first/ address increment	SDO active	0x00
	I^2C mode serial port configuration	Reserved	Reserved	Soft reset	Reserved	Reserved	Soft reset	Reserved	Reserved	0x00
0x004	Readback control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Read back active registers	0x00
0x005	EEPROM customer version ID	EEPROM customer version ID[7:0] (LSB)								0x00
0x006		EEPROM customer version ID[15:8] (MSB)								0x00
Input PLL (PLL1)										
0x010	PLL1 REFA R divider control	10-bit REFA R divider[7:0] (LSB)								0x00
0x011		Reserved						10-bit REFA R divider[9:8] (MSB)		0x00
0x012	PLL1 REFB R divider control	10-bit REFB R divider[7:0] (LSB)								0x00
0x013		Reserved						10-bit REFB R divider[9:8] (MSB)		0x00
0x014	PLL1 reference test divider	Reserved	Reserved	REF_TEST divider						0x00
0x015	PLL1 reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x016	PLL1 feedback N divider control	10-bit PLL1 feedback divider[7:0] (LSB)								0x00
0x017		Reserved						10-bit PLL1 feedback divider[9:8] (MSB)		0x00
0x018	PLL1 charge pump control	PLL1 charge pump tristate	PLL1 charge pump control							0x0C
0x019		Reserved	Reserved	Reserved	Enable SPI control of antibacklash pulse width	Antibacklash pulse width control		PLL1 charge pump mode		0x00
0x01A	PLL1 input receiver control	REF_TEST input receiver enable	REFB differential receiver enable	REFA differential receiver enable	REFB receiver enable	REFA receiver enable	Input REFA, REFB receiver power-down control enable	$\overline{\text{OSC_IN}}$ single-ended receiver mode enable (CMOS mode)	OSC_IN differential receiver mode enable	0x00
0x01B	REF_TEST, REFA, REFB, and ZD_IN control	Reserved	Reserved	Zero delay mode	OSC_IN signal feedback for PLL1	$\overline{\text{ZD_IN}}$ single-ended receiver mode enable (CMOS mode)	ZD_IN differen. receiver mode enable	$\overline{\text{REFB}}$ single-ended receiver mode enable (CMOS mode)	$\overline{\text{REFA}}$ single-ended receiver mode enable (CMOS mode)	0x00
0x01C	PLL1 miscellaneous control	Enable REFB R divider independent division control	OSC_CTRL control voltage to $V_{CC}/2$ when ref clock fails	Reserved	Reference selection mode			Reserved	Reserved	0x00

Addr (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
0x01D	PLL1 loop filter zero resistor control	Reserved	Reserved	Reserved	Reserved	PLL1 loop filter, R_{ZERO}				0x00
0x01E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
Output PLL (PLL2)										
0x0F0	PLL2 charge pump control	PLL2 charge pump control								0x00
0x0F1	PLL2 feedback N divider control	A counter		B counter						0x04
0x0F2	PLL2 control	PLL2 lock detector power-down	Reserved	Enable frequency doubler	Enable SPI control of antibacklash pulse width	Antibacklash pulse width control		PLL2 charge pump mode		0x03
0x0F3	VCO control	Reserved	Reserved	Reserved	Force release of distribution sync when PLL2 is unlocked	Treat reference as valid	Force VCO to midpoint frequency	Calibrate VCO (not auto-clearing)	Reserved	0x00
0x0F4	VCO divider control	Reserved	Reserved	Reserved	Reserved	VCO divider power-down	VCO divider			0x00
0x0F5	PLL2 loop filter control (9 bits)	Pole 2 resistor (R_{POLE2})		Zero resistor (R_{ZERO})			Pole 1 capacitor (C_{POLE1})			0x00
0x0F6		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Bypass internal R_{ZERO} resistor	0x00
0x0F9 to 0x0FE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
Clock Distribution										
0x190	Channel 0 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x00
0x191		10-bit channel divider[7:0] (LSB)								0x1F
0x192		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x193	Channel 1 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x20
0x194		10-bit channel divider[7:0] (LSB)								0x1F
0x195		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x196	Channel 2 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x00
0x197		10-bit channel divider[7:0] (LSB)								0x1F
0x198		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x199	Channel 3 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x20
0x19A		10-bit channel divider[7:0] (LSB)								0x1F
0x19B		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x19C	Channel 4 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x00
0x19D		10-bit channel divider[7:0] (LSB)								0x1F
0x19E		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04

Addr (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
0x19F	Channel 5 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x20
0x1A0		10-bit channel divider[7:0] (LSB)								0x1F
0x1A1		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1A2	Channel 6 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x00
0x1A3		10-bit channel divider[7:0] (LSB)								0x1F
0x1A4		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1A5	Channel 7 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x20
0x1A6		10-bit channel divider[7:0] (LSB)								0x1F
0x1A7		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1A8	Channel 8 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x00
0x1A9		10-bit channel divider[7:0] (LSB)								0x1F
0x1AA		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1AB	Channel 9 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x20
0x1AC		10-bit channel divider[7:0] (LSB)								0x1F
0x1AD		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1AE	Channel 10 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x00
0x1AF		10-bit channel divider[7:0] (LSB)								0x1F
0x1B0		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1B1	Channel 11 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x20
0x1B2		10-bit channel divider[7:0] (LSB)								0x1F
0x1B3		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1B4	Channel 12 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x00
0x1B5		10-bit channel divider[7:0] (LSB)								0x1F
0x1B6		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1B7	Channel 13 control	Invert divider output	Ignore sync	Power-down channel	Lower power mode	Driver mode				0x20
0x1B8		10-bit channel divider[7:0] (LSB)								0x1F
0x1B9		Divider phase[5:0]						10-bit channel divider[9:8] (MSB)		0x04
0x1BA	PLL1 output control	Reserved	Reserved	Reserved	PLL1 output CMOS driver strength	Out PLL1 output				0x00
0x1BB	PLL1 output channel control	PLL1 output driver power-down	Reserved	Reserved	Reserved	Route VCXO clock to Ch 3 divider input	Route VCXO clock to Ch 2 divider input	Route VCXO clock to Ch 1 divider input	Route VCXO clock to Ch 0 divider input	0x80

Addr (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
Readback										
0x22C	Readback 0	Status PLL2 reference clock	Status PLL1 feedback clock	Status VCXO	Status REF_TEST	Status REFB	Status REFA	Lock detect PLL2	Lock detect PLL1	
0x22D	Readback 1	Reserved	Reserved	Reserved	Reserved	Holdover active	Selected reference (in auto mode)	Reserved	VCO calibration in progress	
0x22E	Readback 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0x22F	Readback 3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
Other										
0x230	Status signals	Reserved	Reserved	Status Monitor 0 control						0x00
0x231		Reserved	Reserved	Status Monitor 1 control						0x00
0x232		Reserved	Reserved	Reserved	Enable STATUS_ EEPROM on STATUS0 pin	STATUS1 pin divider enable	STATUS0 pin divider enable	Reserved	Sync dividers (manual control) 0: sync signal inactive 1: dividers held in sync (same as $\overline{\text{SYNC}}$ pin low)	0x00
0x233	Power-down control	Reserved	Reserved	Reserved	Reserved	Reserved	PLL1 power-down	PLL2 power-down	Distribution power-down	0x07
0x234	Update all registers	Reserved							IO_UPDATE	0x00
EEPROM Storage Sequence										
0xA00	Serial port configuration	EEPROM Buffer Segment Default Setting: Size of transfer: one byte								0x00
0xA01		EEPROM Buffer Segment Default Setting: Starting address 0x0000								0x00
0xA02										0x00
0xA03	Readback control and EEPROM customer version ID	EEPROM Buffer Segment Default Setting: Size of transfer: three bytes								0x02
0xA04		EEPROM Buffer Segment Default Setting: Starting address 0x0004								0x00
0xA05										0x04
0xA06	Input PLL (PLL1)	EEPROM Buffer Segment Default Setting: Size of transfer: 15 bytes								0x0E
0xA07		EEPROM Buffer Segment Default Setting: Starting address 0x0010								0x00
0xA08										0x10
0xA09	Output PLL (PLL2)	EEPROM Buffer Segment Default Setting: Size of transfer: 15 bytes								0x0E
0xA0A		EEPROM Buffer Segment Default Setting: Starting address 0x00F0								0x00
0xA0B										0xF0
0xA0C	Clock distribution	EEPROM Buffer Segment Default Setting: Size of transfer: 44 bytes								0x2B
0xA0D		EEPROM Buffer Segment Default Setting: Starting address 0x0190								0x01
0xA0E										0x90
0xA0F	Clock input and REF	EEPROM Buffer Segment Default Setting: Size of transfer: two bytes								0x01
0xA10		EEPROM Buffer Segment Default Setting: Starting address 0x01E0								0x01
0xA11										0xE0
0xA12	Other	EEPROM Buffer Segment Default Setting: Size of transfer: four bytes								0x03
0xA13		EEPROM Buffer Segment Default Setting: Starting address 0x0230								0x02
0xA14										0x30
0xA15	IO_UPDATE	EEPROM Buffer Segment Default Setting: Command: IO_UPDATE								0x80
0xA16	End of data	EEPROM Buffer Segment Default Setting: Command: End of data								0xFF

Addr (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
EEPROM Control										
0xB00	STATUS_ EEPROM (read only)	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STATUS_ EEPROM (read only)	0x00
0xB01	EEPROM error checking readback (read only)	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EEPROM data error (read only)	0x00
0xB02	EEPROM Control 1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SOFT_ EEPROM	Enable EEPROM write	0x00
0xB03	EEPROM Control 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REG2EEPROM	0x00

CONTROL REGISTER MAP BIT DESCRIPTIONS

Serial Port Configuration (Address 0x000 to Address 0x006)

Table 32. SPI Mode Serial Port Configuration

Address	Bits	Bit Name	Description
0x000	7	SDO active	Selects unidirectional or bidirectional data transfer mode. This bit is ignored in I²C mode. 0: SDIO pin used for write and read; SDO is high impedance (default). 1: SDO used for read; SDIO used for write; unidirectional mode.
	6	LSB first/ address increment	SPI MSB or LSB data orientation. This bit is ignored in I²C mode. 0: data-oriented MSB first; addressing decrements (default). 1: data-oriented LSB first; addressing increments.
	5	Soft reset	Soft reset. 1 (self-clearing): soft reset; restores default values to internal registers.
	4	Reserved	Reserved.
	[3:0]	Mirror[7:4]	Bits[3:0] should always mirror Bits[7:4] so that it does not matter whether the part is in MSB first or LSB first mode (see Register 0x000[6]). Set bits as follows: Bit 0 = Bit 7. Bit 1 = Bit 6. Bit 2 = Bit 5. Bit 3 = Bit 4.
0x004	0	Readback active registers	For buffered registers, serial port readback reads from actual (active) registers instead of from the buffer. 0 (default): reads values currently applied to the internal logic of the device. 1: reads buffered values that take effect on the next assertion of the input/output update.

Table 33. I²C Mode Serial Port Configuration

Address	Bits	Bit Name	Description
0x000	[7:6]	Reserved	Reserved.
	5	Soft reset	Soft reset. 1 (self-clearing): soft reset; restores default values to internal registers.
	4	Reserved	Reserved.
	[3:0]	Mirror[7:4]	Bits[3:0] should always mirror Bits[7:4]. Set bits as follows: Bit 0 = Bit 7. Bit 1 = Bit 6. Bit 2 = Bit 5. Bit 3 = Bit 4.
0x004	0	Read back active registers	For buffered registers, serial port readback reads from actual (active) registers instead of from the buffer. 0 (default): reads values currently applied to the internal logic of the device. 1: reads buffered values that take effect on the next assertion of the input/output update.

Table 34. EEPROM Customer Version ID

Address	Bits	Bit Name	Description
0x005	[7:0]	EEPROM customer version ID (LSB)	16-bit EEPROM ID, Bits[7:0]. This register, along with Register 0x006, allows the user to store a unique ID to identify which version of the AD9523 register settings is stored in the EEPROM. It does not affect AD9523 operation in any way (default: 0x00).
0x006	[7:0]	EEPROM customer version ID (MSB)	16-bit EEPROM ID, Bits[15:8]. This register, along with Register 0x005, allows the user to store a unique ID to identify which version of the AD9523 register settings is stored in the EEPROM. It does not affect AD9523 operation in any way (default: 0x00).

Input PLL (PLL1) (Address 0x010 to Address 0x01D)

Table 35. PLL1 REFA R Divider Control

Address	Bits	Bit Name	Description
0x010	[7:0]	REFA R divider	10-bit REFA R divider, Bits[7:0] (LSB). Divide-by-1 to divide-by-1023. 00000000, 00000001: divide-by-1.
0x011	[1:0]	REFA R divider	10-bit REFA R divider, Bits[9:8] (MSB).

Table 36. PLL1 REFB R Divider Control[1]

Address	Bits	Bit Name	Description
0x012	[7:0]	REFB R divider	10-bit REFB R divider, Bits[7:0] (LSB). Divide-by-1 to divide-by-1023. 00000000, 00000001: divide-by-1.
0x013	[1:0]	REFB R divider	10-bit REFB R divider, Bits[9:8] (MSB).

[1] Requires Register 0x01C[7] = 1b for division that is independent of REFA division.

Table 37. PLL1 Reference Test Divider

Address	Bits	Bit Name	Description
0x014	[7:6]	Reserved	Reserved
	[5:0]	REF_TEST divider	6-bit reference test divider. Divide-by-1 to divide-by-63. 000000, 000001: divide-by-1.

Table 38. PLL1 Reserved

Address	Bits	Bit Name	Description
0x015	[7:0]	Reserved	Reserved

Table 39. PLL1 Feedback N Divider Control

Address	Bits	Bit Name	Description
0x016	[7:0]	PLL1 feedback N divider control (N_PLL1)	10-bit feedback divider, Bits[7:0] (LSB). Divide-by-1 to divide-by-1023. 00000000, 00000001: divide-by-1.
0x017	[1:0]	PLL1 feedback N divider control (N_PLL1)	10-bit feedback divider, Bits[1:0] (MSB).

Table 40. PLL1 Charge Pump Control

Address	Bits	Bit Name	Description
0x018	7	PLL1 charge pump tristate	Tristates the PLL1 charge pump.
	[6:0]	PLL1 charge pump control	These bits set the magnitude of the PLL1 charge pump current. Granularity is ~0.5 µA with a full-scale magnitude of ~63.5 µA.
0x019	[7:5]	Reserved	Reserved.
	4	Enable SPI control of antibacklash pulse width	Setting this bit allows user control of the antibacklash pulse width setting in Register 0x019[3:2]. 0 (default): antibacklash period is forced to high. 1: antibacklash period defined by Register 0x019[3:2].
	[3:2]	Antibacklash pulse width control	Controls the PFD antibacklash period. These bits default to the high setting unless reprogrammed using Register 0x019[4] = 1b. The high setting decreases the maximum allowable PLL1 PFD rate. See Table 7 for ranges. 00: minimum. 01: low. 10: high (initial state unless changed via Register 0x019[4] = 1b). 11: maximum.
	[1:0]	PLL1 charge pump mode	Controls the mode of the PLL1 charge pump. 00 (default): tristate. 01: pump up. 10: pump down. 11: normal.

Table 41. PLL1 Input Receiver Control

Address	Bits	Bit Name	Description
0x01A	7	REF_TEST input receiver enable	1: enabled. 0: disabled (default).
	6	REFB differential receiver enable	1: differential receiver mode. 0: single-ended receiver mode (also depends on Register 0x01B[1]) (default).
	5	REFA differential receiver enable	1: differential receiver mode. 0: single-ended receiver mode (also depends on Register 0x01B[0]) (default).
	4	REFB receiver enable	REFB receiver power-down control mode only when Bit 2 = 1. 1: enable REFB receiver. 0: power down (default).
	3	REFA receiver enable	REFA receiver power-down control mode only when Bit 2 = 1. 1: enable REFA receiver. 0: power down (default).
	2	Input REFA and REFB receiver power-down control enable	Enables power-down control of the input receivers, REFA and REFB. 1: power-down control enabled. 0: both receivers enabled (default).
	1	$\overline{\text{OSC_IN}}$ single-ended receiver mode enable (CMOS mode)	Selects which single-ended input pin is enabled when in single-ended receiver mode (Register 0x01A[0] = 0). 1: negative receiver from oscillator input ($\overline{\text{OSC_IN}}$ pin) selected. 0: positive receiver from oscillator input (OSC_IN pin) selected (default).
	0	OSC_IN differential receiver mode enable	1: differential receiver mode. 0: single-ended receiver mode (also depends on Bit 1) (default).

Table 42. REF_TEST, REFA, REFB, and ZD_IN Control

Address	Bits	Bit Name	Description
0x01B	[7:6]	Reserved	0: reserved (default).
	5	Zero delay mode	Selects the zero delay mode used (via the ZD_IN pin) when Register 0x01B[4] = 0. Otherwise, this bit is ignored. 1: internal zero delay mode. The zero delay receiver is powered down. The internal zero delay path from Distribution Divider Channel 0 is used. 0: external zero delay mode. The ZD_IN receiver is enabled.
	4	OSC_IN signal feedback for PLL1	Controls the input PLL feedback path, local feedback from the OSC_IN receiver or zero delay mode. 1: OSC_IN receiver input used for the input PLL feedback (non-zero delay mode). 0: zero delay mode enabled (also depends on Register 0x01B[5] to select the zero delay path.
	3	$\overline{\text{ZD_IN}}$ single-ended receiver mode enable (CMOS mode)	Selects which single-ended input pin is enabled when in the single-ended receiver mode (Register 0x01B[2] = 0). 1: $\overline{\text{ZD_IN}}$ pin enabled. 0: ZD_IN pin enabled.
	2	ZD_IN differential receiver mode enable	1: differential receiver mode. 0: single-ended receiver mode (also depends on Register 0x01B[3]).
	1	$\overline{\text{REFB}}$ single-ended receiver mode enable (CMOS mode)	Selects which single-ended input pin is enabled when in single-ended receiver mode (Register 0x01A[6] = 0). 1: $\overline{\text{REFB}}$ pin enabled. 0: REFB pin enabled.
	0	$\overline{\text{REFA}}$ single-ended receiver mode enable (CMOS mode)	Selects which single-ended input pin is enabled when in single-ended receiver mode (Register 0x01A[5] = 0). 1: $\overline{\text{REFA}}$ pin enabled. 0: REFA pin enabled.

Table 43. PLL1 Miscellaneous Control

Address	Bits	Bit Name	Description				
0x01C	7	Enable REFB R divider independent division control	1: REFB R divider is controlled by Register 0x012 and Register 0x013. 0: REFB R divider is set to the same setting as the REFA R divider (Register 0x010 and Register 0x011). This requires that, for the loop to stay locked, the REFA and REFB input frequencies must be the same.				
	6	OSC_CTRL control voltage to $V_{CC}/2$ when reference clock fails	High permits the OSC_CTRL control voltage to be forced to midsupply when the feedback or input clocks fail. Low tristates the charge pump output. 1: OSC_CTRL control voltage goes to $V_{CC}/2$. 0: OSC_CTRL control voltage tracks the tristated (high impedance) charge pump (through the buffer).				
	5	Reserved	Reserved.				
	[4:2]	Reference selection mode	Programs the REFA, REFB mode selection (default = 000).				
			REF_SEL Pin	**Bit 4**	**Bit 3**	**Bit 2**	**Description**
			X[1]	0	0	0	Nonrevertive: stay on REFB.
			X[1]	0	0	1	Revert to REFA.
			X[1]	0	1	0	Select REFA.
			X[1]	0	1	1	Select REFB.
			0	1	X[1]	X[1]	REF_SEL pin = 0 (low): REFA.
			1	1	X[1]	X[1]	REF_SEL pin = 1 (high): REFB.
	[1:0]	Reserved	0: reserved (default).				

[1] X = don't care.

Table 44. PLL1 Loop Filter Zero Resistor Control

Address	Bits	Bit Name	Description				
0x01D	[7:4]	Reserved	Reserved.				
	[3:0]	PLL1 loop filter, R_{ZERO}	Programs the value of the zero resistor, R_{ZERO}.				
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**R_{ZERO} Value (kΩ)**
			0	0	0	0	883
			0	0	0	1	677
			0	0	1	0	341
			0	0	1	1	135
			0	1	0	0	10
			0	1	0	1	10
			0	1	1	0	10
			0	1	1	1	10
			1	0	0	0	Use external resistor

Output PLL (PLL2) (Address 0x0F0 to Address 0x0F6)

Table 45. PLL2 Charge Pump Control

Address	Bits	Bit Name	Description
0x0F0	[7:0]	PLL2 charge pump control	These bits set the magnitude of the PLL2 charge pump current. Granularity is ~3.5 µA with a full-scale magnitude of ~900 µA.

Table 46. PLL2 Feedback N Divider Control

Address	Bits	Bit Name	Description	
0x0F1	[7:6]	A counter	A counter word.	
	[5:0]	B counter	B counter word.	
	Feedback Divider Constraints			
	A Counter (Bits[7:6])		**B Counter (Bits[5:0])**	**Allowed N Division (4 × B + A)**
	A = 0 or A = 1		B = 4	16, 17
	A = 0 to A = 2		B = 5	20, 21, 22
	A = 0 to A = 2		B = 6	24, 25, 26
	A = 0 to A = 3		B ≥ 7	28, 29 … continuous to 255

Table 47. PLL2 Control

Address	Bits	Bit Name	Description
0x0F2	7	PLL2 lock detector power-down	Controls power-down of the PLL2 lock detector. 1: lock detector powered down. 0: lock detector active.
	6	Reserved	Default = 0; value must remain 0.
	5	Enable frequency doubler	Enables doubling of the PLL2 reference input frequency. 1: enabled. 0: disabled.
	4	Enable SPI control of antibacklash pulse width	Setting this bit allows user control of the antibacklash pulse width setting in Register 0x0F2[3:2]. 0 (default): antibacklash period is forced to high. 1: antibacklash period defined by Register 0x0F[3:2] (recommended setting).
	[3:2]	Antibacklash pulse width control	Controls the PFD antibacklash period. These bits default to the high setting unless reprogrammed using Register 0x0F2[4] = 1b. The high setting decreases the maximum allowable PLL2 PFD rate. See Table 12 for ranges. 00 minimum. 01: low. 10: high (initial state unless changed via Register 0x0F2[4] = 1b). 11: maximum.
	[1:0]	PLL2 charge pump mode	Controls the mode of the PLL2 charge pump. 00: tristate. 01: pump up. 10: pump down. 11 (default): normal.

Table 48. VCO Control

Address	Bits	Bit Name	Description
0x0F3	[7:5]	Reserved	Reserved.
	4	Force release of distribution sync when PLL2 is unlocked	0 (default): distribution is held in sync (static) until the output PLL locks for the first time. Then it is automatically released from sync with all dividers synchronized. 1: overrides the PLL2 lock detector state; forces release of the distribution from sync.
	3	Treat reference as valid	0 (default): uses the PLL1 VCXO indicator to determine when the reference clock to the PLL2 is valid. 1: treats the reference clock as valid even if PLL1 does not consider it to be valid.
	2	Force VCO to midpoint frequency	Selects VCO control voltage functionality. 0 (default): normal VCO operation. 1: forces VCO control voltage to midscale.
	1	Calibrate VCO (not autoclearing)	1: initiates VCO calibration (this is not an autoclearing bit). 0: resets the VCO calibration.
	0	Reserved	Reserved.

Table 49. VCO Divider Control

Address	Bits	Bit Name	Description			
0x0F4	[7:4]	Reserved	Reserved.			
	3	VCO divider power-down	1: powers down the divider. 0: normal operation.			
	[2:0]	VCO divider	Note that the VCO divider connects to all output channels.			
			Bit 2	**Bit 1**	**Bit 0**	**Divider Value**
			0	0	0	Divide-by-4
			0	0	1	Divide-by-5
			0	1	0	Divide-by-6
			0	1	1	Divide-by-7
			1	0	0	Divide-by-8
			1	0	1	Divide-by-9
			1	1	0	Divide-by-10
			1	1	1	Divide-by-11

Table 50. PLL2 Loop Filter Control

Address	Bits	Bit Name	Description			
0x0F5	[7:6]	Pole 2 resistor (R_{POLE2})	**Bit 7**	**Bit 6**	**R_{POLE2} (Ω)**	
			0	0	900	
			0	1	450	
			1	0	300	
			1	1	225	
	[5:3]	Zero resistor (R_{ZERO})	**Bit 5**	**Bit 4**	**Bit 3**	**R_{ZERO} (Ω)**
			0	0	0	3250
			0	0	1	2750
			0	1	0	2250
			0	1	1	2100
			1	0	0	3000
			1	0	1	2500
			1	1	0	2000
			1	1	1	1850
	[2:0]	Pole 1 capacitor (C_{POLE1})	**Bit 2**	**Bit 1**	**Bit 0**	**C_{POLE1} (pF)**
			0	0	0	0
			0	0	1	8
			0	1	0	16
			0	1	1	24
			1	0	0	24
			1	0	1	32
			1	1	0	40
			1	1	1	48
0x0F6	[7:1]	Reserved	Reserved.			
	0	Bypass internal R_{ZERO} resistor	Bypasses the internal R_{ZERO} resistor (R_{ZERO} = 0 Ω). Requires the use of a series external zero resistor. This bit is the MSB of the loop filter control register (Address 0x0F5 and Address 0x0F6).			

Clock Distribution (Register 0x190 to Register 0x1B9)

Table 51. Channel 0 to Channel 13 Control (This Same Map Applies to All 14 Channels)

Address	Bits	Bit Name	Description				
0x190	7	Invert divider output	Inverts the polarity of the divider's output clock.				
	6	Ignore sync	0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal.				
	5	Power-down channel	1: powers down the entire channel. 0: normal operation.				
	4	Lower power mode (differential modes only)	Reduces power used in the differential output modes (LVDS/LVPECL/HSTL). This reduction may result in power savings, but at the expense of performance. Note that this bit does not affect output swing and current, just the internal driver power. 1: low strength/lower power. 0: normal operation.				
	[3:0]	Driver mode	Driver mode.				
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Driver Mode**
			0	0	0	0	Tristate output
			0	0	0	1	LVPECL (8 mA)
			0	0	1	0	LVDS (3.5 mA)
			0	0	1	1	LVDS (7 mA)
			0	1	0	0	HSTL-0 (16 mA)
			0	1	0	1	HSTL-1 (8 mA)
			0	1	1	0	CMOS (both outputs in phase) + Pin: true phase relative to divider output − Pin: true phase relative to divider output
			0	1	1	1	CMOS (opposite phases on outputs) + Pin: true phase relative to divider output − Pin: complement phase relative to divider output
			1	0	0	0	CMOS + Pin: true phase relative to divider output − Pin: high-Z
			1	0	0	1	CMOS + Pin: high-Z − Pin: true phase relative to divider output
			1	0	1	0	CMOS + Pin: high-Z − Pin: high-Z
			1	0	1	1	CMOS (both outputs in phase) + Pin: complement phase relative to divider output − Pin: complement phase relative to divider output
			1	1	0	0	CMOS (both outputs out of phase) + Pin: complement phase relative to divider output − Pin: true phase relative to divider output
			1	1	0	1	CMOS + Pin: complement phase relative to divider output − Pin: high-Z
			1	1	1	0	CMOS + Pin: high-Z − Pin: complement phase relative to divider output
			1	1	1	1	Tristate output
0x191	[7:0]	Channel divider, Bits[7:0] (LSB)	Division = Channel Divider Bits[9:0] + 1. For example, [9:0] = 0 is divided by 1, [9:0] = 1 is divided by 2 … [9:0] = 1023 is divided by 1024. 10-bit channel divider, Bits[7:0] (LSB).				
0x192	[7:2]	Divider phase	Divider initial phase after a sync is asserted relative to the divider input clock (from the VCO divider output). LSB = ½ of a period of the divider input clock. Phase = 0: no phase offset. Phase = 1: ½ period offset, … Phase = 63: 31 period offset.				
	[1:0]	Channel divider, Bits[9:8] (MSB)	10-bit channel divider, Bits[9:8] (MSB).				

Table 52. PLL1 Output Control (PLL1_OUT, Pin 72)

Address	Bits	Bit Name	Description
0x1BA	[7:5]	Reserved	Reserved
	4	PLL1 output CMOS driver strength	CMOS driver strength 1: weak 0: strong
	[3:0]	PLL1 output divider	0000: divide-by-1 0001: divide-by-2 (default) 0010: divide-by-4 0100: divide-by-8 1000: divide-by-16 No other inputs permitted

Table 53. PLL1 Output Channel Control

Address	Bits	Bit Name	Description
0x1BB	7	PLL1 output driver power-down	PLL1 output driver power-down
	[6:4]	Reserved	Reserved
	3	Route VCXO clock to Channel 3 divider input	1: channel uses VCXO clock. Routes VCXO clock to divider input. 0: channel uses VCO divider output clock
	2	Route VCXO clock to Channel 2 divider input	1: channel uses VCXO clock. Routes VCXO clock to divider input. 0: channel uses VCO divider output clock
	1	Route VCXO clock to Channel 1 divider input	1: channel uses VCXO clock. Routes VCXO clock to divider input. 0: channel uses VCO divider output clock
	0	Route VCXO clock to Channel 0 divider input	1: channel uses VCXO clock. Routes VCXO clock to divider input. 0: channel uses VCO divider output clock

Readback (Address 0x22C to Address 0x22D)

Table 54. Readback Registers (Readback 0 and Readback 1)

Address	Bits	Bit Name	Description
0x22C	7	Status PLL2 reference clock	1: OK 0: off/clocks are missing
	6	Status PLL1 feedback clock	1: OK 0: off/clocks are missing
	5	Status VCXO	1: OK 0: off/clocks are missing
	4	Status REF_TEST	1: OK 0: off/clocks are missing
	3	Status REFB	1: OK 0: off/clocks are missing
	2	Status REFA	1: OK 0: off/clocks are missing
	1	Lock detect PLL2	1: locked 0: unlocked
	0	Lock detect PLL1	1: locked 0: unlocked
0x22D	[7:4]	Reserved	Reserved
	3	Holdover active	1: holdover is active (both references are missing) 0: normal operation
	2	Selected reference (in auto mode)	Selected reference (applies only when the device automatically selects the reference; for example, not in manual control mode) 1: REFB 0: REFA
	1	Reserved	Reserved
	0	VCO calibration in progress	1: VCO calibration in progress 0: VCO calibration not in progress

Other (Address 0x230 to Address 0x234)

Table 55. Status Signals

Address	Bits	Bit Name	Description						
0x230	[7:6]	Reserved	Reserved						
	[5:0]	Status Monitor 0 control	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Muxout**
			0	0	0	0	0	0	GND
			0	0	0	0	0	1	PLL1 and PLL2 locked
			0	0	0	0	1	0	PLL1 locked
			0	0	0	0	1	1	PLL2 locked
			0	0	0	1	0	0	Both references are missing (REFA and REFB)
			0	0	0	1	0	1	Both references are missing and PLL2 is locked
			0	0	0	1	1	0	REFB selected (applies only to auto select mode)
			0	0	0	1	1	1	REFA is OK
			0	0	1	0	0	0	REFB is OK
			0	0	1	0	0	1	REF_TEST is OK
			0	0	1	0	1	0	VCXO is OK
			0	0	1	0	1	1	PLL1 feedback is OK
			0	0	1	1	0	0	PLL2 reference clock is OK
			0	0	1	1	0	1	Reserved
			0	0	1	1	1	0	REFA and REFB are OK
			0	0	1	1	1	1	All clocks are OK (except REF_TEST)
			0	1	0	0	0	0	PLL1 feedback is divide-by-2
			0	1	0	0	0	1	PLL1 PFD down divide-by-2
			0	1	0	0	1	0	PLL1 REF divide-by-2
			0	1	0	0	1	1	PLL1 PFD up divide-by-2
			0	1	0	1	0	0	GND
			0	1	0	1	0	1	GND
			0	1	0	1	1	0	GND
			0	1	0	1	1	1	GND
									All bit combinations after 010111 are reserved
0x231	[7:6]	Reserved	Reserved						
	[5:0]	Status Monitor 1 control	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Muxout**
			0	0	0	0	0	0	GND
			0	0	0	0	0	1	PLL1 and PLL2 locked
			0	0	0	0	1	0	PLL1 locked
			0	0	0	0	1	1	PLL2 locked
			0	0	0	1	0	0	Both references are missing (REFA and REFB)
			0	0	0	1	0	1	Both references are missing and PLL2 is locked
			0	0	0	1	1	0	REFB selected (applies only to auto select mode)
			0	0	0	1	1	1	REFA is OK
			0	0	1	0	0	0	REFB is OK
			0	0	1	0	0	1	REF_TEST is OK
			0	0	1	0	1	0	VCXO is OK
			0	0	1	0	1	1	PLL1 feedback is OK
			0	0	1	1	0	0	PLL2 reference clock is OK
			0	0	1	1	0	1	Reserved
			0	0	1	1	1	0	REFA and REFB are OK
			0	0	1	1	1	1	All clocks are OK (except REF_TEST)
			0	1	0	0	0	0	GND
			0	1	0	0	0	1	GND
			0	1	0	0	1	0	GND
			0	1	0	0	1	1	GND
			0	1	0	1	0	0	PLL2 feedback is divide-by-2
			0	1	0	1	0	1	PLL2 PFD down divide-by-2
			0	1	0	1	1	0	PLL2 REF divide-by-2
			0	1	0	1	1	1	PLL2 PFD up divide-by-2
									All bit combinations after 010111 are reserved

Address	Bits	Bit Name	Description
0x232	[7:5]	Reserved	Reserved.
	4	Enable STATUS_EEPROM on STATUS0 pin	Enables the EEPROM status on the STATUS0 pin. 1: enable status.
	3	STATUS1 pin divider enable	Enables a divide-by-4 on the STATUS1 pin, allowing dynamic signals to be viewed at a lower frequency (such as the PFD input clocks). Not to be used with dc states on the status pins, which occur when the settings of Register 0x231[5:0] are in the range of 000000 to 001111. 1: enabled. 0: disabled.
	2	STATUS0 pin divider enable	Enables a divide-by-4 on the STATUS0 pin, allowing dynamic signals to be viewed at a lower frequency (such as the PFD input clocks). Not to be used with dc states on the status pins, which occur when the settings of Register 0x230[5:0] are in the range of 000000 to 001111. 1: enable. 0: disable.
	1	Reserved	Reserved.
	0	Sync dividers (manual control)	Set bit to put dividers in sync; clear bit to release. Functions like $\overline{\text{SYNC}}$ pin low. 1: sync. 0: normal.

Table 56. Power-Down Control

Address	Bits	Bit Name	Description
0x233	[7:3]	Reserved	Reserved.
	2	PLL1 power-down	1: power-down (default). 0: normal operation.
	1	PLL2 power-down	1: power-down (default). 0: normal operation.
	0	Distribution power-down	Powers down the distribution. 1: power-down (default). 0: normal operation.

Table 57. Update All Registers

Address	Bits	Bit Name	Description
0x234	[7:1]	Reserved	Reserved.
	0	IO_UPDATE	This bit must be set to 1 to transfer the contents of the buffer registers into the active registers, which happens on the next SCLK rising edge. This bit is self-clearing; that is, it does not have to be set back to 0. 1 (self-clearing): update all active registers to the contents of the buffer registers.

EEPROM Buffer (Address 0xA00 to Address 0xA16)

Table 58. EEPROM Buffer Segment

Address	Bits	Bit Name	Description
0xA00 to 0xA16	[7:0]	EEPROM Buffer Segment Register 1 to EEPROM Buffer Segment Register 23	The EEPROM buffer segment section stores the starting address and number of bytes that are to be stored and read back to and from the EEPROM. Because the register space is noncontiguous, the EEPROM controller needs to know the starting address and number of bytes in the register space to store and retrieve from the EEPROM. In addition, there are special instructions for the EEPROM controller: operational codes (that is, IO_UPDATE and end-of-data) that are also stored in the EEPROM buffer segment. The on-chip default setting of the EEPROM buffer segment registers is designed such that all registers are transferred to/from the EEPROM, and an IO_UPDATE is issued after the transfer (see the Programming the EEPROM Buffer Segment section).

EEPROM Control (Address 0xB00 to Address 0xB03)

Table 59. STATUS_EEPROM

Address	Bits	Bit Name	Description
0xB00	[7:1]	Reserved	Reserved.
	0	STATUS_EEPROM (read only)	This read-only bit indicates the status of the data transferred between the EEPROM and the buffer register bank during the writing and reading of the EEPROM. This signal is also available at the STATUS0 pin when Register 0x232[4] is set. 0: data transfer is complete. 1: data transfer is not complete.

Table 60. EEPROM Error Checking Readback

Address	Bits	Bit Name	Description
0xB01	[7:1]	Reserved	Reserved.
	0	EEPROM data error (read only)	This read-only bit indicates an error during the data transfer between the EEPROM and the buffer. 0: no error; data is correct. 1: incorrect data detected.

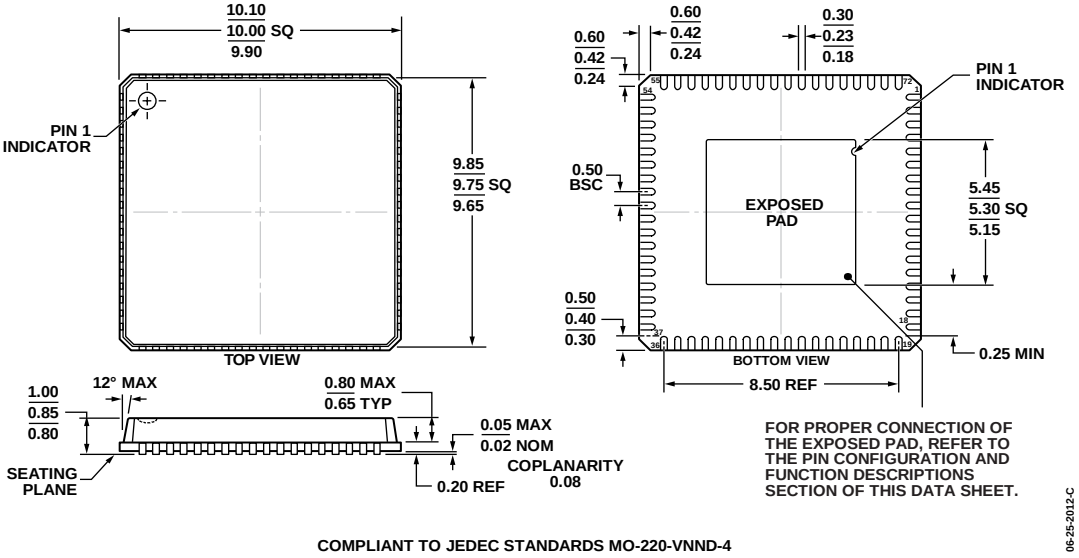
Table 61. EEPROM Control 1

Address	Bits	Bit Name	Description
0xB02	[7:2]	Reserved	Reserved.
	1	SOFT_EEPROM	When the EEPROM_SEL pin is tied low, setting the SOFT_EEPROM bit resets the AD9523 using the settings saved in EEPROM. 1: soft reset with EEPROM settings (self-clearing).
	0	Enable EEPROM write	Enables the user to write to the EEPROM. 0: EEPROM write protection is enabled. User cannot write to EEPROM (default). 1: EEPROM write protection is disabled. User can write to EEPROM.

Table 62. EEPROM Control 2

Address	Bits	Bit Name	Description
0xB03	[7:1]	Reserved	Reserved.
	0	REG2EEPROM	Transfers data from the buffer register to the EEPROM (self-clearing). 1: setting this bit initiates the data transfer from the buffer register to the EEPROM (writing process); it is reset by the I^2C master after the data transfer is done.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 46. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9523BCPZ	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-6
AD9523BCPZ-REEL7	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-6
AD9523/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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